SRS-DTC Links

WG5 RD51 Miniweek

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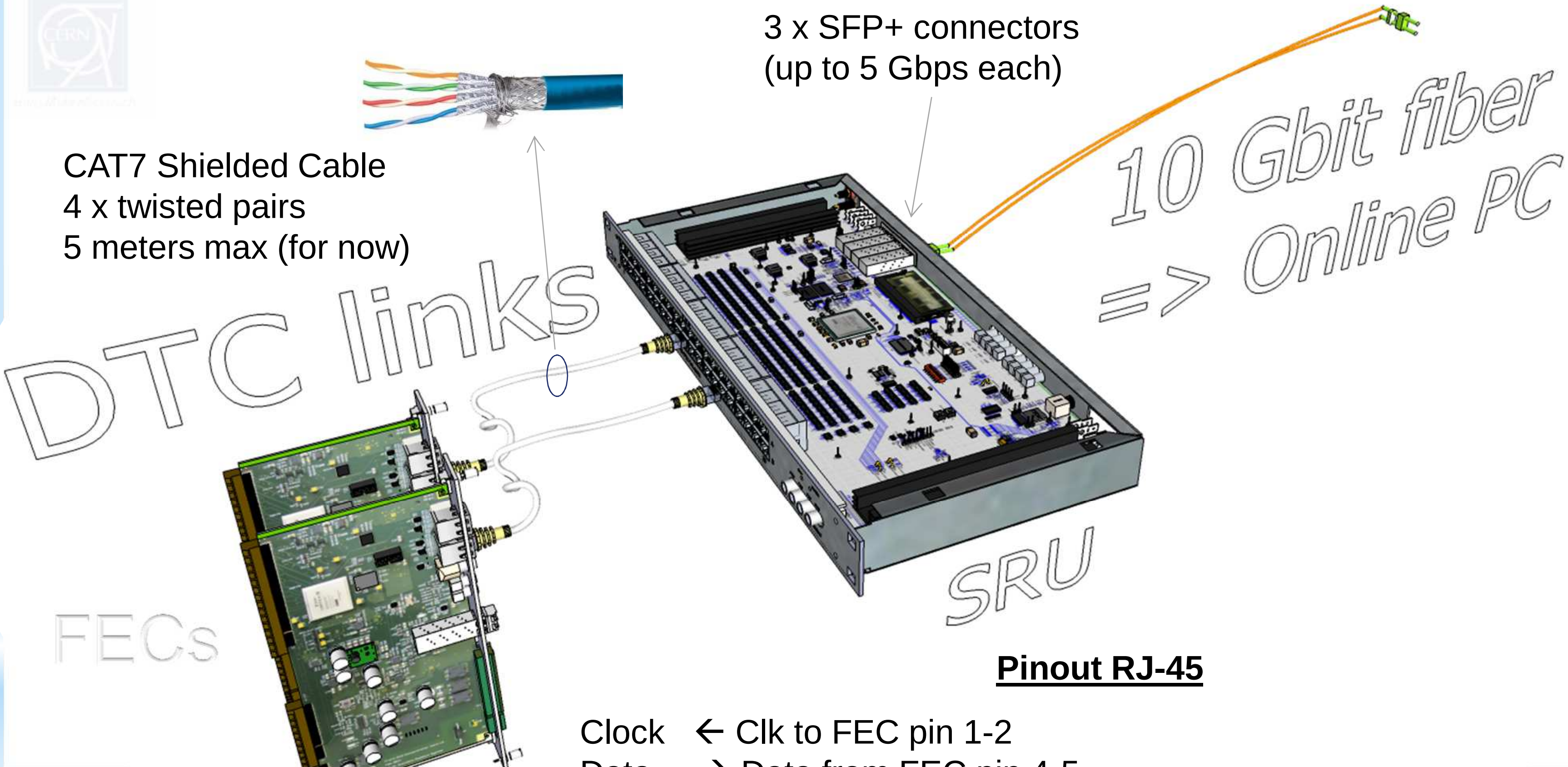
Outline

1. Overview
2. Purpose
3. Architecture
4. Phase Alignment
5. High-Speed Data
6. Measurements
7. Status

1. Overview



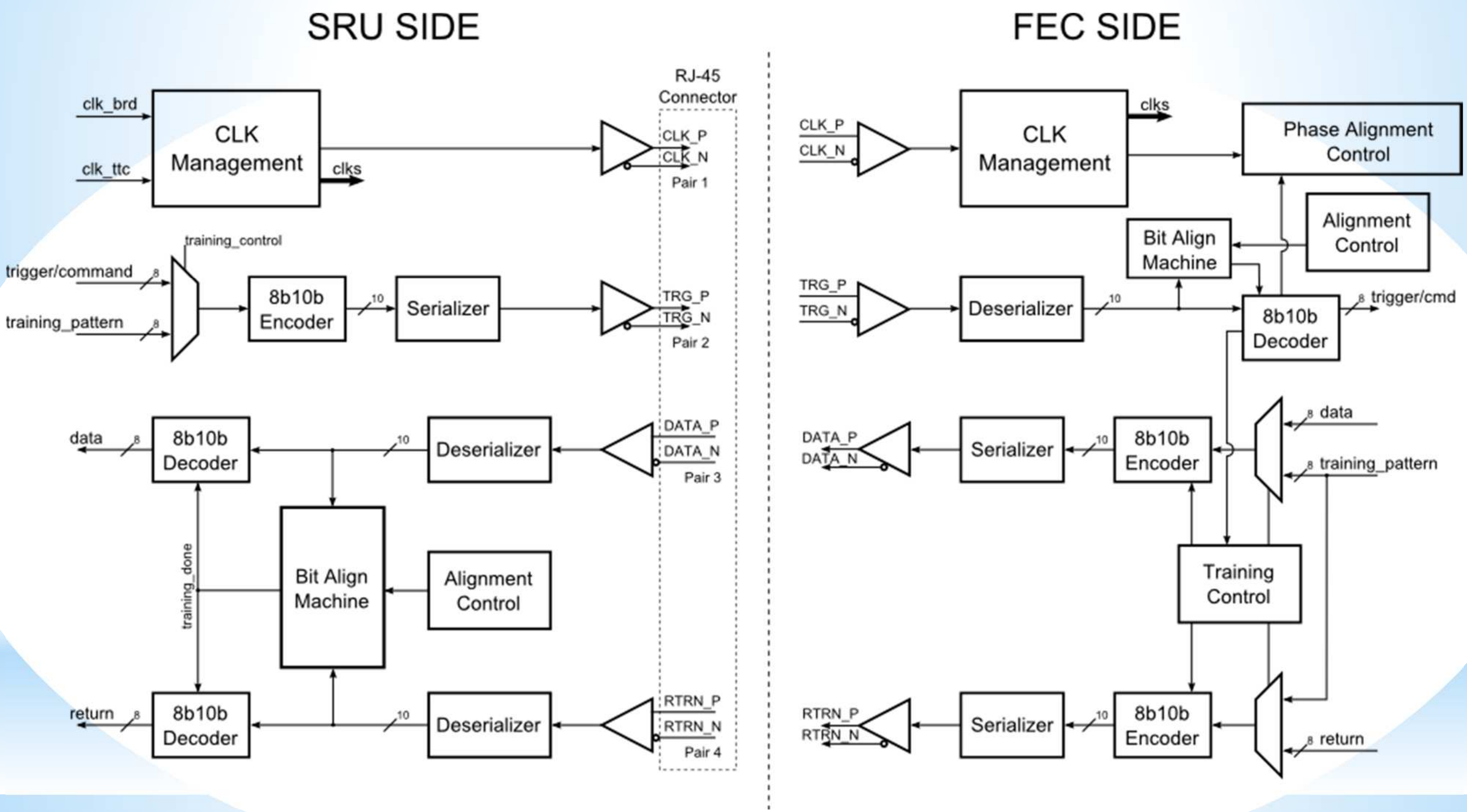
Pinout RJ-45

Clock ← Clk to FEC pin 1-2
Data → Data from FEC pin 4-5
Trigger ← Trigger/Commands to FEC pin 3-6
Return →Additional line for data, clk synchronization,… pin 7-8

2. Purpose

- Provide clock (40 Mhz)
- Send/Receive trigger
- Send/Receive slow control frames
- Receive data from the detectors at high-speed rate

3. Architecture

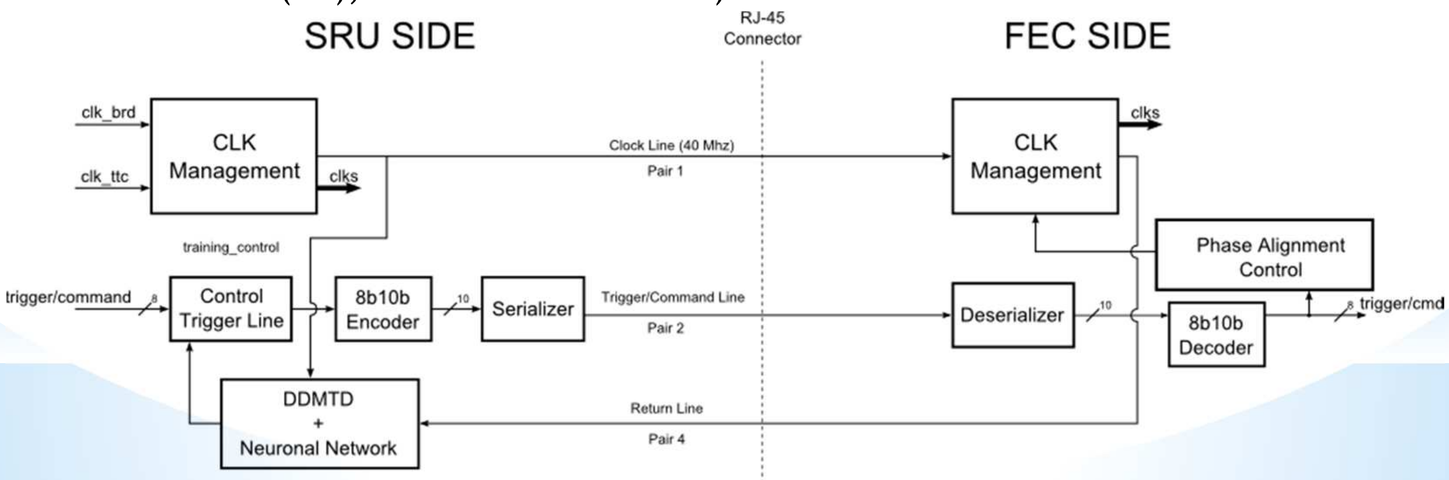


4. Phase Alignment

The 40 Mhz clock is provided by TTC chip. Then this clock is sent from the SRU board to the FEC board. In this way all boards work with same clock and the whole system is synchronized. Is it really the same one? No, exactly. Same frequency but different phase.

We need to align the phase. HOW?

Using a **Digital Dual-Mixer Time Difference (DDMTD)** method and a small **Neuronal Network** (see R. J. Aliaga, J. M. Monzó, M. Spaggiari, N. Ferrando, R. Gadea and R. J. Colom. *"PET System Synchronization and Timing Resolution using High-Speed Data Links"*, Real Time Conference (RT), 2010 17th IEEE-NPSS).

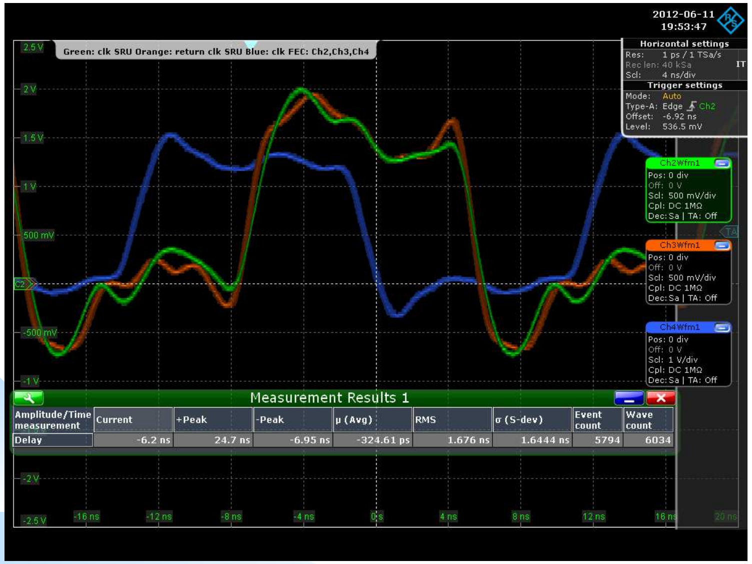


4. Phase Alignment

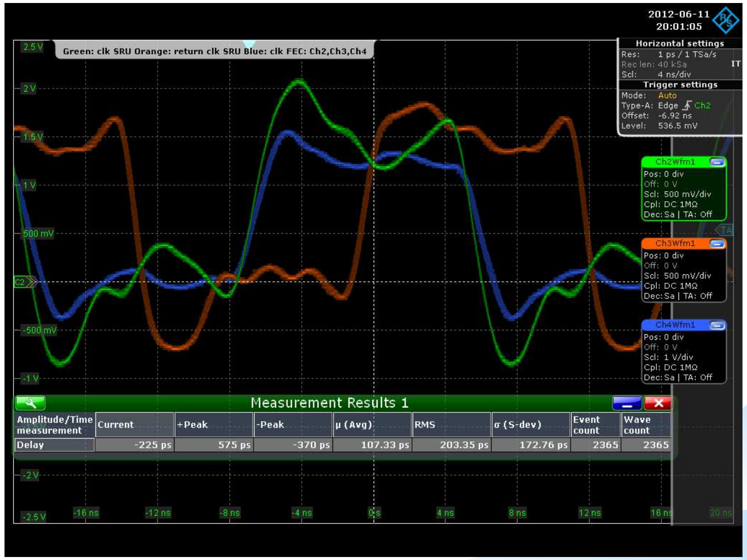
DDMTD makes it possible to get the introduced delay by the cable. In this way we can compensate that delay, so the rising edge of the two clock is produced at the same time.

When the phase synchronization is achieved the return line will be free (around ms).

Initial Phase



Phase After Alignment



5. High-Speed Data

- High-speed clocks are generated from 40 Mhz clock on the FEC side to send data from FEC board to SRU board. The jitter can be a problem in the high-speed clock since the PLL into FPGA is not so good. For this reason, we have included a jitter-cleaner chip in the new FEC board (with Virtex 6)

- We are capable of sending data at 1 Gbps using a CAT7 shielded cable of 5 meters of length

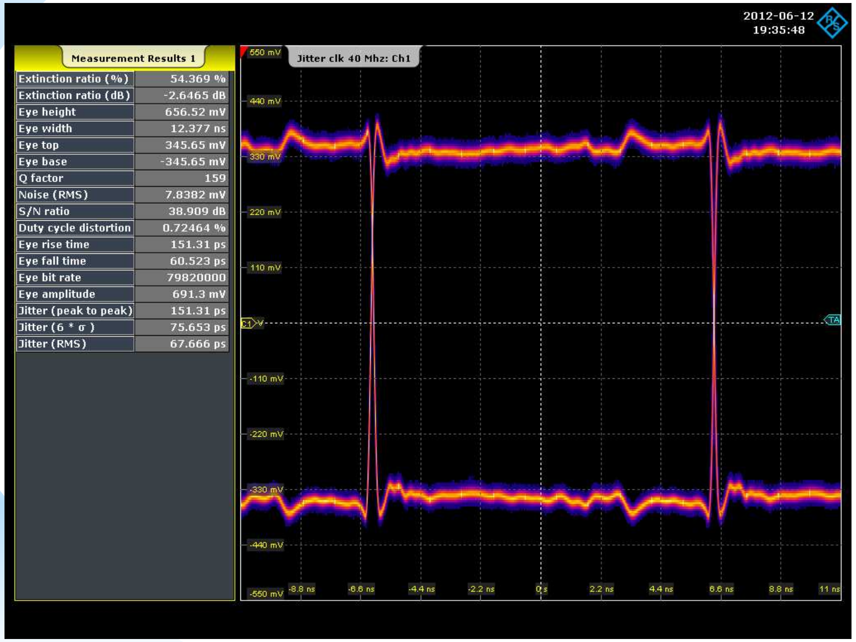
- BER (Bit Error Rate) value is quite good $<10^{-12}$ using a strenuous PRBS (PRBS29)

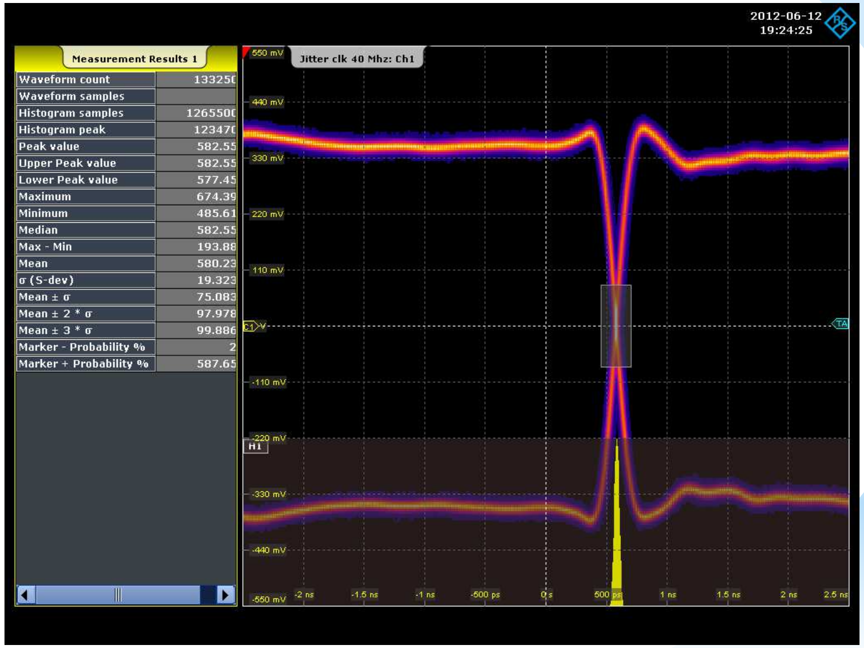
- 8b10b encoding is used to achieve DC-balance and distinguish among different types of frames, as trigger frames and command frames

- The rate of data have to be multiple of the TTC clock, so the phase synchronization is achieved much easier. Instead of sending at 1 Gbps we will be data at 960 Mbps, for example

6. Measurements

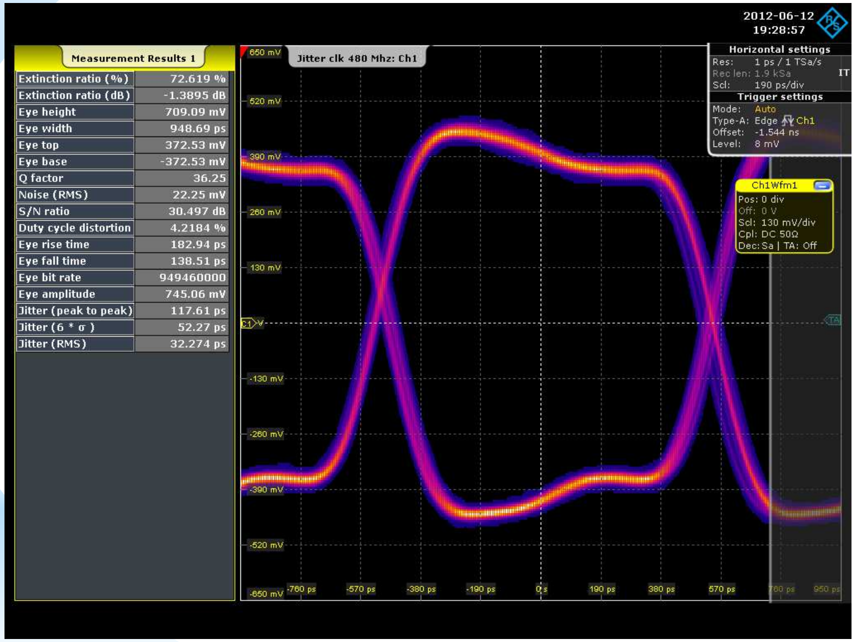
40 Mhz Clock Jitter (on FEC side)

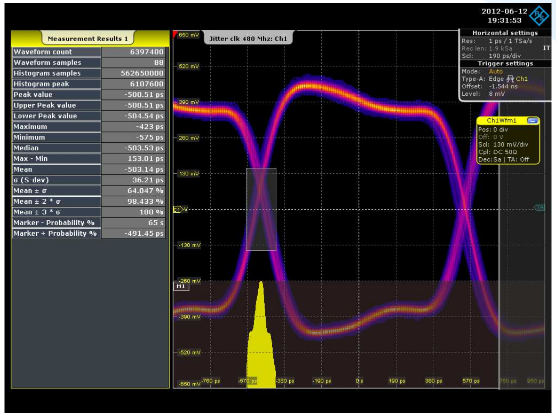


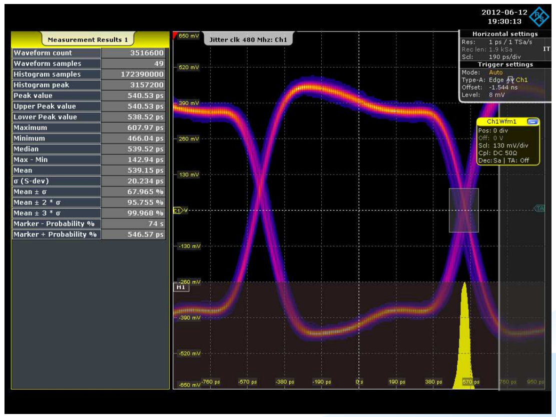


6. Measurements

480 Mhz Clock Jitter (on FEC side)

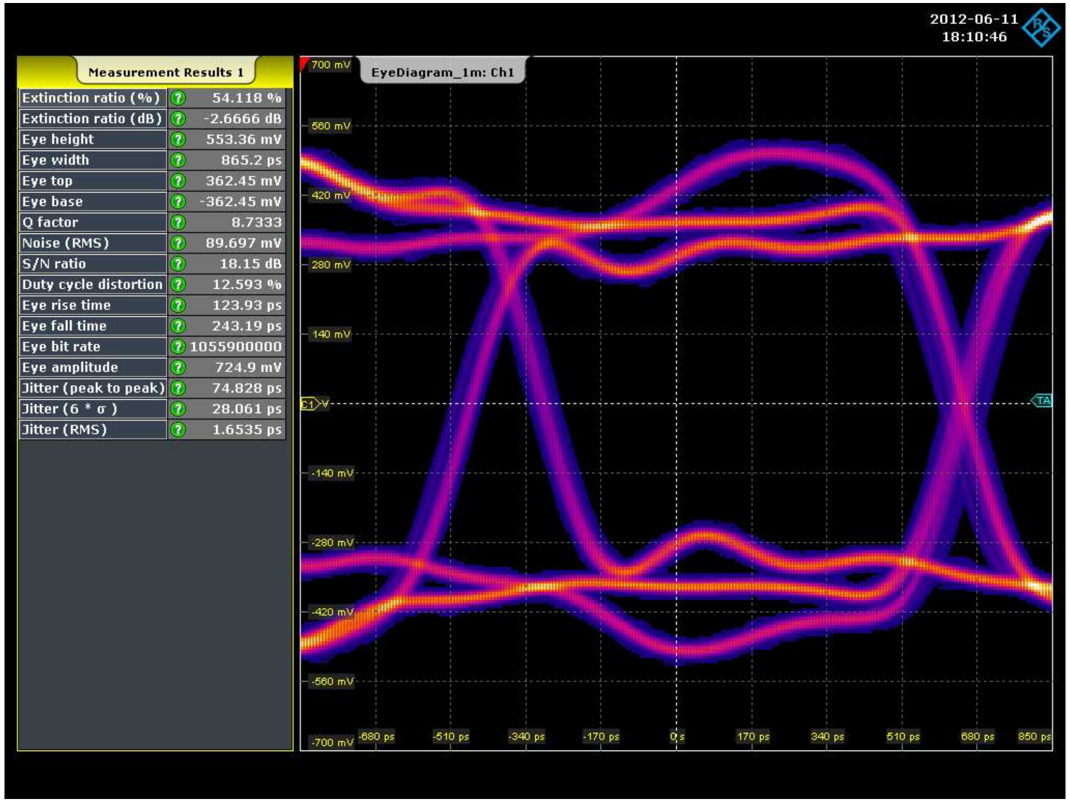






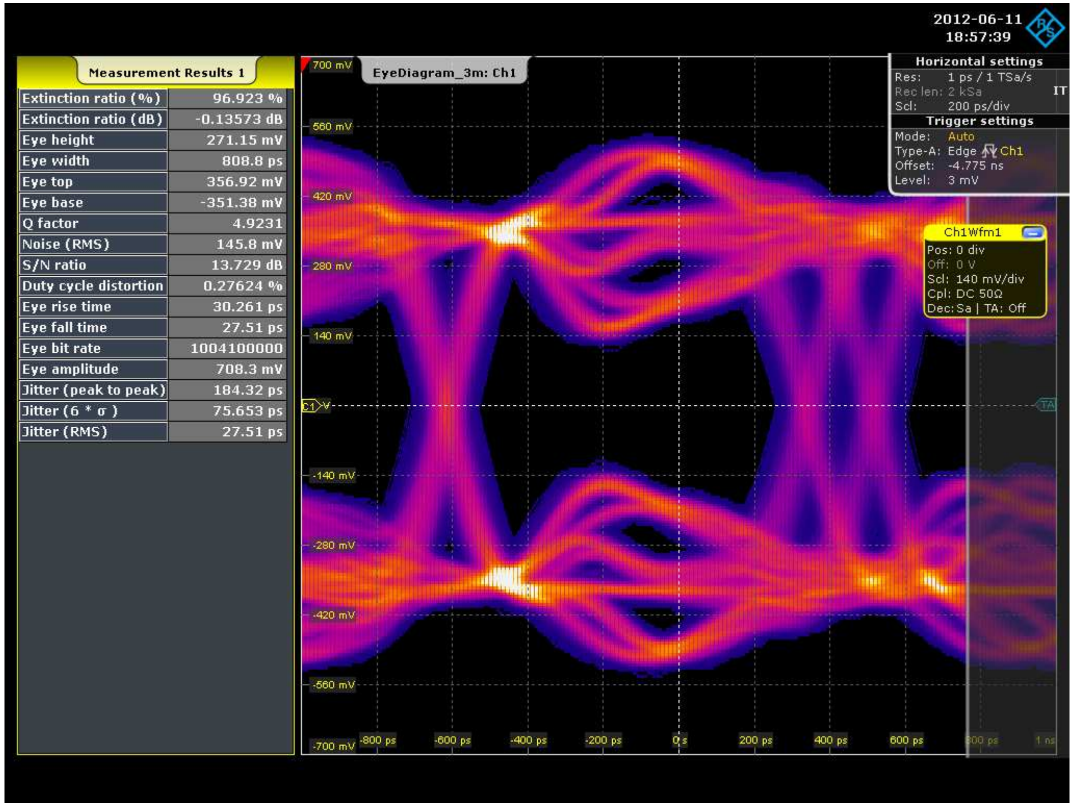
6. Measurements

Data Jitter (1 m of cable at 960 Mbps) – Eye Diagram



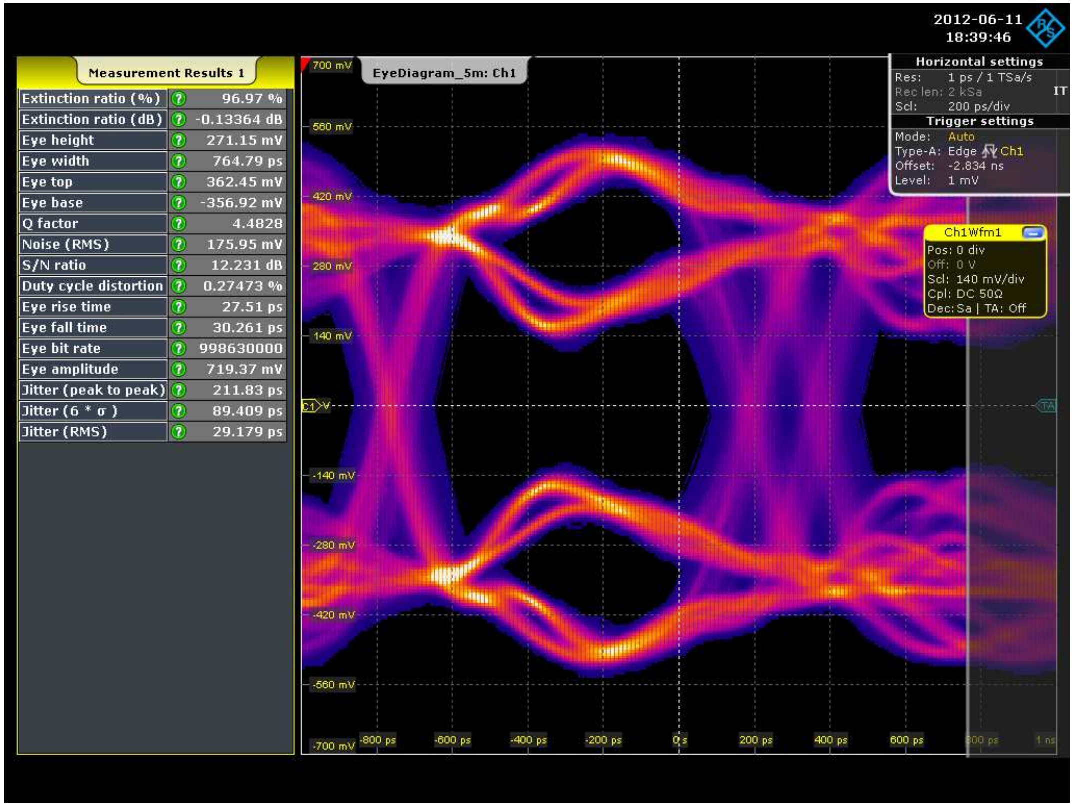
6. Measurements

Data Jitter (3 m of cable at 960 Mbps) – Eye Diagram



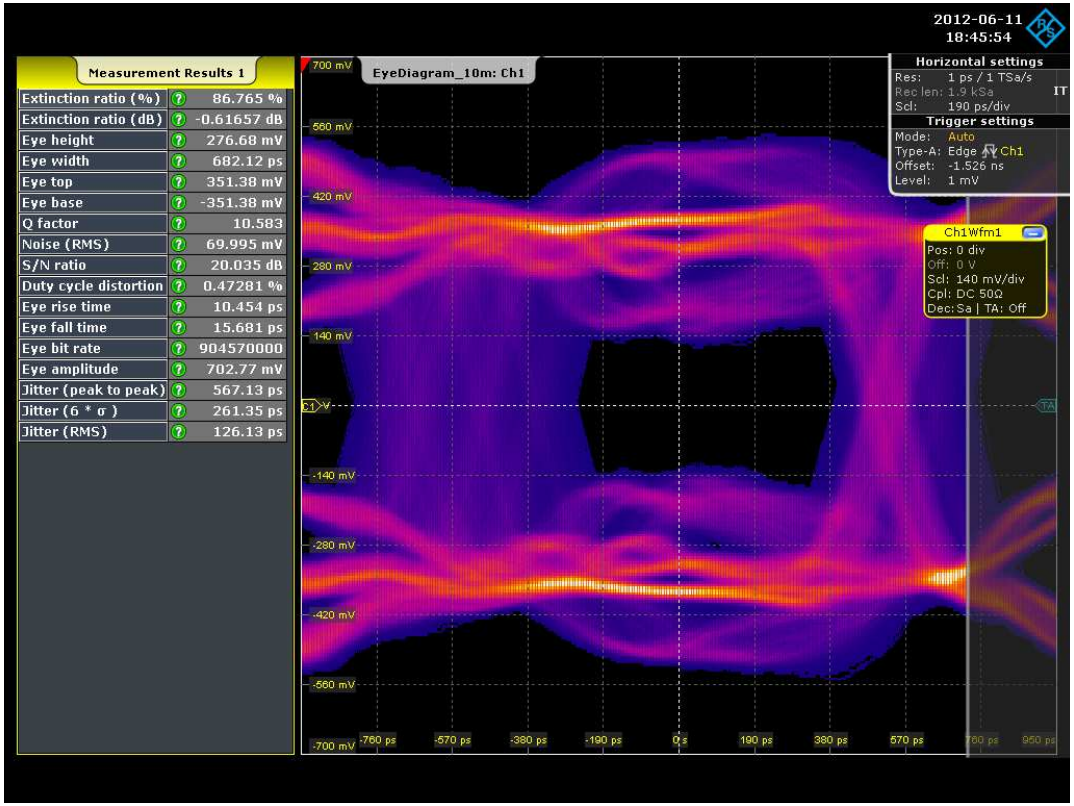
6. Measurements

Data Jitter (5 m of cable at 960 Mbps) – Eye Diagram



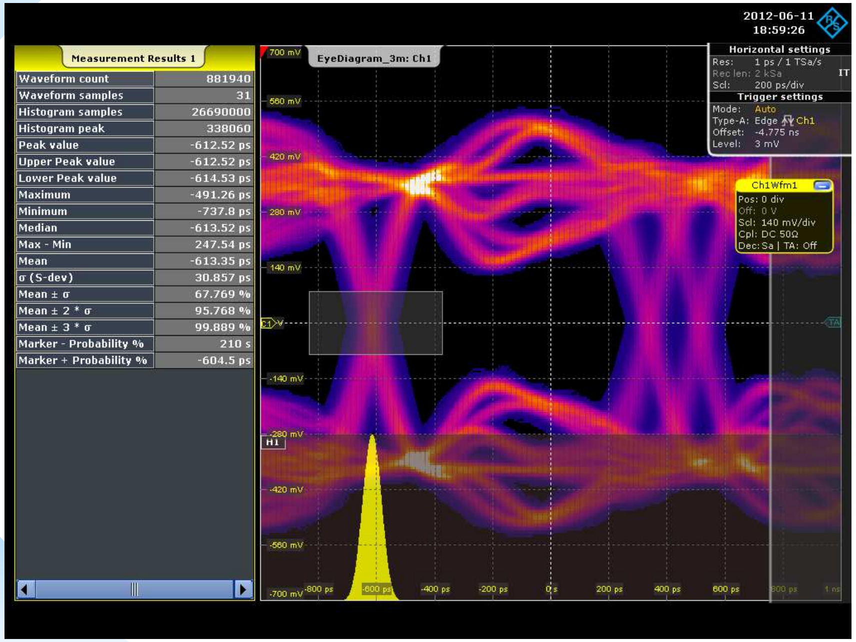
6. Measurements

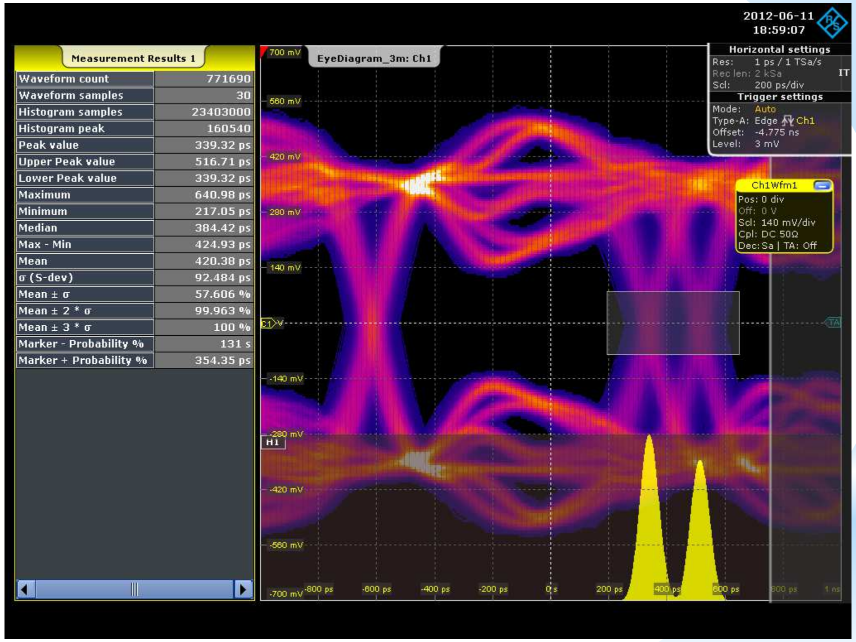
Data Jitter (10 m of cable at 960 Mbps) – Eye Diagram



6. Measurements

Data Jitter (3 m of cable at 960 Mbps) – Histogram





7. Status

The current status of the DTC link is quite good. We have implemented the most diffucult parts, both high-speed transmission and phase synchronization. Next week we will have ready the first version with the following functions available (for two RJ-45 connectors):

- Clock synchronization
- Slow control frames (PC → SRU board → FEC board)
- Send data at high-speed (960 Mbps) from FEC board to send board

We keep on adding new functions and extending the code to cover the 40 RJ-45 connectors.

Thank you very much!!