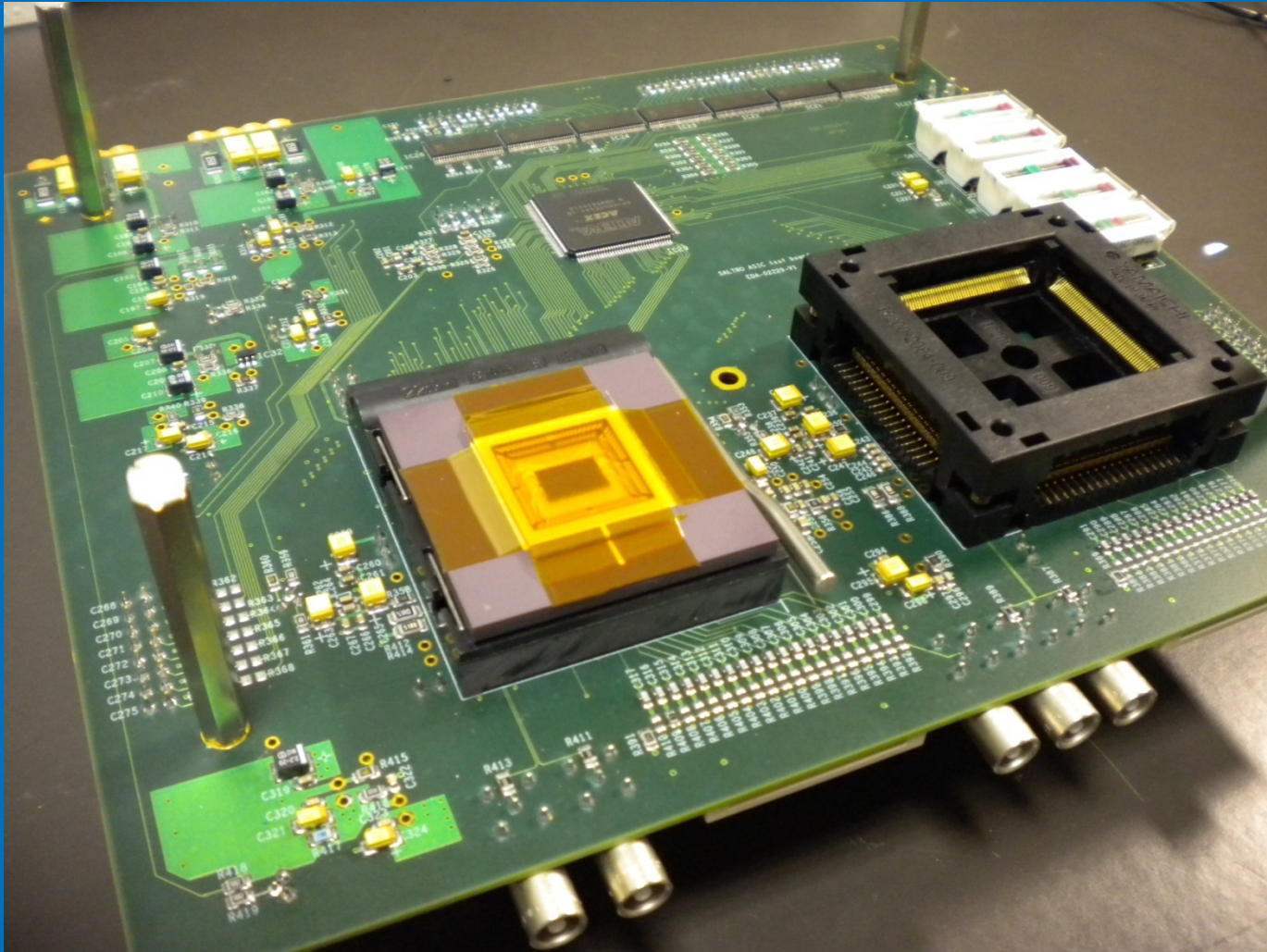
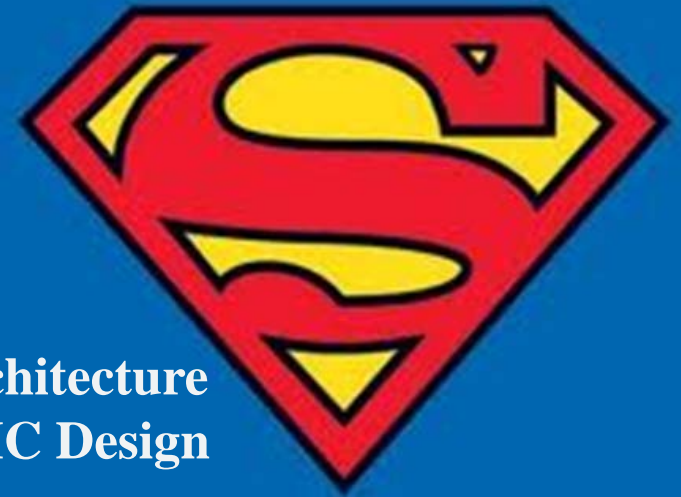


# The 16-channel Super-ALTRO Demonstrator



# The 16-channel Super-ALTRO Demonstrator



## People :

**Luciano Musa ... S-Altro Specifications and Architecture**

**Paul Aspell ... Coordinator of Demonstrator ASIC Design**

**Hugo França-Santos ... ADC**

**Eduardo Garcia ... Digital Signal Processing & Control**

**Massimiliano De Gaspari ... Front-end, Integration, Tests**

## Presented at:

**CERN**

**November 29<sup>th</sup>, 2011**

# Outline

- **Motivations for the project**
- **System architecture**
  - **Pre-amplifier shaper (PASA)**
  - **ADC**
  - **Digital Signal Processor (DSP)**
  - **Clock tree**
  - **Top-level simulations**
  - **Assembly, floorplan, layout**
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  - **Test setup**
  - **Measurements: gain, noise, power, power pulsing**
- **Conclusions**

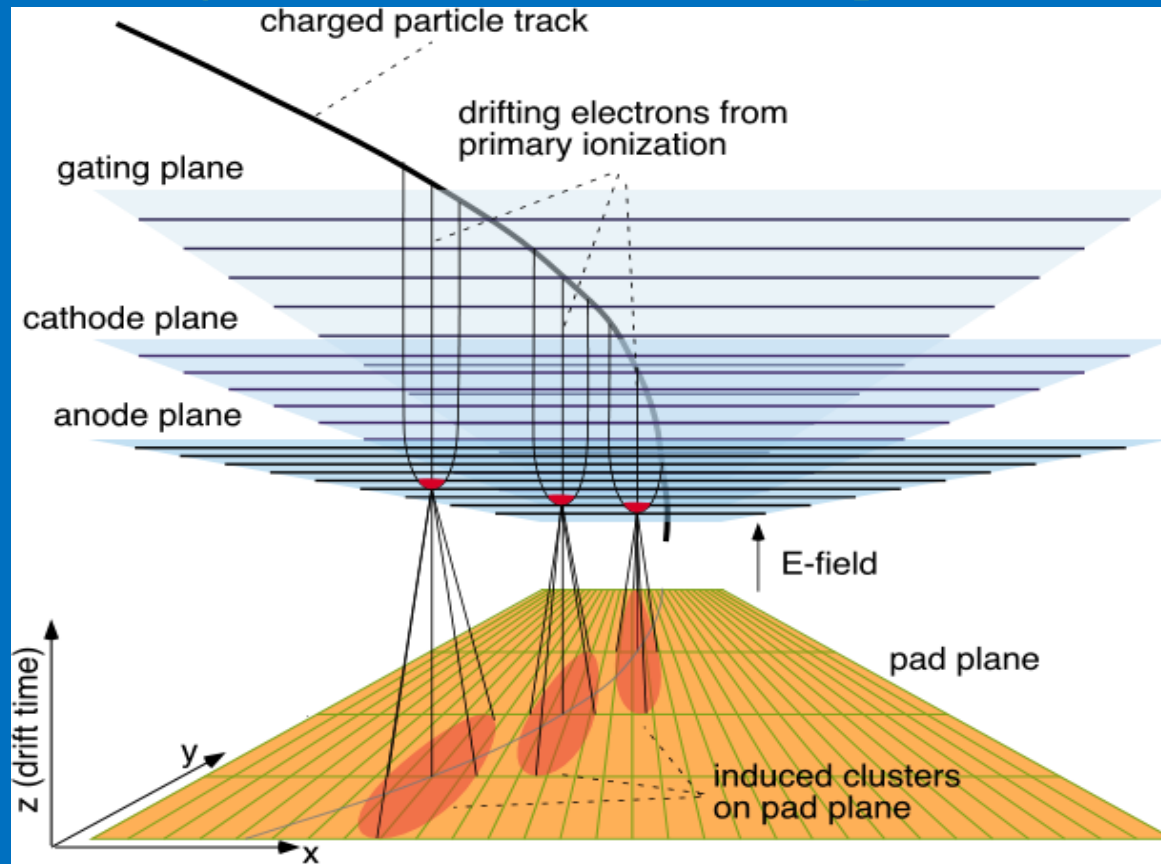
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# Alice TPC: MWPC readout

## Time Projection Chamber:

track finding, momentum measurement, particle identification



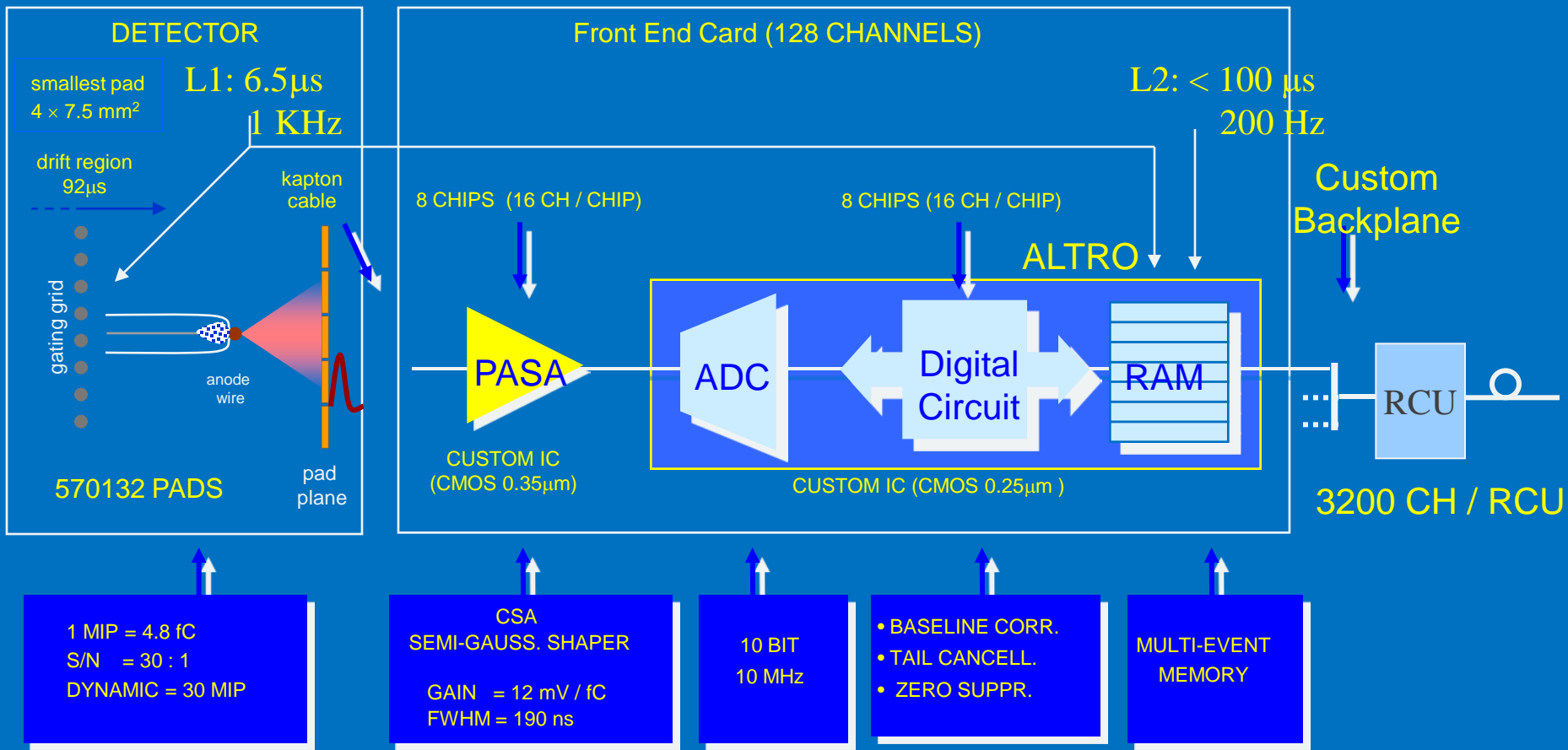
Charge measurement:  $dE/dx$

Trigger rate: 200 Hz Pb-Pb, 1 KHz p-p

Multi-Wire Proportional Chamber:

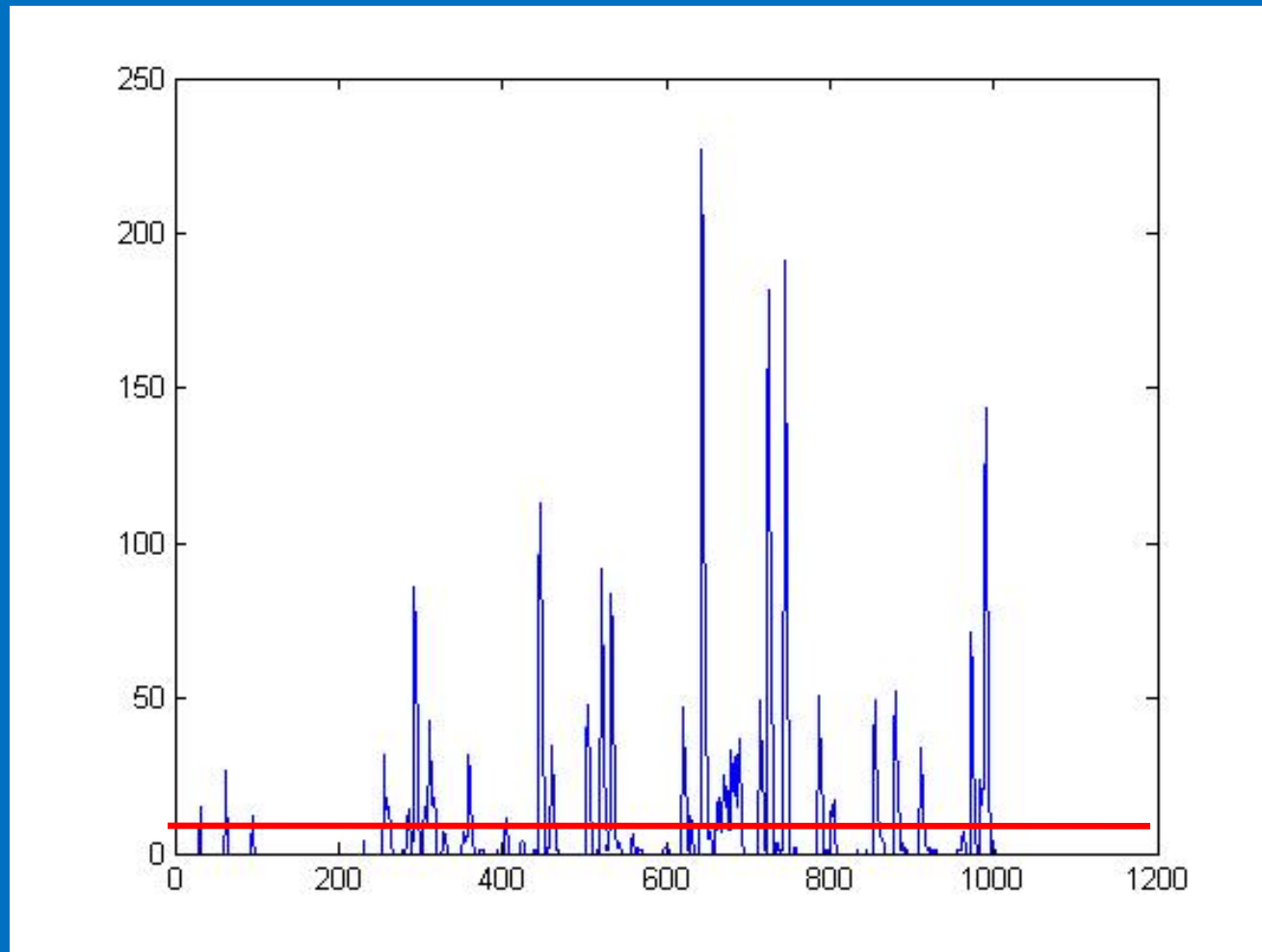
Induced signal (rise 100ps) with long ion tail (tenths usec)

# Alice TPC: ALTRO



**PreAmplifier Shaping Amplifier = PASA**  
**ALice Tpc Read Out = ALTRO**  
**Two-chips system, 4x7.5mm pads**

# Why an ADC and DSP based architecture?



**Using a binary system, a threshold is set according to the noise level**

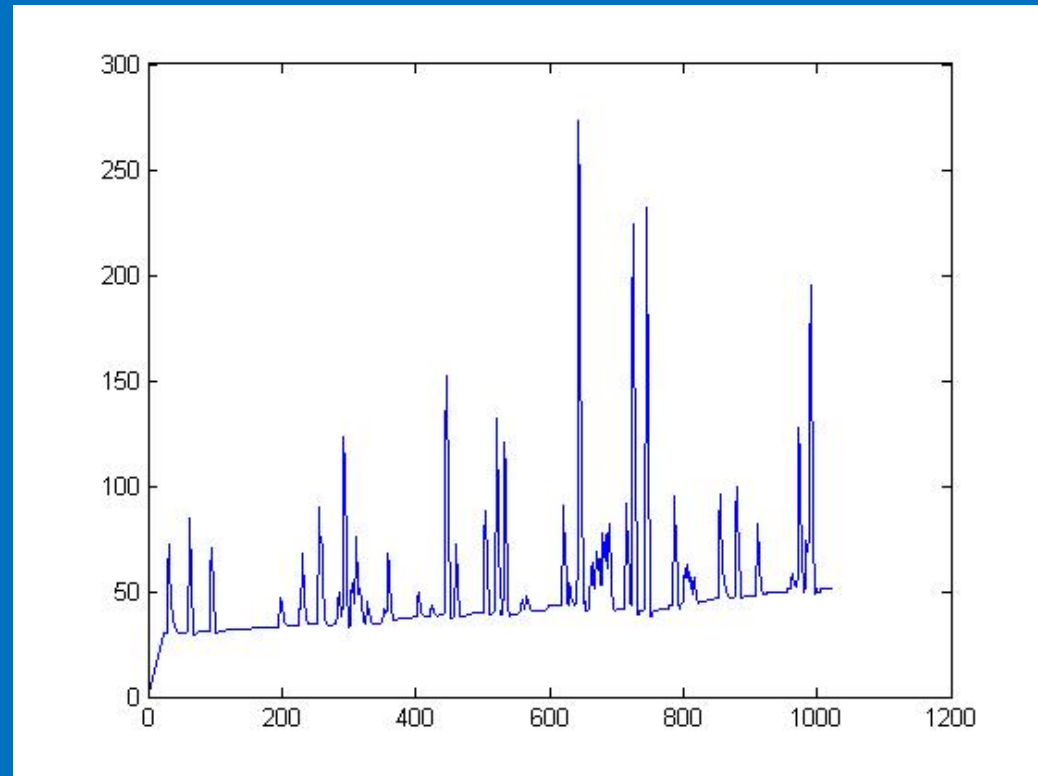
# Why an ADC and DSP based architecture?

**With an “unfriendly” detector...**

**Using a binary system, how can I set a threshold?**

**Low threshold => always 1**

**High threshold => miss small events**



**Additionally:**

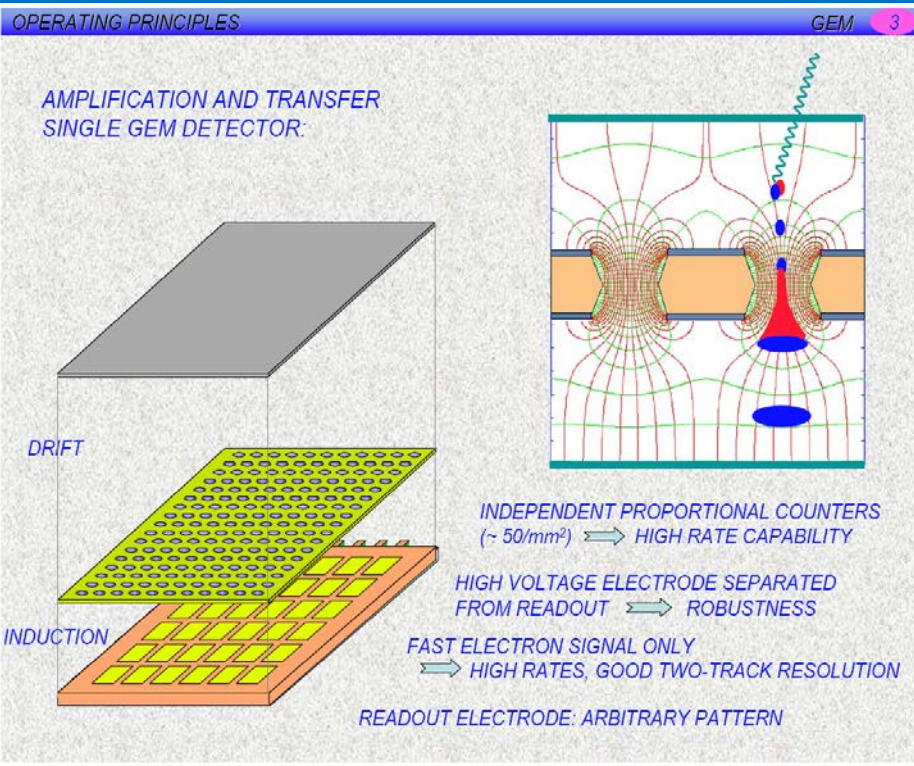
**Pulse distortions, pile-up**

**Baseline drift, error in the amplitude measurement**

**=> One ADC per channel and a Digital Signal Processor are needed**

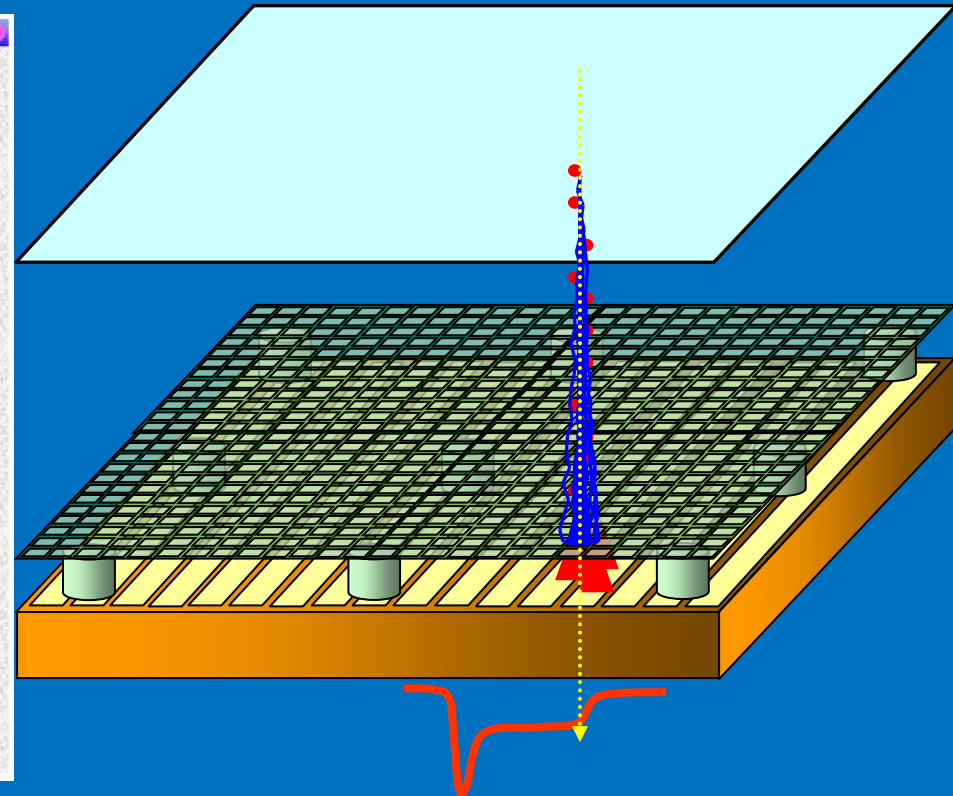


# GEM, MicroMegas



**Yulan Li, Beijing TPC School, 2008**

**GEM: electron-induced signal (20ns rise, 100ns pulse duration)**



**Paul Colas, Beijing TPC School, 2008**

**MicroMegas: fast collected signal with ion tail (100nsec)**

# Motivation for the Super-ALTRO

## **Alice, high-luminosity LHC:**

**increased multiplicity (quicker electronics)**

**GEM for continuous readout**

## **Linear Collider TPC (LCTPC), CLIC/ILC:**

**pads as small as 1x4mm, GEM/MicroMegas readout, beam pulses**

**CLIC = 1msec x 5Hz**

**ILC = 177ns x 50Hz**

## **S-ALTRO requirements:**

**Small size**

**Handling signals of both polarities, variable gain and shaping time**

**10bit, 40MHz sampling**

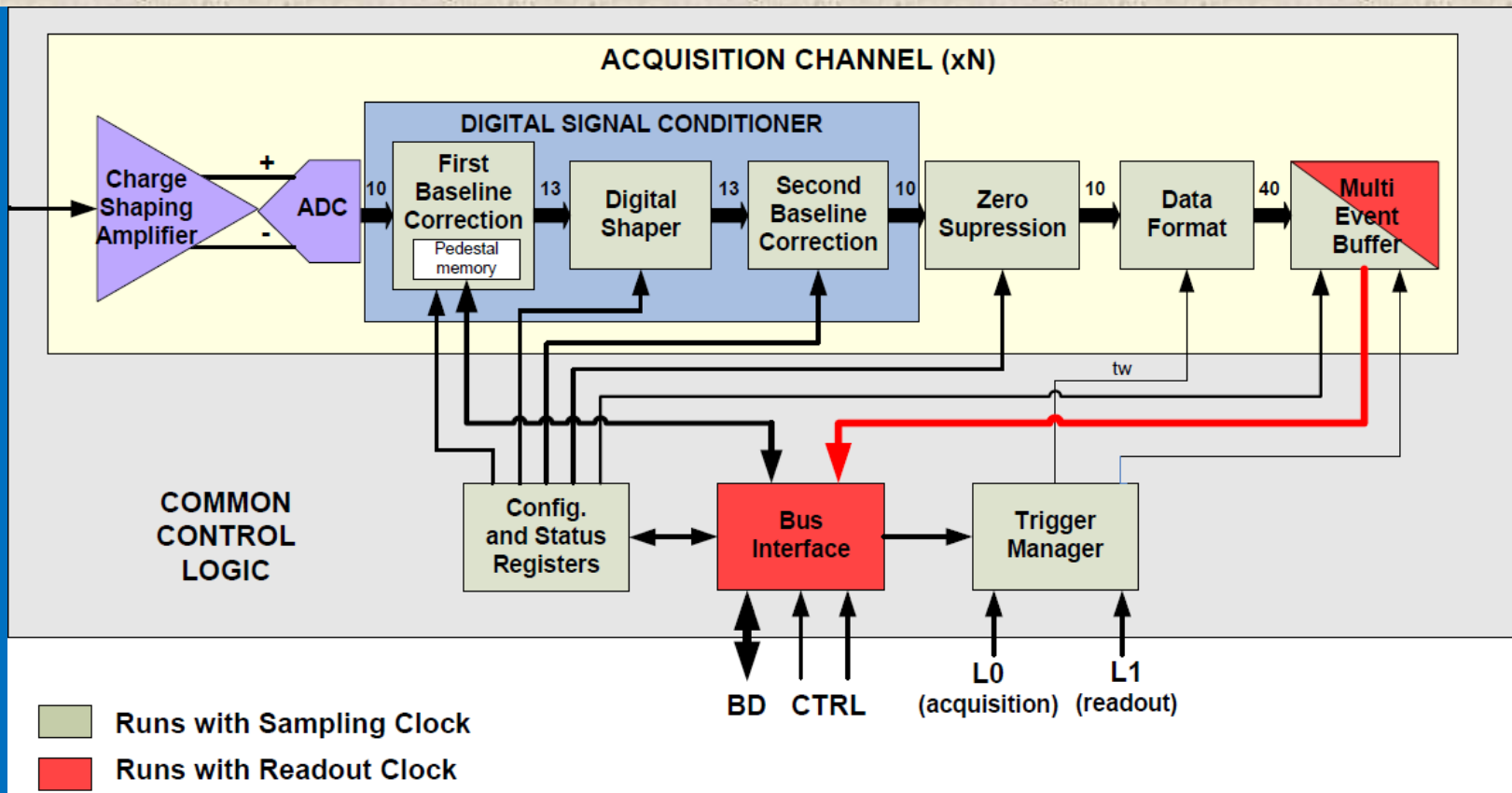
**Advanced DSP capabilities and zero suppression**

**Power pulsing (peculiarity of CLIC/ILC beam timing)**

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# System architecture



**Level 1: Starts the data acquisition.**

**Level 2: Validates data from previous L1.**

**BD : 40 bit bidirectional bus; 20 bits address + 20 bit data.**

**CTRL : 6 bits.**

**Sampling clock : max 40MHz. Readout clock : max 80MHz.**

# Project overview

## **Application:**

**Designed mainly for the readout of the LC TPC.  
Tests of GEM and MicroMegas.**

## **Fundamental data requirements:**

**Signal charge, channel number and a time stamp.  
Data processing of 100us of data sampled at 10MHz (25us @40MHz).**

## **Goal:**

**To demonstrate integration per channel of a low-noise programmable analog front-end, an ADC and Digital Signal Processor in a single chip.  
Prepare ideas for TPC readout in the ILC & CLIC (power pulsing).**

## **Architecture:**

**Based on existing PASA + ALTRO electronics for the ALICE TPC.**

## **Technology: IBM 0.13um CMOS 8RF DM.**

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# PASA specifications

Single-ended input, differential output

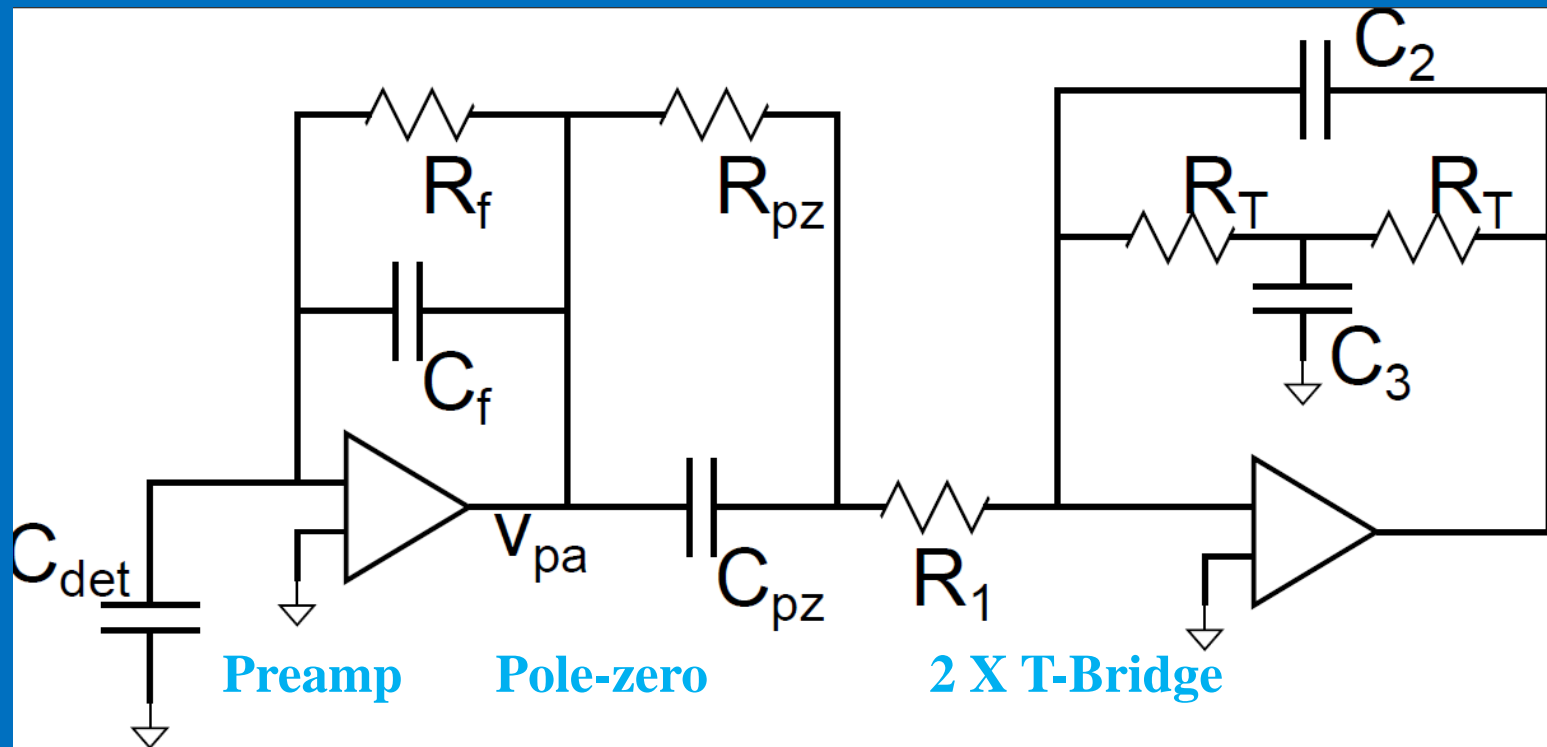
4<sup>th</sup> order CR-RC<sup>4</sup> filter

Minimum Ionizing Particle: 4.8fC

Dynamic range: 30MIP

Noise: <1000e<sup>-</sup>

Based on PCA16 prototype by Gerd Trampitsch (different technology options)



# Preamplifier/shaper

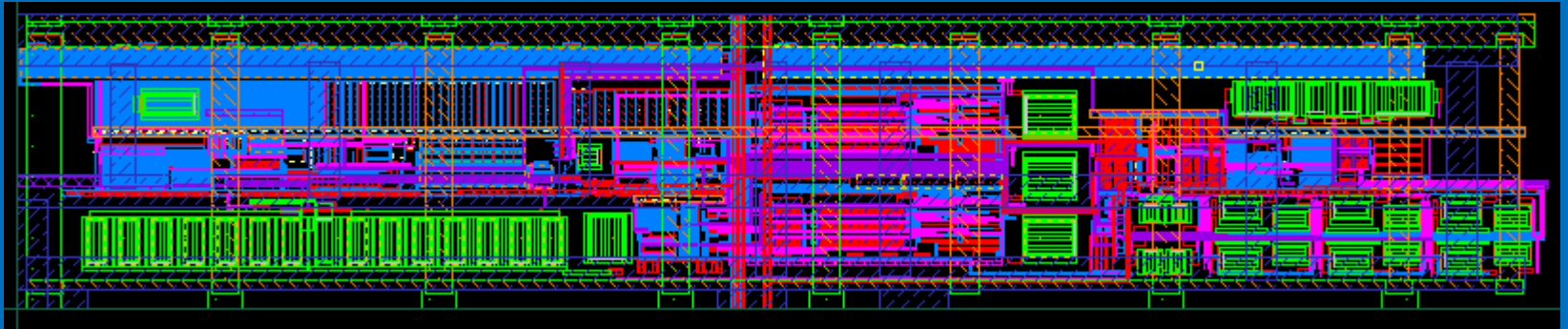
## Programmability options:

- Polarity switch
- Shutdown switch
- Preamplifier enable
- Gain control (2 bits: 12-15-19-27mV/fC)
- Peaking time control (3 bits: 30-60-90-120ns) for GEM tests
- Bias decay (analog)

Size: 1100um X 210um

Power: 8.4mW/channel

Supply: 1.5V



Feedback capacitance:  $C_f=790\text{fF}$

Input capacitance:  $C_{in}=3\text{pF}$

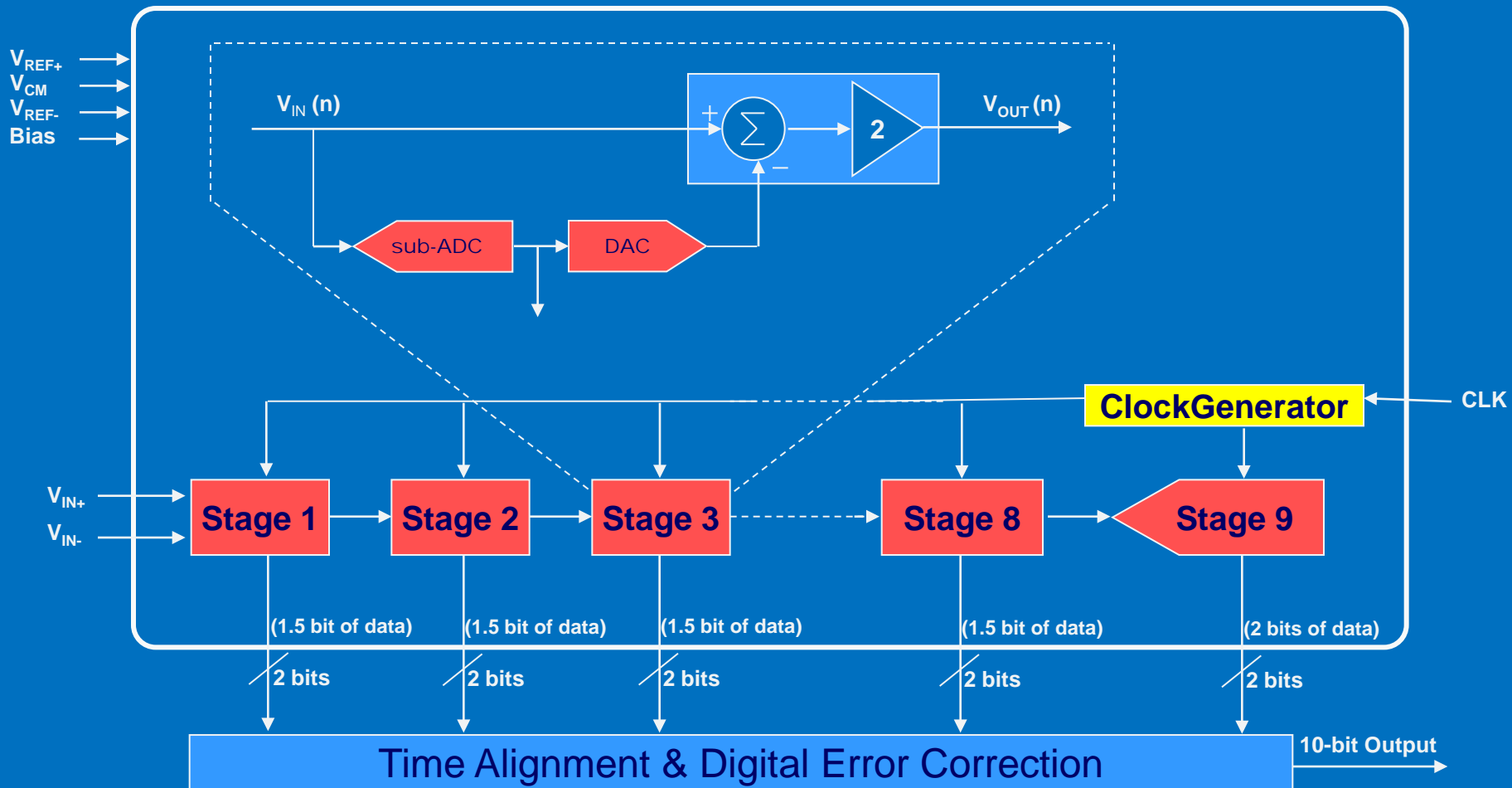
Feedback resistance: 2.3M $\Omega$ @1V, 300k $\Omega$ @0V BiasDecay



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# Pipeline ADC



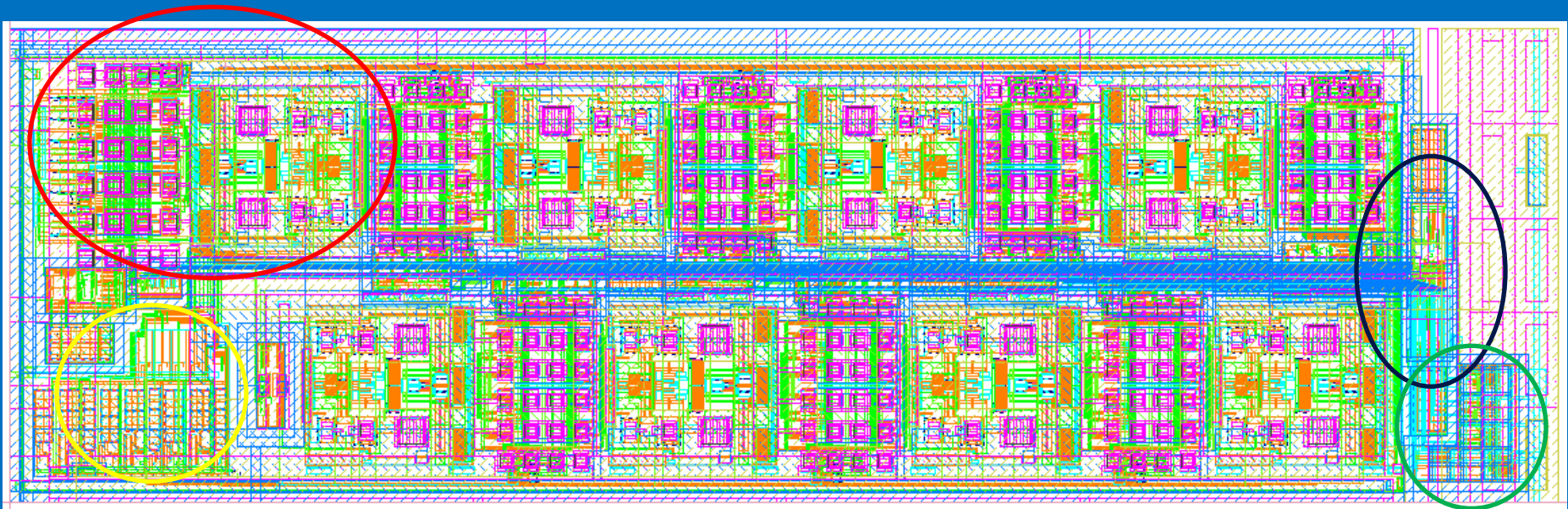
**CERN ADC prototype by Hugo França-Santos:**

**10bit, 40MHz, 1.5V supply, 34mW power, 0.7mm<sup>2</sup> area**

# Pipeline ADC

- 10 bit pipeline architecture: 8 1.5-bit stages (redundancy) + 1 2-bit flash ADC
- Optimized for 40MHz sampling frequency
- No input S/H (output spectrum of PASA is known – no aliasing)
- Double sampling (double set of sampling/multiplying caps)
- Sampling/multiplying caps 500fF (first stage), 330fF (other stages)
- $V_{\text{ref}}$  0.25V, 0.75V, 1.25V
- Dynamic comparators setting thresholds at  $V_{\text{ref}}/4$
- Transmission gates with charge injection cancellation
- Isolation analog/digital with BFMOAT and guardrings

# Pipeline ADC: layout



**First stage**

**Bias circuitry**

**Clock generator**

**Digital error correction**

**Size: 1500um X 500um**

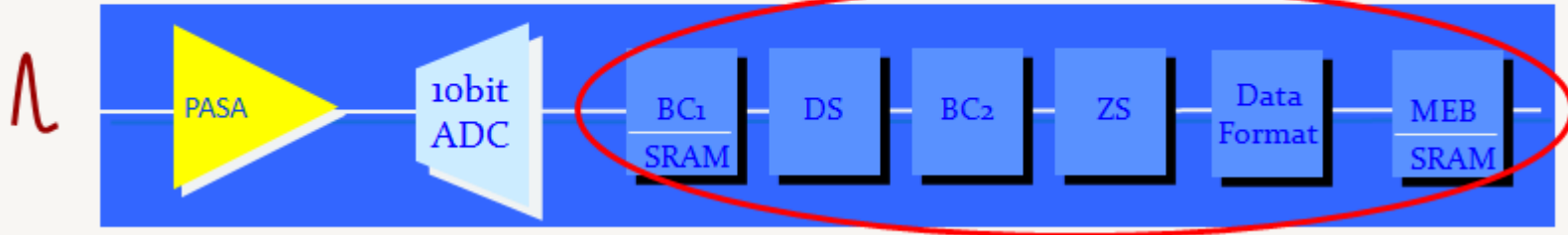
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# DSP functions

S-ALTRO acquisition channel

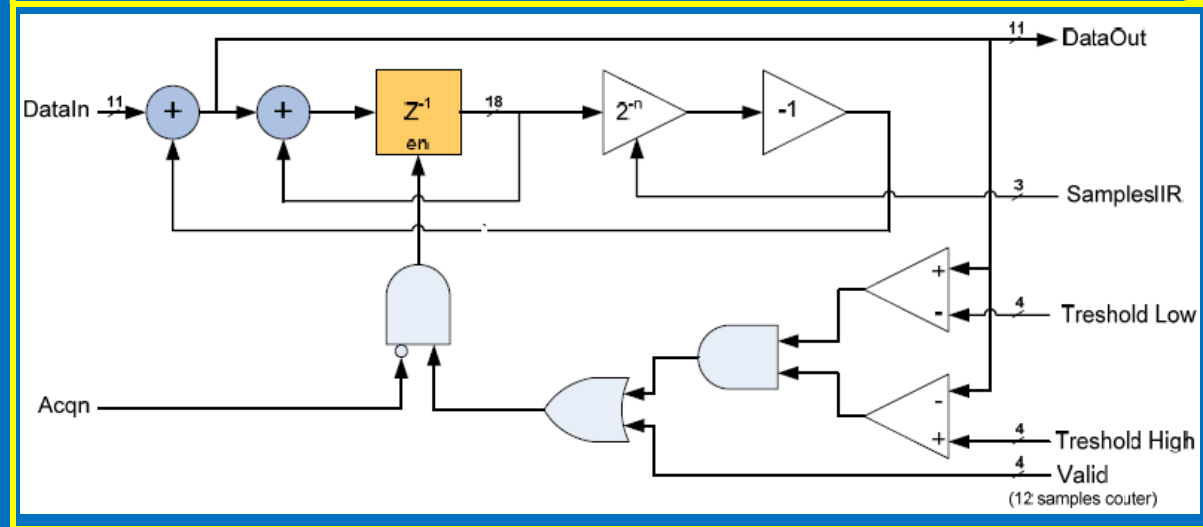
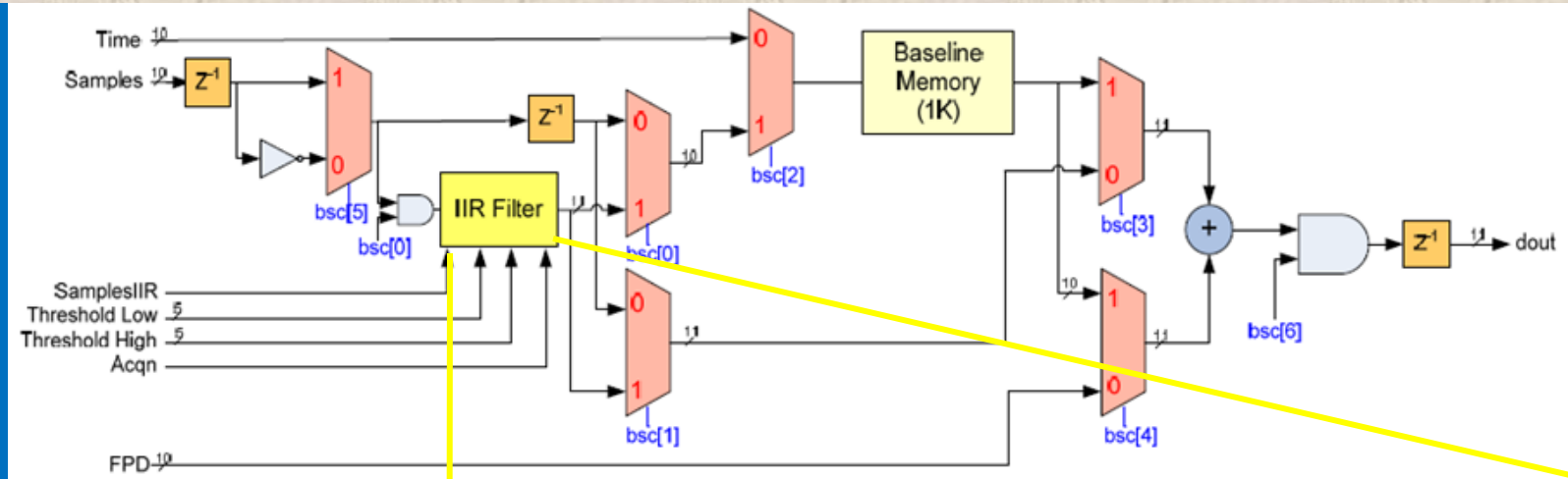
DSP



DSP design by Eduardo Garcia

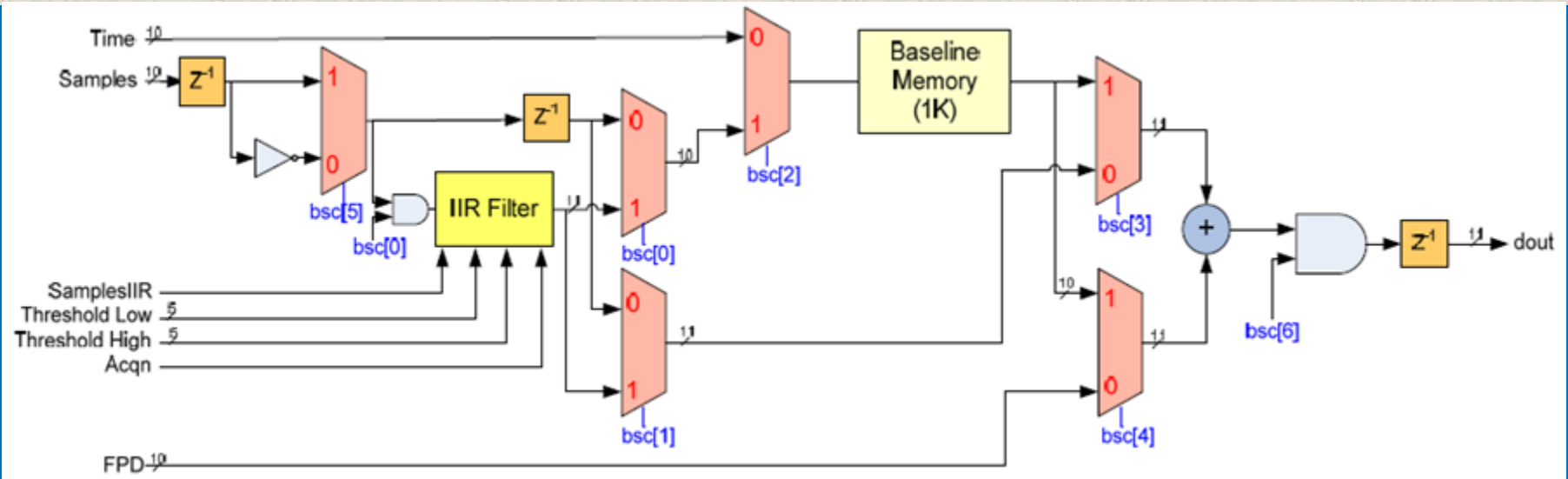
|                       |   |
|-----------------------|---|
| Baseline Correction 1 | Removes the systematic offsets that are introduced due to clock noise pickup and switching of the gating grid of the detector. A Pedestal Memory is used for storage of baseline constants which are used for look-up table correction of the baseline. |
| Digital Shaper        | General-purpose digital shaper. Example: remove the distortion of the signal shape due to long ion tails  |
| Baseline Correction 2 | Reduces non-systematic baseline movements based on a moving average filter.   |
| Zero Suppression      | Removes samples that fall below a programmable threshold.   |
| Data Format           | Converts the 10bit data stream into 40bit words including time stamp.   |
| Multi-Event Buffer    | In order to reduce the dead time of the system, data are saved in a memory for later readout.   |

# Baseline Correction 1



**The IIR filter is only active outside the acquisition window and when there is no signal; it computes the baseline at the beginning of the acquisition window.**

# Baseline Correction 1



**Fixed pedestal fpd. Variable pedestal vpd averaged outside the acquisition window (L1-L2), excluding pulses. Systematic offset  $f(t)$  stored in the Baseline Memory.**

**Most useful modes of operation:**

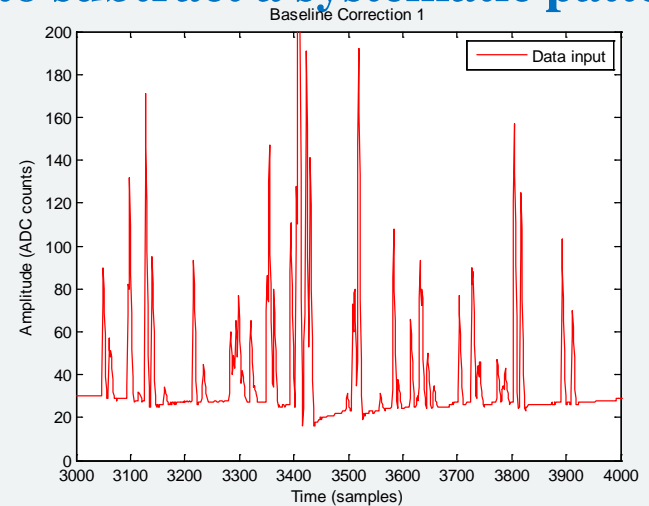
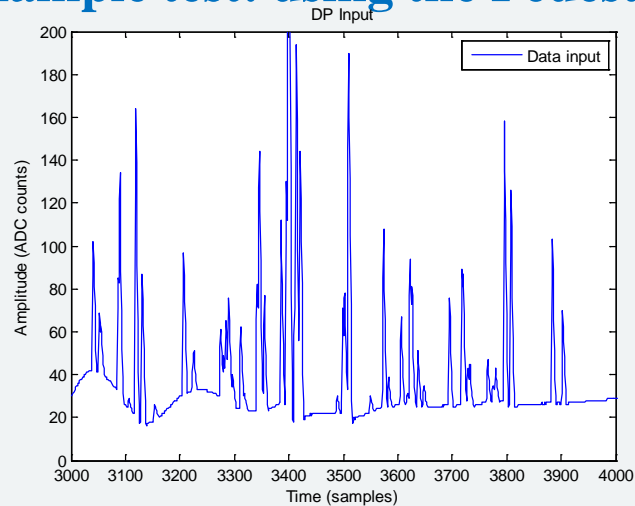
**din-fpd**

- **din-f(t)**
- **din-f(din)**
- **din-vpd-fpd**
- **din-vpd-f(t)**
- **f(t)-fpd** → very useful for test purposes

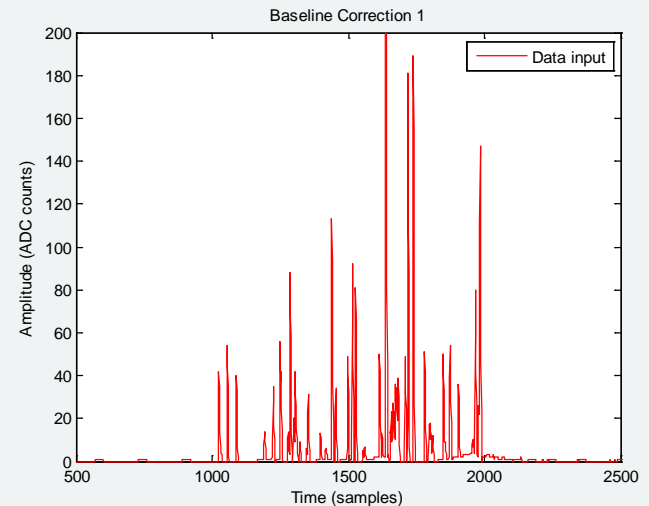
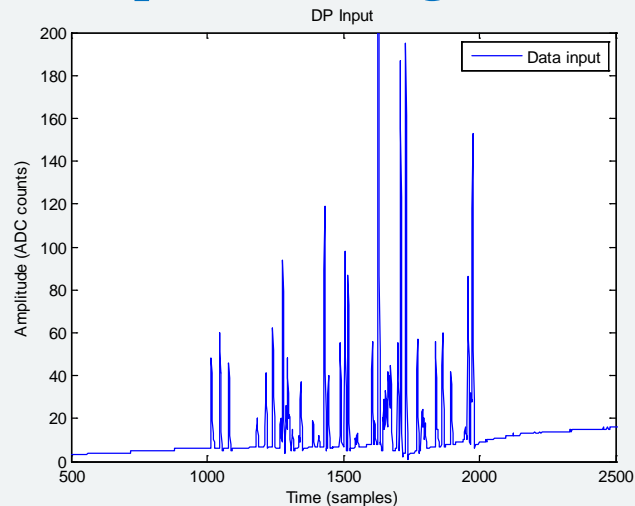


# BC1: simulation

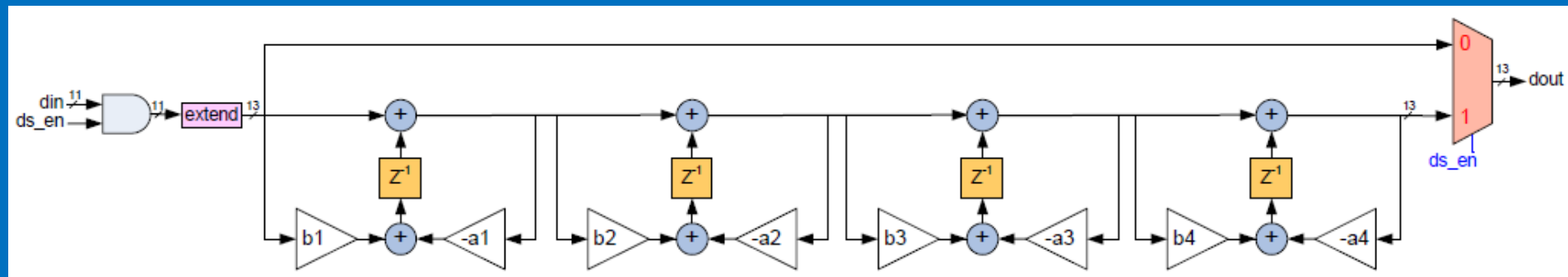
**BC1 example test: using the Pedestal Memory to subtract a systematic pattern.**



**BC1 example test: using the IIR filter to remove slow drifts of the baseline.**



# Digital Shaper (Tail Cancellation Filter)



$$F(z) = \frac{1 + L_1 z^{-1}}{1 - K_1 z^{-1}} \cdot \frac{1 + L_2 z^{-1}}{1 - K_2 z^{-1}} \cdot \frac{1 + L_3 z^{-1}}{1 - K_3 z^{-1}} \cdot \frac{1 + L_4 z^{-1}}{1 - K_4 z^{-1}} \quad \forall 0 \leq K_i, L_i < 1$$

**Cascade of 4 first order filters.**

**Programmable coefficients L1-L4, K1-K4 set the poles and zeroes of the transfer function. Long signal tail or undershoot can be corrected by proper choice of these 8 coefficients.**

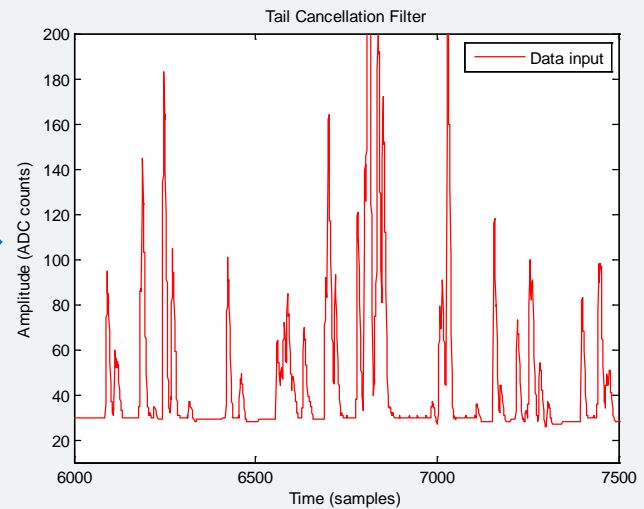
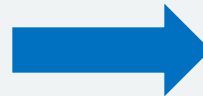
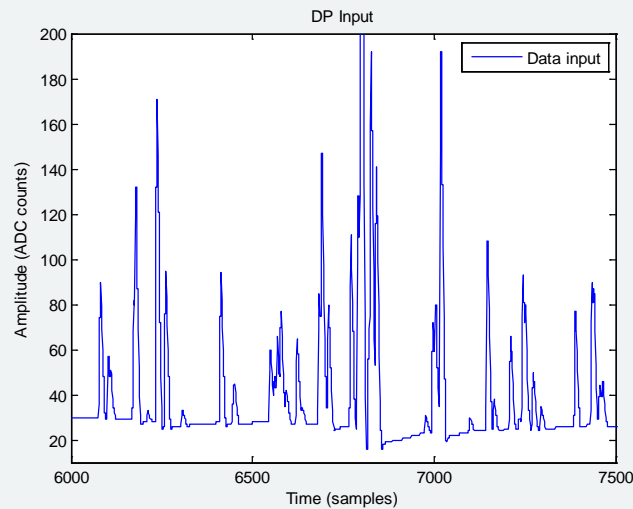
**Internal resolution 12bits.**

**ALTRO: 20442 gates**

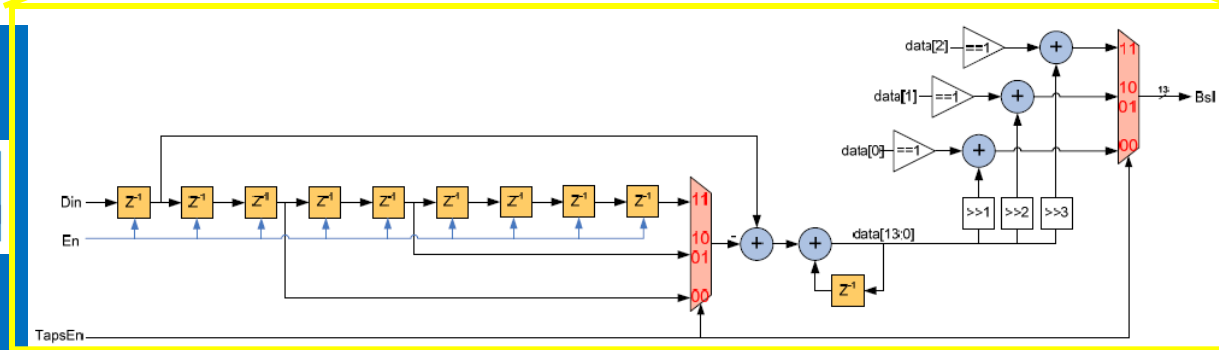
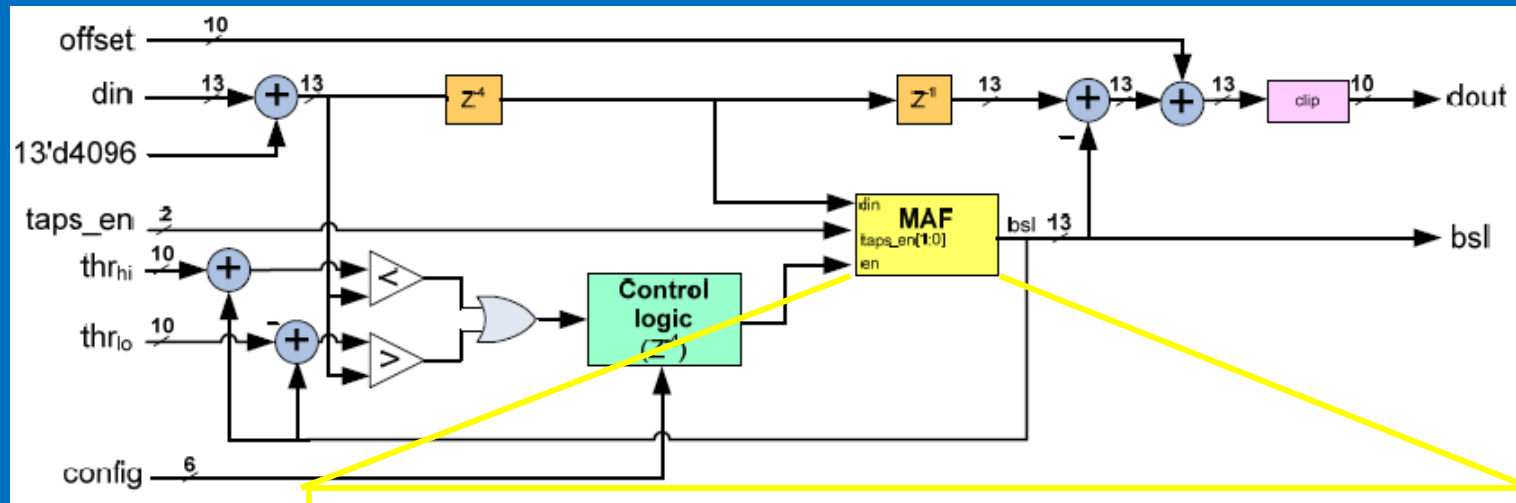
**Super-ALTRO: 11217 gates (change in architecture)**

# Digital Shaper: simulation

**DS example test: removing the undershoot of the analog pulse.**



# Baseline Correction 2



$$F(z) = z^{-1} \left[ 1 - \frac{1}{N} (1 + z^{-1} + z^{-2} + \dots + z^{-(N-1)}) \right]$$

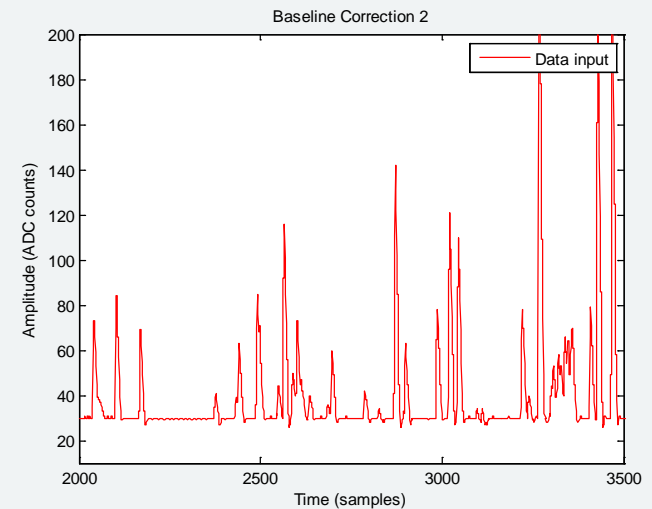
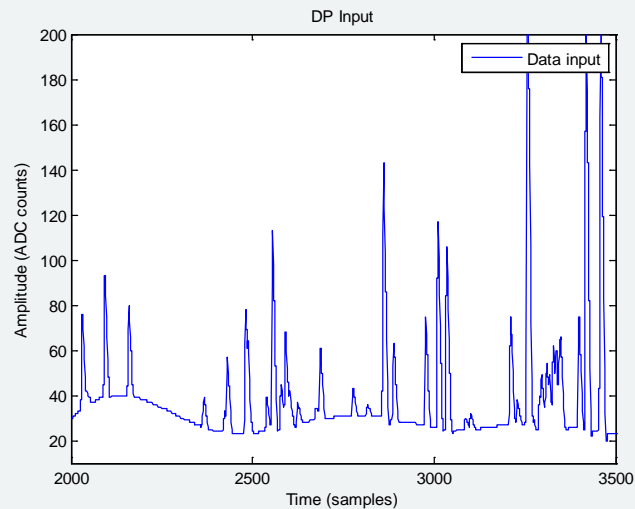
**Global threshold + per-channel (noise) thresholds, to average only the baseline and not the pulses.**

**Programmable number of samples (speed of the Moving Average Filter).**

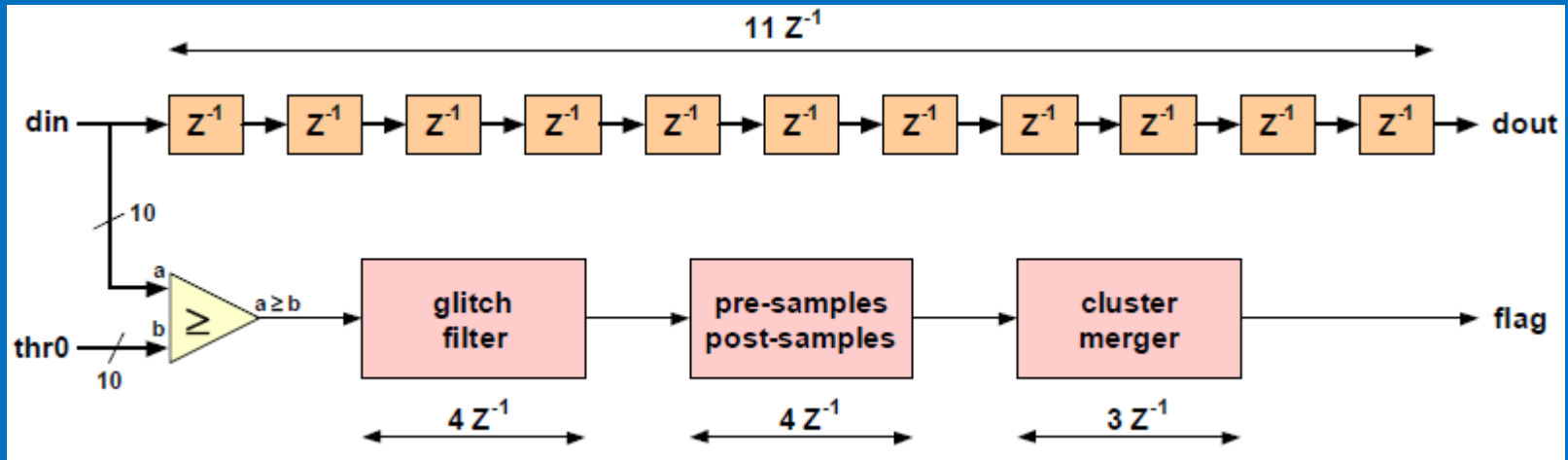
**SNR improved as compared to ALTRO, due to round-off instead of truncation.**

# BC2: simulation

**BC2 example test: computing and removing a baseline fluctuation during the acquisition.**



# Zero Suppression



**Per-channel threshold.**

**Possibility to skip glitches.**

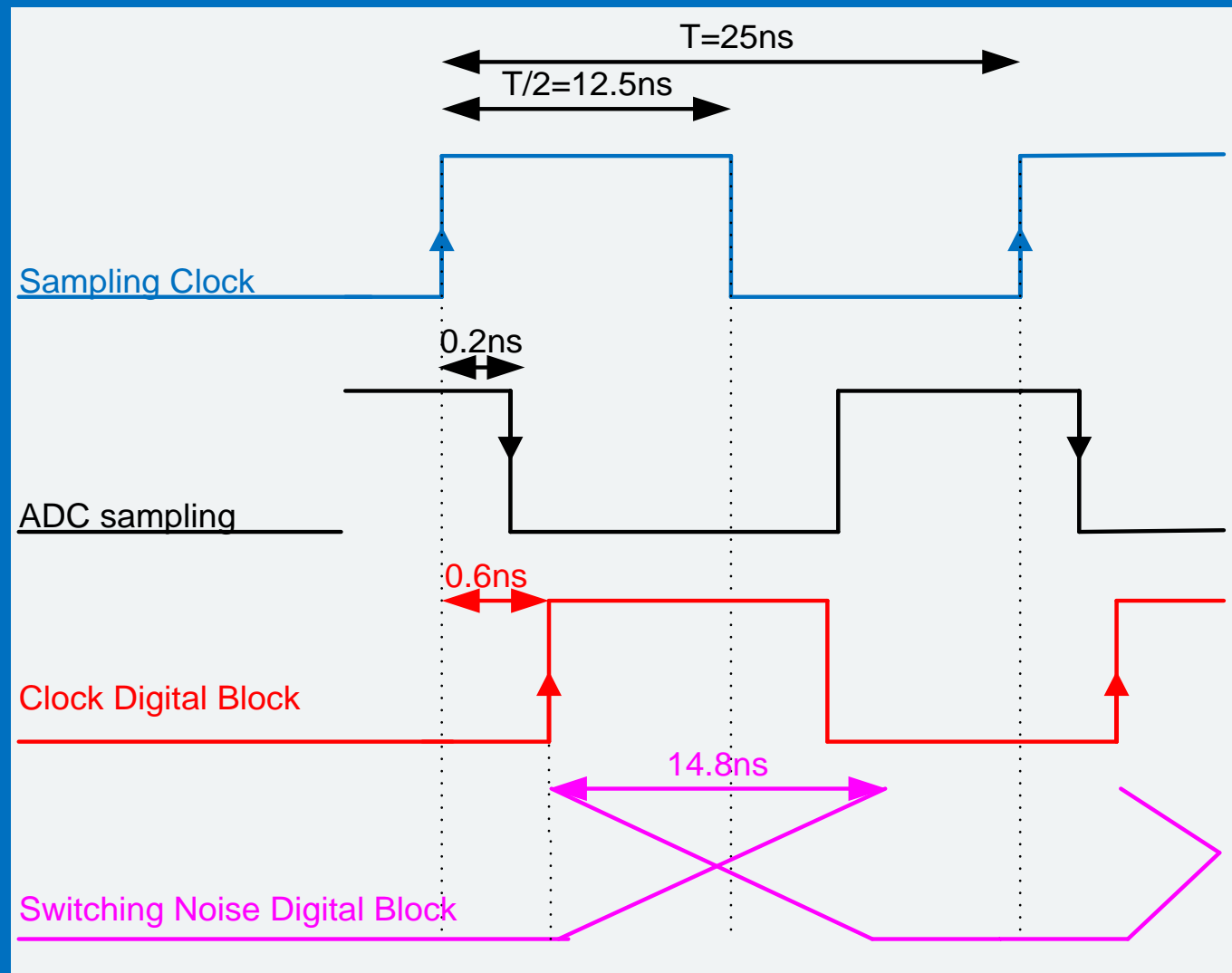
**Possibility to store pre- and post-pulse samples.**

**Possibility to merge together consecutive pulses.**

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# Clocking scheme

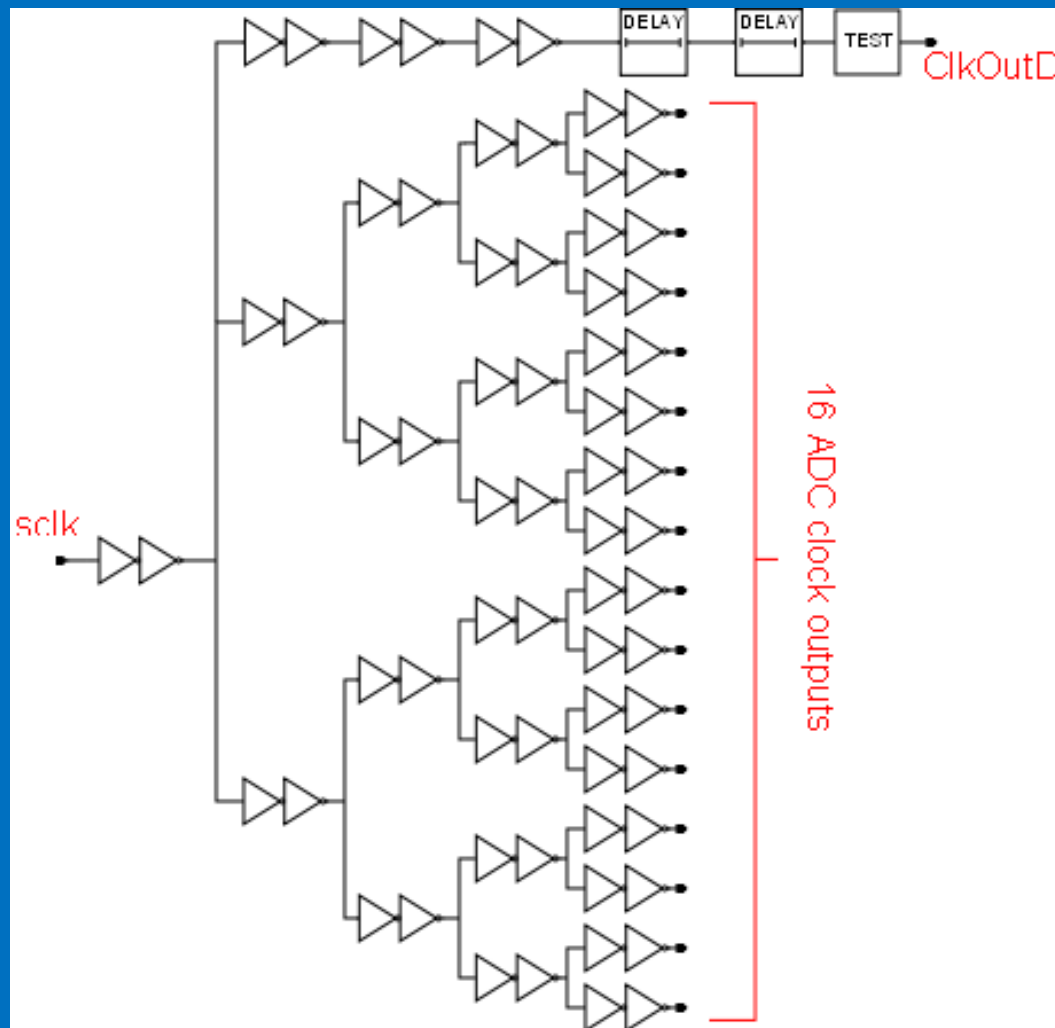


**Shown in red shading: part most sensitive to noise**



# Clock tree: design

Input clock



Clock Digital Block

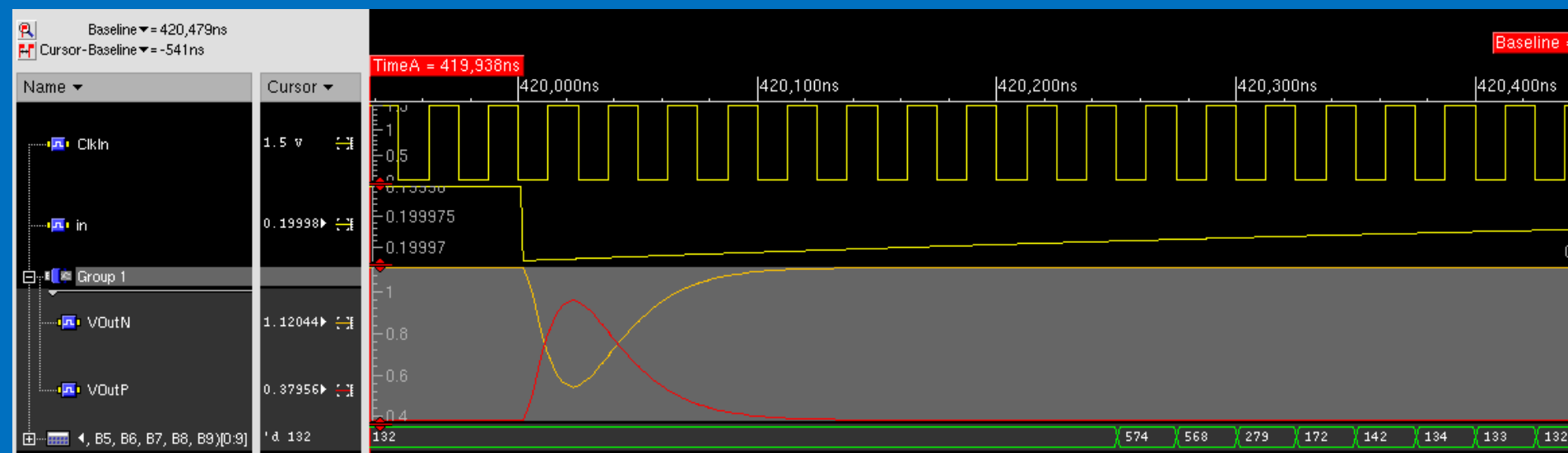
Clock 16 ADCs

Buffer the clock to the 16 channels, deliver a delayed clock to the digital block.  
Fully symmetrical structure (also in layout)

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# Front-end: Verilog-AMS model



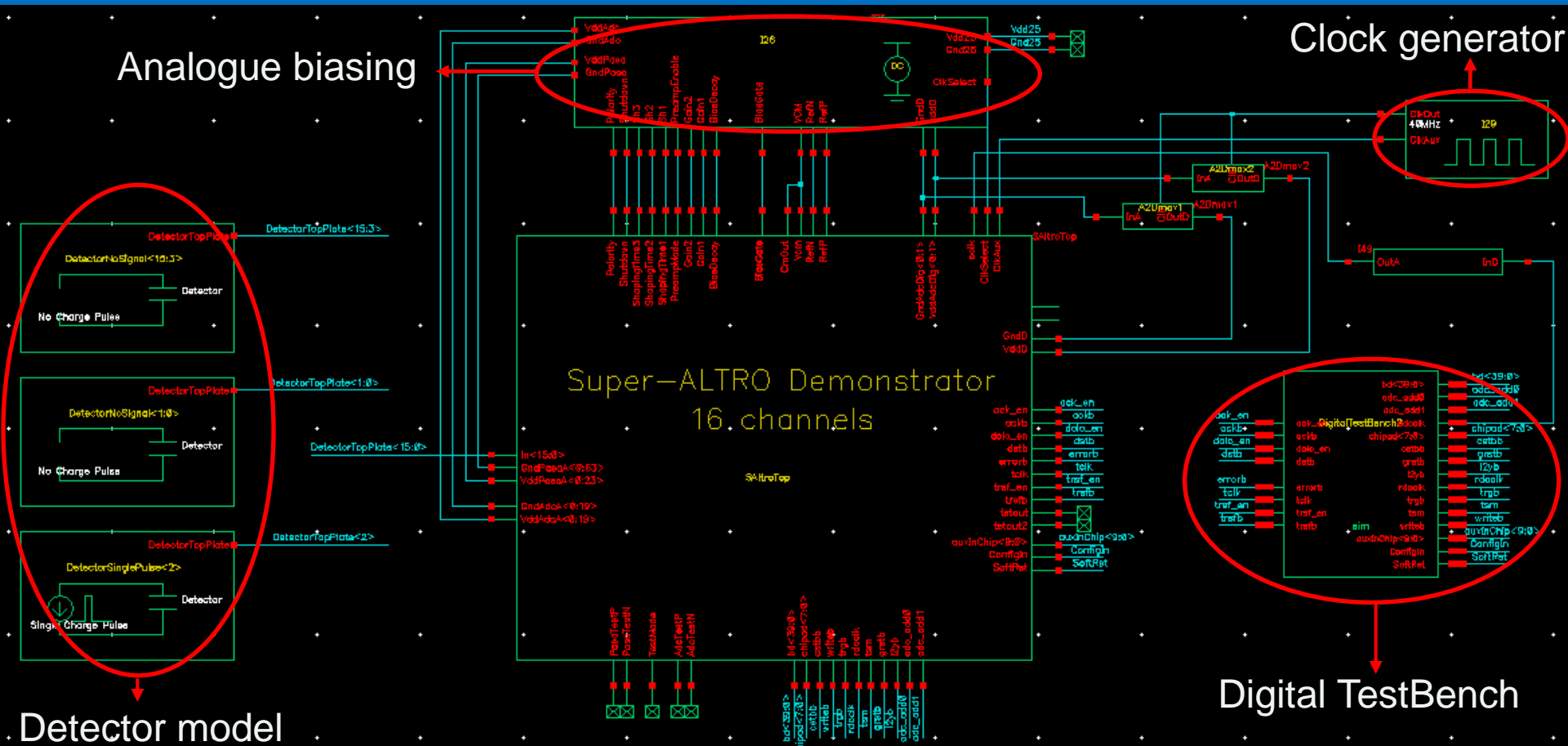
**Verilog-AMS model developed for the PASA and the ADC.**

**PASA: the model produces waveforms similar to the schematic simulations**

**ADC: the model was verified to produce the same results, with the same latency, as the schematic (within the resolution of the schematic model of the ADC).**

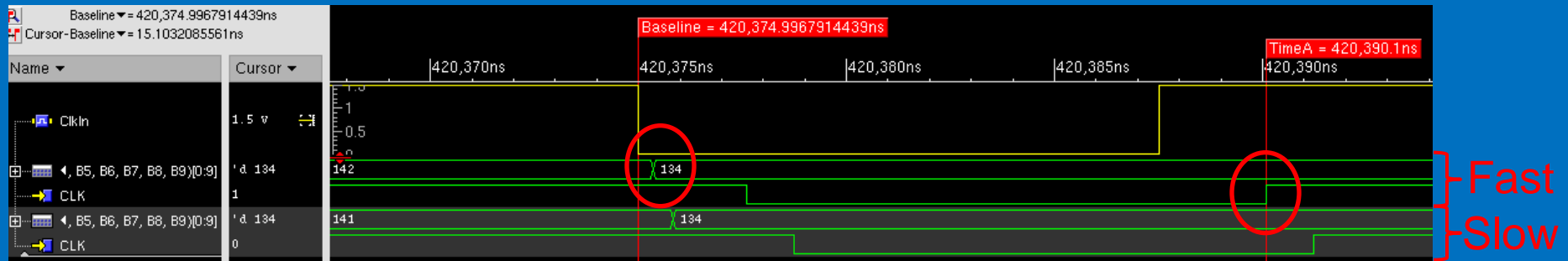
# Mixed-mode top level simulation

- **Goal: simulation of the full acquisition chain.**
- **Possible using Verilog-AMS and Verilog descriptions.**
- **This example uses a simple digital processing (input - 5 ADC counts).**

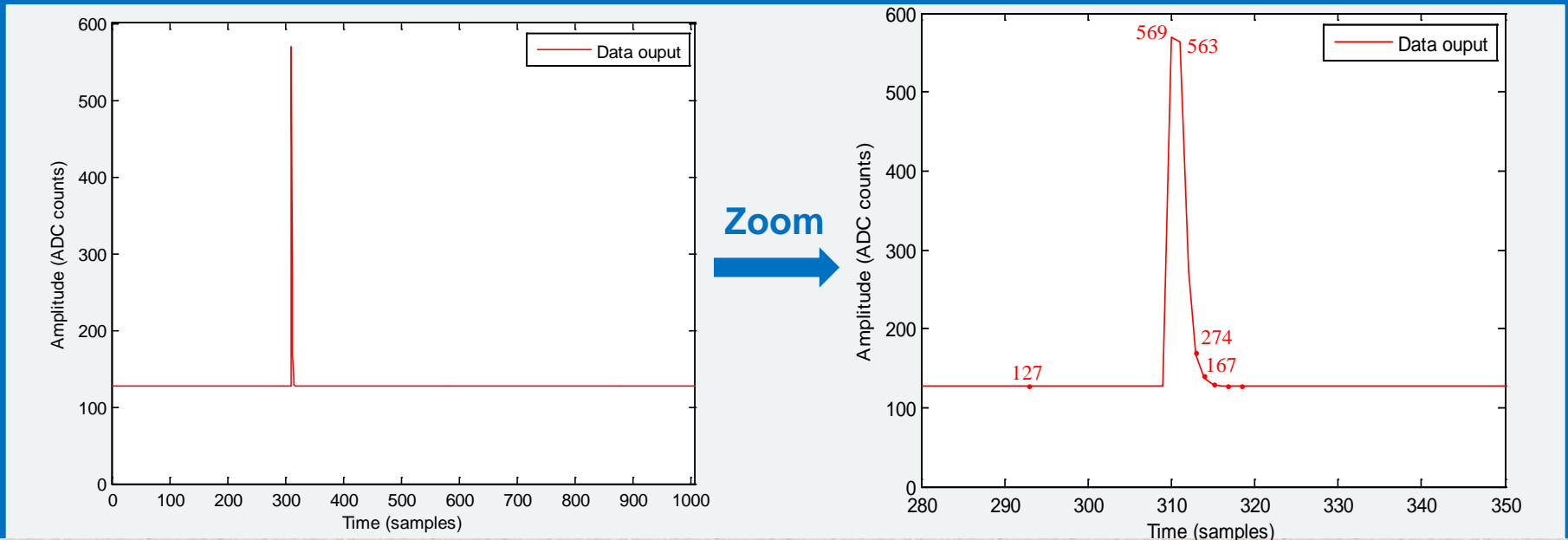


# Mixed-mode top level simulation

**Important issue: check the synchronization between the ADC output and the DSP input. Timing corners information included in Verilog-AMS models.**



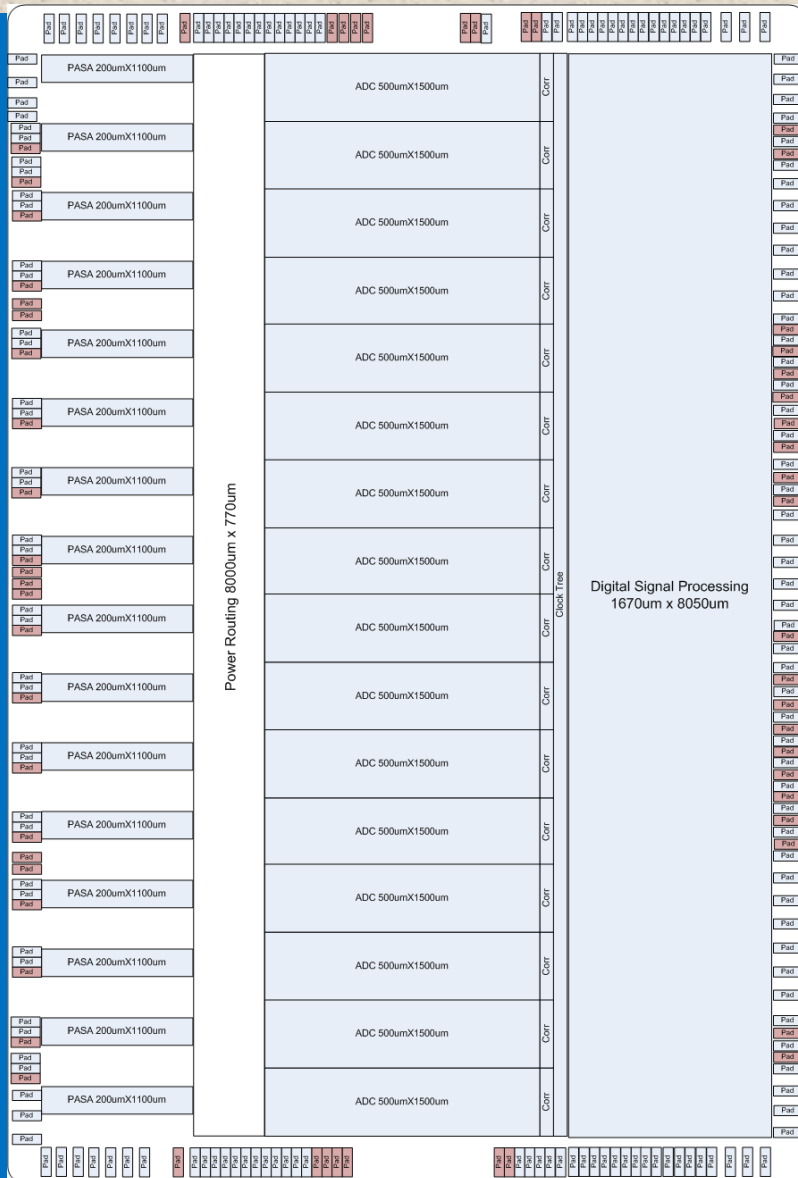
## Readout of one S-ALTRO channel:



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# Super-ALTRO Demonstrator Floorplan



**16-channels:**

**PASA**

**210um X 1100um**

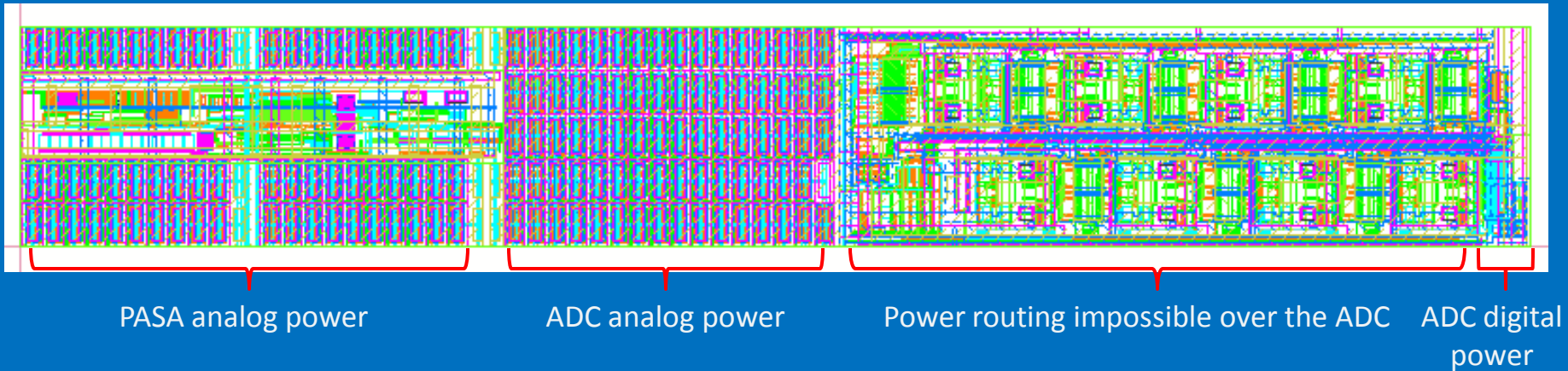
**ADC**

**500um X 1500um**

**Digital Signal Processing**

**1670um X 8050um**

# Front-end: layout



**Large width of the ADC analog power routing allows an IR voltage supply drop lower than 10mV. Space used for decoupling and routing of reference voltages.**

**Power supply decoupling capacitors:**

**600pF /channel PASA**

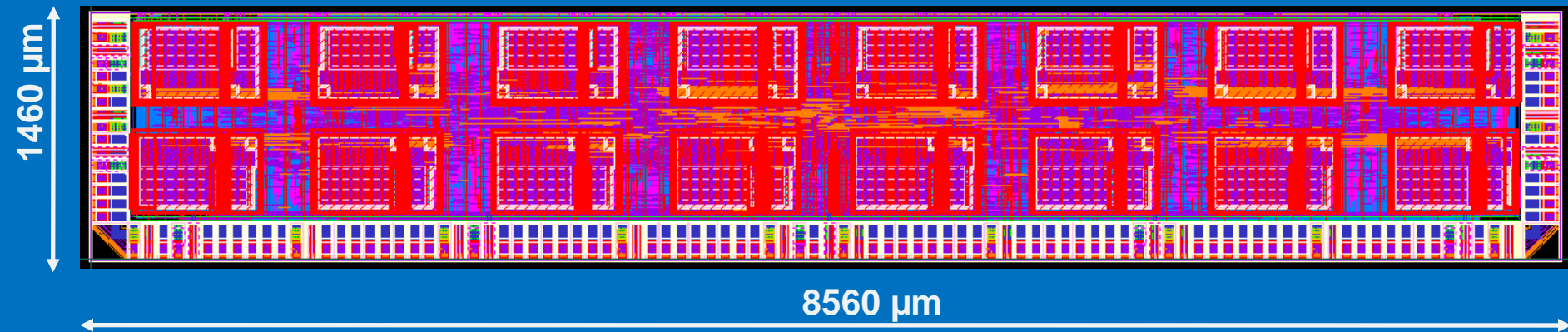
**600pF /channel ADC analog**

**40pF /channel ADC reference voltages**

**80pF/channel ADC digital**



# DSP: layout



**Most of the area is for the memories, provided by the foundry as an IP block: oversized with respect to the effective memory capacitance.**

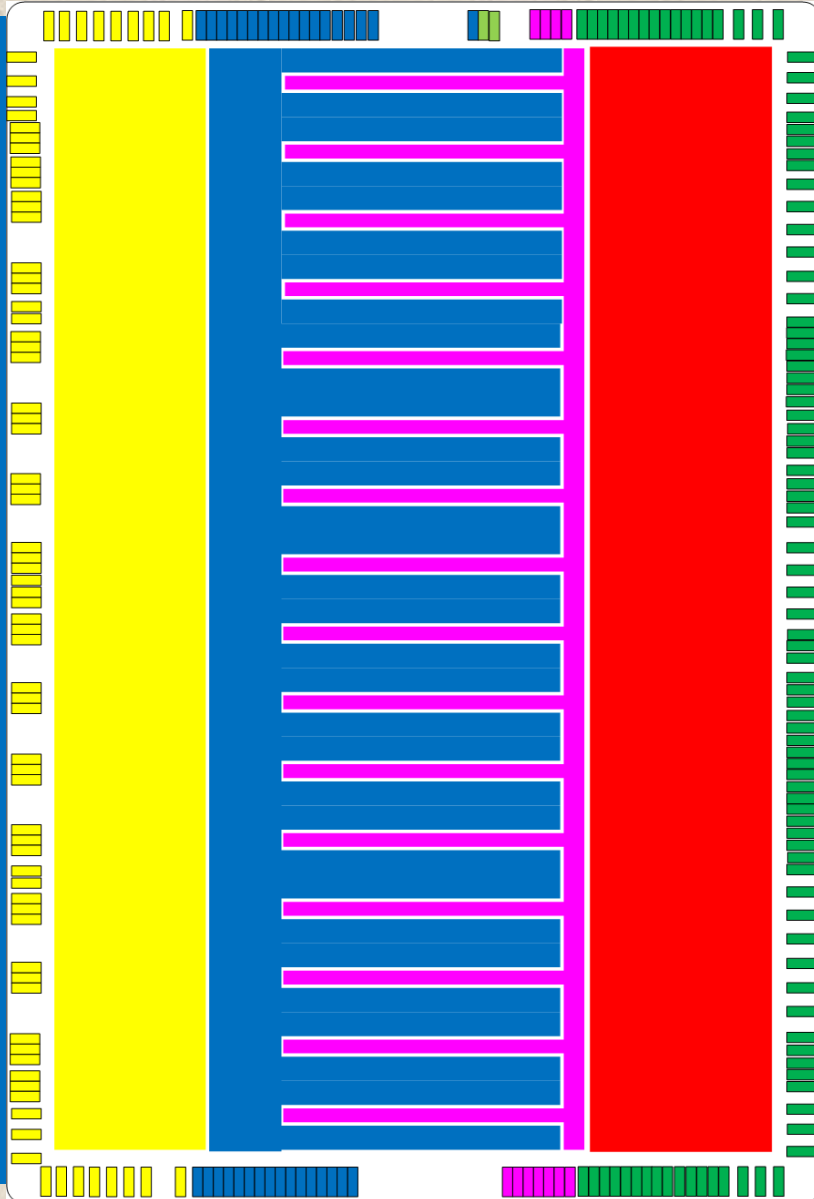
**The logic circuitry fills a fraction of the space between the memories.**

**Average power (considered in rail analysis): 118.62 mW.**

**Worst IR drop peak: 7.2 mV.**

**Pads distribution for minimum influence on the front-end.**

# Power domains



## Power domains:

PASA analog

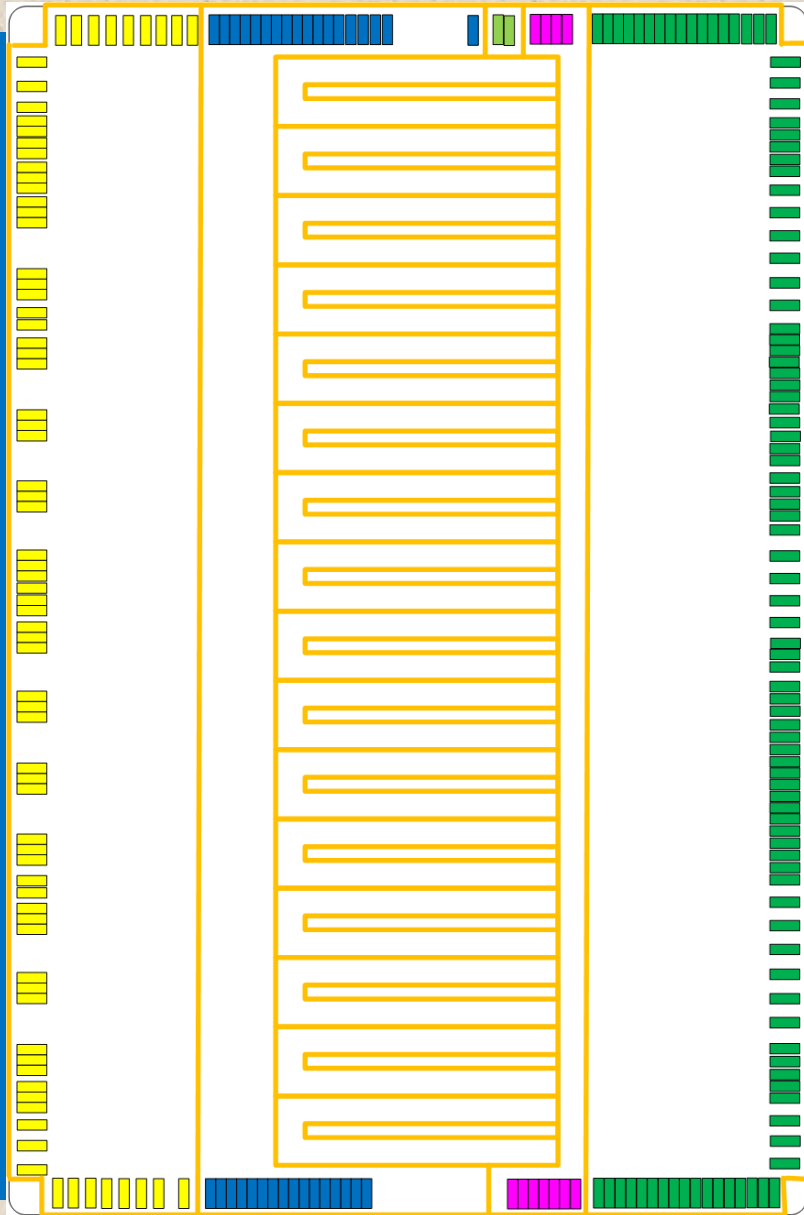
ADC analog

ADC digital

Digital core

Digital Pads

# Substrate partitioning with BFMOAT

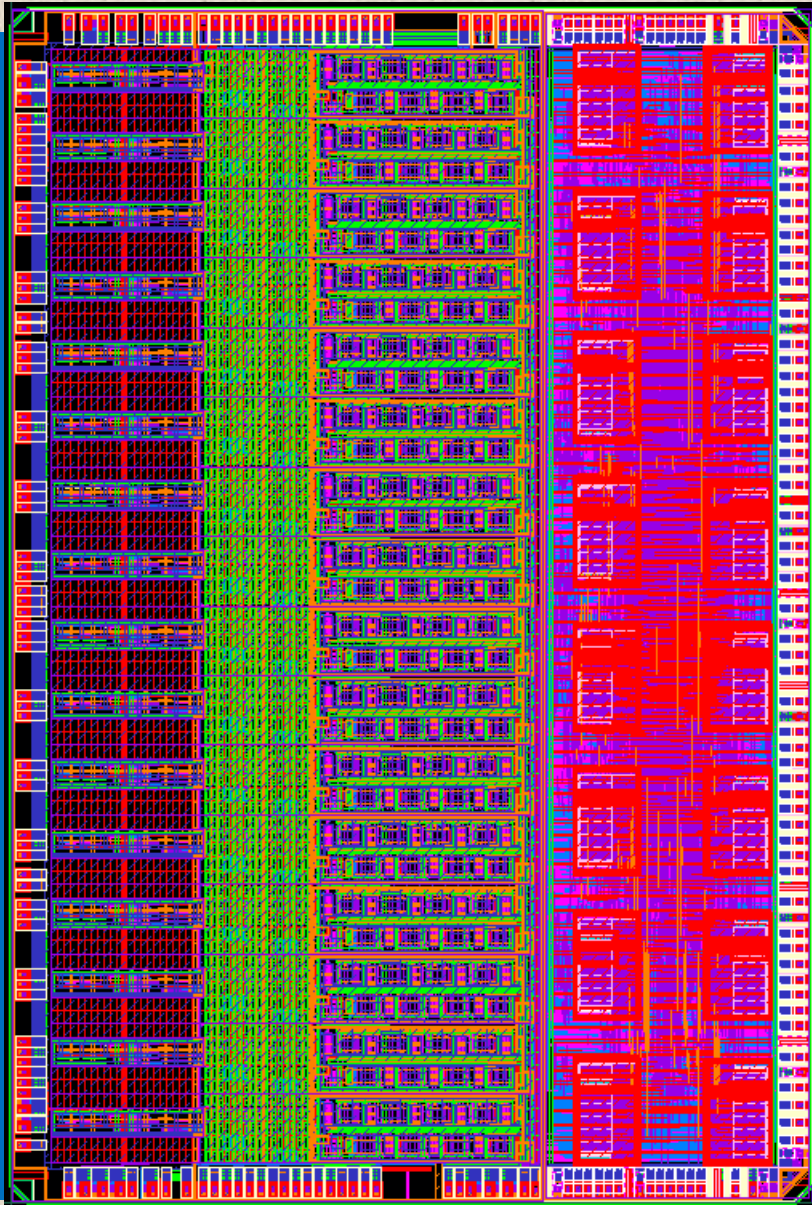


**BFMOAT: high resistivity ( $p^-$ ) substrate region, placed between different power domains to insulate them from each other.**

**The effective substrate resistance between adjacent regions depends on the width and perimeter of the BFMOAT layer.**

**NW/P+ guardrings on both sides of the BFMOAT implants**

# Final layout



**Size: 5750um x 8560um  
(49.22mm<sup>2</sup>)**

**Submitted July 2010**

**Packaged in 2 different  
packages:**

**PGA180 for testing purposes**

**QFP208 for applications**

**+ naked dies available**

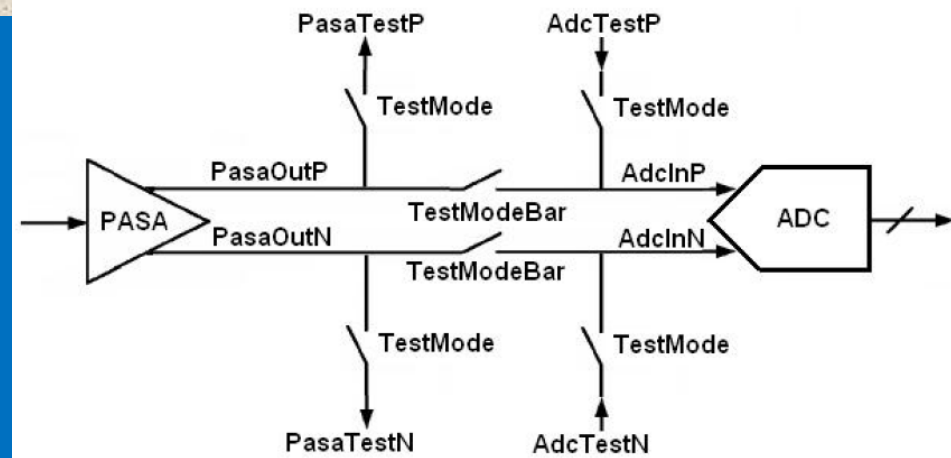
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# On-chip test/debug features

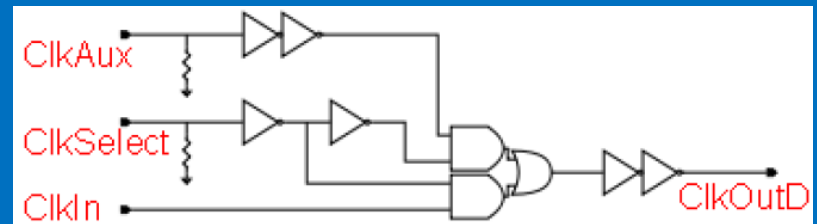
-Test mode channel 15:

Test PASA and ADC independently

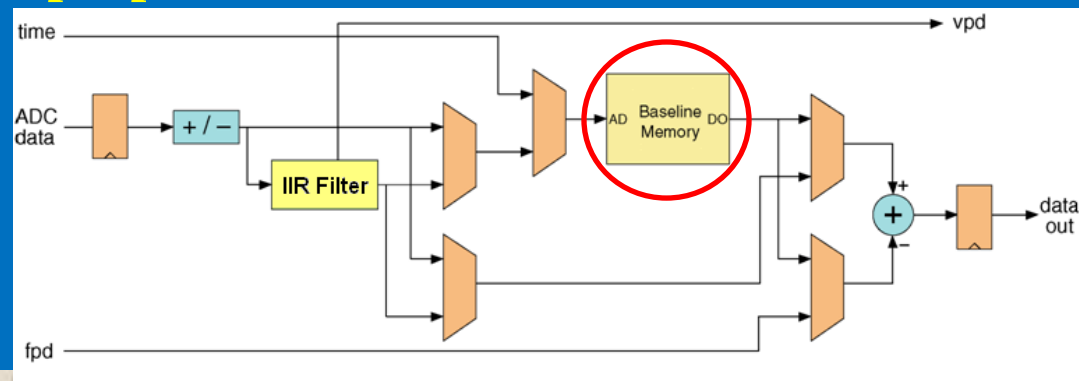


-Clock tree:

Dedicated clock to DSP, phase scan



-The baseline memory can be used to generate a pattern to be injected into the processing chain for test purposes.



# Requirements for testing

**The Test Board must be able to test each block of the Super-ALTRO independently, using the test/debug features.**

**Shutdown / power pulsing tests controlled using the Board Controller  
FPGA:**

**1) LDO shutdown (voltage regulators):**

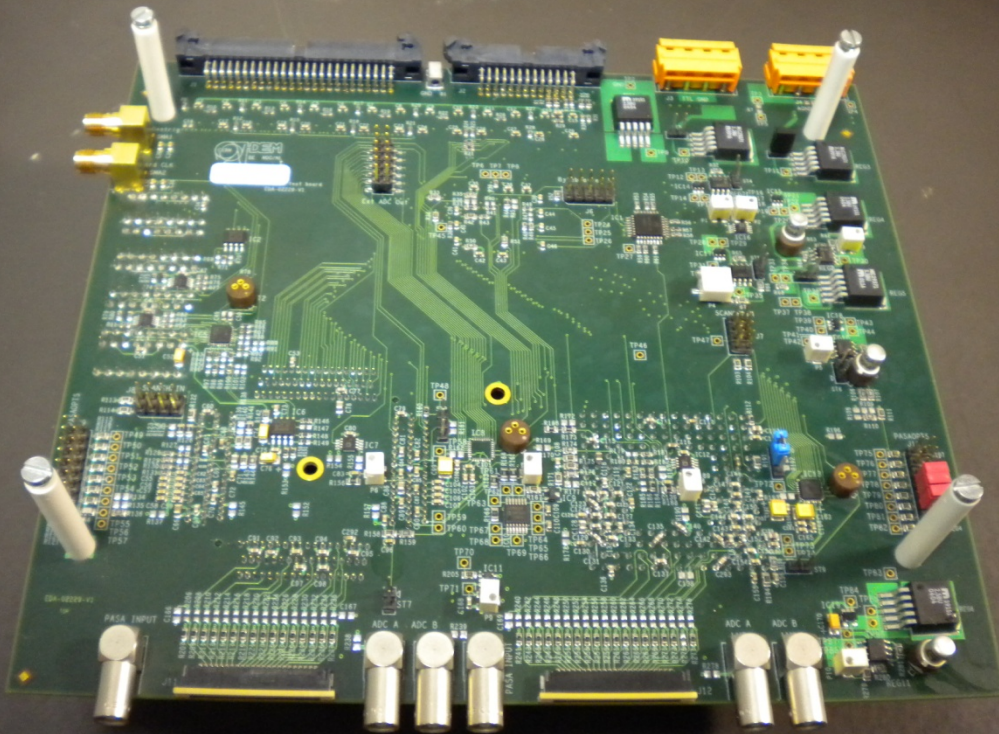
- **PASA**
- **ADC analog**
- **ADC digital, decrease the supply voltage**

**2) Smart shutdown (dedicated control lines):**

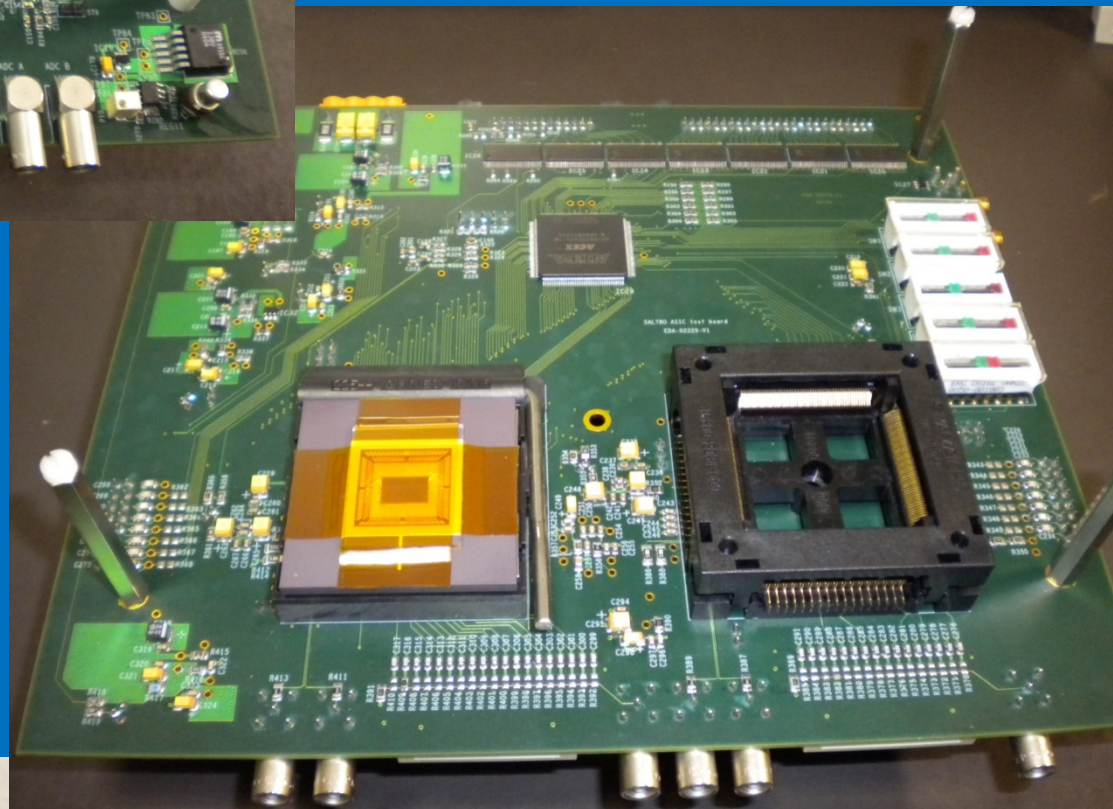
- **PASA shutdown feature**
- **ADC bias resistor switch**
- **Removal of the sampling and/or readout clock (enable lines)**

# Test Board

**Top side: Voltage Regulators, Clock Distribution, Level Shifters, external ADCs, Connectors**



**Bottom side: S-Altro sockets (PGA and CQFP), Board Controller FPGA, Transceivers**

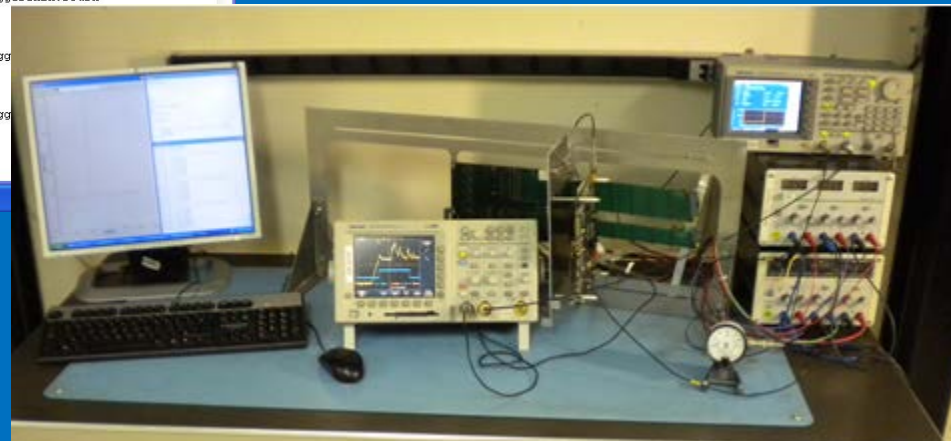




# Test GUI

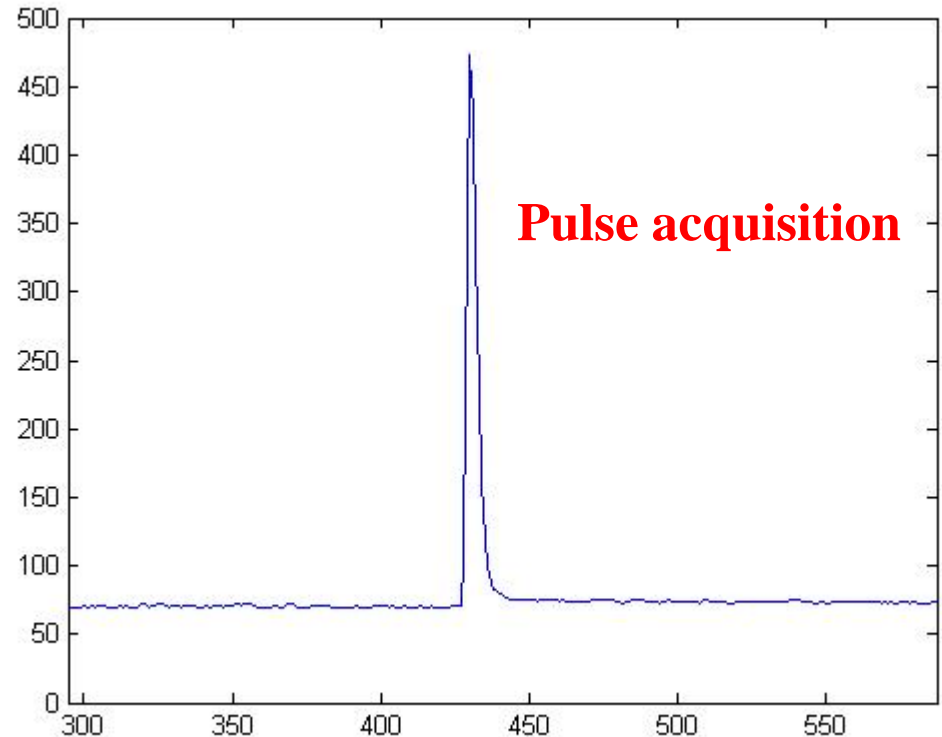
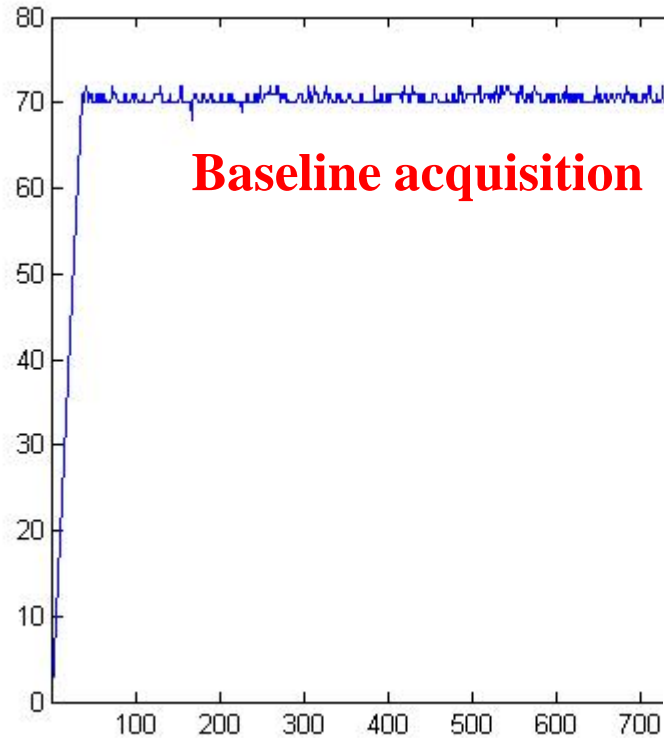
**Graphical User Interface:  
control of configuration  
registers, signal acquisitions**

The screenshot displays the SAgui.py software interface. The main window shows a tree view of hardware registers, including DDL, RCU configuration registers, RCU status registers, RCU TTC registers, RCU memories, RCU commands, FECs, and ALTROS. A settings dialog is open, showing event number (0), a dump file selection button, and a display checkbox. A terminal window shows the execution of various commands, including 'rcu-sh b Config.rcush' and 'rcu-sh b TriggerINEM.rcush'. A graph window shows ADC counts (Y-axis, -50 to 300) versus Timebins (X-axis, 0 to 1200), with a prominent peak at approximately 400 timebins.



# Example acquisitions

Examples of acquisitions with PASA gain=12mV/fC, shaping time = 120ns, input cap 1.8pF, sampling clock frequency = 20MHz



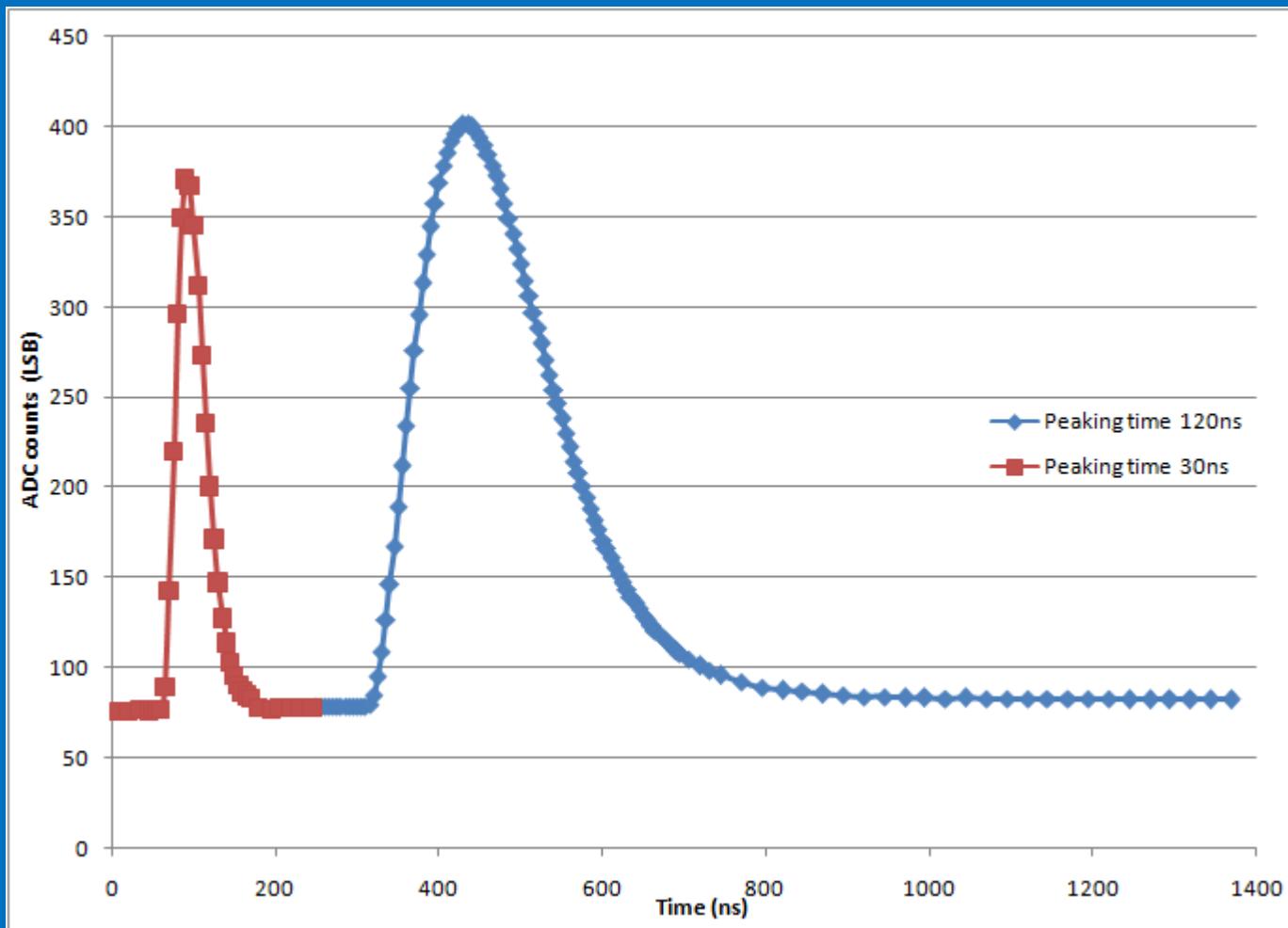
# Outline

- **Motivations for the project**
- **System architecture**
  - **Pre-amplifier shaper (PASA)**
  - **ADC**
  - **Digital Signal Processor (DSP)**
  - **Clock tree**
  - **Top-level simulations**
  - **Assembly, floorplan, layout**
- **Tests**
  - **Test setup**
  - **Measurements: gain, noise, power, power pulsing**
- **Conclusions**

# Test conditions

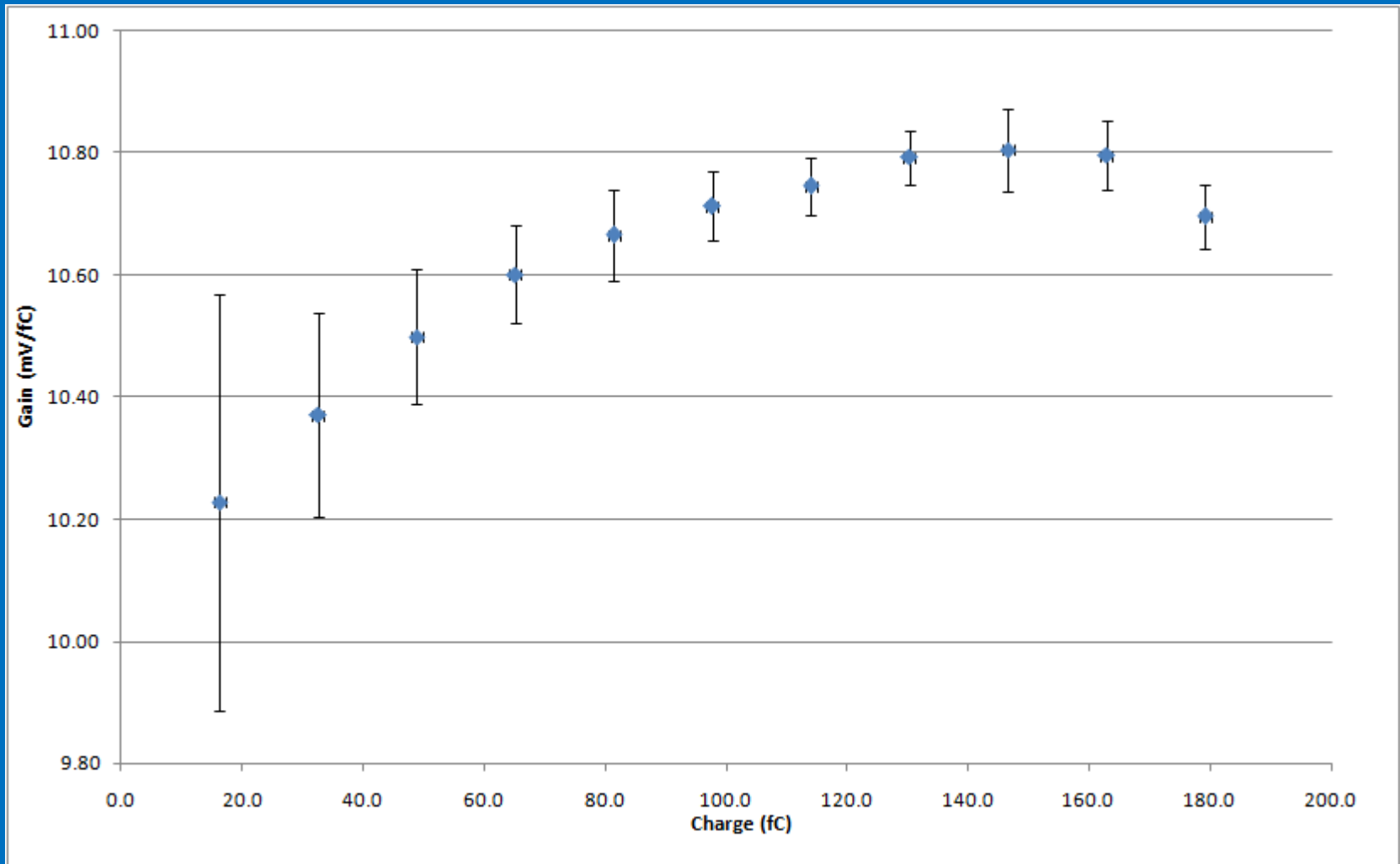
- **Sampling clock 10-20-40MHz, readout clock 40MHz.**
- **Chip PGA3: the inputs of the PASA are not bonded. This avoids noise injection from the ground plane of the test board.**
- **Chip PGA4: all inputs bonded.**

# Acquired pulses



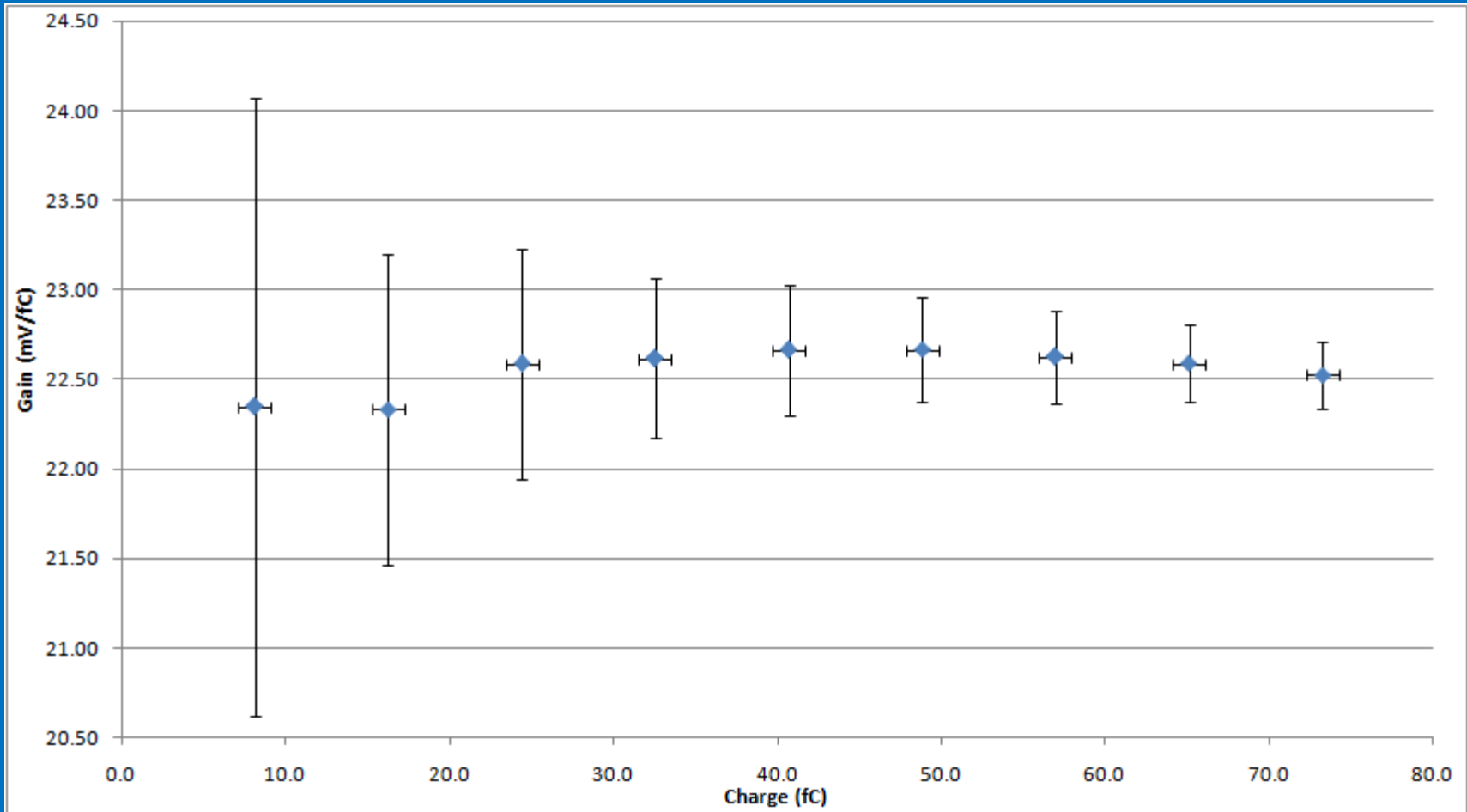
**Examples of acquisitions at 30ns and 120ns shaping time.  
Signal scan with a granularity of 5ns.**

# Gain measurement 1



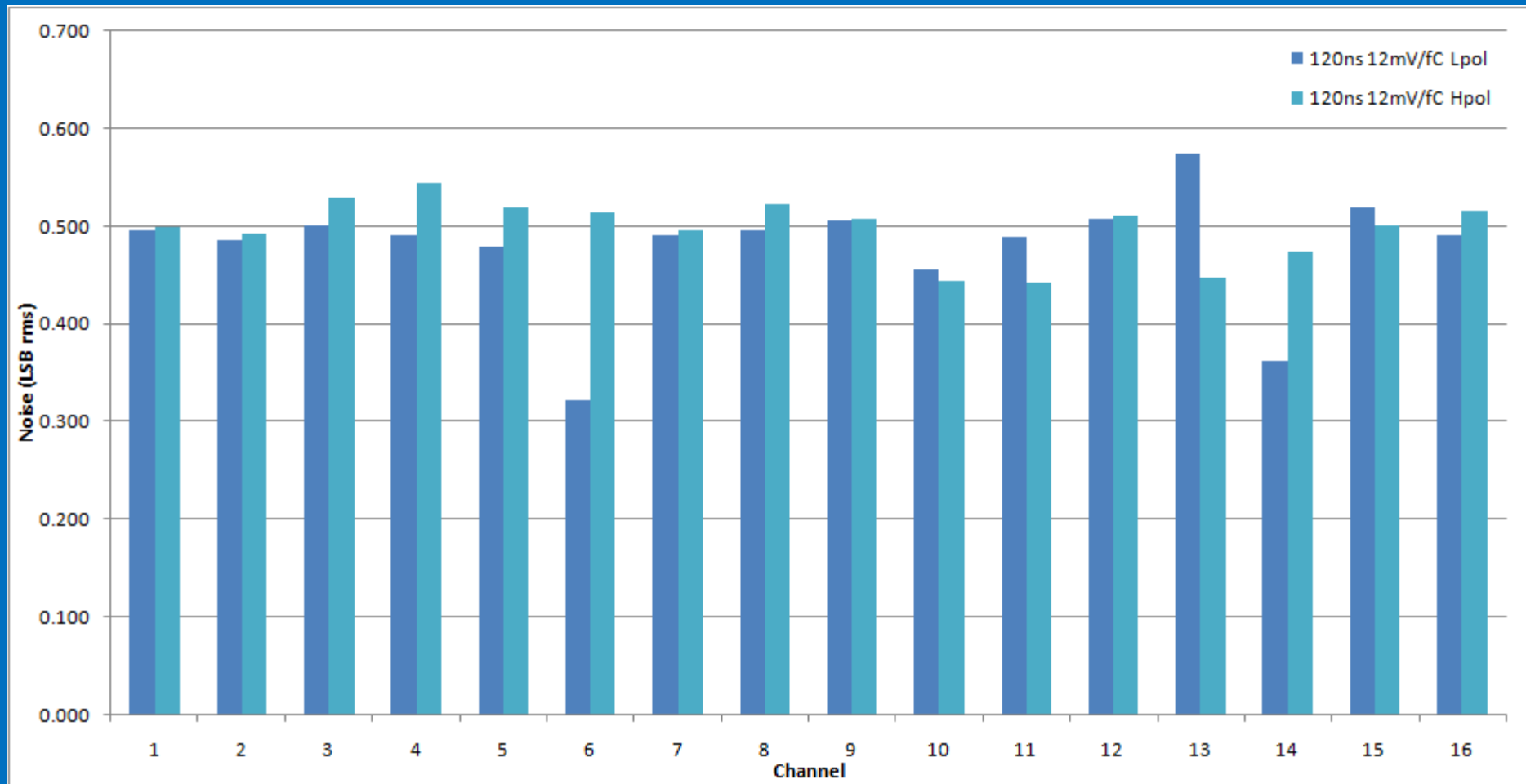
**PASA configuration: 12mV/fC, 120ns, High polarity**  
**Measured gain 10.6mV/fC 1.9%**

# Gain measurement 2



**PASA configuration: 27mV/fC, 30ns, Low polarity**  
**Measured gain 22.5mV/fC 0.9%**

# Noise: PGA3



**PGA3: inputs not bonded**

**Noise constant across channels**

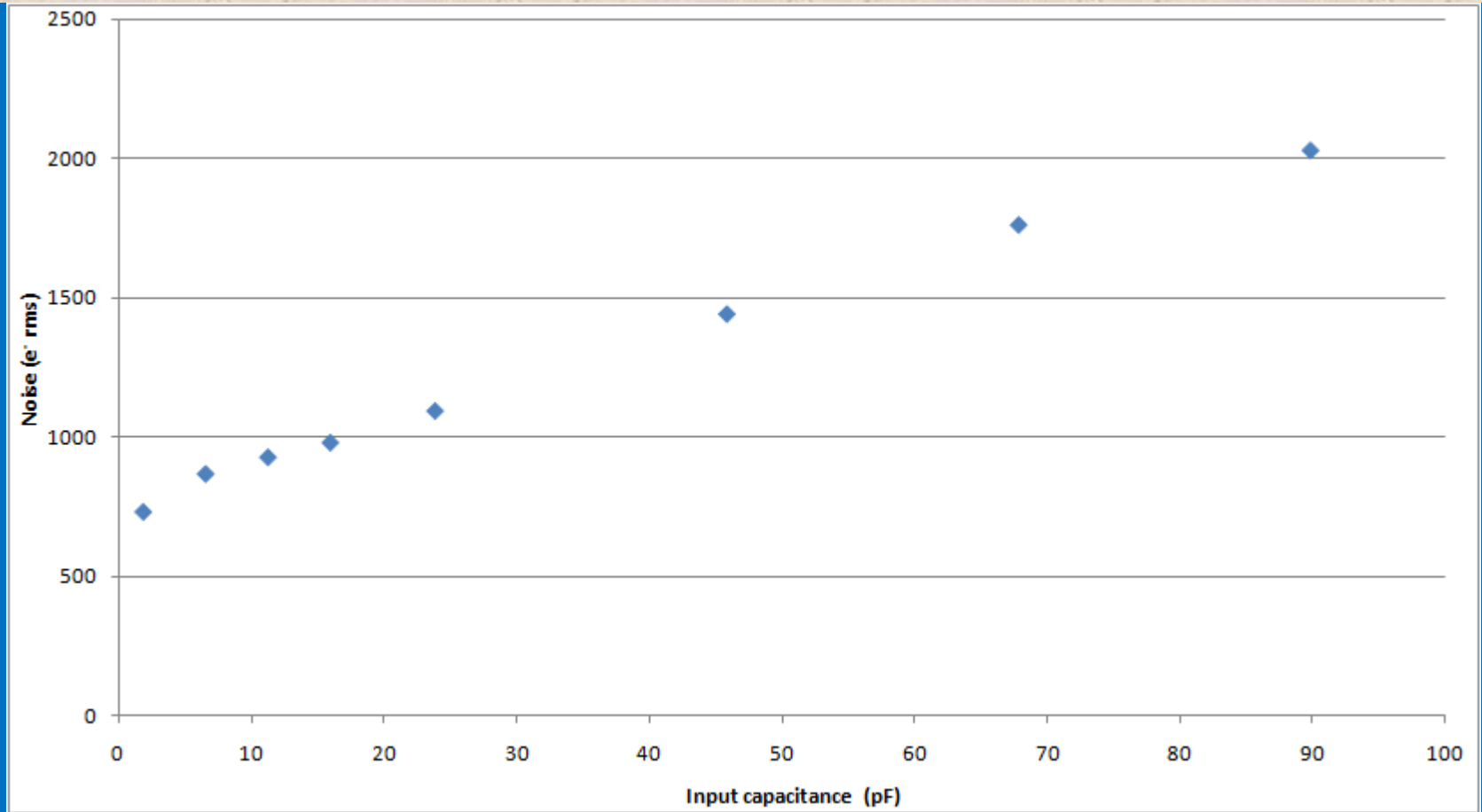


# Noise summary

|      | Config    | 120ns L 12 | 120ns L 27 | 30ns L 12 | 30ns L 27 | 120ns H 12 | 30ns H 12 |
|------|-----------|------------|------------|-----------|-----------|------------|-----------|
| PGA3 | Noise LSB | 0.480      | 0.655      | 0.526     | 0.683     | 0.498      | 0.504     |
|      | Noise fC  | 0.088      | 0.051      | 0.103     | 0.059     | 0.092      | 0.100     |
|      | Noise e-  | 547        | 316        | 641       | 370       | 574        | 625       |
| PGA4 | Noise LSB | 0.709      | 1.346      | 1.475     | 3.263     | 0.668      | 1.279     |
|      | Noise fC  | 0.129      | 0.104      | 0.287     | 0.283     | 0.123      | 0.254     |
|      | Noise e-  | 809        | 649        | 1796      | 1768      | 770        | 1587      |

Measured noise averaged over 16 channels

# Noise: PGA4

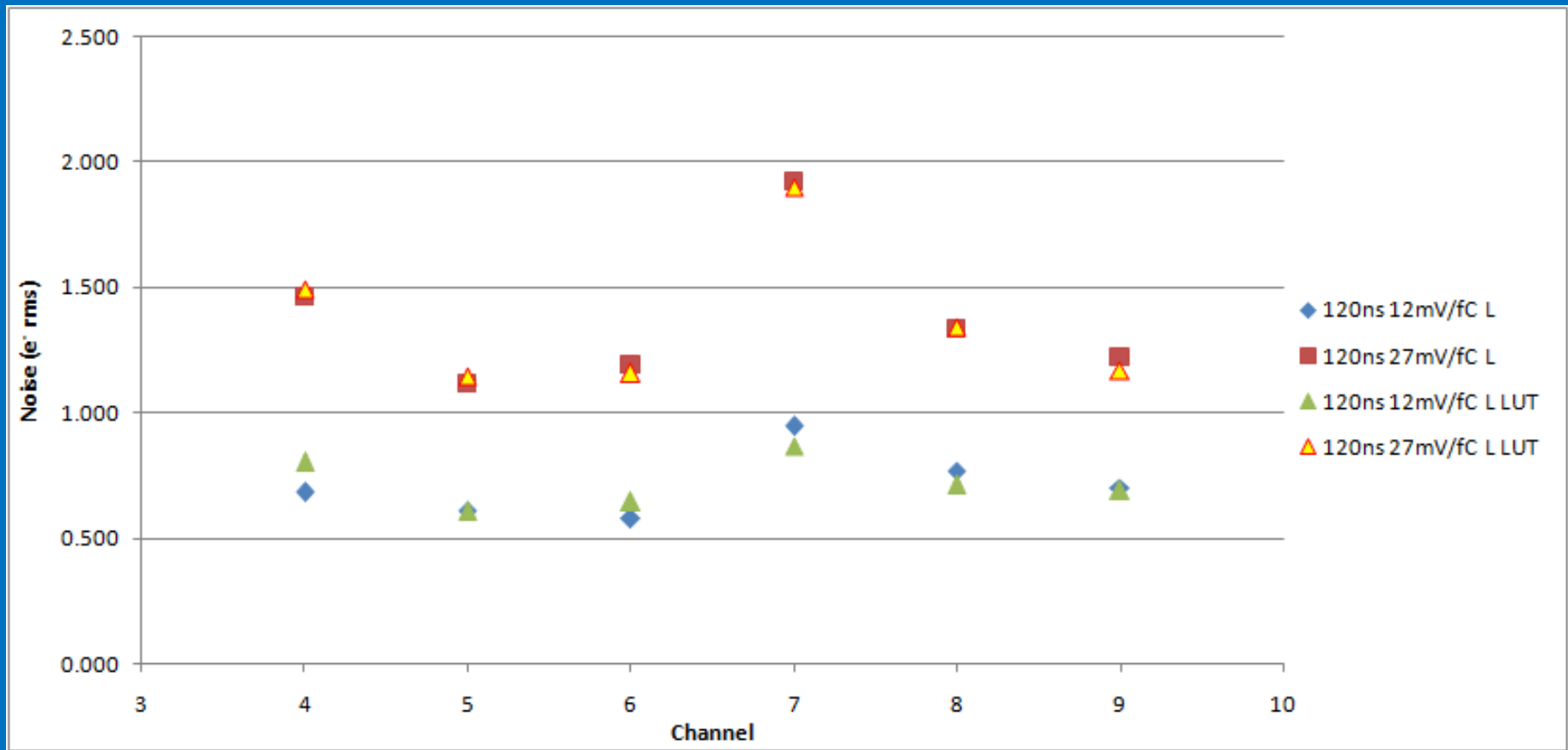


**Measured noise for different input capacitances.**

**PGA4, Channel 0, 120ns, 12mV/fC**

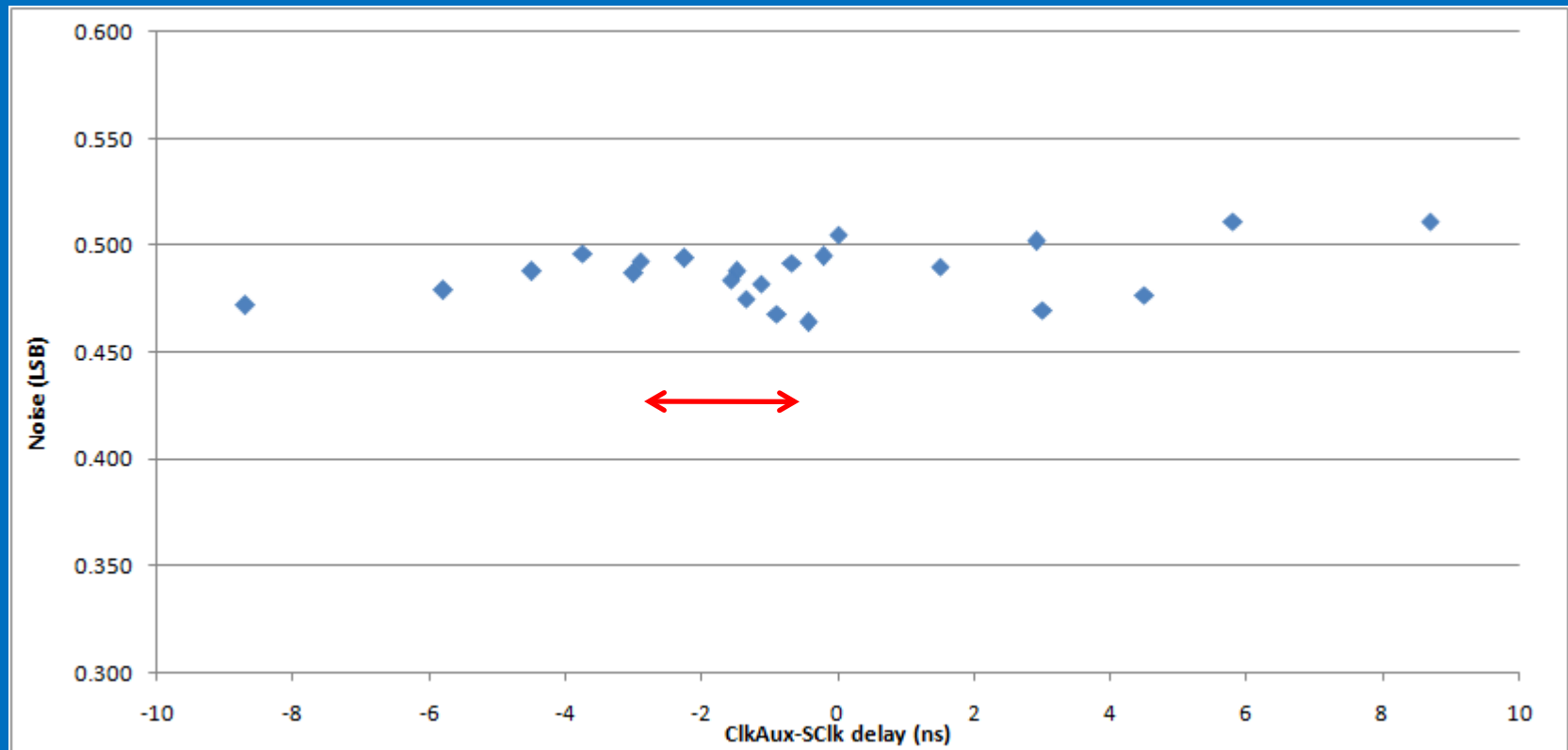
**Slope:  $15e^-/pF$**

# Noise



**Influence of the amount of switching logic on the noise: basic data acquisition and data acquisition with BC1 memory (Look-Up Table) switching.**

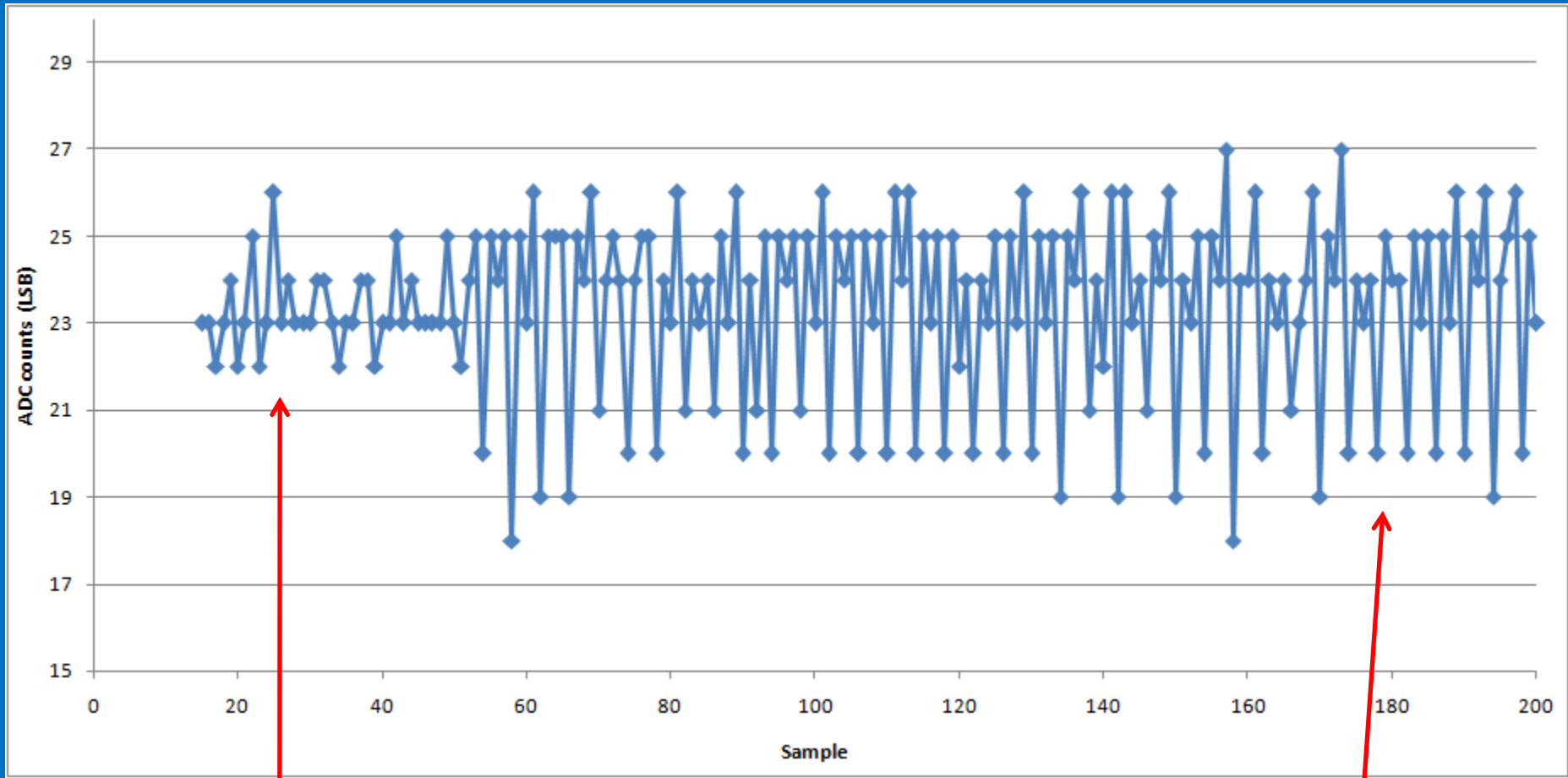
# Noise: effects of the clock phase



**Noise with different phase shifts between ADCs and DSP: no significant difference.**

**The red arrow marks the region where a noise increase can be expected.**

# Noise: effects of memories



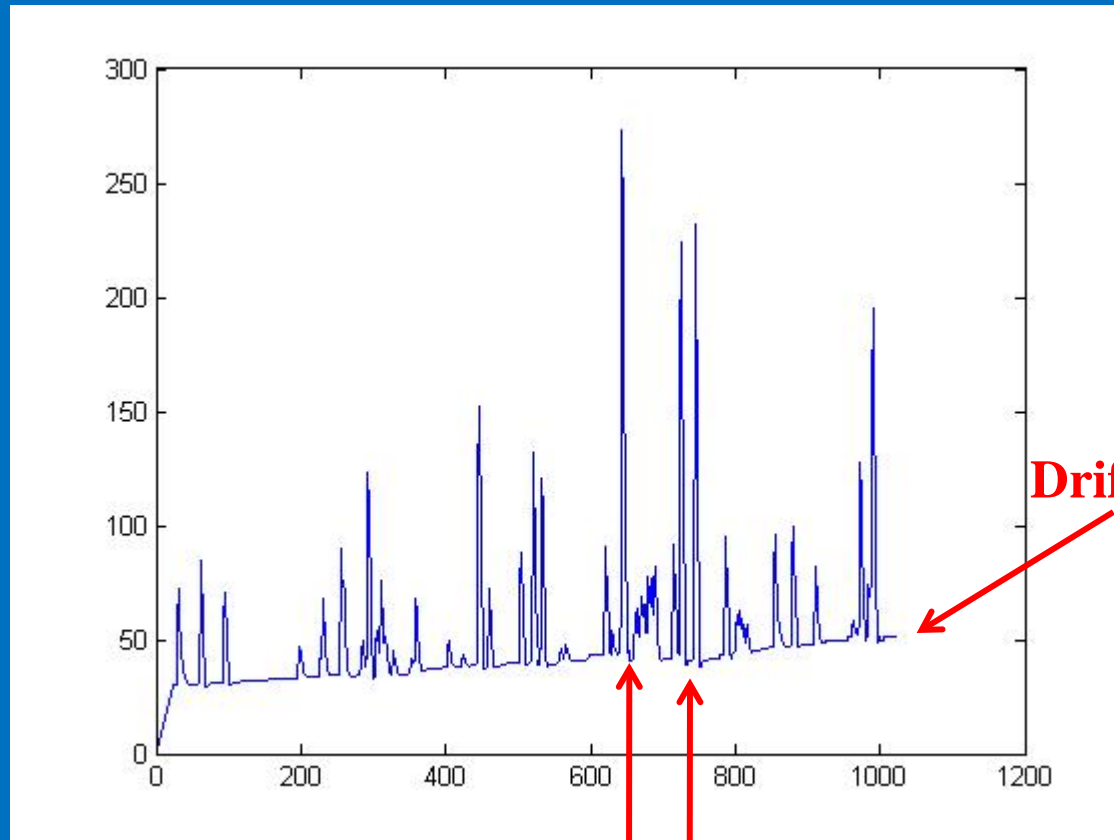
**First 20 samples: lower noise (MEBs are not saving data).**

**Shaping time: 30ns**

**Periodicity: 4<sup>th</sup> clock cycle.**

# DSP tests 1

**Known pattern written in the Pedestal Memory (Baseline Correction 1) and used as test input**

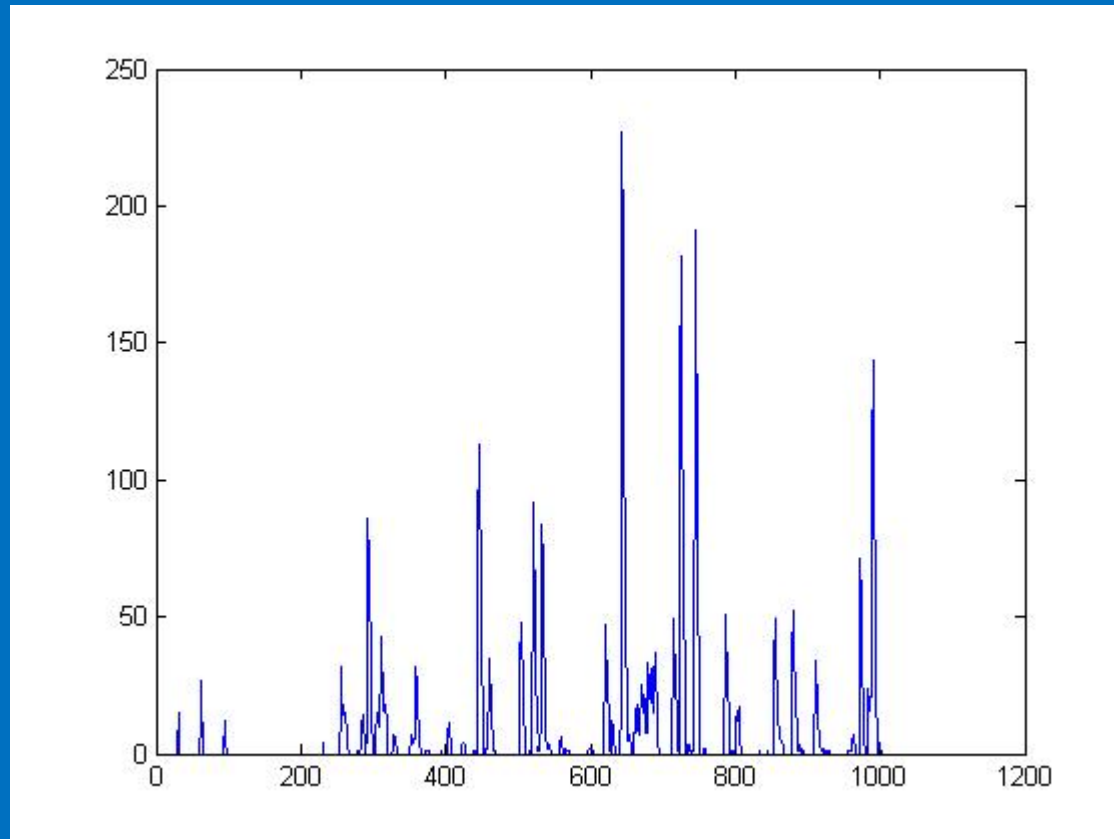


**Drift of the baseline**

**Undershoots**

**Emulates the pattern produced by a real detector**

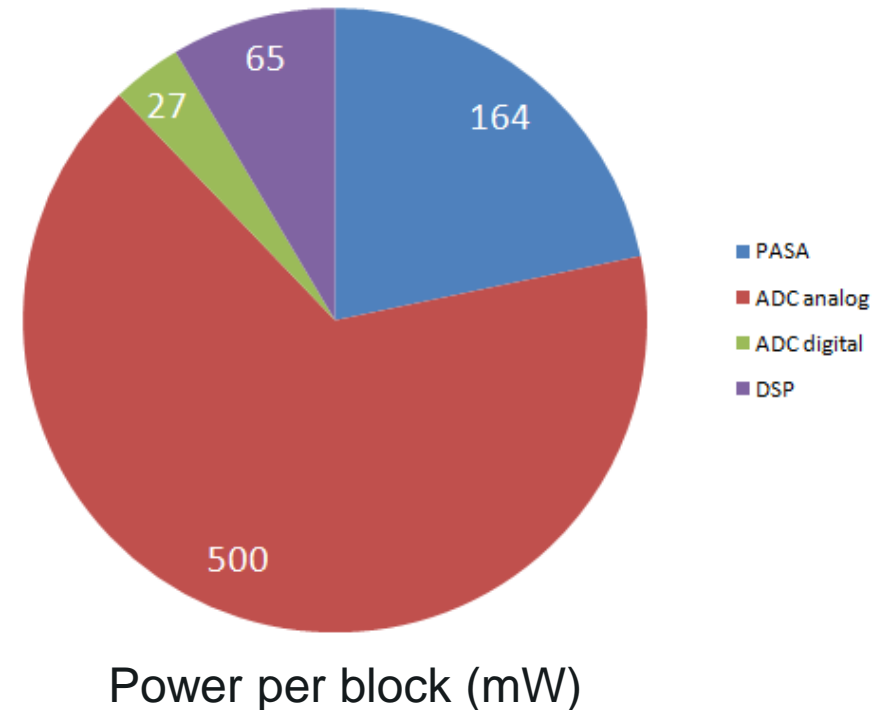
# DSP tests 2



**The DSP removes offsets, undershoots, baseline drifts**

# Power consumption

|             | 40MHz operation | Smart shutdown |
|-------------|-----------------|----------------|
| PASA        | 10.26mW/ch      | 235uW/ch       |
| ADC analog  | 31.28mW/ch      | 394uW/ch       |
| ADC digital | 1.71mW/ch       | ≈0             |
| DSP         | 4.04mW/ch       | 10.8uW/ch      |

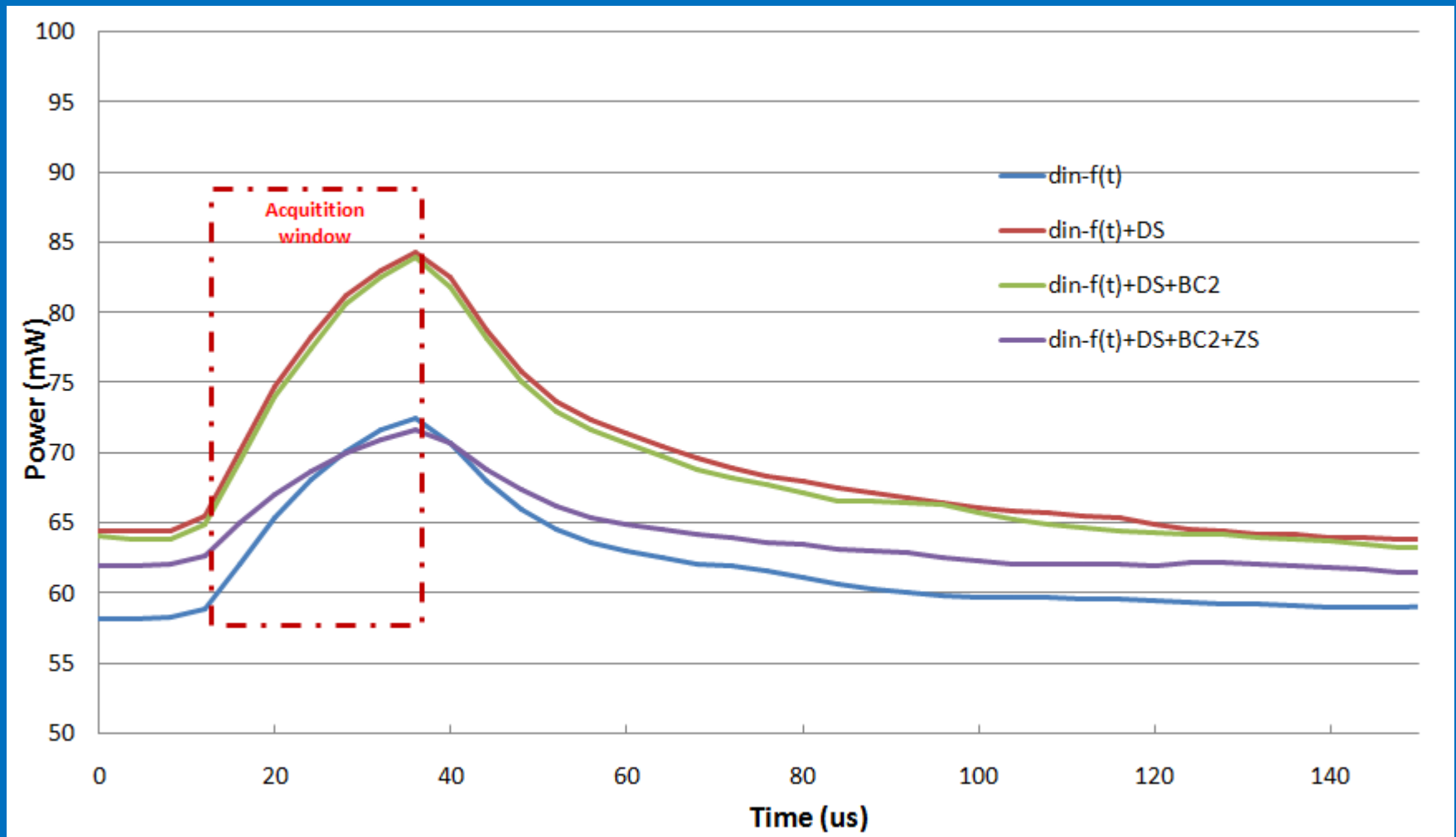


**Smart shutdown: shutdown control lines for PASA and ADC, clock removal for the DSP.**

**Total power consumption: 757mW.**

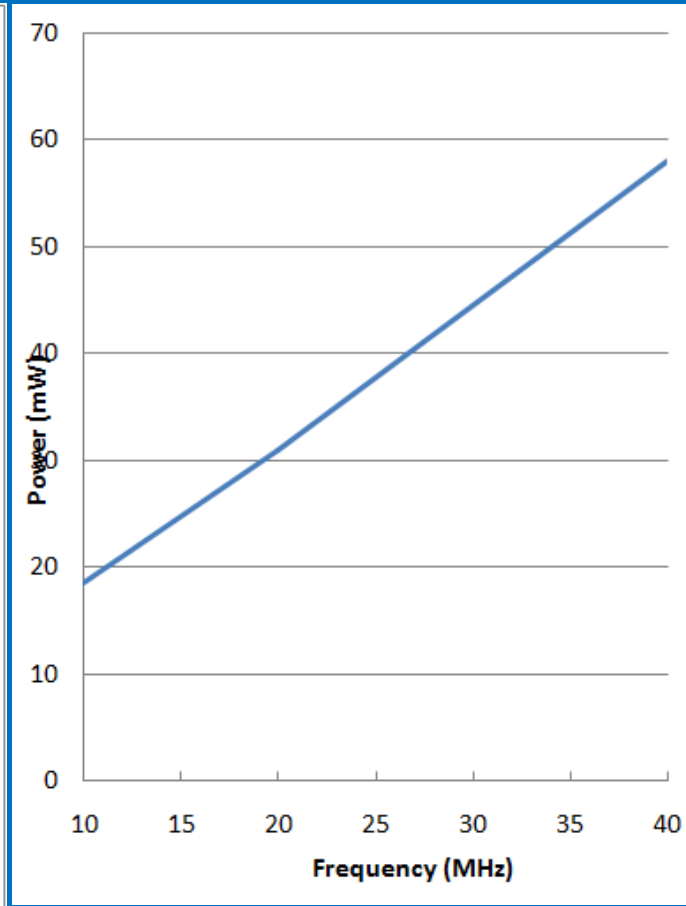
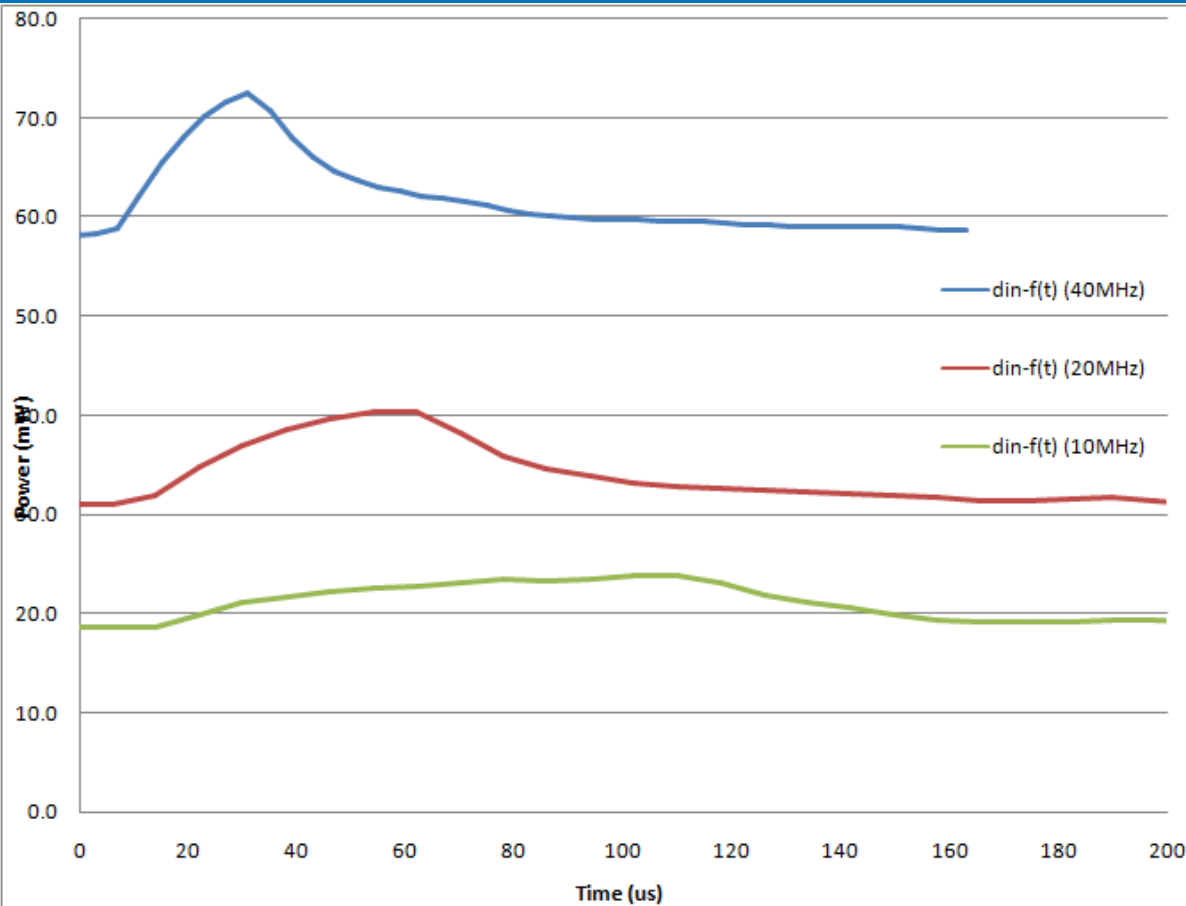


# Power consumption: DSP



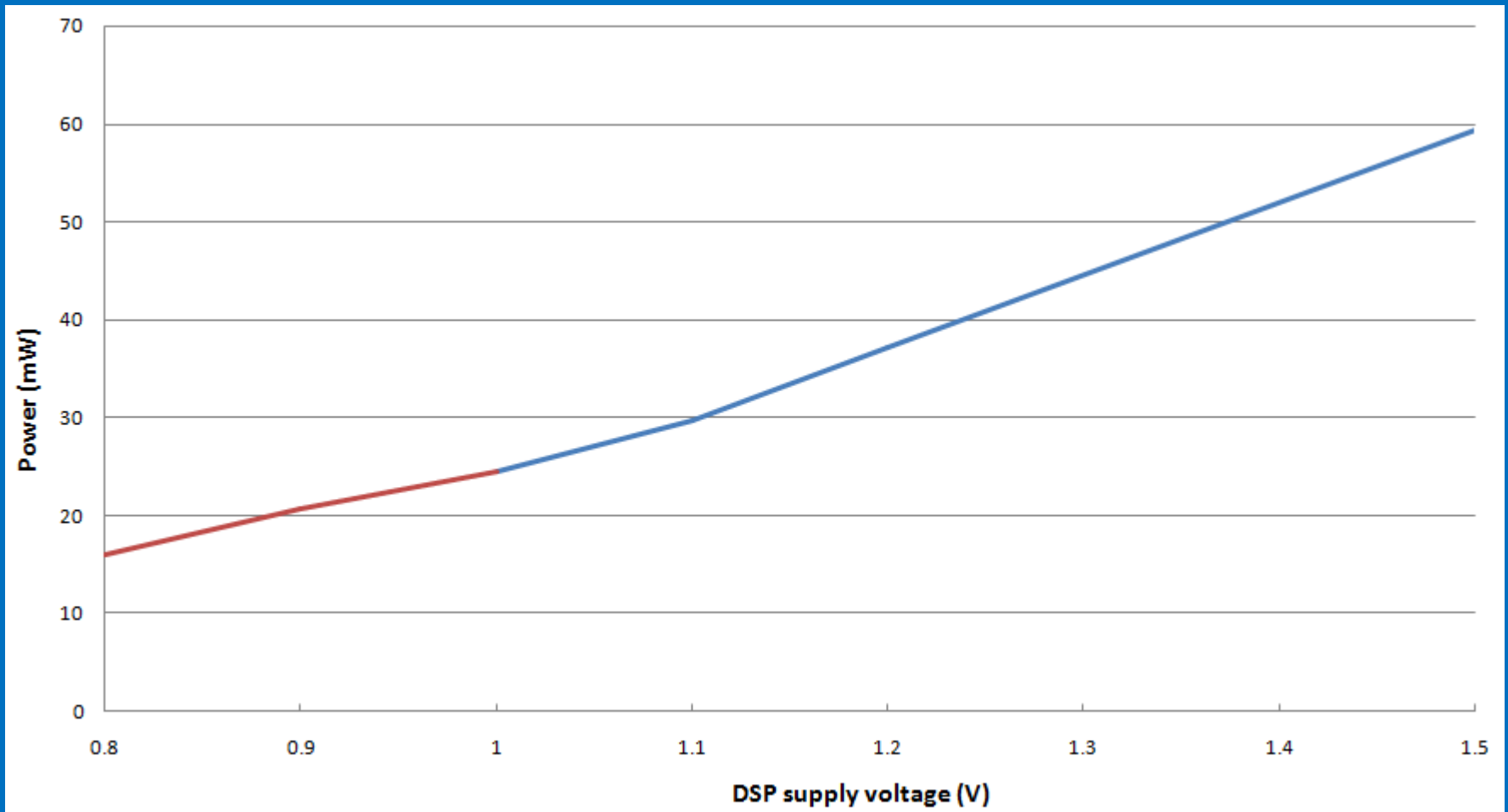
**Power consumption of the DSP when acquiring at 40MHz sampling frequency. Different DSP functionalities included.**

# Power consumption: DSP



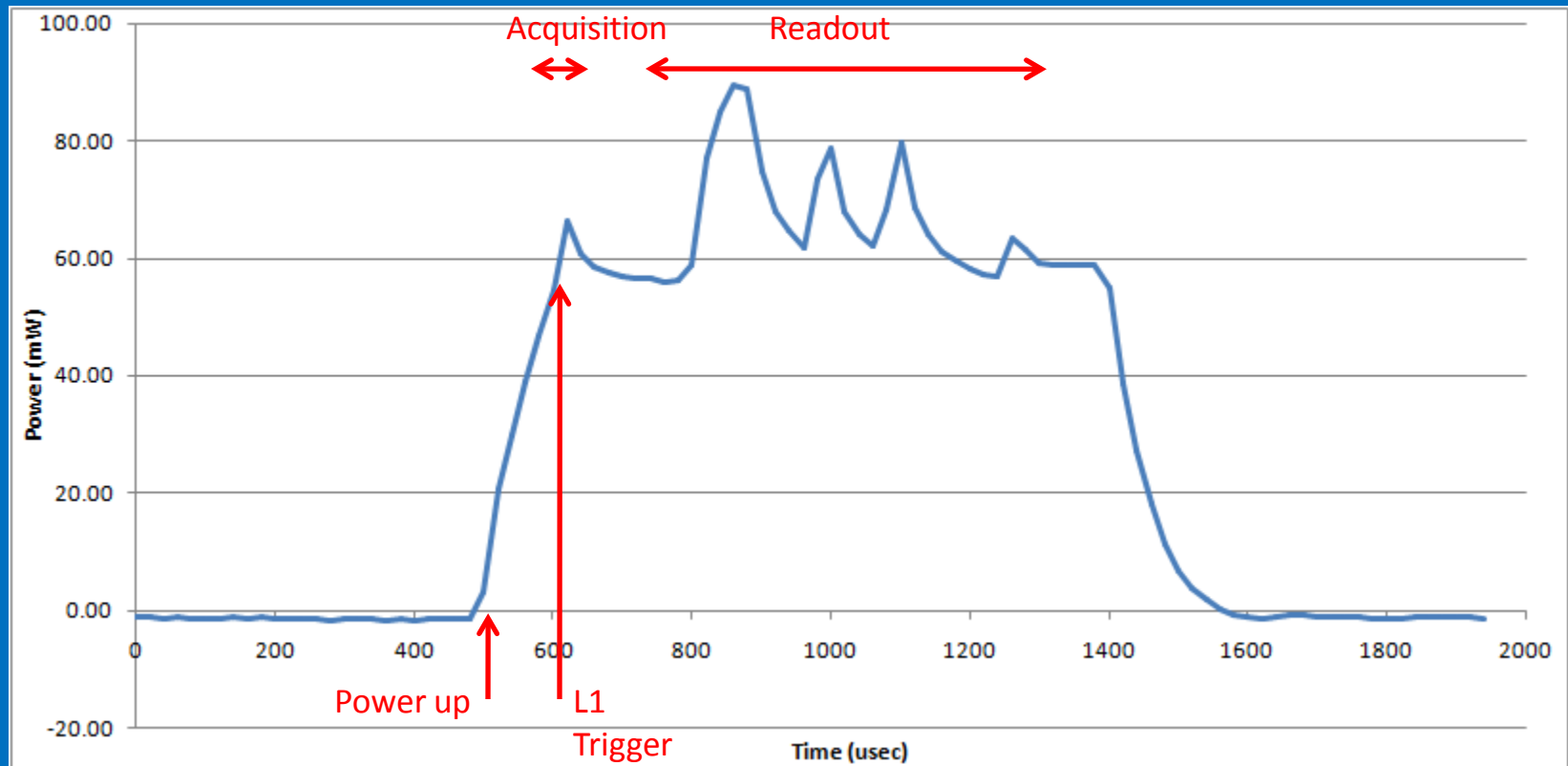
**Power consumption of the DSP for different sampling clock frequencies (10-20-40MHz).**

# Power consumption: DSP



**Power consumption of the DSP at different supply voltages.  
Efficient operation down to 1V supply.**

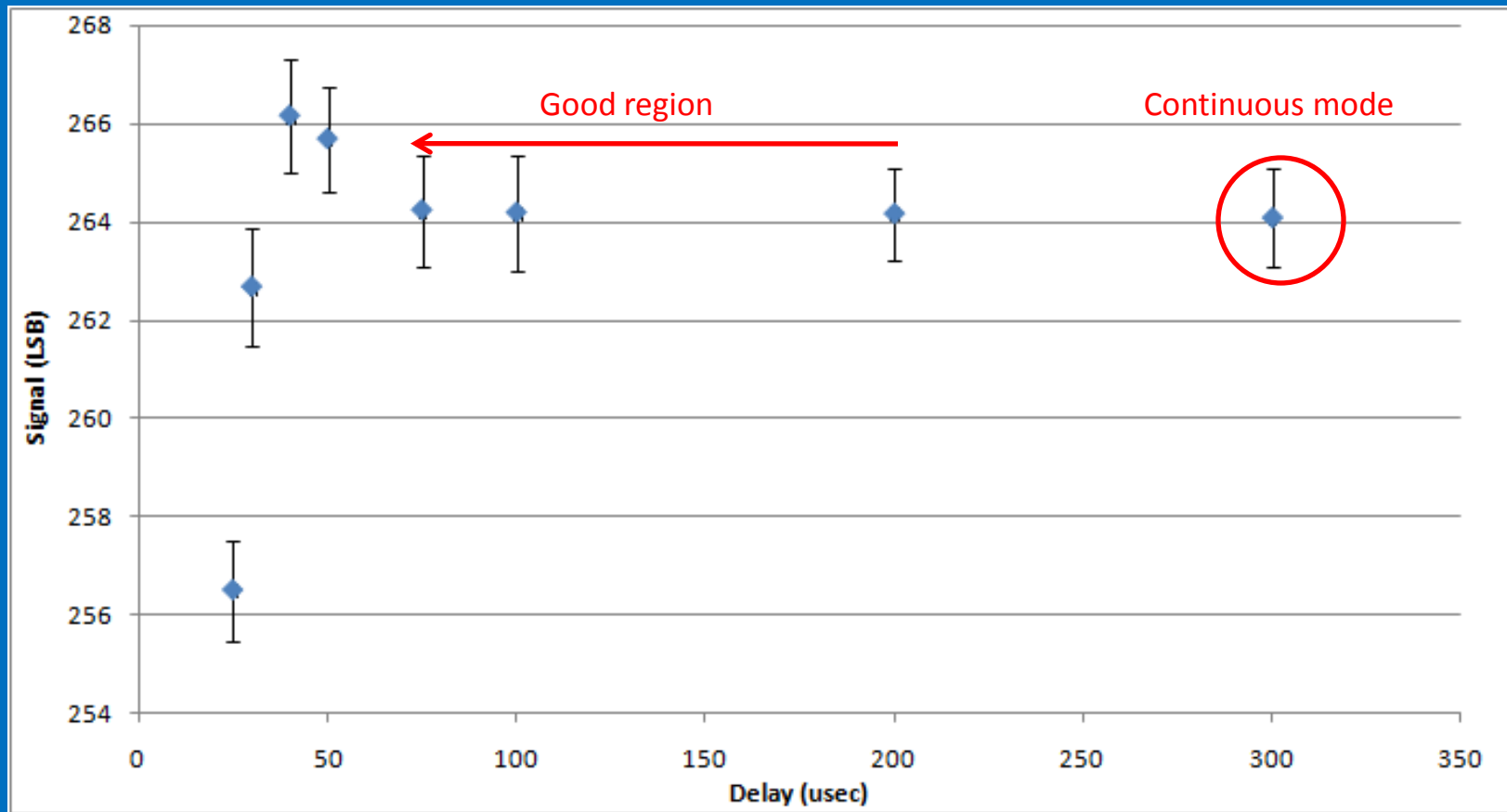
# Power pulsing cycle



**Power consumption of the DSP during a power pulsing cycle  
(smart shutdown).**

**Minimum delay between power up and L1 trigger has to be determined.**

# Power pulsing cycle



**A test pulse is injected after power up; the amplitude of the pulse is monitored with different delays between power up and L1.  
100usec delay gives good results: difference with continuous mode <1LSB**

# Power pulsing: results

|             | Power (mW) |
|-------------|------------|
| PASA        | 2.68       |
| ADC analog  | 24.96      |
| ADC digital | 0.01       |
| DSP         | 0.40       |
| Total       | 28.1       |

**Power pulsing cycles are repeated at a frequency of 5Hz.  
Power reduction by a factor 27!  
(continuous mode: 757mW)**

# Outline

- **Motivations for the project**
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  - **ADC**
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  - **Clock tree**
  - **Top-level simulations**
  - **Assembly, floorplan, layout**
- **Tests**
  - **Test setup**
  - **Measurements: gain, noise, power, power pulsing**
- **Conclusions**

# Conclusions

## Conclusions:

- **The 16 channel Super-ALRO Demonstrator has been designed, prototyped and tested successfully.**
- **The chip is already usable for the Linear Collider TPC prototype.  
The area is  $3.07\text{mm}^2/\text{channel}$  (LCTCP requirement:  $<4\text{mm}^2$ )**
- **Using appropriate design techniques, integration of low-noise analog components and digital functions is possible with little effect on noise performance.**
- **Power pulsing approach has been demonstrated effective in reducing the power consumption, while preserving the performance.**



# Outlook of the project

- **The Super-ALTRO Demonstrator opens possibilities of design optimization for lower power and higher number of channels.**
- **The system can be used for detector tests, e.g. using GEM readout.**
- **Since integration has been proved, the next steps should attack the power consumption of the ADC.**

# Acknowledgements

## **Thanks:**

**Francis Anghinolfi, Sandro Bonacini, Jorgen Christiansen, Antoine Junique, Lucie Linssen, Magnus Mager, Alessandro Marchioro, Christian Patauner, Attiq Ur Rehman, Adam Szczepankiewicz, Gerd Trampitsch, Felix Reidt**

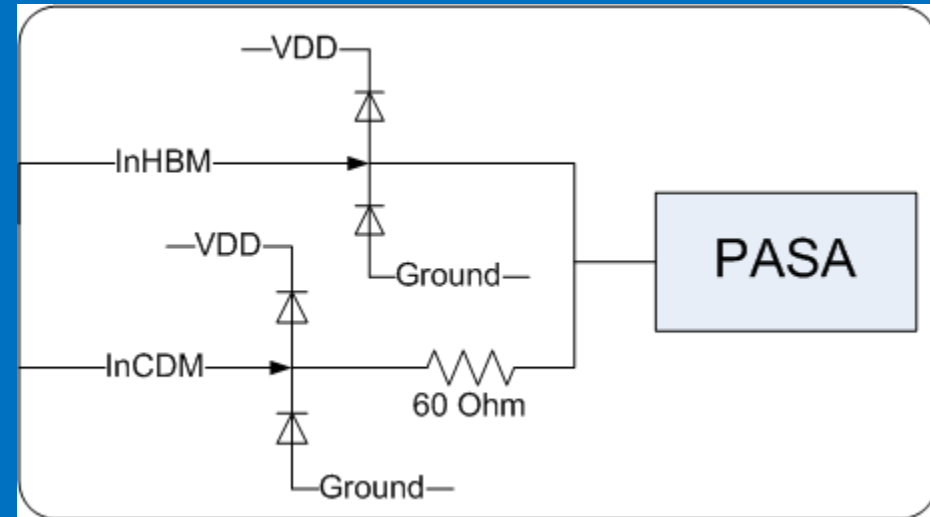
**And thank you all for your attention!**

# Back-up slides

# PASA: ESD protections

Each PASA has two input pads in parallel (only one bonded):

- Simple double diode protection scheme (Human Body Model)
- Structure with series resistor for enhanced protection (Charged Device Model)

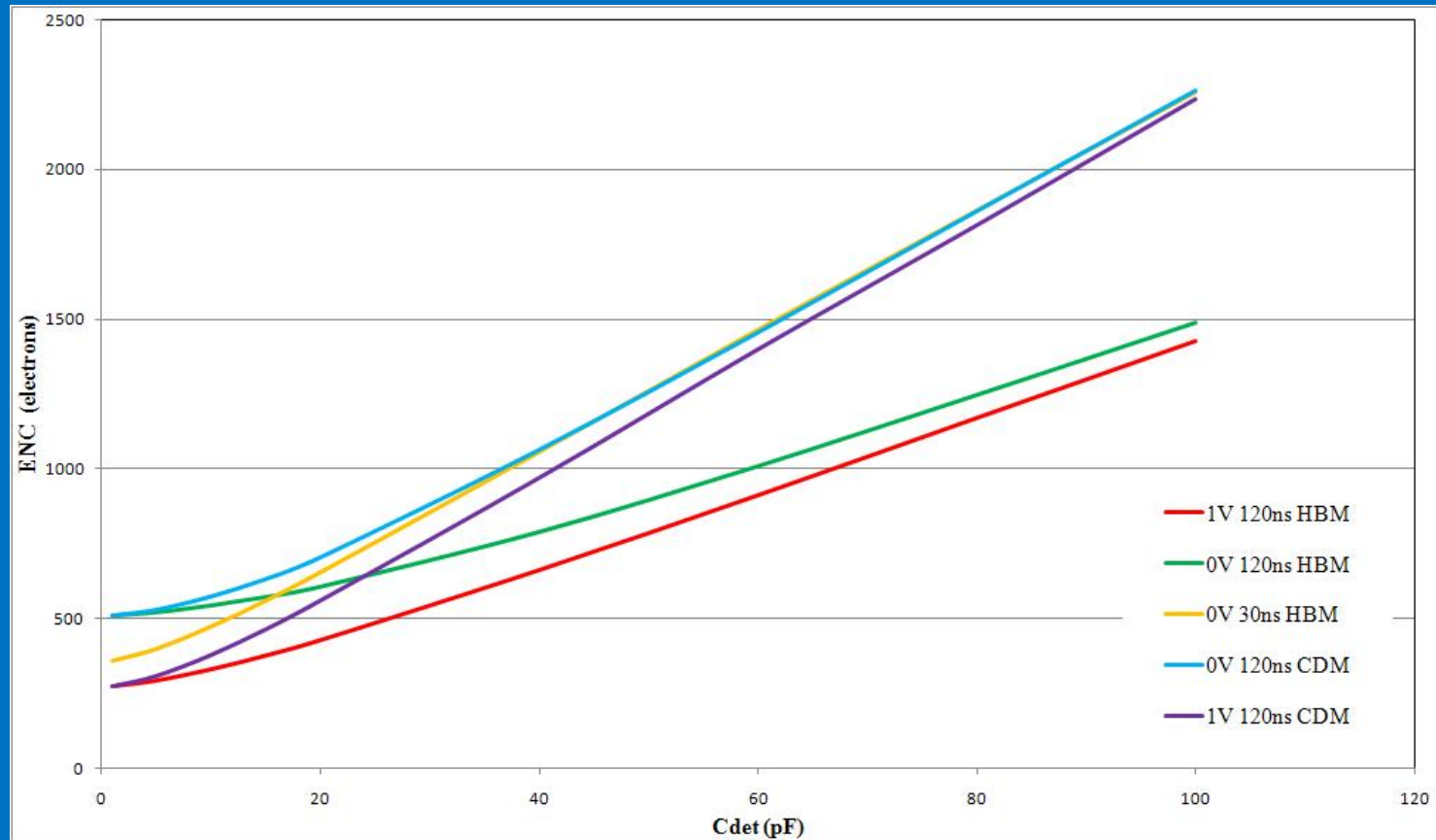


**Drawback: the series resistor adds noise to the input signal.**

**PASA noise:  $300e^-$  @ 10pF detector capacitance**

**Noise increase (simulated): 20-30%**

# PASA: Equivalent Noise Charge

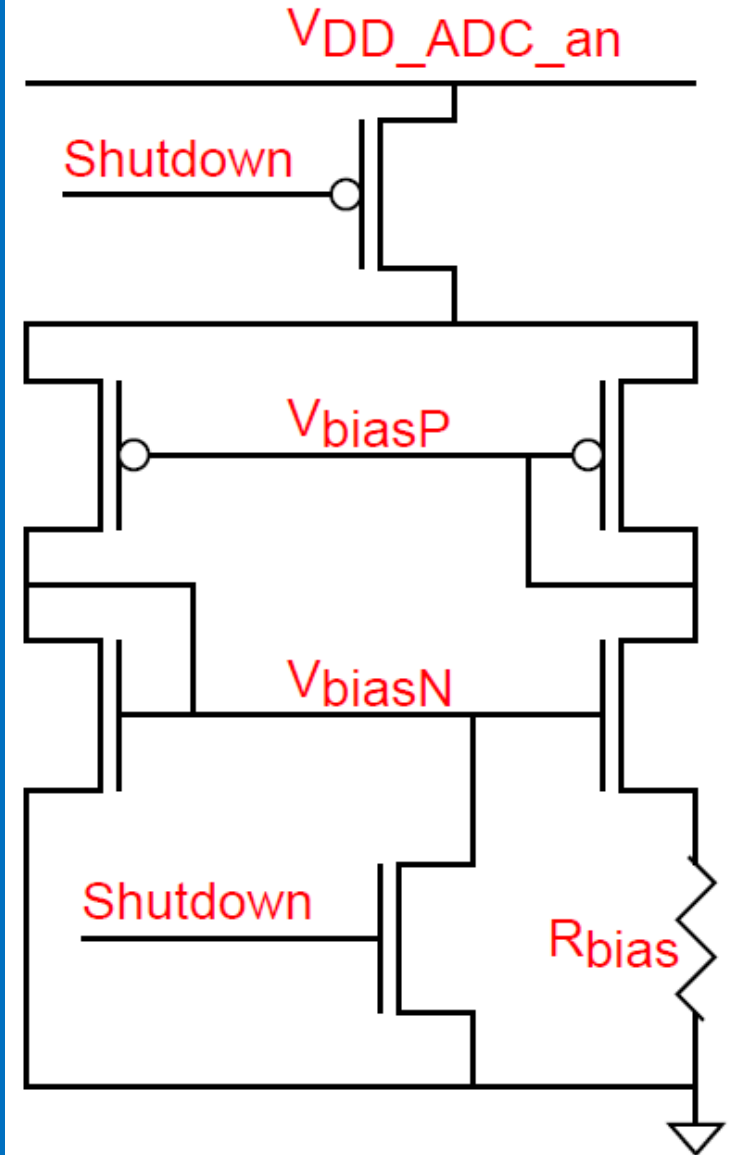


**Simulations: dependency of the noise on detector capacitance, shaping time, feedback resistance, and type of ESD protection**

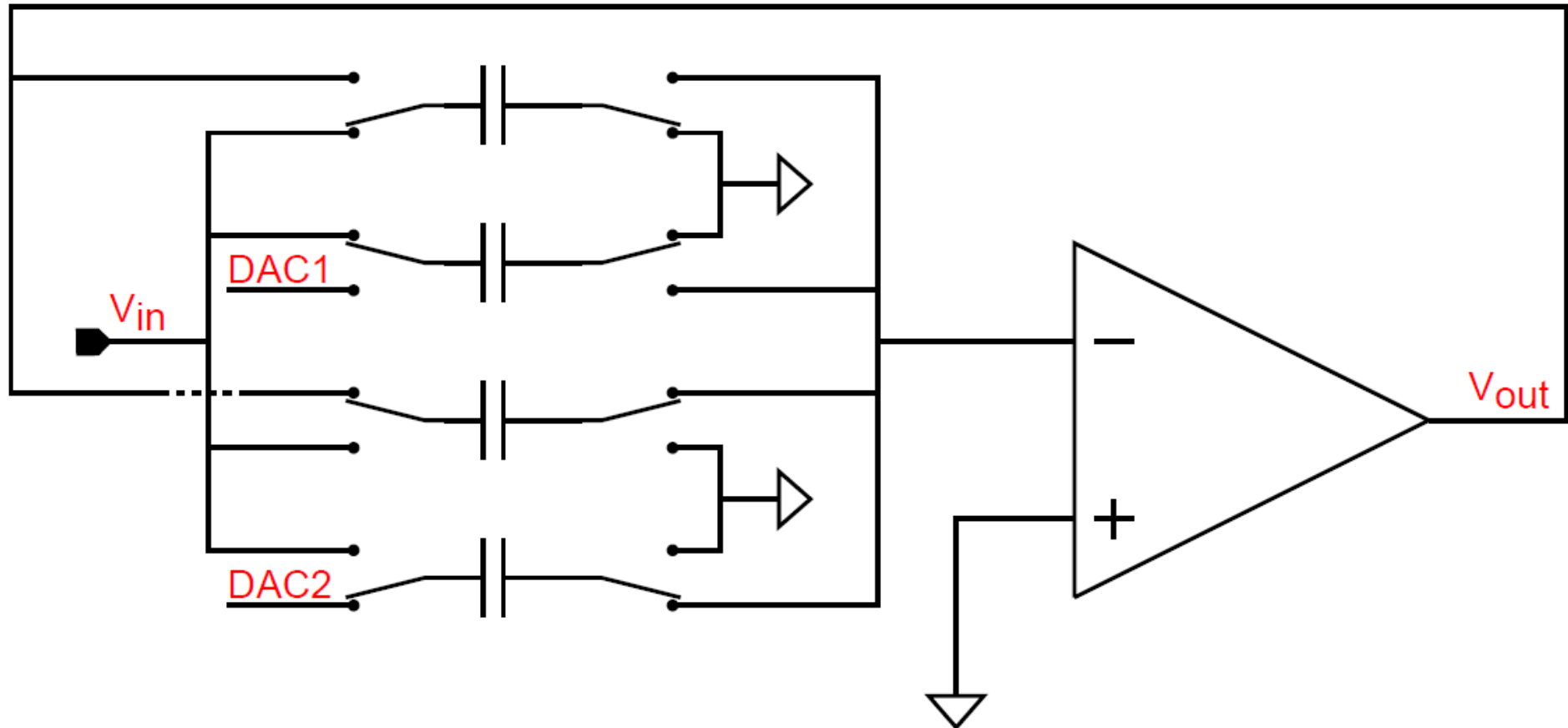
# PASA: Shutdown switch

**Beta-multiplier gives better PSRR than conventional resistor with diode-connected transistor.**

**The shutdown line controls the main beta-multiplier. Therefore, it can remove the biasing to the whole PASA.**



# Pipeline ADC: MDAC



**Simplified (single-ended) MDAC. Grounds are intended as AC grounds.**

**Switched capacitor network: multiply by 2 with equal capacitors.**

**Non-overlapping clocks for the switches.**

# Pipeline ADC: Main Amplifier

**Two-stages telescopic cascode differential amplifier with common-mode feedback amplifier (not shown) and gain boosting**

**$C_c=1.8\text{pF}$ , Gain 100dB,**

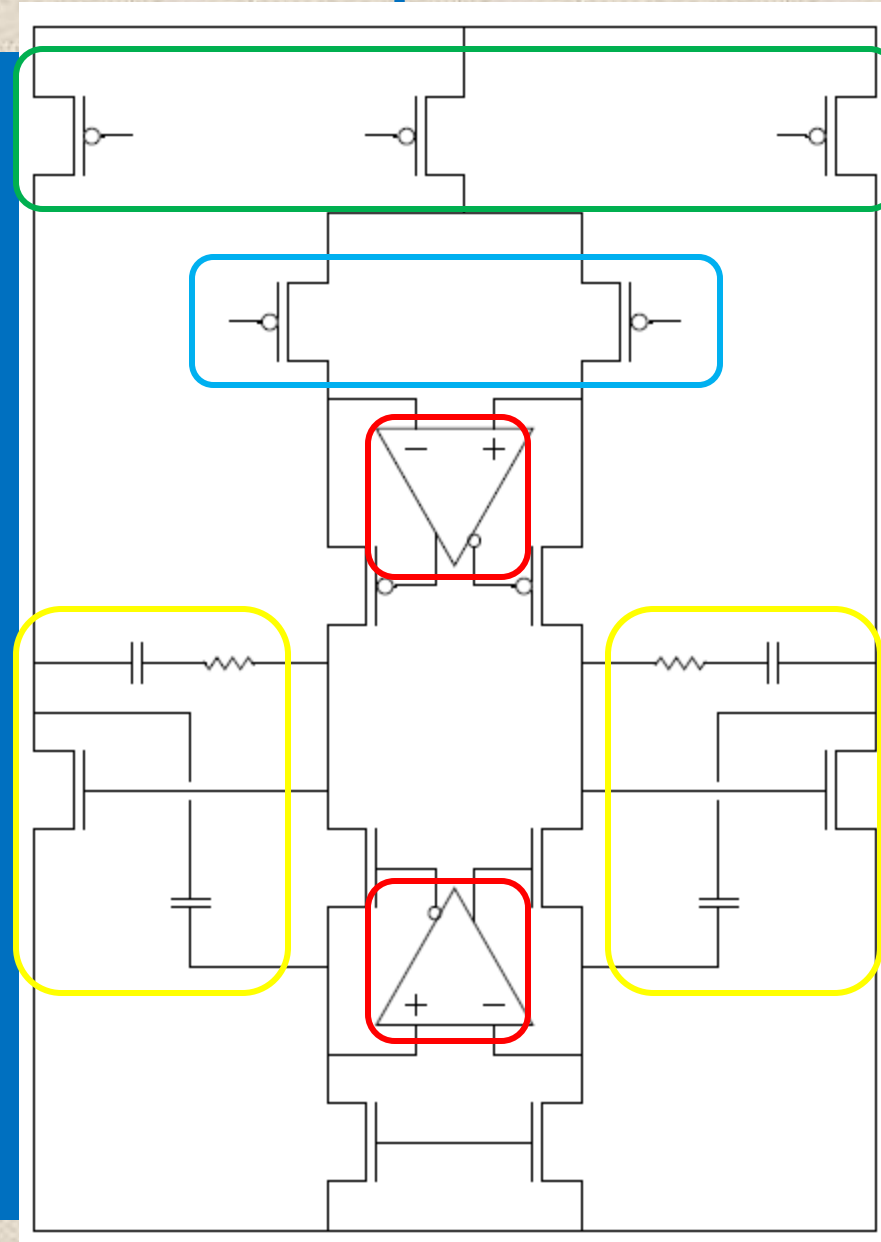
**GBW 330MHz, PM 70 , 4mW**

**Input diff pair**

**Gain boosting amplifiers**

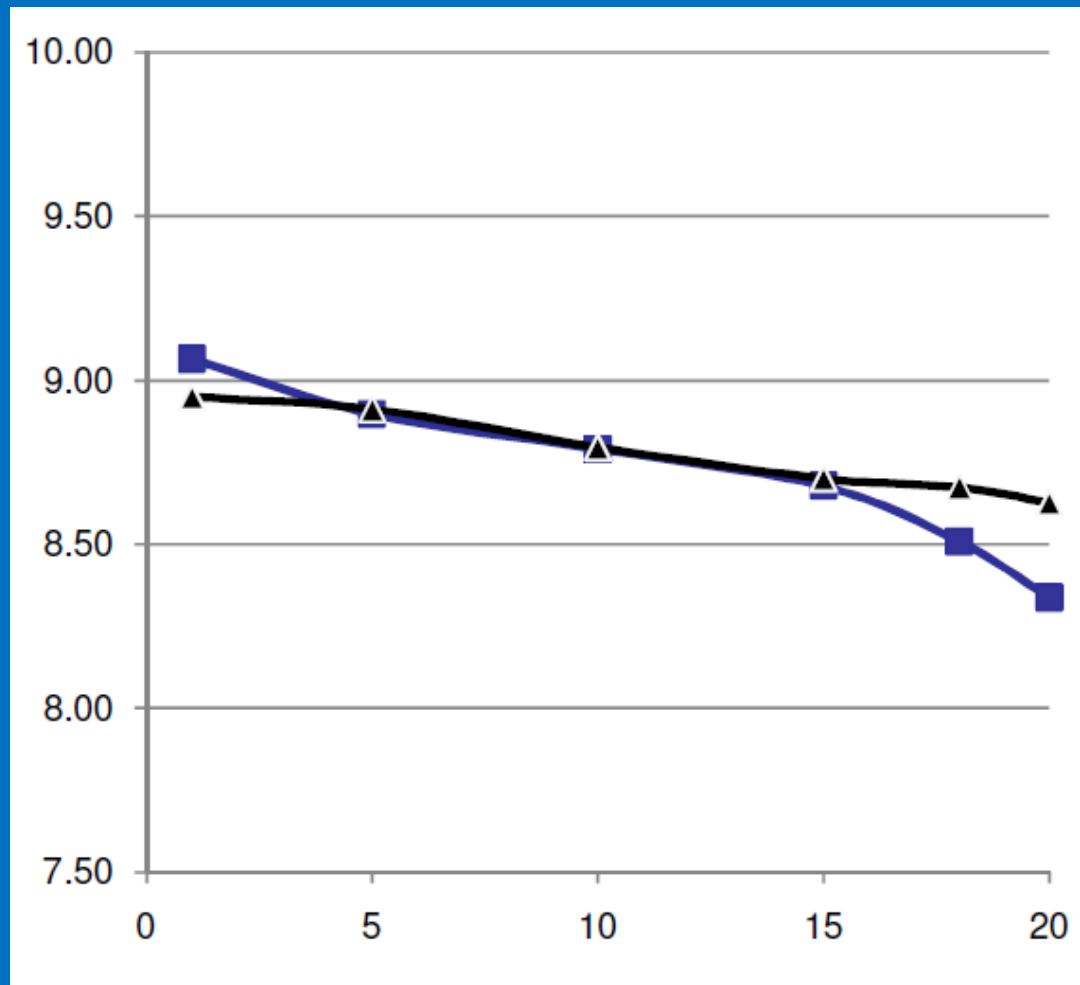
**Current sources**

**Output transistors with compensation caps**





# Pipeline ADC: test results



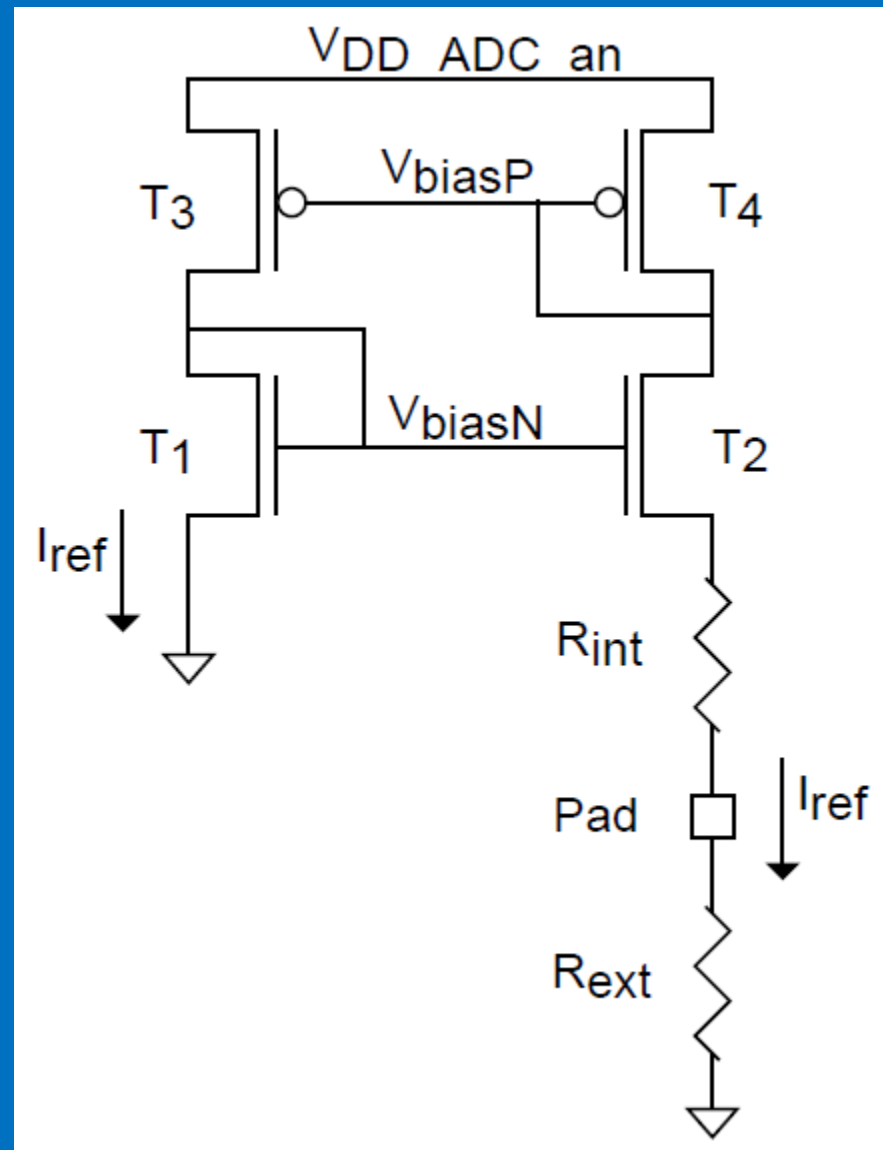
**ENOB as a function of input signal frequency, sampling at 40MHz,  
2 ADCs under test**

# Bias circuitry: beta-multiplier

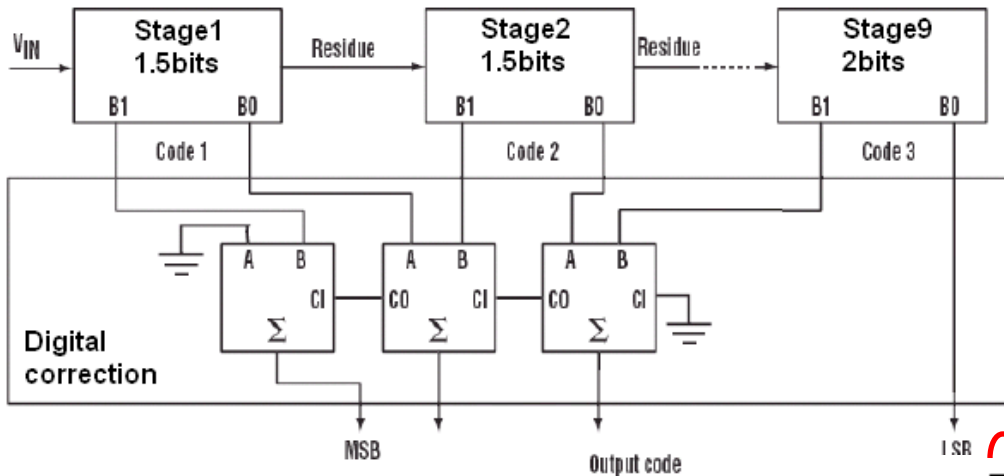
**The off-chip resistor is meant to adjust externally the power consumption of the ADC (useful for different sampling frequencies and to test power-pulsing)**

**ADC prototype: 1 beta-multiplier per ADC + 1 off-chip resistor per ADC**

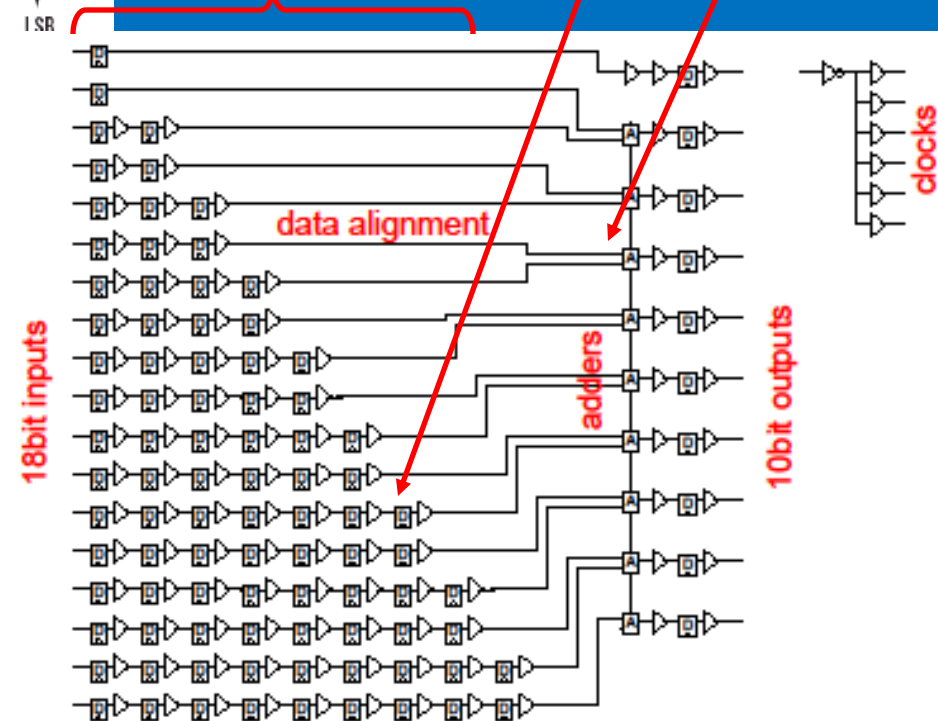
**SAltro: 1 beta-multiplier + 1 off-chip resistor + the BiasReference signal is routed to all channels**



# Digital error correction (redundancy)



**D Flip-flops**  
**Adders**

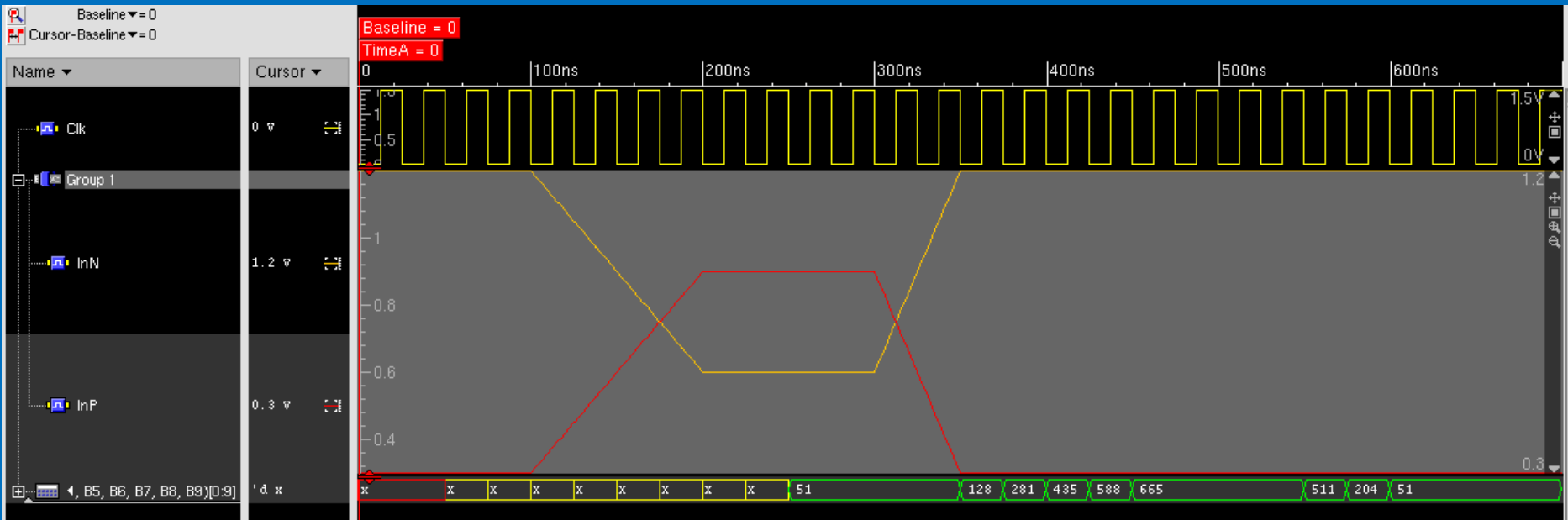


18 bits from the 9 ADC stages are reduced to a 10-bit output word.

The digital correction is clocked on the falling edge of the clock.

# Digital error correction: verification

**In order to run chip-level simulations, an analytical Verilog-AMS model has been written and verified for each block.**



**Arbitrary analog input waveform converted to digital simulated in Spectre (schematic, extracted parasitics, extreme corners and Monte Carlo) and in Verilog-AMS: results correct**

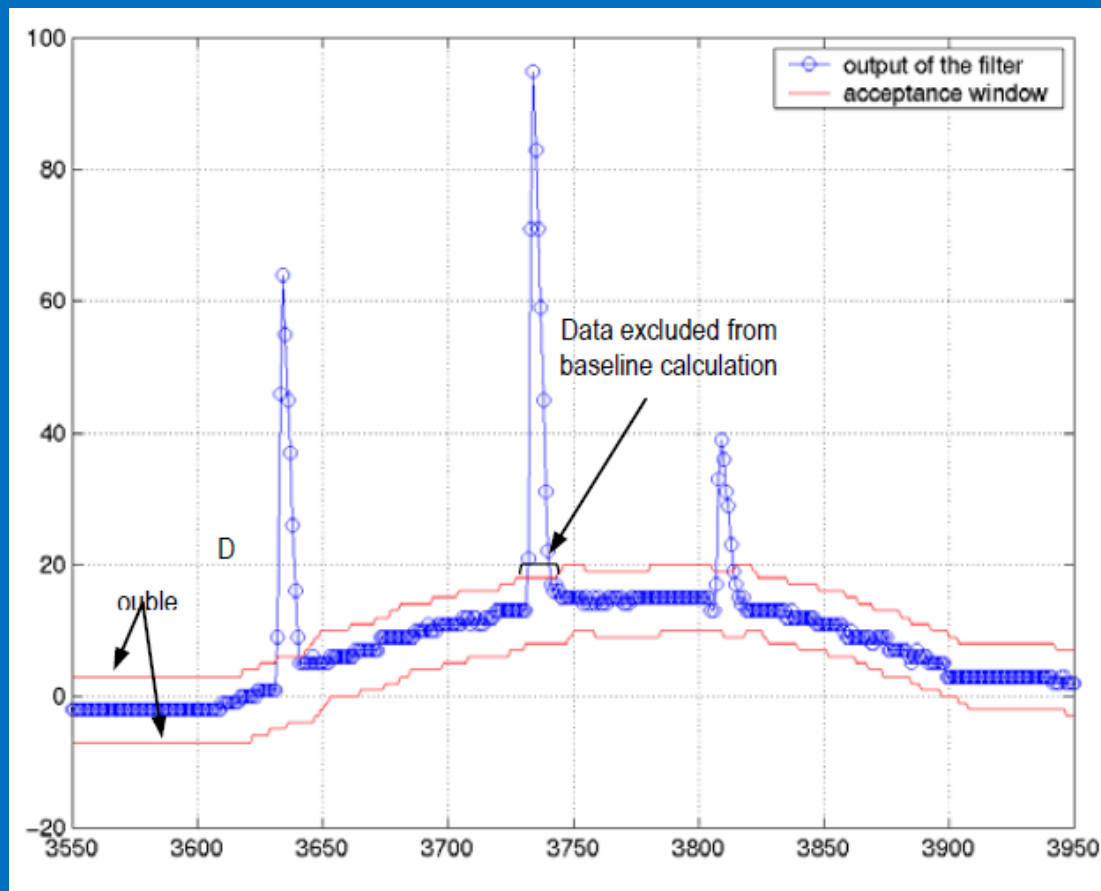
# Verilog-AMS example: PASA

```
`include "constants.vams"
`include "disciplines.vams"
module Pasa1ch ( Gnd, SupplyP, VOutP, VOutN, BiasDecay,
gain1, gain2,
in, polarity, PreampEn, sh1, sh2, sh3, shutdown, substrate );
inout substrate;
inout sh3;
inout gain2;
inout Gnd;
inout in;
inout BiasDecay;
inout shutdown;
inout sh2;
inout SupplyP;
inout VOutN;
inout VOutP;
inout sh1;
inout PreampEn;
inout polarity;
inout gain1;
electrical in, VOutP, VOutN;
electrical Gnd, SupplyP, BiasDecay, gain1, gain2, polarity,
PreampEn,
sh1, sh2, sh3, shutdown, substrate;
electrical PreampOut, PZOut, OutInt1, OutInt2, OutSe;
branch (in, PreampOut) cap, res;
parameter Cf=0.8E-12; // integrating capacitor
parameter Rs=1E6; // feedback resistance
parameter real Dcl=0.2; // DC input level of the preamplifier

parameter Rpz=Rs/14;
parameter Cpz=Cf*14;
parameter R1=1200; // series resistance of the pole-zero
// cancellation network
parameter G=15; // DC gain of the T-bridged amplifiers
parameter pi=3.14;
parameter pa=2*pi*10E6; // one pole of the shapers (radians)
parameter pb=2*pi*30E6; // one pole of the shapers (radians)
parameter BaselineP=1.170; // DC level of the positive output
parameter BaselineN=0.330; // DC level of the negative output
analog begin
I(cap) <+ Cf*ddt(V(cap));
V(res) <+ Rs*I(res);
V(PreampOut) <+ -10E3*(V(in)-Dcl);
V(PZOut) <+ R1*( (V(PreampOut)-V(PZOut))/Rpz) +
Cpz*ddt(V(PreampOut)-V(PZOut)) );
V(OutInt1) <+ V(PZOut)-(1/pa)*ddt(V(OutInt1));
V(OutInt2) <+ V(OutInt1)-(1/pb)*ddt(V(OutInt2));
V(OutSe) <+ G*V(OutInt2);
if (V(polarity)>0.75) begin
V(VOutP) <+ BaselineN+V(OutSe);
V(VOutN) <+ BaselineP-V(OutSe);
end else begin
V(VOutP) <+ BaselineP+V(OutSe);
V(VOutN) <+ BaselineN-V(OutSe);
end
end
endmodule
```

**Verilog-AMS is an extension of Verilog**

# Threshold system



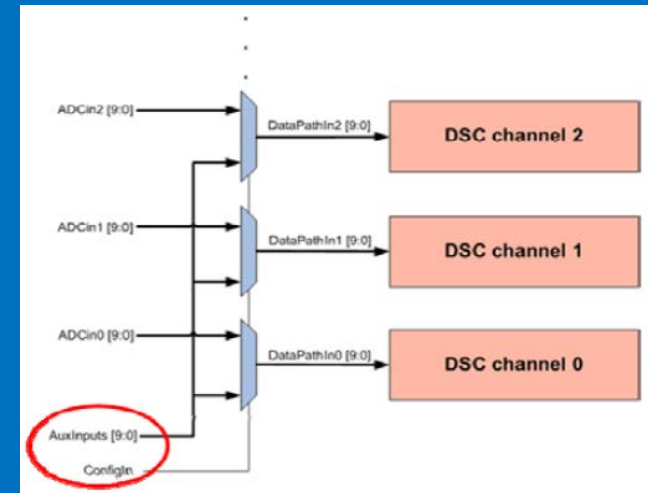
**Threshold system: thr\_hi, thr\_lo, noise per channel.**

# On-chip test/debug features

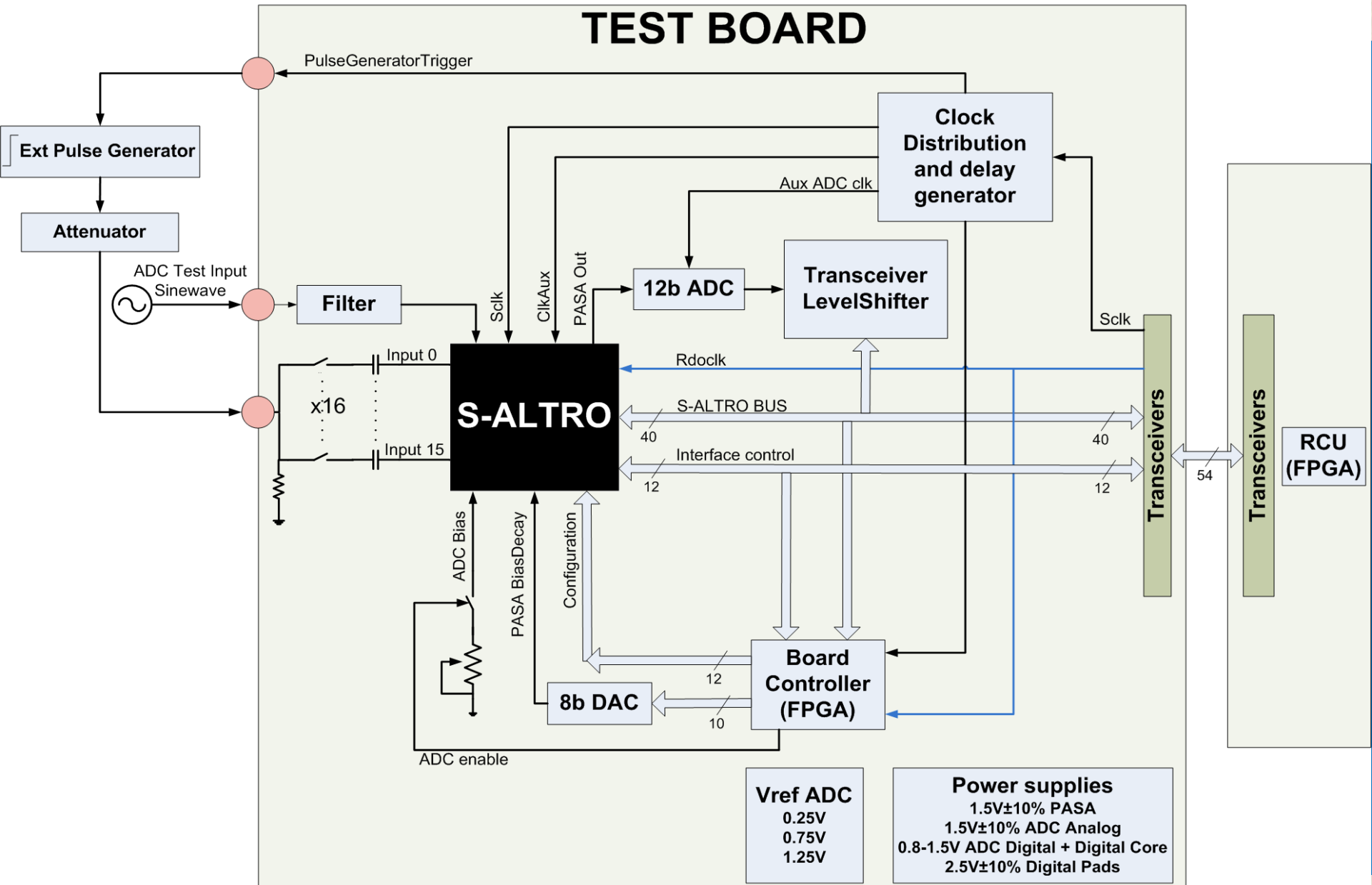
- **Scan mode:** all registers in the chip are connected in a JTAG-like fashion; a pattern is provided to the dedicated input. Analysis of the output pattern provides information on critical timings.

- **Auxiliary inputs to the DSP:** a 10bit auxiliary input is routed to some multiplexers and can replace the inputs to the DSP from the ADC, in case the analog part gives problems.

- **Test mode TSM:** continuous read-out, without Data Format / MEB. Useful for testing detectors in continuous mode.

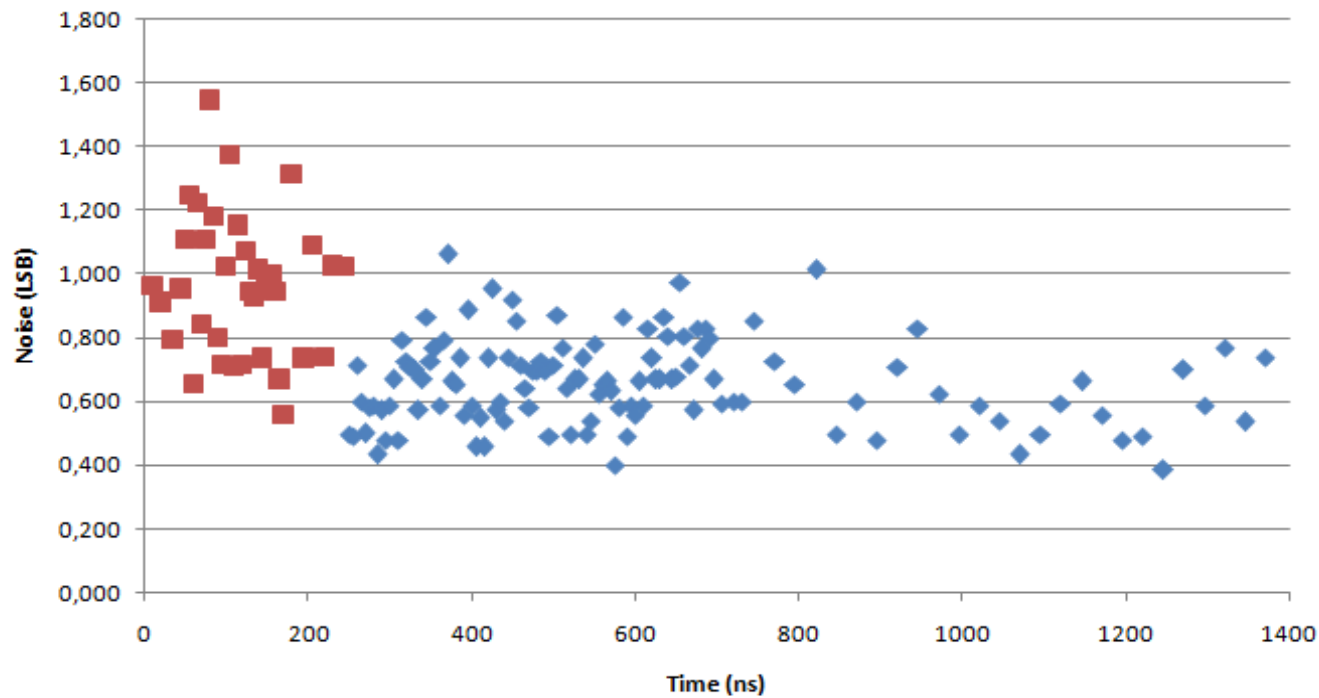
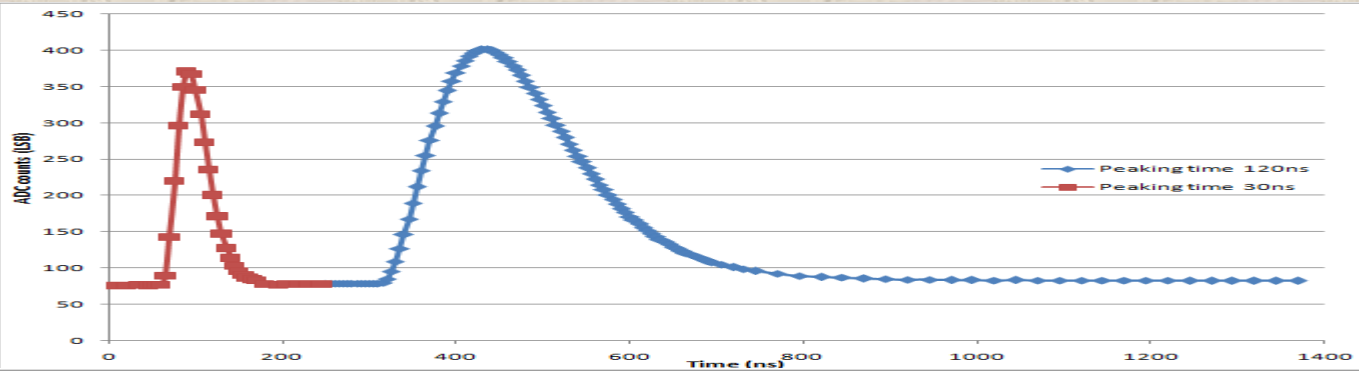


# Test Board Design



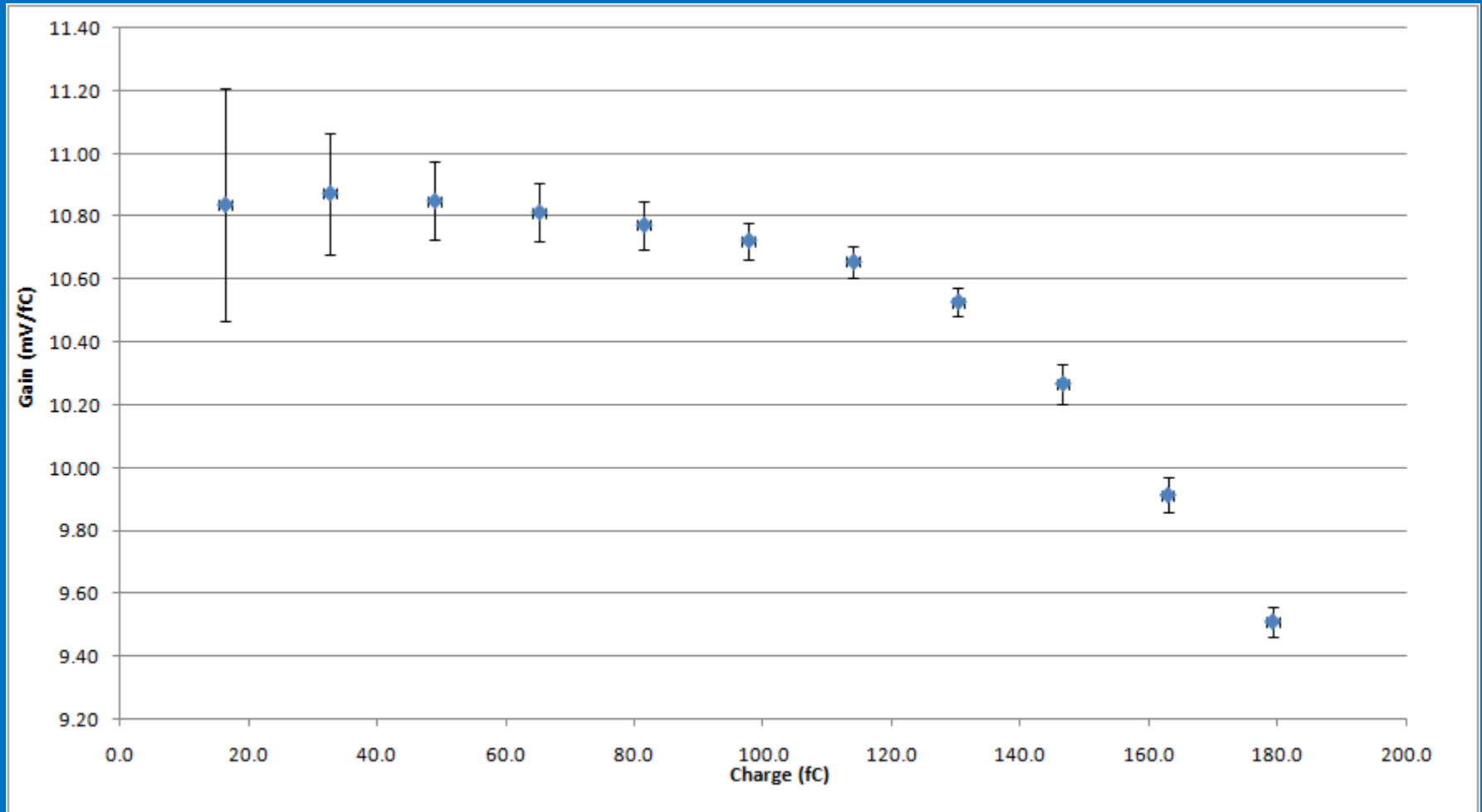


# Acquired pulses + noise



**Transient noise during acquisition of pulses.**

# Gain plot



**12mV/fC, 120ns, Low polarity**

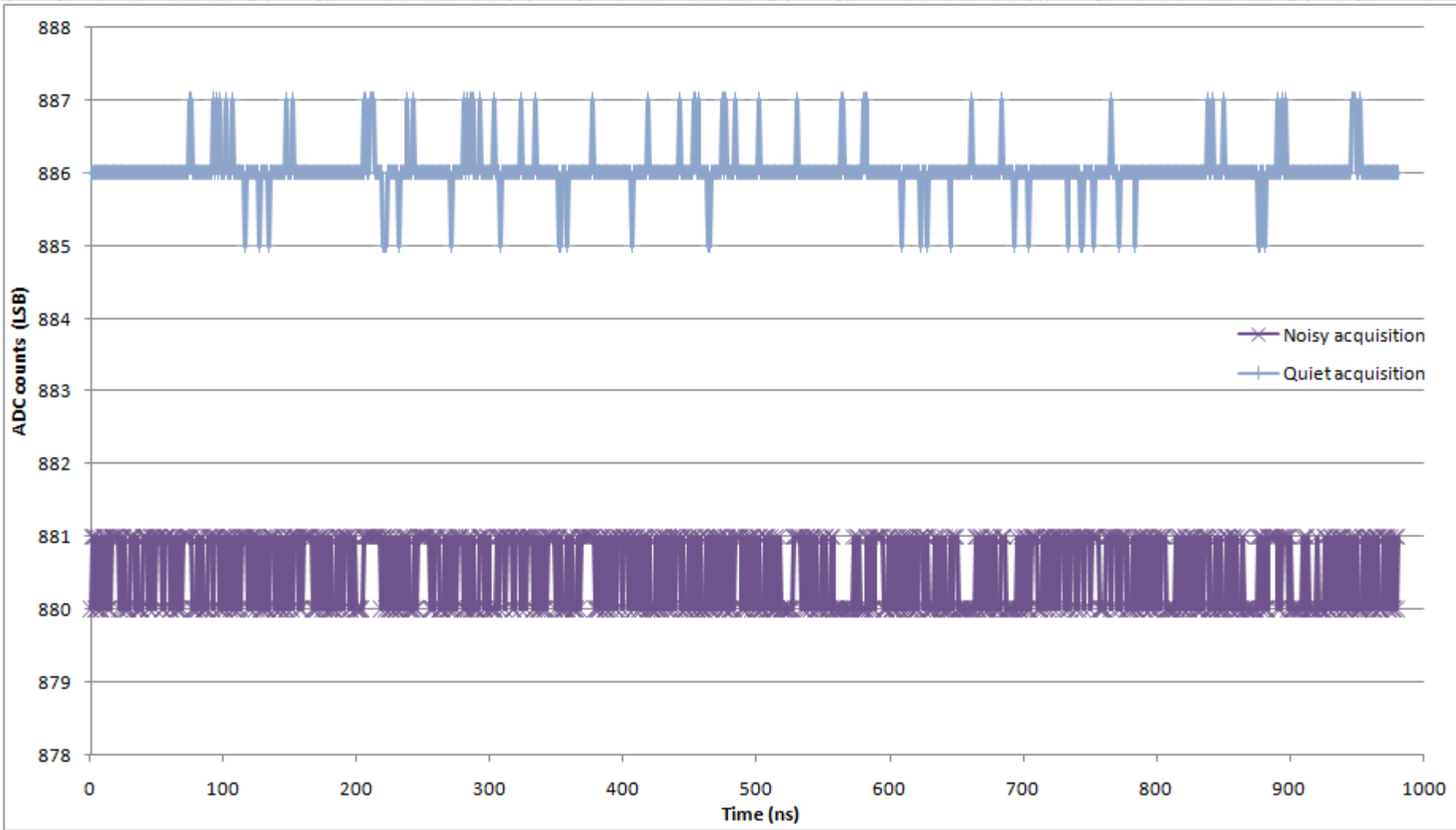
**gain: 10.7mV/fC 4.1%**

# Crosstalk & baseline

**Crosstalk between adjacent channels <0.7%.**

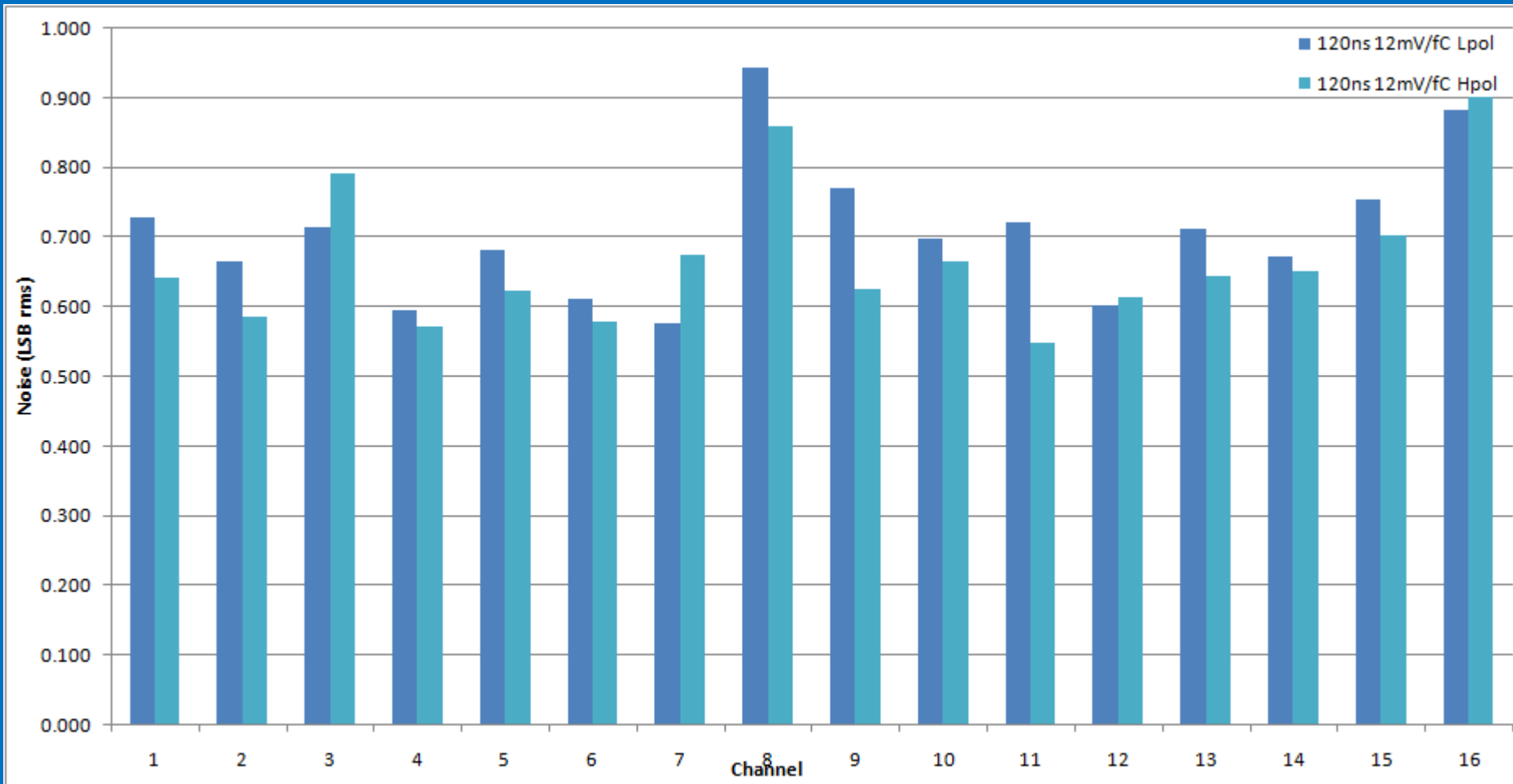
**Channel-to-channel maximum baseline difference of about 30LSB (60mV).**

# Noise 1



**The influence of the ADC resolution on noise**

# Noise: PGA4



**PGA4 inputs bonded**

**Noise variation with the channel number**

# Zero Suppression example

