Specification

SAltro16 carrier board

This document is a specification concerning the principle of mounting the SAltro16 die onto a small board to simplify its mounting onto electronics.

Document History

Rev.	Date	Author	Comment
0	2011-11-27	Björn Lundberg	
1	2012-01-01	Björn Lundberg	Added bond info

Background

The SAltro16 chip is a 16-channel integrated low-noise amplifier, signal shaper, 10-bit ADC and a digital signal processing unit and was developed by CERN in order to be able to build compact detector electronics.
Unfortunately the chip is only made in small quantities so that chip-scale packaging is not an option since developing a chip-scale package would be too costly.
The available mounting options for the SAltro16 chip on a detector are

a) Using standard packaging
b) Bond chip-die directly on read-out board
c) Use intermediate chip-carrier board

Option a) takes too much space and options b) relies too much on the individual chip-yield. This document describes option c), bonding the die onto a small intermediate chip carrier board.

Specification

The bare SAltro16 chip is a silicon die measuring 8.56x5.75 mm^2 with 229 bond-pads.
A chip carrier board's function is to fan out the die's bond-pads onto a footprint that is comparable to the size of the die itself while still possible to mount using standard component-mounting techniques. It should also allow chip-testing on a per-die basis instead of testing a complete mounted board with several bonded dies.

The size of the carrier board was chosen to be 11x8mm^2 as this allows enough space for the bond-pads as well as some passive components that should be placed close to the chip and to save board-space on the read-out board.
A BGA footprint with 0.5 pitch was selected in order to fit enough pads to fan out all the dies bond-pads.

Description

The SAltro16 carrier board has the die mounted on top together with some passive components around its peripheral on top of a 1.0mm thick PCB as shown in figure 1.
The passive components are de-coupling capacitors and filter networks (RC) and the capacitors and resistors are of the size 0201 or 0603 Metric which is 1.0x0.5mm^2 in size.

The bottom side of the PCB has a 0.5mm pitch BGA pattern arranged in a non-fully populated 13x20 ball-matrix with pin designation as shown in figure 2.
Table 1 list the pins in the BGA footprint

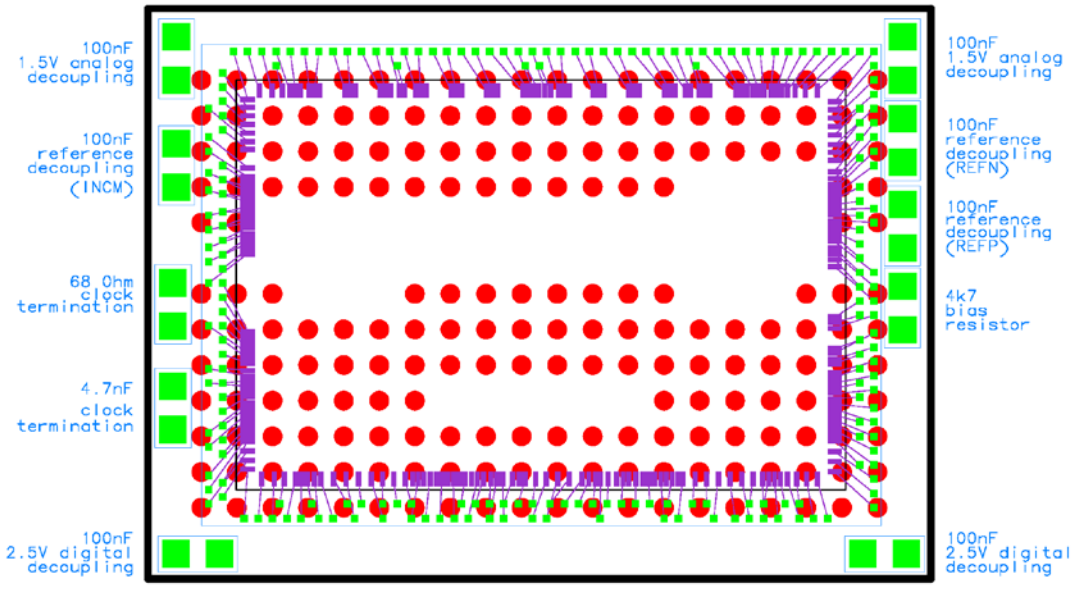


Figure 1 **Saltro16 carrier board chip bonding & component mounting**

Figure 2 **Carrier board and die in natural size!**

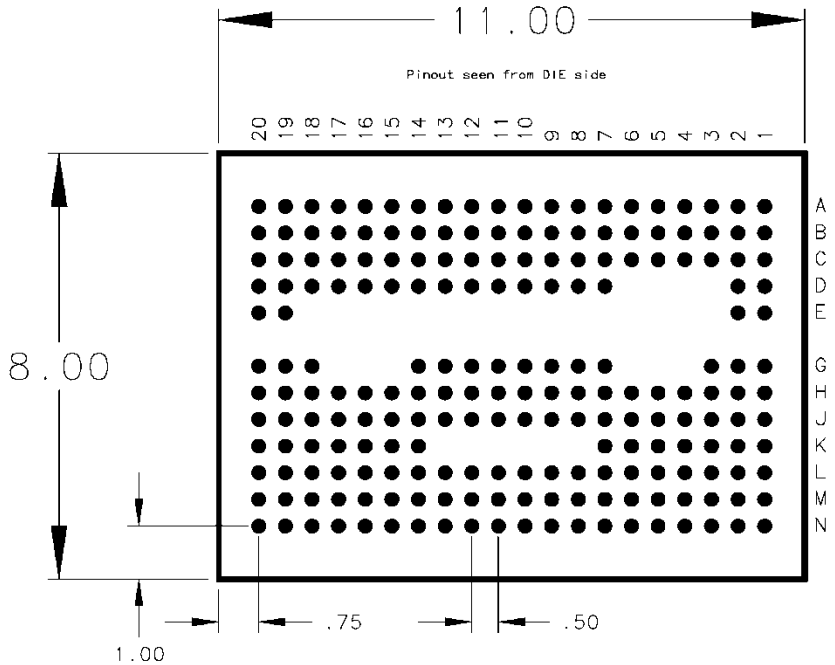


Figure 3 **SAltro16 carrier board footprint**

Table 1 BGA footprint pinlist

Pin function	Pin designation
Analog ground	D1, D7-D20, G2
Digital ground	H6-H18,J5-J15
Analog power	C5-C18
ADC power	G7-G14
Digital power	G3,H2,H3,K4-K5
Output driver	K6,K7,K14-K16,L5,L6,L8-L10,L13-L16
Chip guardring (ground)	H4,H5
Chipaddress AD0-AD7	H1,J2-J4,J17,J19,K17,J20
Input 15-0	A3-A18
InputGround 15-0	B3-B18
Outputs 0,1,2…39	N1,M1,N2,M2,N3,M3…N19,M19,N20,M20
ADCTestN, ADCTestP	C2,D2
Gain1,Gain2	A19,B19
Shaper1-Shaper3	A20,C19,B20
RefN (2 pins), RefP	C1,E19,E1
TestMode	A1
Shutdown	A2
PasaTestN,PasaTestP	B1,B2
Preampenable	C3
DecayBias	C4
CMOut1,2	G20,G1
CLKAUX	G18
ADCAdd0,1	K2,J1
_TRG	K1
_L2Y	L2
_TMS	K3
_ACK	L4
_ACKEN	L3
SCANEN	L7
RDOClk	L11
ScanMode	L12
_CSTB	J16
_DSTB	L17
_RST	J18
_DOLOEN	K18
_GRST	K19
_TRSF	L18
_TRSFEN	L19
_ERROR	L20

Chip bonding

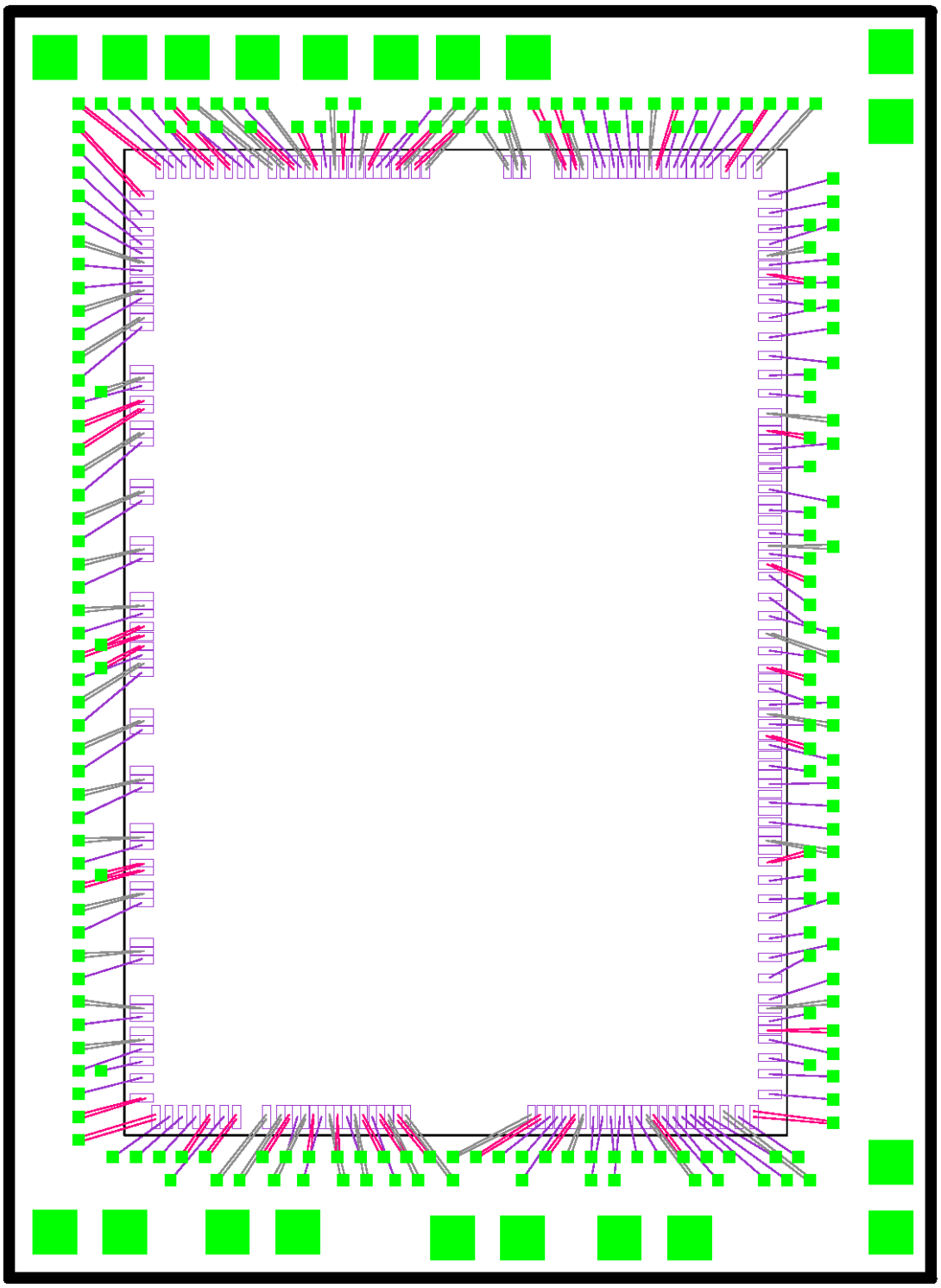


Figure 4 SAltro16 bonding

Figure 3 shows the expected bonding scheme for the SAltro16 die and the location of the bond-pads on the die.
The minimum distance between the die and the bond-pads is 125um which requires that the dicing doesn't give larger die than according to specifications.

In order to further decrease power impedance and increase the performance of the power delivery system by lowering resistance and inductance of power bonds, power pads should have multiple bond-wires attached.
Shown in figure 3 are the ground bond-wires in grey and power bond-wires in red.

The copper-area below the die itself has ground potential which is the same as the die substrate. However because of the density of the carrier-board, the area below the die itself can't be cleared from traces or vias and therefore the die should be glued onto the board with non-conducting glue.
The ground-plane below the die will however be connected with the other planes inside the board in order to help transport heat away from the die.

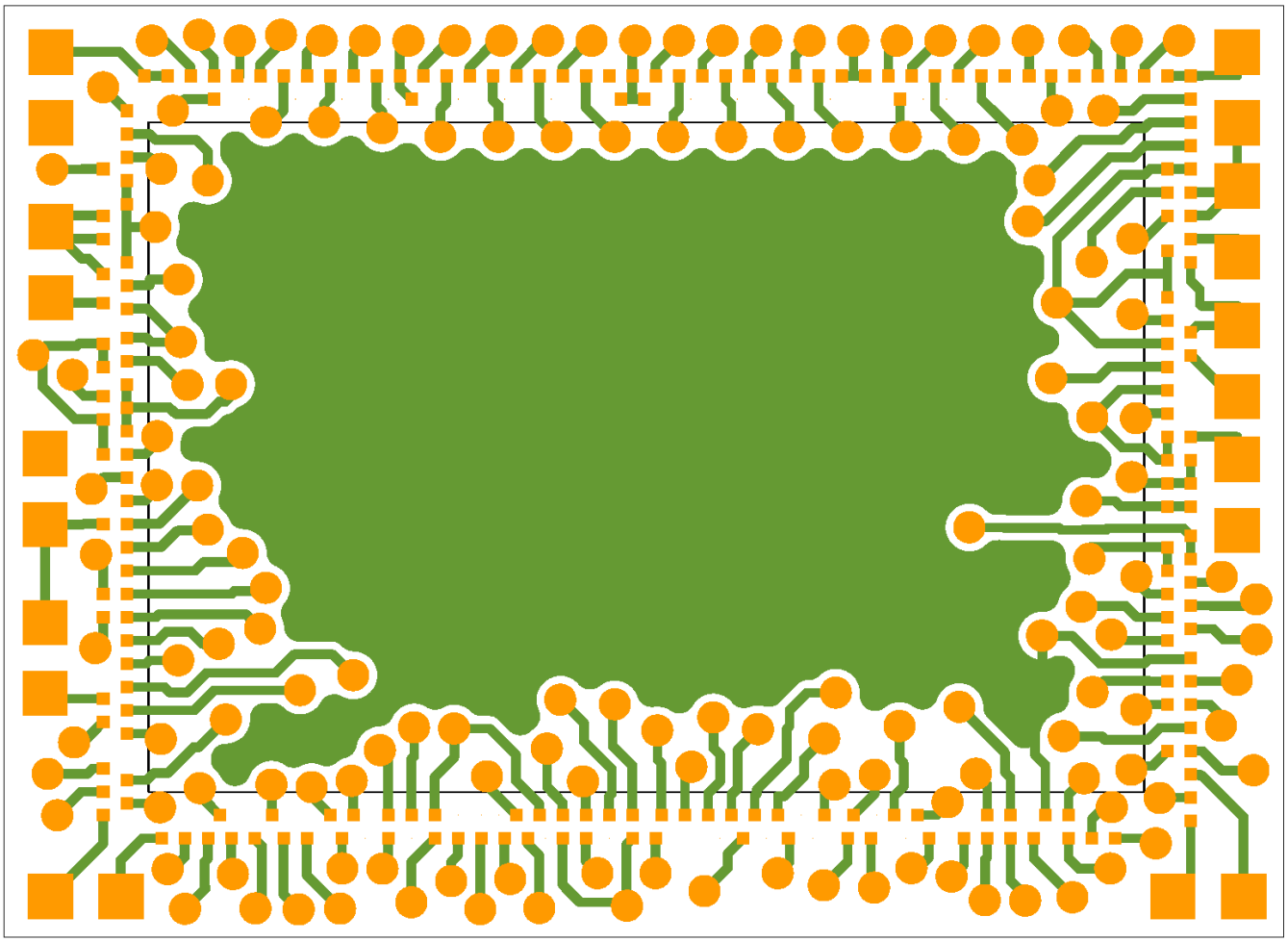


Figure 5 **Top-layer layout view of carrier-board with die outline**

Stack-up

The printed-circuit board (PCB) carrying the SAltro16 die is a 1.0mm thick 8-layer board with 6 signal layers and 2 power-planes. The chip is directly glued and bonded onto the PCB bondpads, a technology called chip-on-board or COB.
A similar technique is when several chips are bonded onto a PCB which is called a multi-chip-module on laminate or MCM-L.
The bonding of the chips directly onto the PCB requires that the surface finish of the PCB can handle the bond-welding of the chip bond-wires and normally a 5um Nickel barrier with a 50nm Gold plating is required (electroplated Nickel-Gold or ENIG).
The suggested stack-up is shown in table 2.

Table 2 Carrier board stack-up

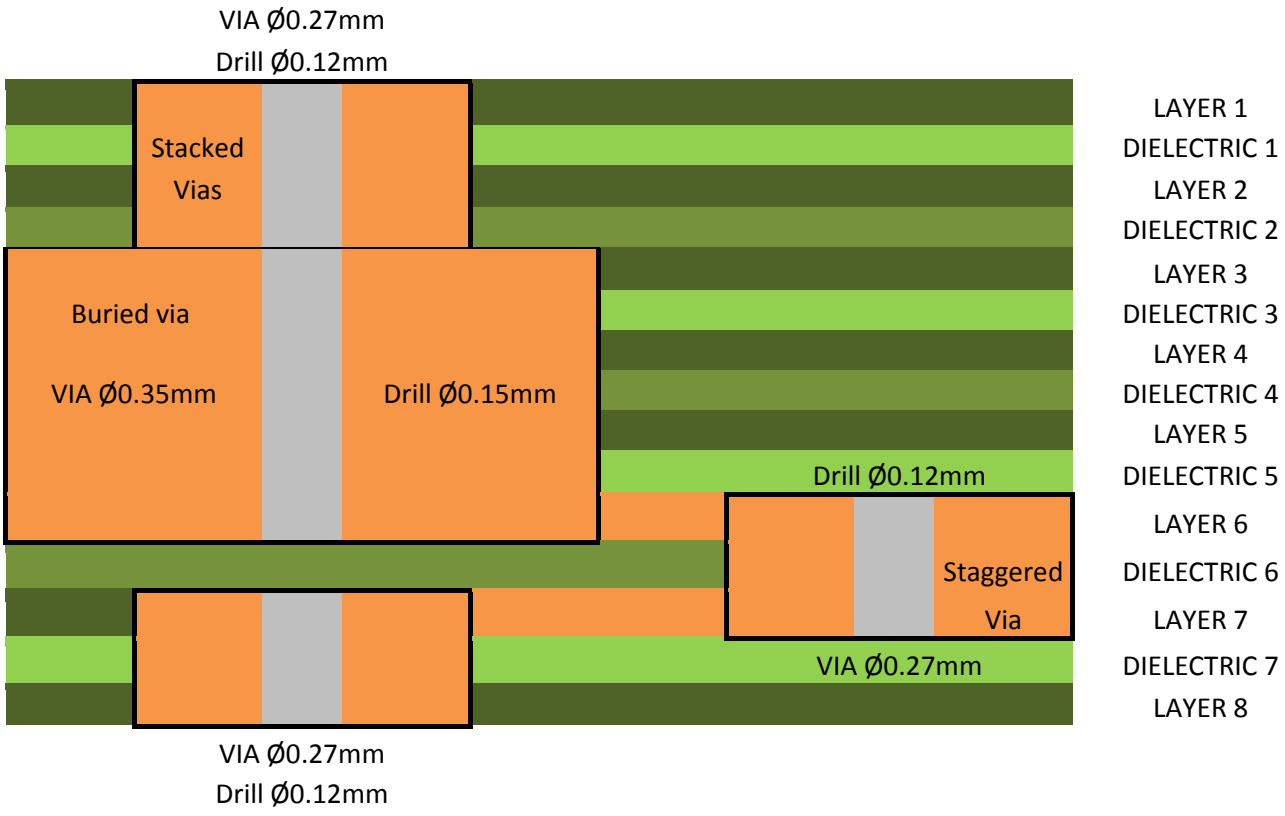
Layer no	Saltro16bga board stack-up Stackup	Material	Layer Thickness unpressed	Layer Thickness pressed
	Plating Gold			
	Plating Nickel	Soldermask	0.02	0.02
	Plating	Copper	0.02	0.02
1	TOP	Copper	0.018	0.018
	Prepreg	2x1080	0.065	0.0362
2	SIGNAL	Copper	0.018	0.018
	CORE	2x1080	0.065	0.065
3	SIGNAL	Copper	0.018	0.018
	Prepreg	2x1080	0.26	0.242
4	PLANE	Copper	0.018	0.018
	CORE	1x106	0.05	0.05
5	PLANE	Copper	0.018	0.018
	Prepreg	2x1080	0.26	0.242
6	SIGNAL	Copper	0.018	0.018
	CORE	2x1080	0.065	0.065
7	SIGNAL	Copper	0.018	0.018
	Prepreg	2x1080	0.065	0.0362
8	BOTTOM	Copper	0.018	0.018
	Plating	Copper	0.02	0.02
	Plating Nickel	Soldermask	0.02	0.02
	Plating Gold			
	Total thickness		1.054	0.9604

Although impedance matching of a board normally is critical in order to get best possible signal integrity, on a board of this size where the vias are more critical that the traces, impedance matching is in practice impossible to maintain and is therefore not enforced although it should be simulated and extracted as an S-parameter file in order to correctly simulate the board where it will be mounted.

Since the density of the board is very high and since the bottom side should be free from any copper except the BGA balls, the design has to be a high-density interconnect board (HDI) using a variety of via techniques interconnecting the different layers.
In order to get the most routing possibilities, the design utilizes blind and buried vias as well as microvias.
A blind via is a via that connects a subset of the available layers but starts from either top or bottom whereas a buried via only connects internal layers and isn't visible from external surfaces. Microvias are small laser-drilled vias (i.e. hole < 0.3mm) that only connects 2 layers of a multi-layer board and exist in different varieties:
Stacked microvias – seen as single via footprint but manufactured as several 2-layer vias
Staggered microvias – several microvias connecting several layers by offsetting the different 2-layer vias.
The buried vias in this design is between layers 3 and 6 and stacked & staggered microvias connect layers 1-3 and 6-8.

Table 3 Via build-up

Stacked & staggered via build-up



Power de-coupling

In order to de-coupling high-frequency noise, it's critical to have as low inductance and low equivalent series resistance (ESR) of the de-coupling capacitors, therefore the capacitors are placed as close to the chip power bond-pads as is physically possible.
The capacitor selection should also be performed with great care in order to get a component with a minimal stray-inductance and ESR and a generic de-coupling capacitor should not be selected.
The power impedance should be simulated to be able to simulate sufficient power de-coupling on the module where the carrier board will be mounted.
The innermost di-electric layer between the two powerplanes should be as thin as possible in order to increase its capacitance and therefore act as power de-coupling with minimal stray inductance for the highest frequency noise components.

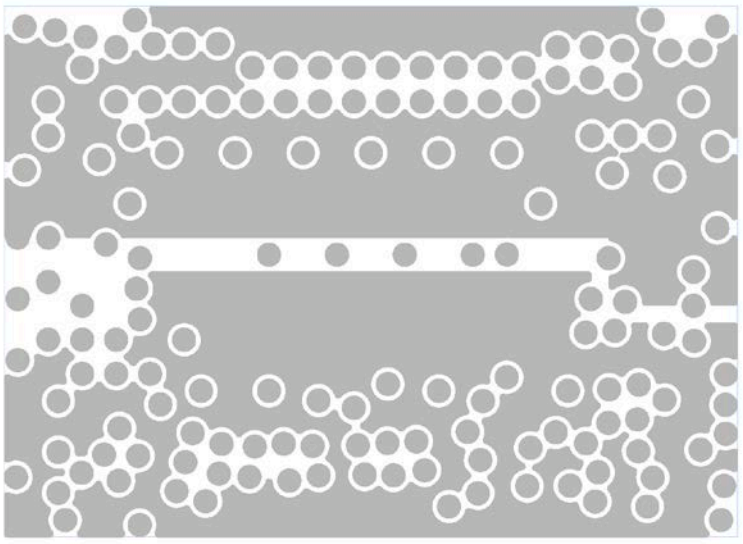


Figure 6 Board internal ground-plane

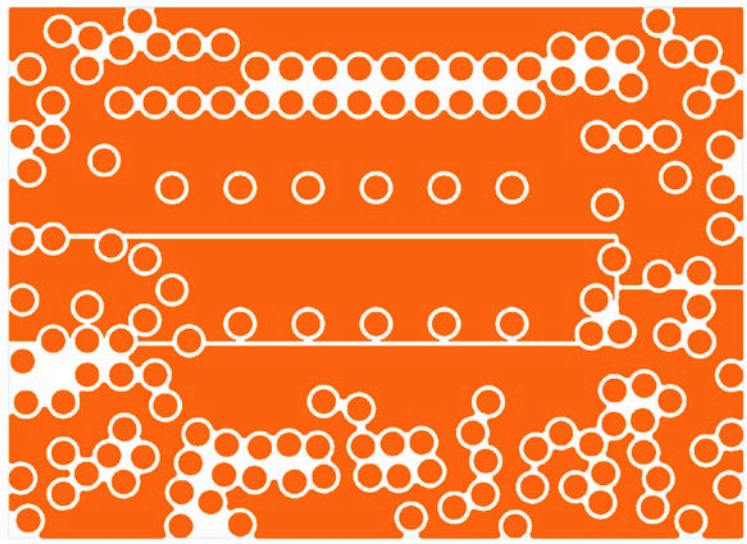


Figure 7 Board internal power-plane

It should be noted when adding power-planes to a dense design that the vias don’t perforate and separate the planes and as can be seen from figures 3 & 4, enough space is available to ensure that the planes are continuous.

The planes are split in an analog part and a digital part reflecting the way the die itself is split up into similar regions. Normally the analog and digital parts should be connected at one point on a board, but since this is a special board that’s supposed to reflect the way the chip is built, the power-split is maintained.