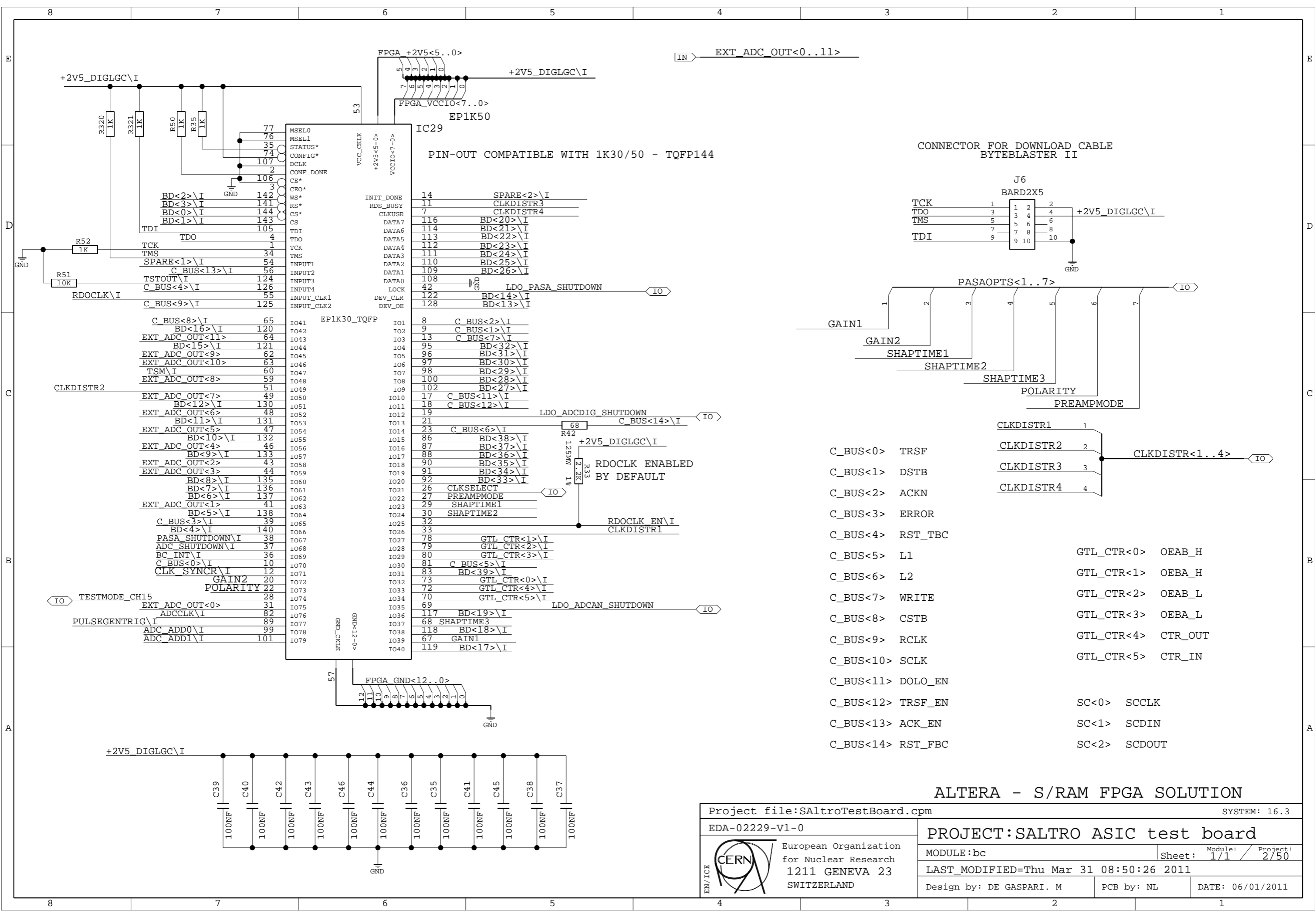


PLACE THIS CONNECTION AT THE EXTERNAL CORNER OF THE CARD
 ADDITIONAL GND CONNECTIONS FOR TEST/DEBUGGING PURPOSE

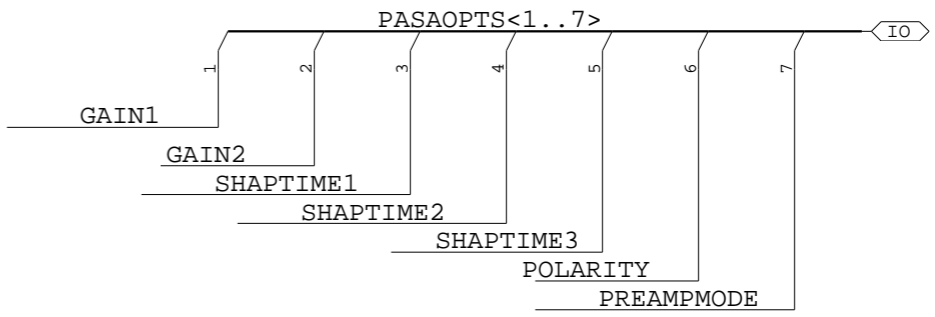
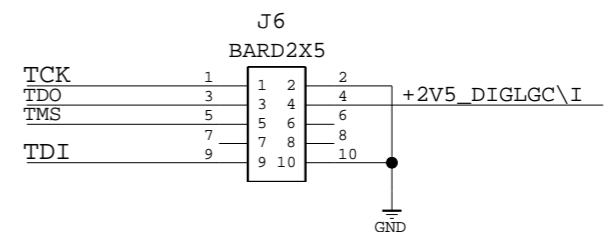
11 10 9 8 7 6 5 4 3 2 1
 P O M L K J I H G F E D C B A



IC29
PIN-OUT COMPATIBLE WITH 1K30/50 - TQFP144

| | | | | | | |
|-----------------|-----|------|-------------|------|-----|--------------------|
| MSEL0 | 77 | IO41 | EP1K30_TQFP | IO1 | 8 | C_BUS<2>\I |
| MSEL1 | 76 | IO42 | | IO2 | 9 | C_BUS<1>\I |
| STATUS* | 35 | IO43 | | IO3 | 13 | C_BUS<7>\I |
| CONFIG* | 74 | IO44 | | IO4 | 95 | BD<32>\I |
| DCLK | 107 | IO45 | | IO5 | 96 | BD<31>\I |
| CONF_DONE | 2 | IO46 | | IO6 | 97 | BD<30>\I |
| CE* | 106 | IO47 | | IO7 | 98 | BD<29>\I |
| CEO* | 3 | IO48 | | IO8 | 100 | BD<28>\I |
| WS* | 142 | IO49 | | IO9 | 102 | BD<27>\I |
| RS* | 141 | IO50 | | IO10 | 17 | C_BUS<11>\I |
| CS* | 144 | IO51 | | IO11 | 18 | C_BUS<12>\I |
| CS* | 143 | IO52 | | IO12 | 19 | C_BUS<14>\I |
| TDI | 105 | IO53 | | IO13 | 21 | C_BUS<6>\I |
| TDO | 4 | IO54 | | IO14 | 23 | C_BUS<6>\I |
| TCK | 1 | IO55 | | IO15 | 86 | BD<38>\I |
| TMS | 34 | IO56 | | IO16 | 87 | BD<37>\I |
| SPARE<1>\I | 54 | IO57 | | IO17 | 88 | BD<36>\I |
| C_BUS<13>\I | 56 | IO58 | | IO18 | 90 | BD<35>\I |
| TSTOUT\I | 124 | IO59 | | IO19 | 91 | BD<34>\I |
| C_BUS<4>\I | 126 | IO60 | | IO20 | 92 | BD<33>\I |
| C_BUS<9>\I | 125 | IO61 | | IO21 | 26 | CLKSELECT |
| C_BUS<8>\I | 65 | IO62 | | IO22 | 27 | PREAMPMODE |
| BD<16>\I | 120 | IO63 | | IO23 | 29 | SHAPTIME1 |
| EXT_ADC_OUT<11> | 64 | IO64 | | IO24 | 30 | SHAPTIME2 |
| BD<15>\I | 121 | IO65 | | IO25 | 32 | |
| EXT_ADC_OUT<9> | 62 | IO66 | | IO26 | 33 | |
| EXT_ADC_OUT<10> | 63 | IO67 | | IO27 | 78 | GTL_CTR<1>\I |
| TSM\I | 60 | IO68 | | IO28 | 79 | GTL_CTR<2>\I |
| EXT_ADC_OUT<8> | 59 | IO69 | | IO29 | 80 | GTL_CTR<3>\I |
| BD<12>\I | 130 | IO70 | | IO30 | 81 | C_BUS<5>\I |
| EXT_ADC_OUT<6> | 48 | IO71 | | IO31 | 83 | BD<39>\I |
| BD<11>\I | 131 | IO72 | | IO32 | 73 | GTL_CTR<0>\I |
| EXT_ADC_OUT<5> | 47 | IO73 | | IO33 | 72 | GTL_CTR<4>\I |
| BD<10>\I | 132 | IO74 | | IO34 | 70 | GTL_CTR<5>\I |
| EXT_ADC_OUT<4> | 46 | IO75 | | IO35 | 69 | LDO_ADCAN_SHUTDOWN |
| BD<9>\I | 133 | IO76 | | IO36 | 117 | BD<19>\I |
| EXT_ADC_OUT<3> | 44 | IO77 | | IO37 | 68 | SHAPTIME3 |
| BD<8>\I | 135 | IO78 | | IO38 | 118 | BD<18>\I |
| BD<7>\I | 136 | IO79 | | IO39 | 67 | GAIN1 |
| BD<6>\I | 137 | IO40 | | IO40 | 119 | BD<17>\I |
| EXT_ADC_OUT<1> | 41 | | | | | |
| BD<5>\I | 138 | | | | | |
| C_BUS<3>\I | 39 | | | | | |
| BD<4>\I | 140 | | | | | |
| PASA_SHUTDOWN\I | 38 | | | | | |
| ADC_SHUTDOWN\I | 37 | | | | | |
| BC_INT\I | 36 | | | | | |
| C_BUS<0>\I | 10 | | | | | |
| CLK_SYNCR\I | 12 | | | | | |
| GAIN2 | 20 | | | | | |
| POLARITY | 22 | | | | | |
| TESTMODE_CH15 | 28 | | | | | |
| EXT_ADC_OUT<0> | 31 | | | | | |
| ADCCLK\I | 82 | | | | | |
| PULSEGENTRIG\I | 89 | | | | | |
| ADC_ADD0\I | 99 | | | | | |
| ADC_ADD1\I | 101 | | | | | |

CONNECTOR FOR DOWNLOAD CABLE
BYTEBLASTER II



| | | |
|-----------|---|----------------|
| CLKDISTR1 | 1 | |
| CLKDISTR2 | 2 | CLKDISTR<1..4> |
| CLKDISTR3 | 3 | |
| CLKDISTR4 | 4 | |

| | |
|-----------|---------|
| C_BUS<0> | TRSF |
| C_BUS<1> | DSTB |
| C_BUS<2> | ACKN |
| C_BUS<3> | ERROR |
| C_BUS<4> | RST_TBC |
| C_BUS<5> | L1 |
| C_BUS<6> | L2 |
| C_BUS<7> | WRITE |
| C_BUS<8> | CSTB |
| C_BUS<9> | RCLK |
| C_BUS<10> | SCLK |
| C_BUS<11> | DOLO_EN |
| C_BUS<12> | TRSF_EN |
| C_BUS<13> | ACK_EN |
| C_BUS<14> | RST_FBC |

| | |
|------------|---------|
| GTL_CTR<0> | OEAB_H |
| GTL_CTR<1> | OEBA_H |
| GTL_CTR<2> | OEAB_L |
| GTL_CTR<3> | OEBA_L |
| GTL_CTR<4> | CTR_OUT |
| GTL_CTR<5> | CTR_IN |

| | |
|-------|--------|
| SC<0> | SCCLK |
| SC<1> | SCDIN |
| SC<2> | SCDOUT |

ALTERA - S/RAM FPGA SOLUTION

Project file: SALTroTestBoard.cpm SYSTEM: 16.3

EDA-02229-v1-0

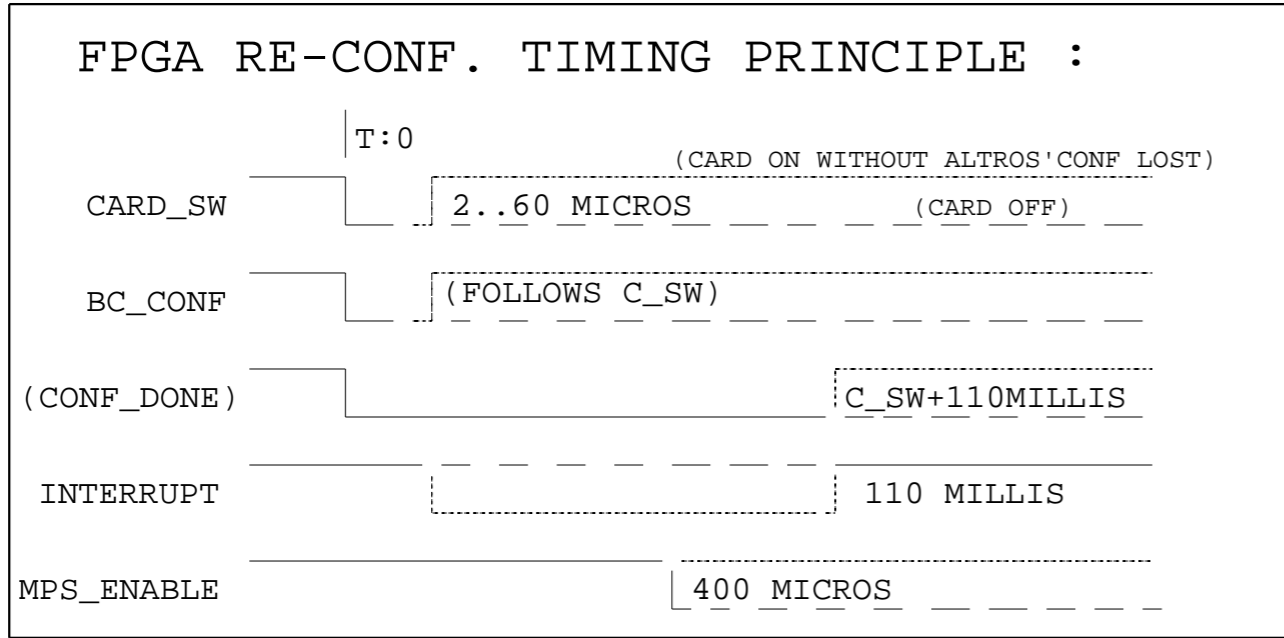
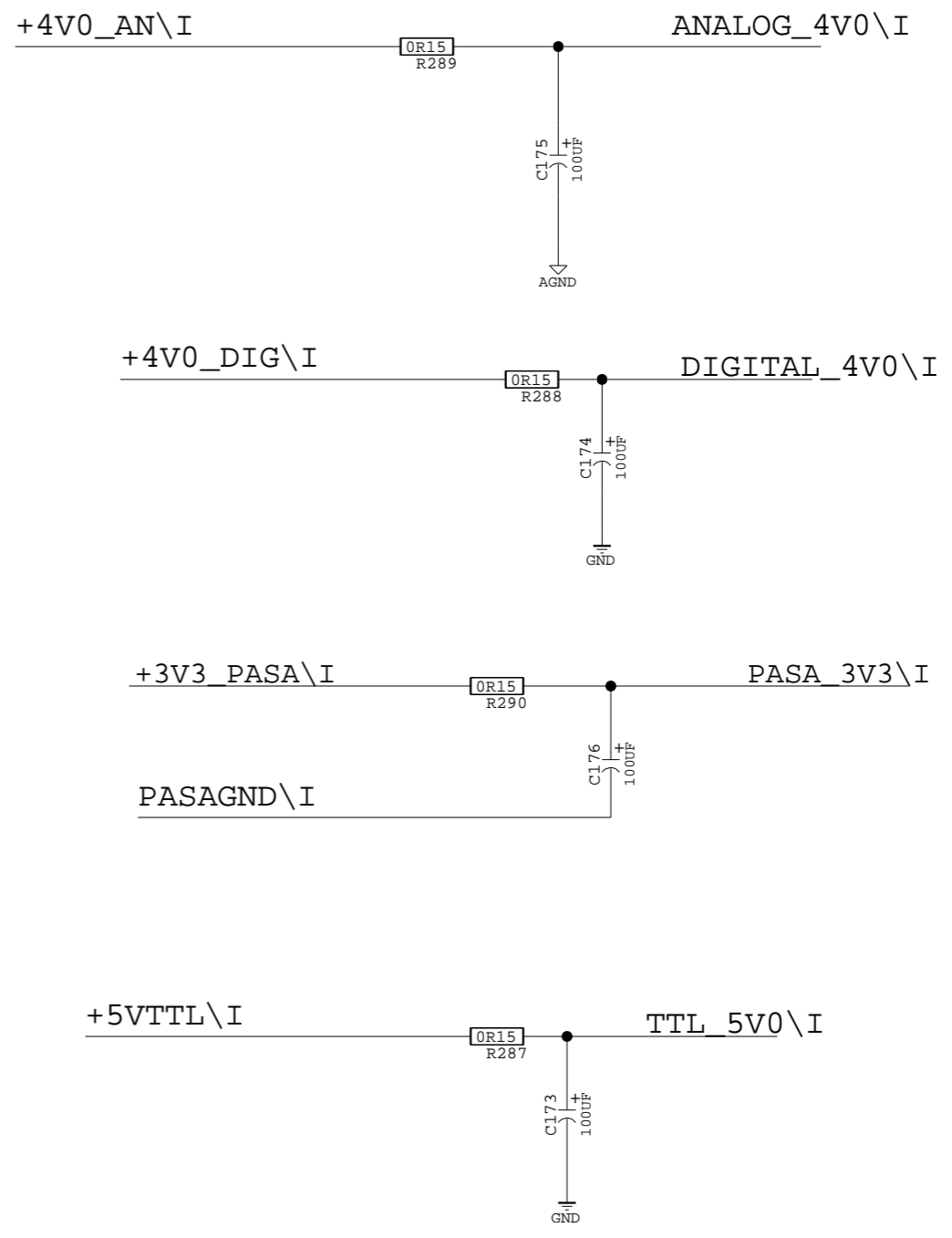
PROJECT: SALTRO ASIC test board

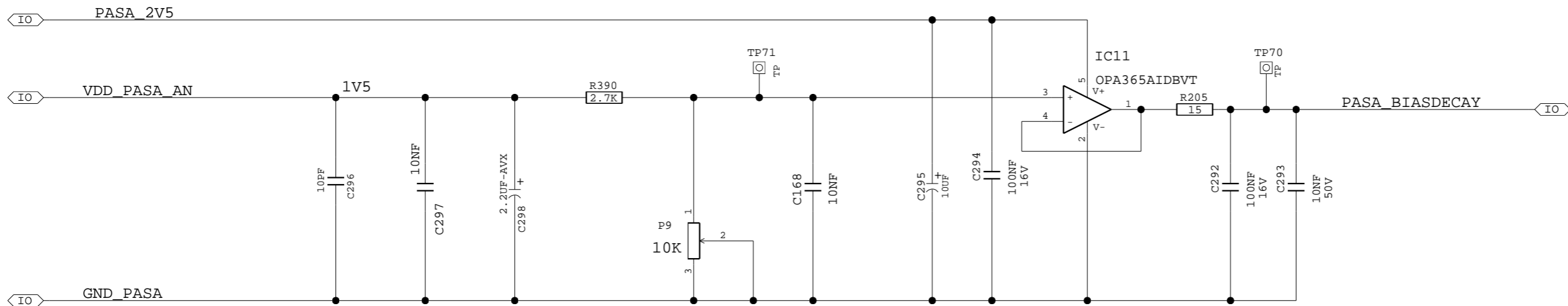
MODULE: bc Sheet: 1/1 Project: 2/50

LAST_MODIFIED=Thu Mar 31 08:50:26 2011

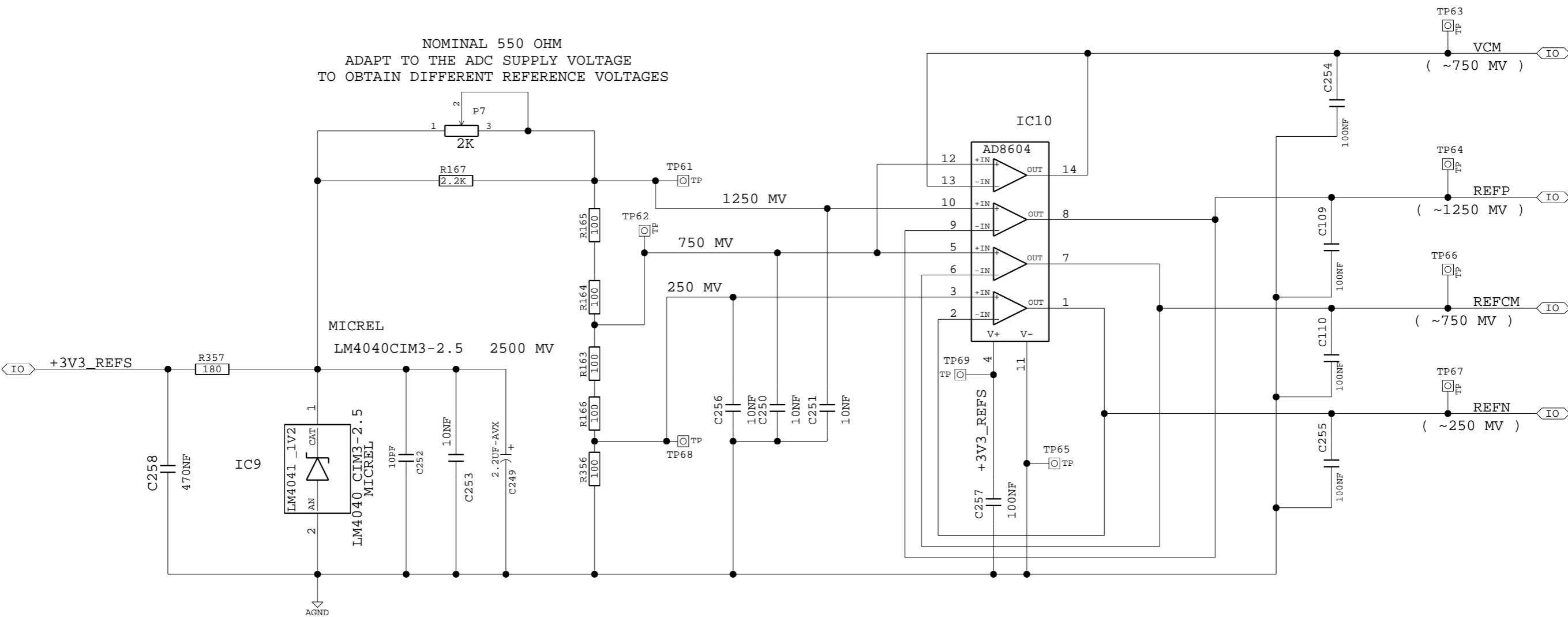
Design by: DE GASPARI. M PCB by: NL DATE: 06/01/2011

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SWITZERLAND

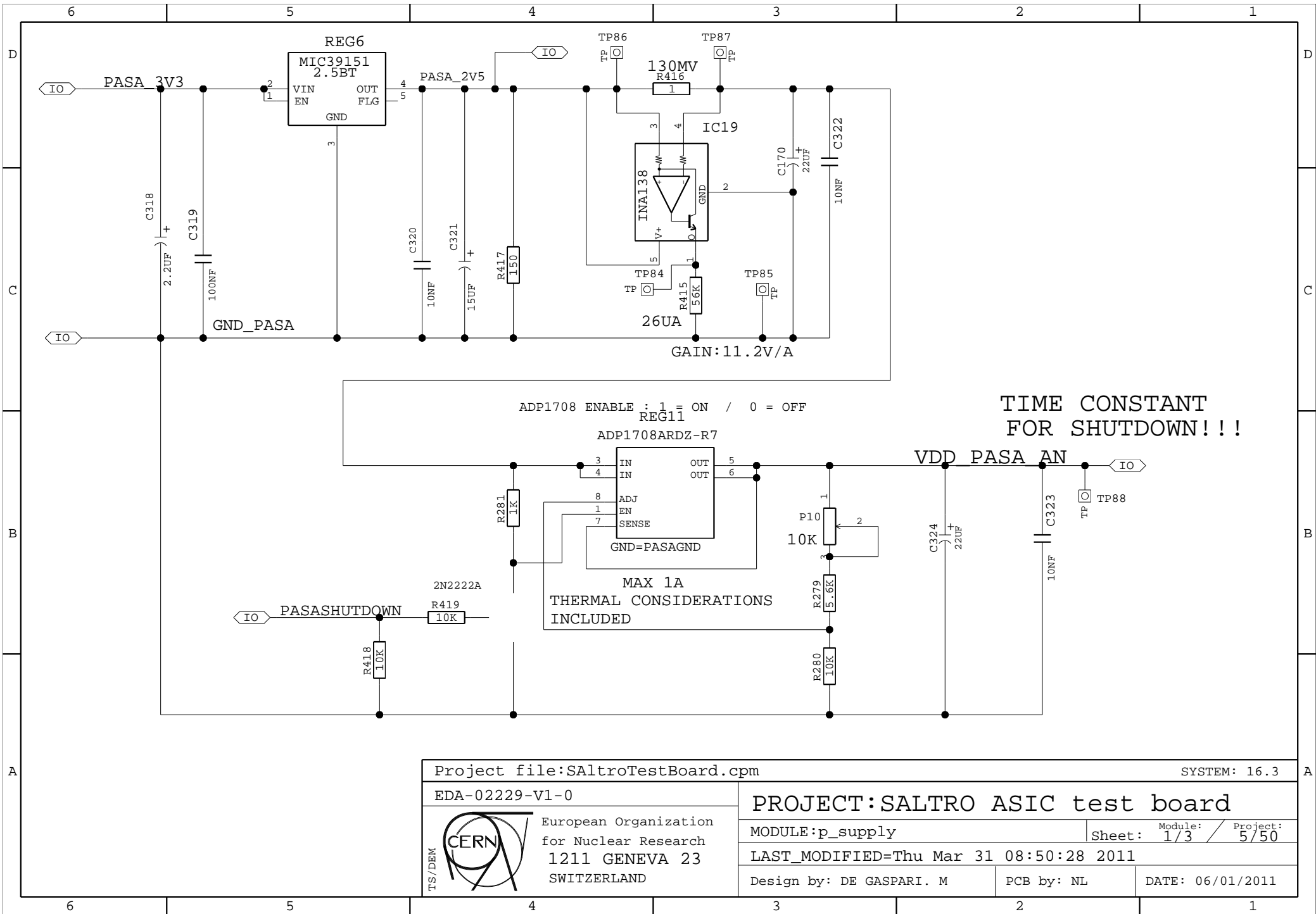




NOMINAL 550 OHM
 ADAPT TO THE ADC SUPPLY VOLTAGE
 TO OBTAIN DIFFERENT REFERENCE VOLTAGES



| | | | |
|--|--|---------------------------------|------------------|
| Project file: SALTroTestBoard.cpm | | SYSTEM: 16.3 | |
| EDA-02229-v1-0 | | PROJECT: SALTRO ASIC test board | |
|  European Organization for Nuclear Research 1211 GENEVA 23 SWITZERLAND | MODULE: vref | Sheet: 1/1 | Project: 4/50 |
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| | Design by: DE GASPARI. M | PCB by: NL | DATE: 06/01/2011 |

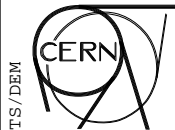


Project file: SaltroTestBoard.cpm

SYSTEM: 16.3

EDA-02229-V1-0

PROJECT: SALTRO ASIC test board



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MODULE: p_supply

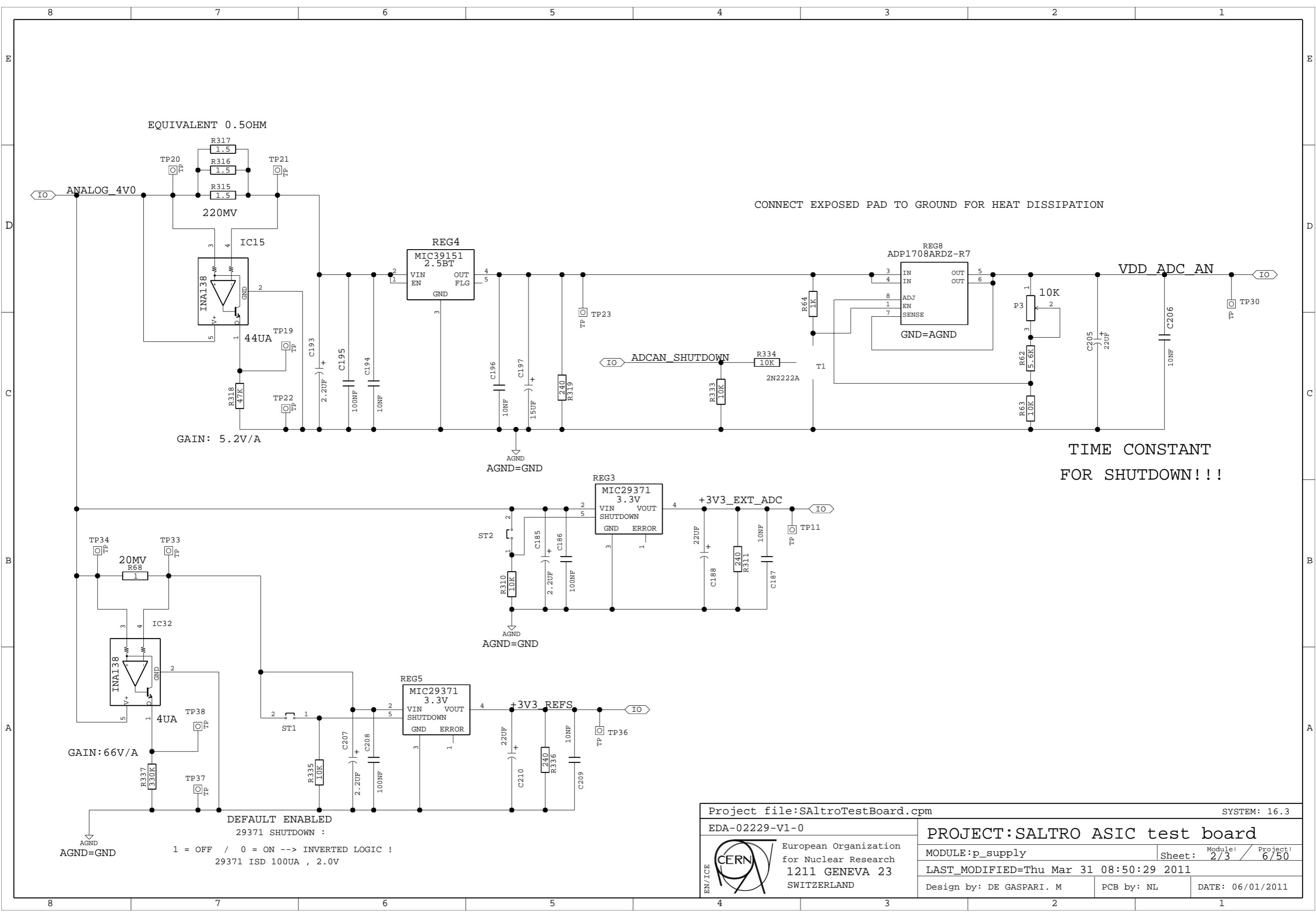
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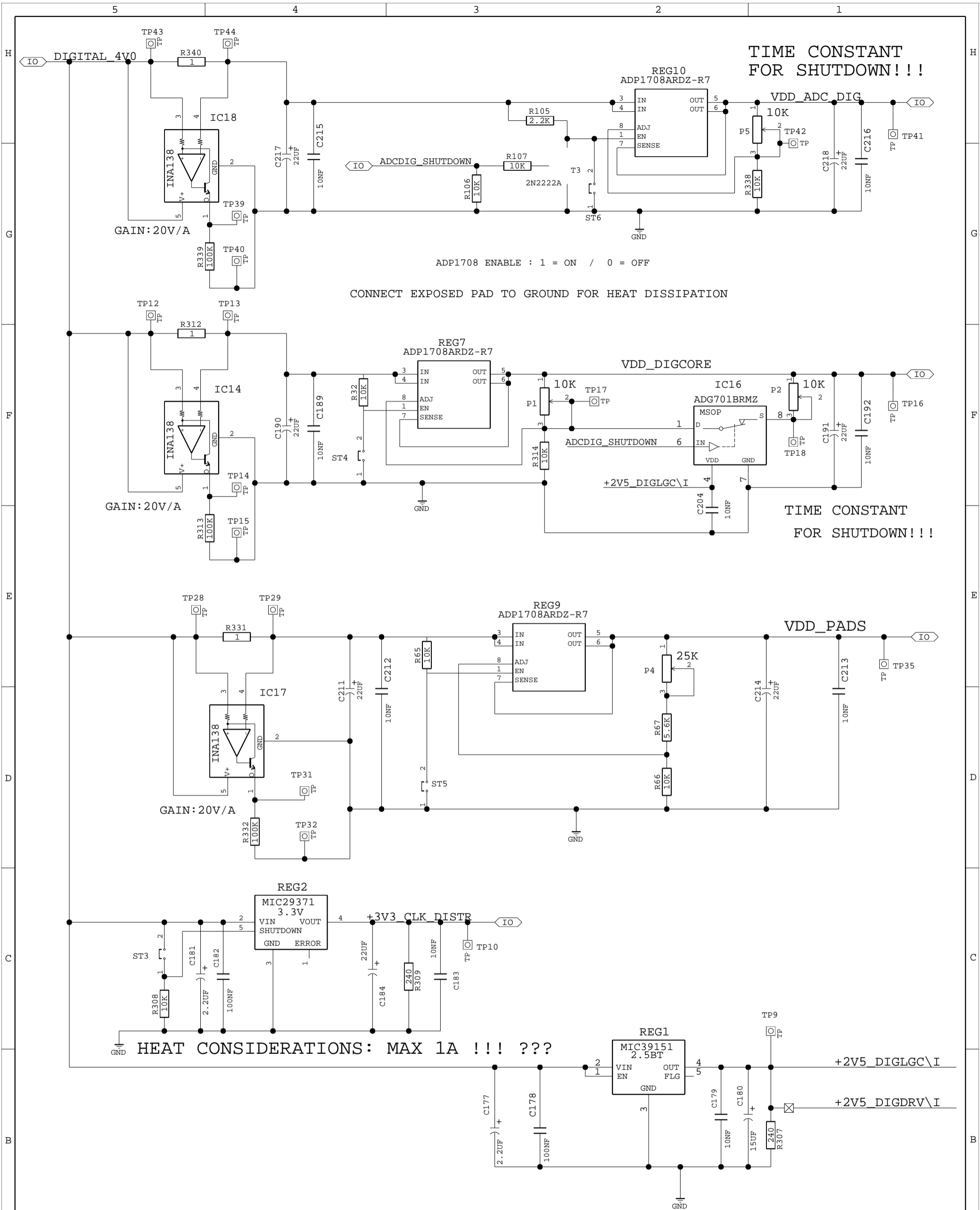
Design by: DE GASPARI. M

PCB by: NL

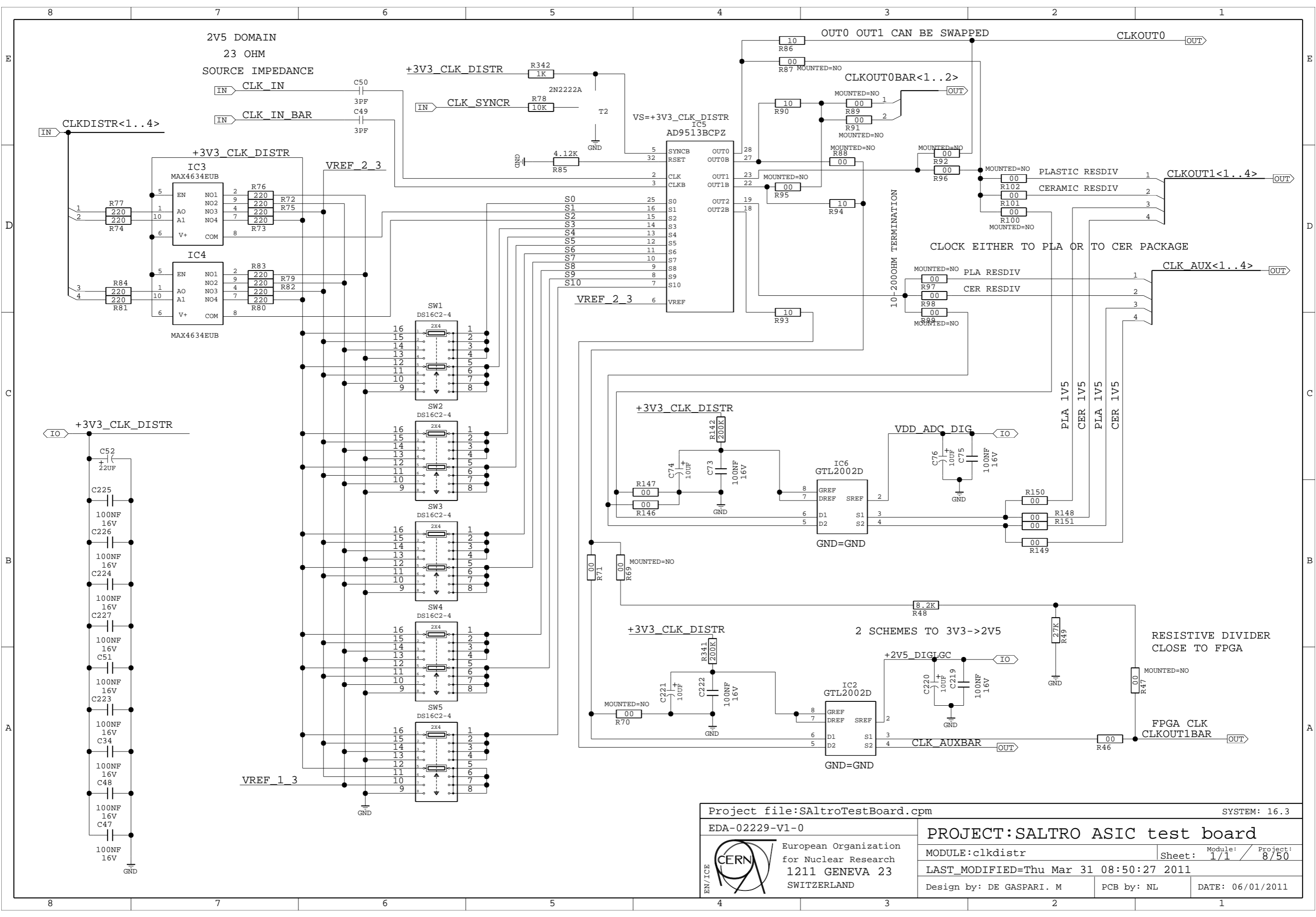
DATE: 06/01/2011




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| Project file: SALTROTestBoard.cpm | | SYSTEM: 16.3 | |
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|  European Organization for Nuclear Research 1211 GENEVA 23 SWITZERLAND | | MODULE: p_supply | Sheet: 2/3 / Project: 6/50 |
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| Design by: DE GASPARI. M | PCB by: NL | DATE: 06/01/2011 | |

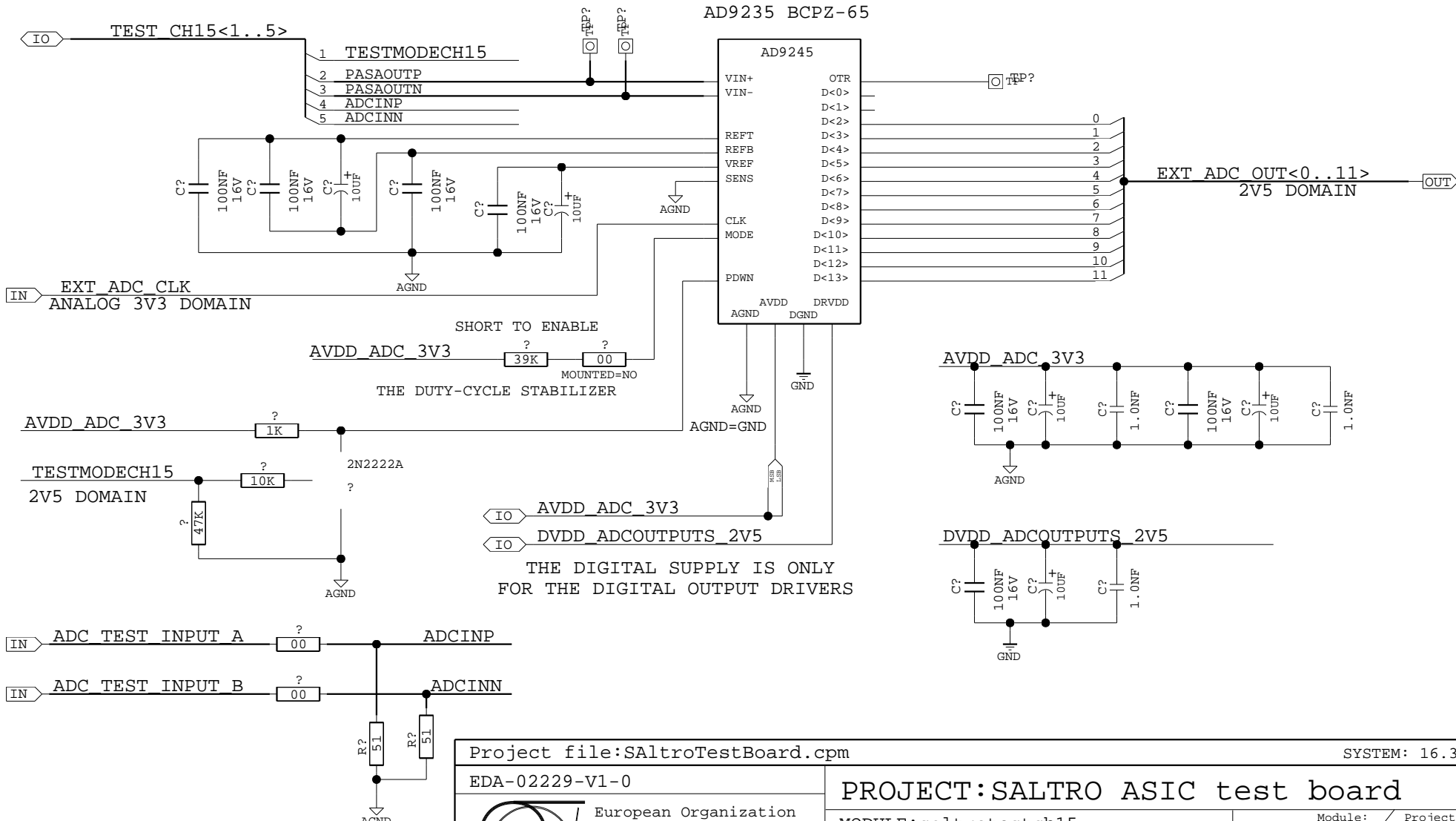


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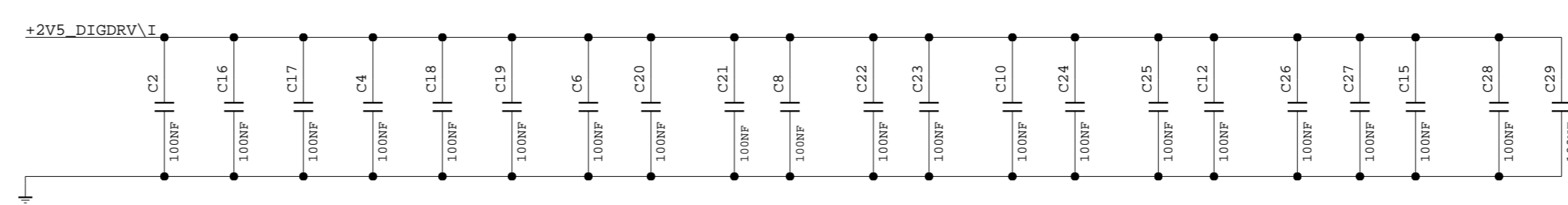
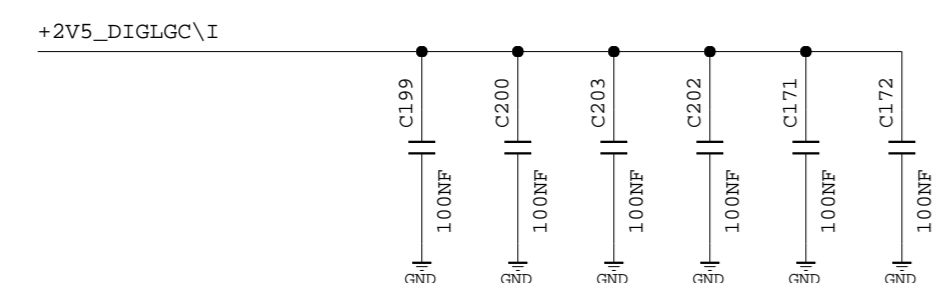
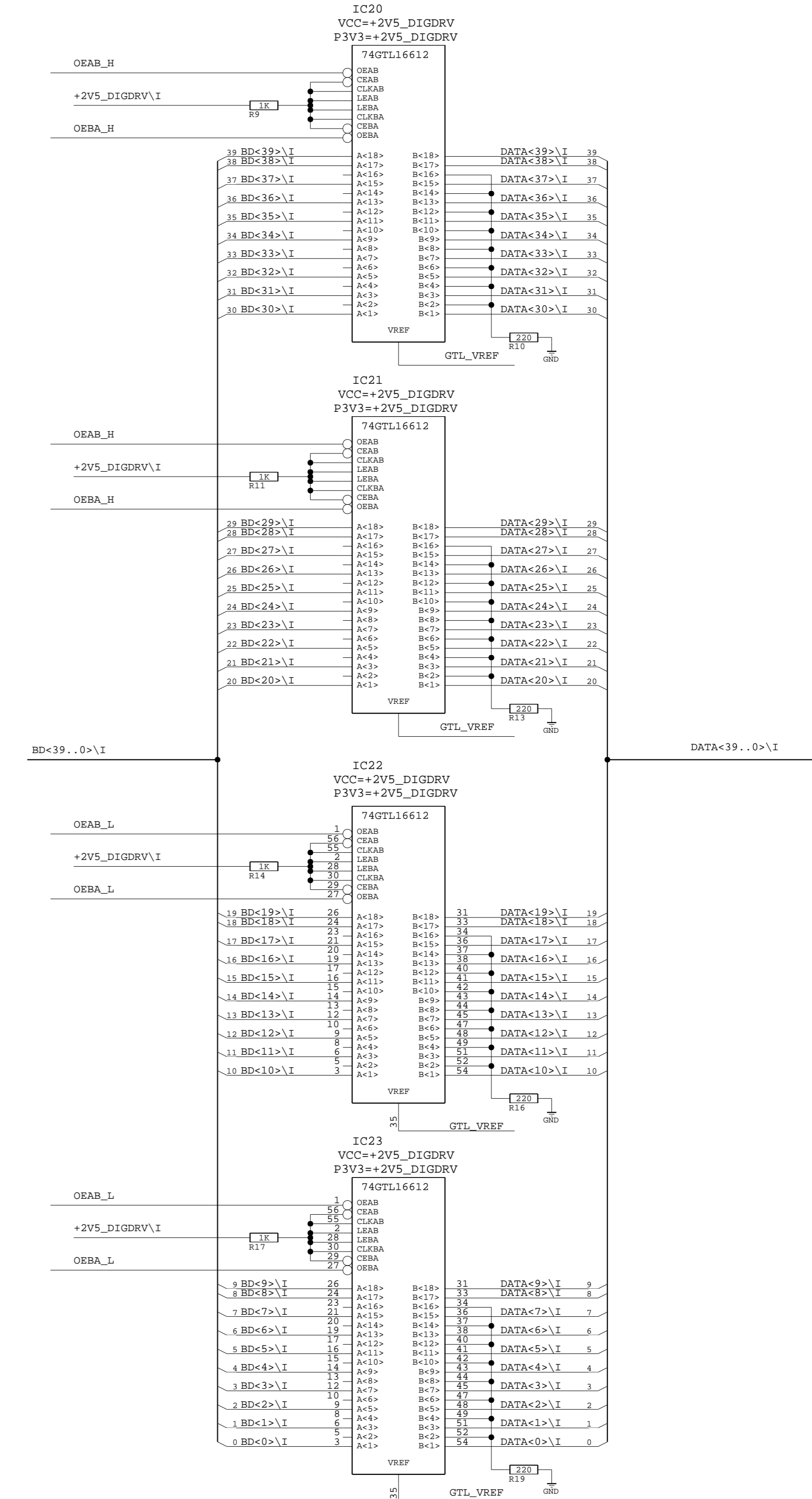
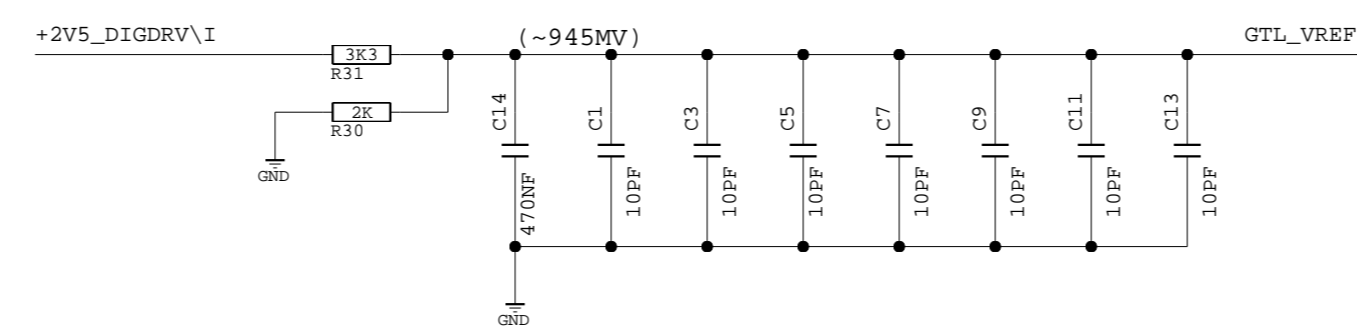
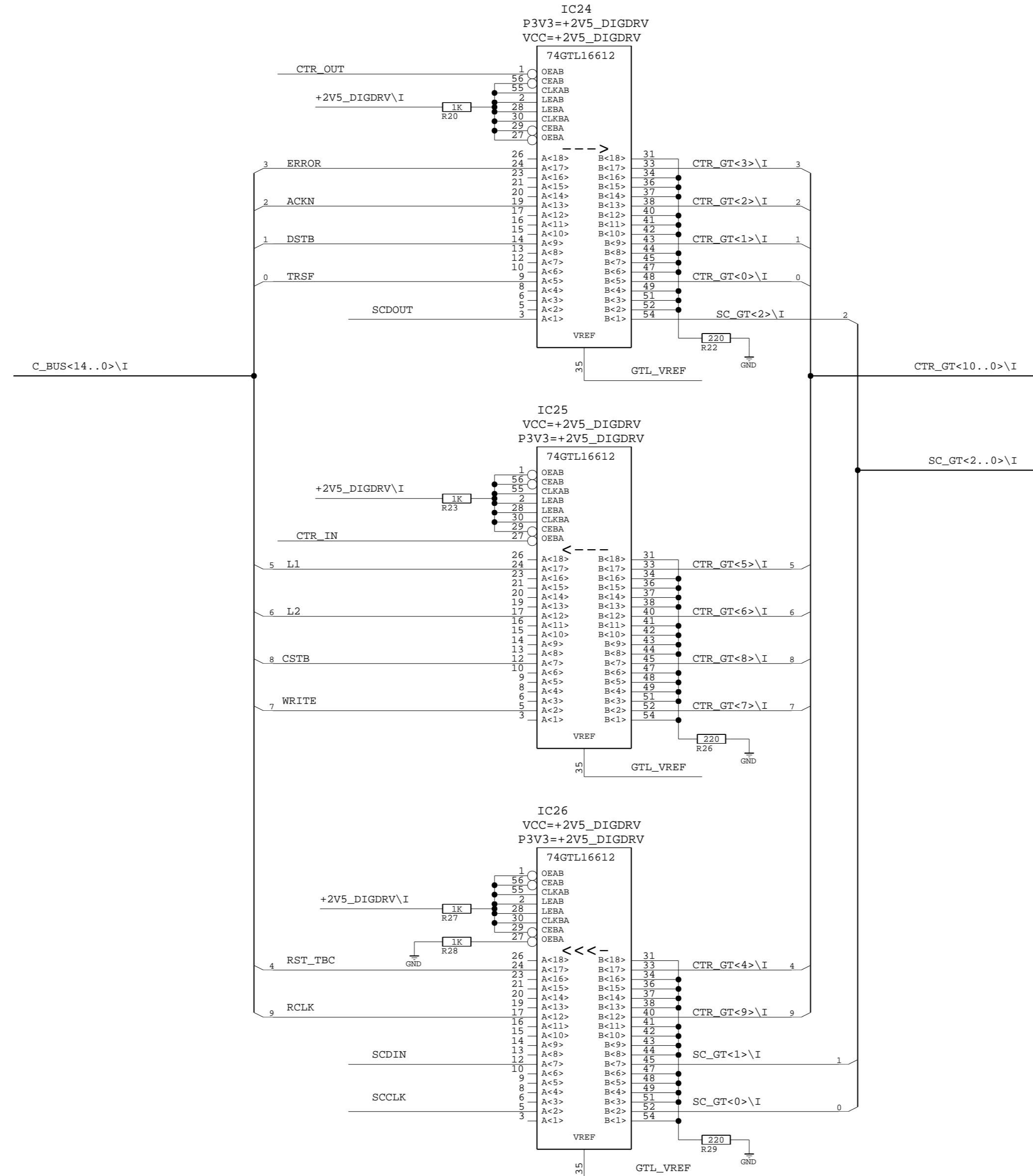
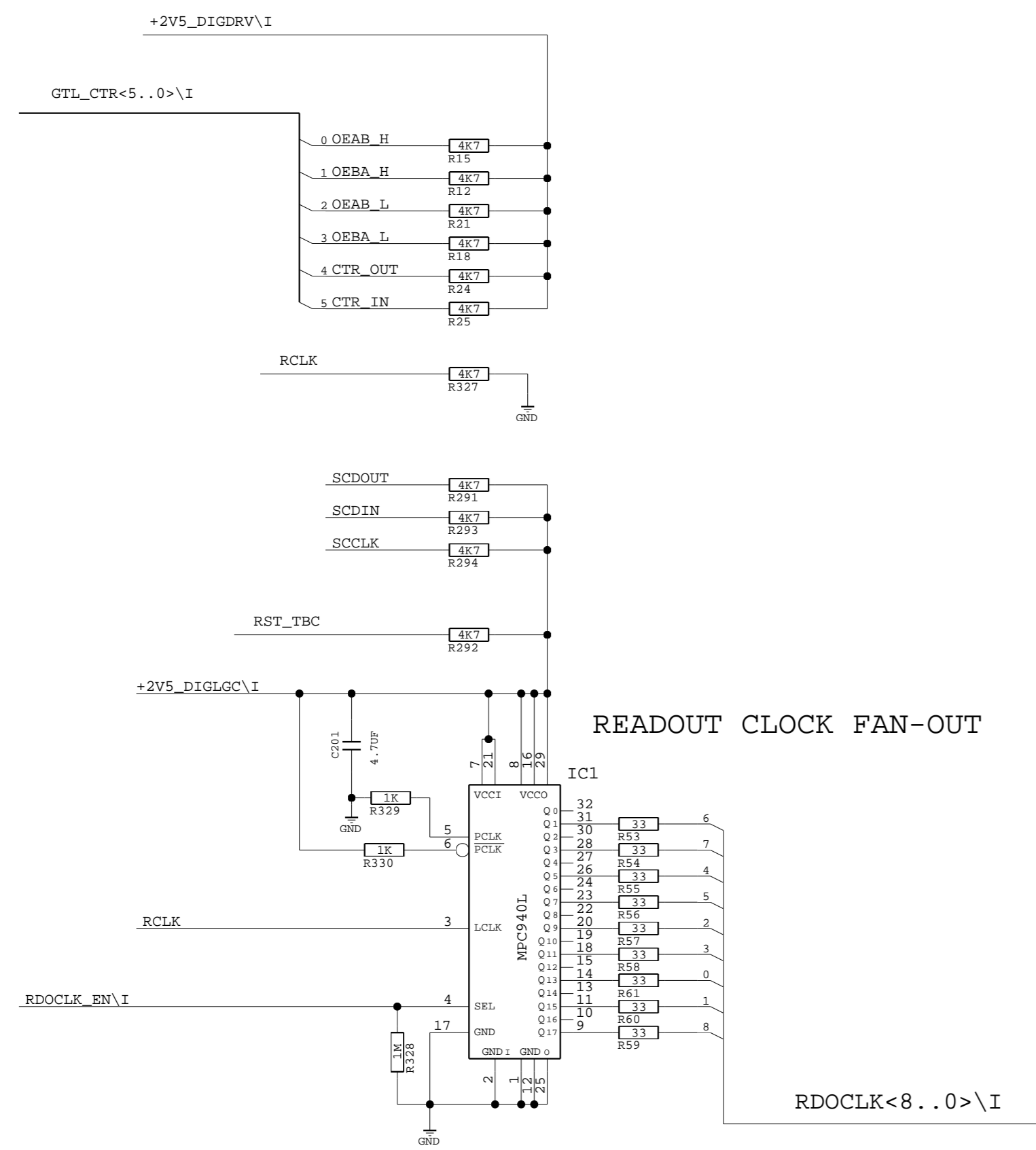


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|  European Organization for Nuclear Research 1211 GENEVA 23 SWITZERLAND | MODULE: clkdistr | Sheet: 1/1 | Project: 8/50 |
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| Design by: DE GASPARI. M | PCB by: NL | DATE: 06/01/2011 | |

AD9235 BCPZ-65
 PACKAGE LFCSP32
 COMPATIBILITY: DON'T CONNECT
 PINS 5-6
 (LEAST SIGNIFICANT BITS)
 AD9235 BCPZ-65

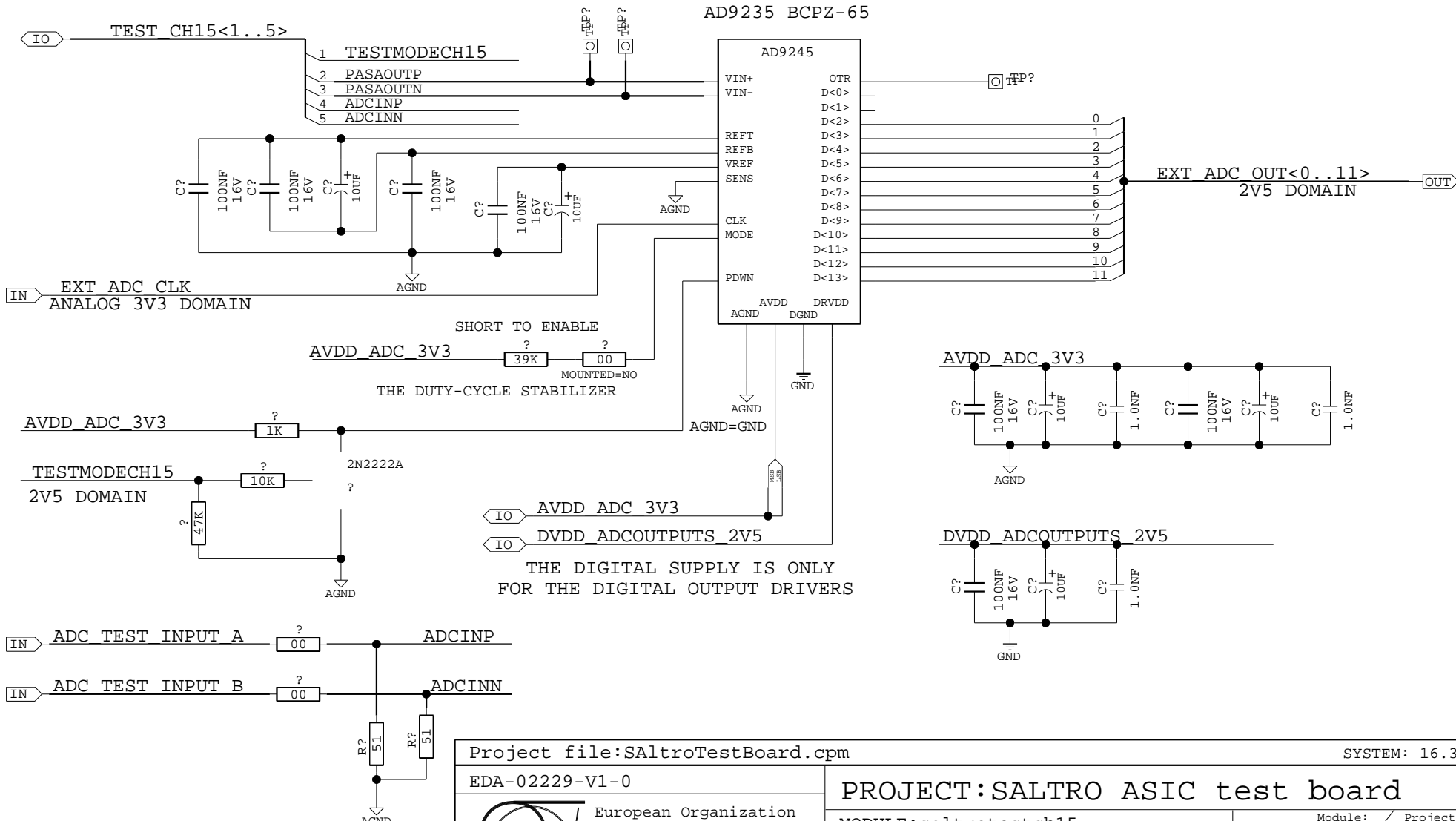


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| | Design by: DE GASPARI. M | PCB by: NL | DATE: 06/01/2011 |

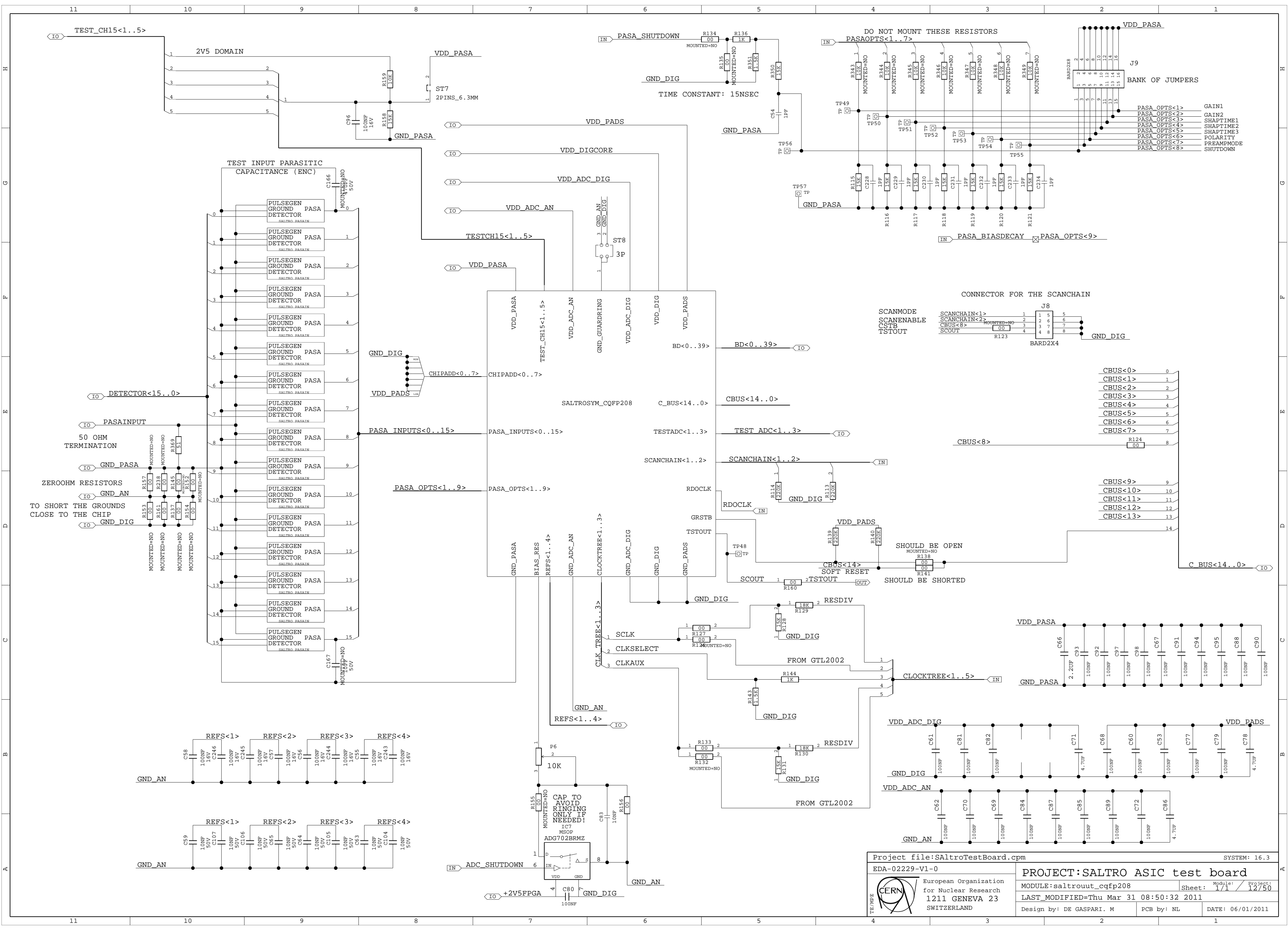


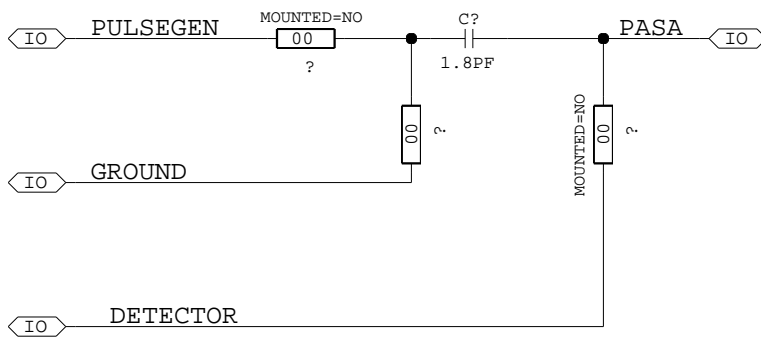
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PHILIPS GTL16612 DGG (IN TSSOP PACKAGE)

AD9235 BCPZ-65
 PACKAGE LFCSP32
 COMPATIBILITY: DON'T CONNECT
 PINS 5-6
 (LEAST SIGNIFICANT BITS)
 AD9235 BCPZ-65



| | | | |
|--|--|---------------------------------|------------------|
| Project file: SaltroTestBoard.cpm | | SYSTEM: 16.3 | |
| EDA-02229-V1-0 | | PROJECT: SALTRO ASIC test board | |
|  European Organization for Nuclear Research 1211 GENEVA 23 SWITZERLAND | MODULE: saltrotestch15 | Sheet: 1/1 / Project: 11/50 | |
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| | Design by: DE GASPARI. M | PCB by: NL | DATE: 06/01/2011 |





Project file: SAltroTestBoard.cpm

SYSTEM: 16.3

EDA-02229-V1-0

PROJECT: SALTRO ASIC test board



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1211 GENEVA 23
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MODULE: saltro_pasain

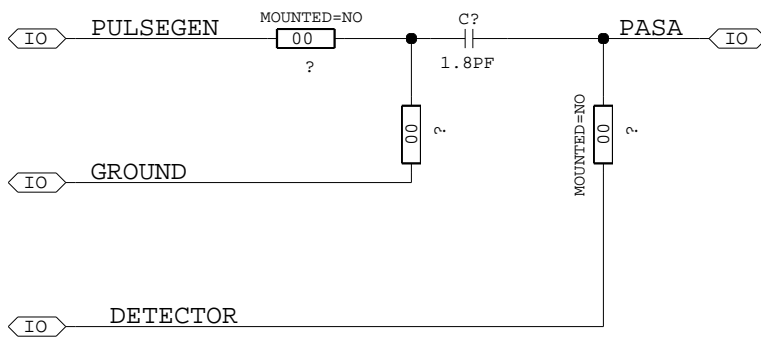
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LAST_MODIFIED=Mon Mar 28 17:35:29 2011

Design by: DE GASPARI. M

PCB by: NL

DATE: 06/01/2011



Project file: SAltroTestBoard.cpm

SYSTEM: 16.3

EDA-02229-V1-0

PROJECT: SALTRO ASIC test board



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1211 GENEVA 23
SWITZERLAND

MODULE: saltro_pasain

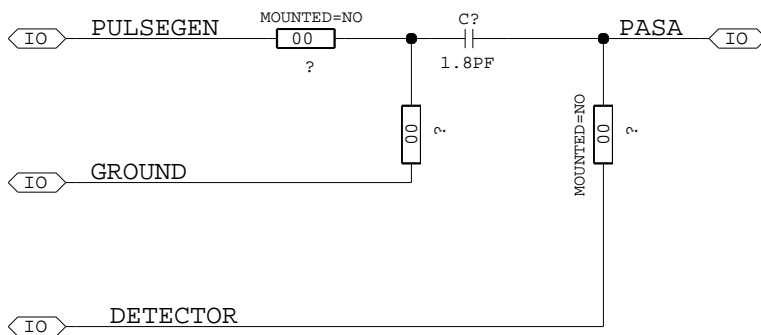
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Design by: DE GASPARI. M

PCB by: NL

DATE: 06/01/2011



Project file: SALTroTestBoard.cpm

SYSTEM: 16.3

EDA-02229-V1-0

PROJECT: SALTRO ASIC test board



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for Nuclear Research
1211 GENEVA 23
SWITZERLAND

MODULE: saltro_pasain

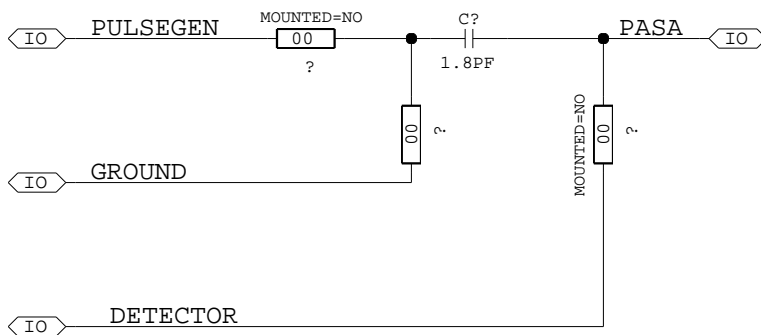
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Design by: DE GASPARI. M

PCB by: NL

DATE: 06/01/2011

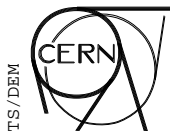


Project file: SALTroTestBoard.cpm

SYSTEM: 16.3

EDA-02229-V1-0

PROJECT: SALTRO ASIC test board



European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND

MODULE: saltro_pasain

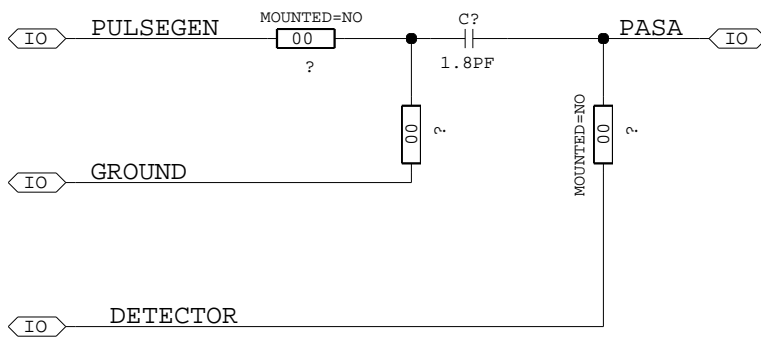
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LAST_MODIFIED=Mon Mar 28 17:35:29 2011

Design by: DE GASPARI. M

PCB by: NL

DATE: 06/01/2011



Project file: SALTroTestBoard.cpm

SYSTEM: 16.3

EDA-02229-V1-0

PROJECT: SALTRO ASIC test board



European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND

MODULE: saltro_pasain

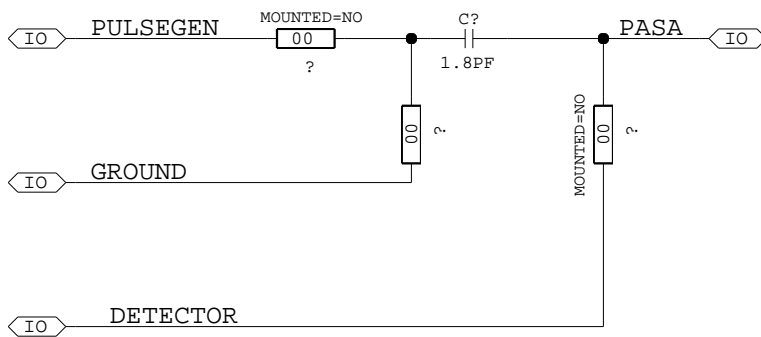
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LAST_MODIFIED=Mon Mar 28 17:35:29 2011

Design by: DE GASPARI. M

PCB by: NL

DATE: 06/01/2011



Project file: SAltroTestBoard.cpm

SYSTEM: 16.3

EDA-02229-V1-0

PROJECT: SALTRO ASIC test board



European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND

MODULE: saltro_pasain

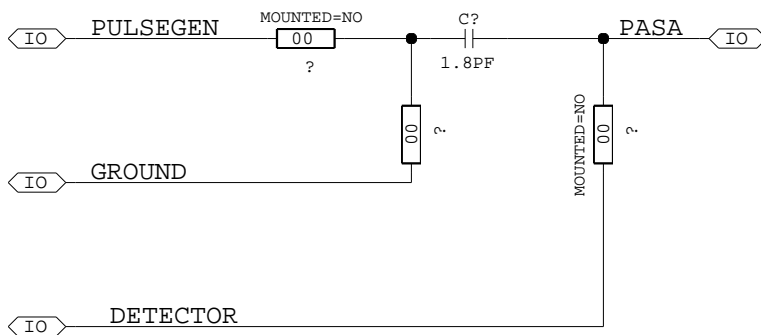
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LAST_MODIFIED=Mon Mar 28 17:35:29 2011

Design by: DE GASPARI. M

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DATE: 06/01/2011



Project file: SAltroTestBoard.cpm

SYSTEM: 16.3

EDA-02229-V1-0

PROJECT: SALTRO ASIC test board



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1211 GENEVA 23
SWITZERLAND

MODULE: saltro_pasain

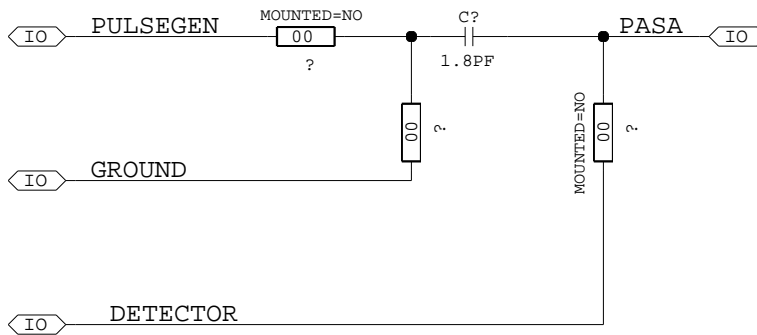
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Design by: DE GASPARI. M

PCB by: NL

DATE: 06/01/2011



Project file: SALTroTestBoard.cpm

SYSTEM: 16.3

EDA-02229-V1-0

PROJECT: SALTRO ASIC test board



European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND

MODULE: saltro_pasain

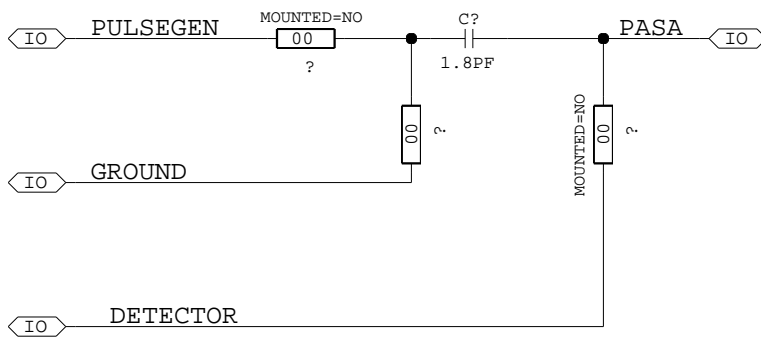
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Design by: DE GASPARI. M

PCB by: NL

DATE: 06/01/2011



Project file: SAltroTestBoard.cpm

SYSTEM: 16.3

EDA-02229-V1-0

PROJECT: SALTRO ASIC test board



European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND

MODULE: saltro_pasain

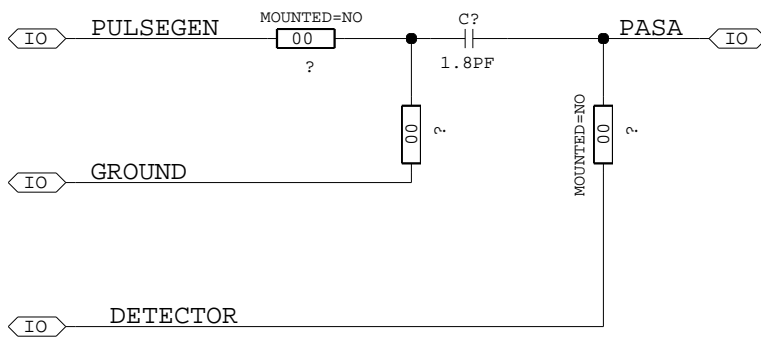
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Design by: DE GASPARI. M

PCB by: NL

DATE: 06/01/2011



Project file: SAltroTestBoard.cpm

SYSTEM: 16.3

EDA-02229-V1-0

PROJECT: SALTRO ASIC test board



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for Nuclear Research
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MODULE: saltro_pasain

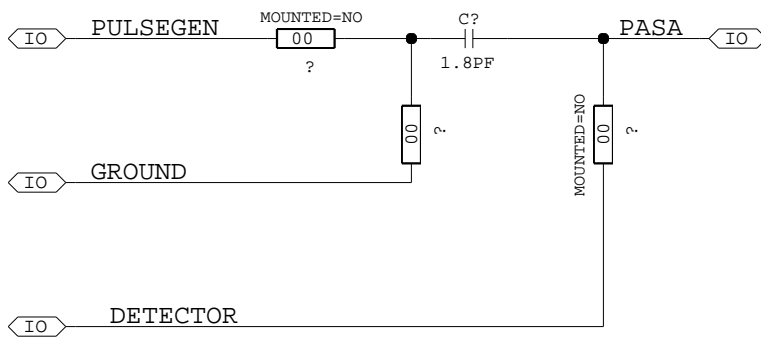
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Design by: DE GASPARI. M

PCB by: NL

DATE: 06/01/2011



Project file: SAltroTestBoard.cpm

SYSTEM: 16.3

EDA-02229-V1-0

PROJECT: SALTRO ASIC test board



European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND

MODULE: saltro_pasain

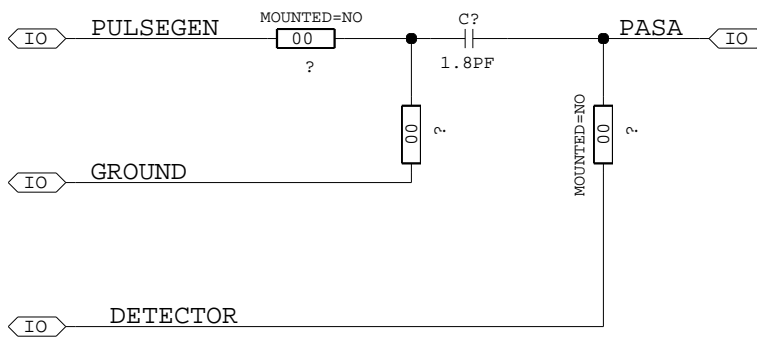
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Design by: DE GASPARI. M

PCB by: NL

DATE: 06/01/2011



Project file: SAltroTestBoard.cpm

SYSTEM: 16.3

EDA-02229-V1-0

PROJECT: SALTRO ASIC test board



European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND

MODULE: saltro_pasain

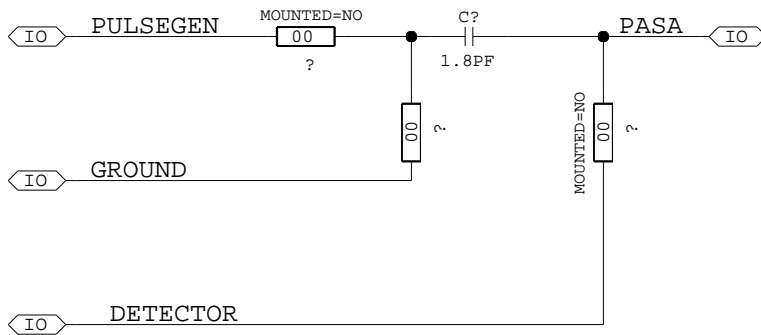
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Design by: DE GASPARI. M

PCB by: NL

DATE: 06/01/2011



Project file: SAltroTestBoard.cpm

SYSTEM: 16.3

EDA-02229-V1-0

PROJECT: SALTRO ASIC test board



European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND

MODULE: saltro_pasain

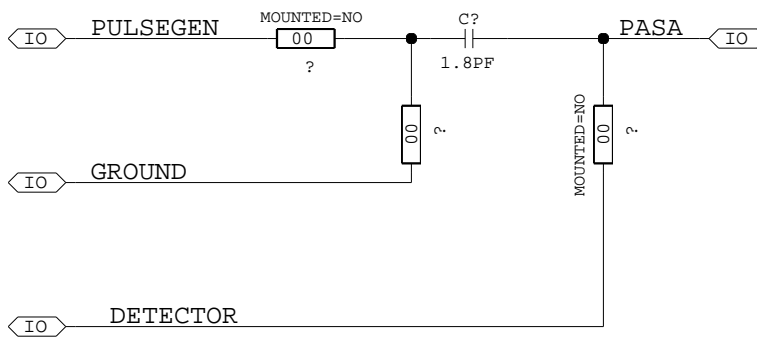
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Design by: DE GASPARI. M

PCB by: NL

DATE: 06/01/2011



Project file: SAltroTestBoard.cpm

SYSTEM: 16.3

EDA-02229-V1-0

PROJECT: SALTRO ASIC test board



European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND

MODULE: saltro_pasain

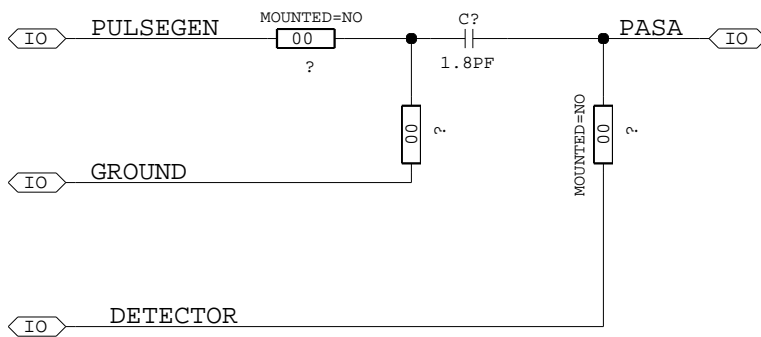
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LAST_MODIFIED=Mon Mar 28 17:35:29 2011

Design by: DE GASPARI. M

PCB by: NL

DATE: 06/01/2011



Project file: SAltroTestBoard.cpm

SYSTEM: 16.3

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PROJECT: SALTRO ASIC test board



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MODULE: saltro_pasain

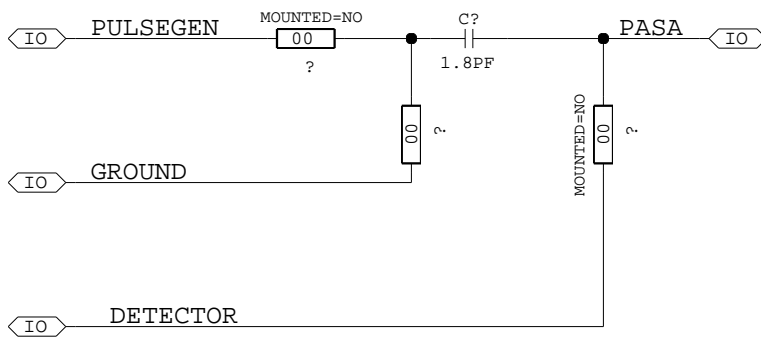
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LAST_MODIFIED=Mon Mar 28 17:35:29 2011

Design by: DE GASPARI. M

PCB by: NL

DATE: 06/01/2011



Project file: SALTroTestBoard.cpm

SYSTEM: 16.3

EDA-02229-V1-0

PROJECT: SALTRO ASIC test board



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MODULE: saltro_pasain

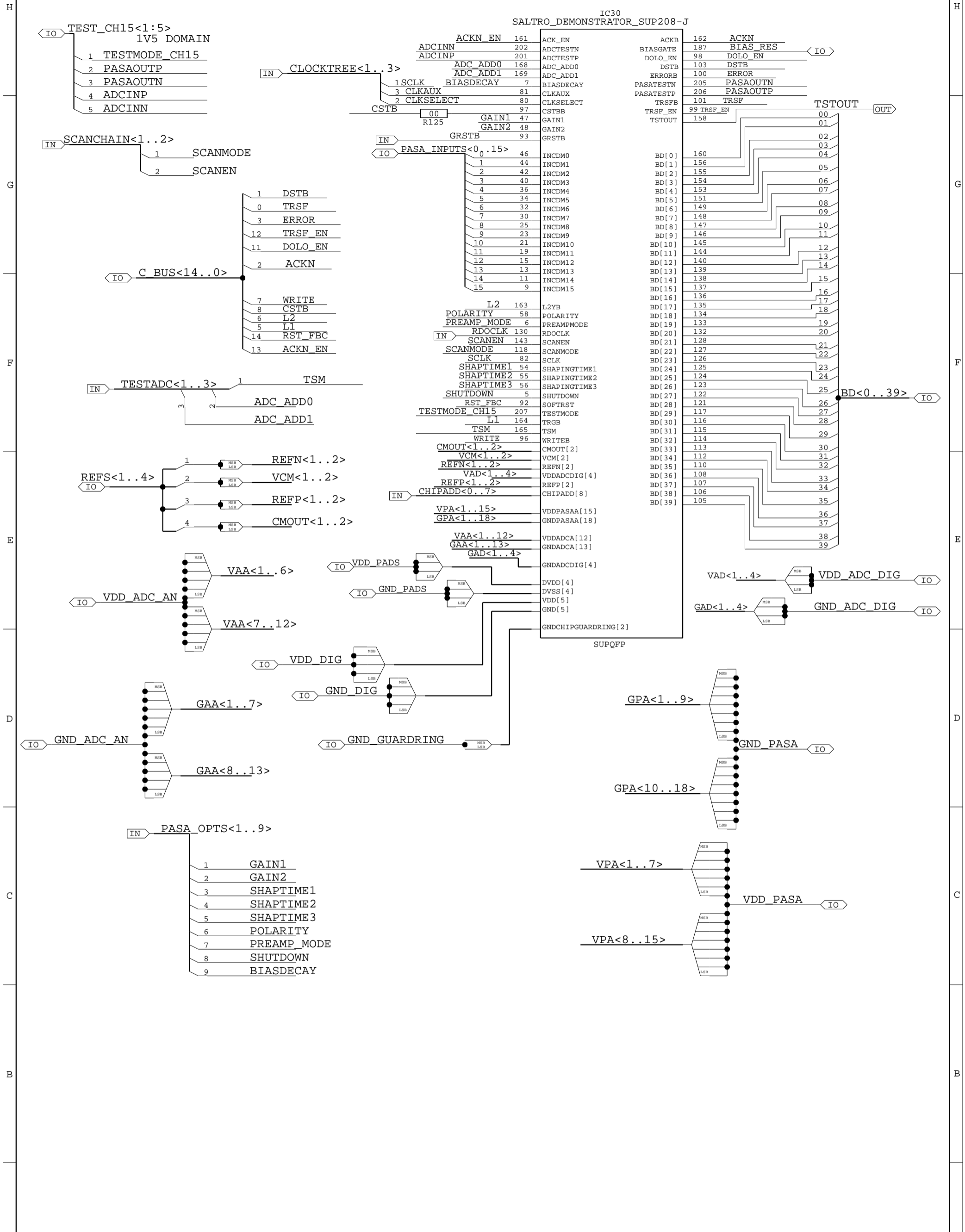
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LAST_MODIFIED=Mon Mar 28 17:35:29 2011

Design by: DE GASPARI. M


PCB by: NL

DATE: 06/01/2011



Project file: SALTROTestBoard.cpm SYSTEM: 16.3

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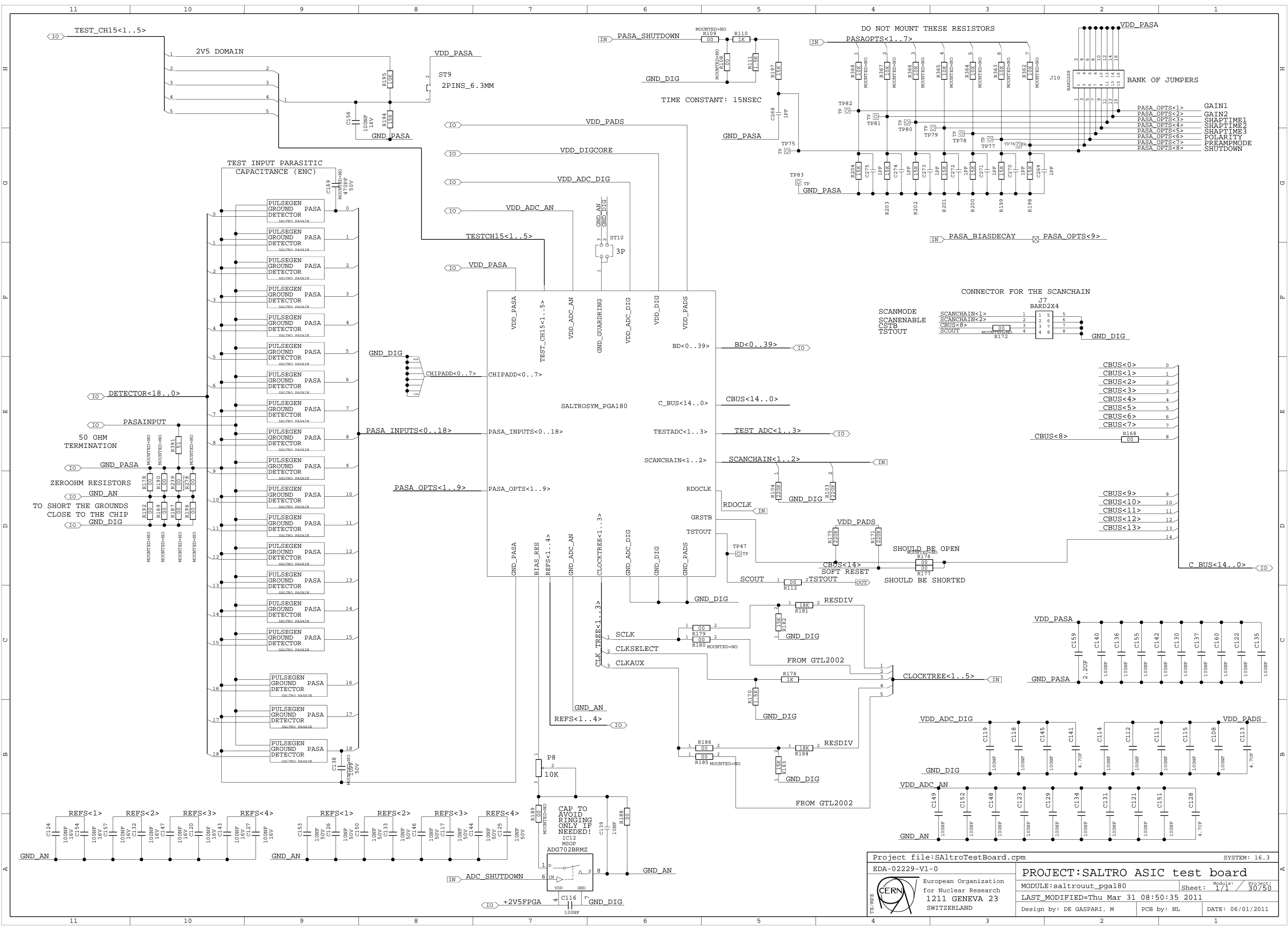
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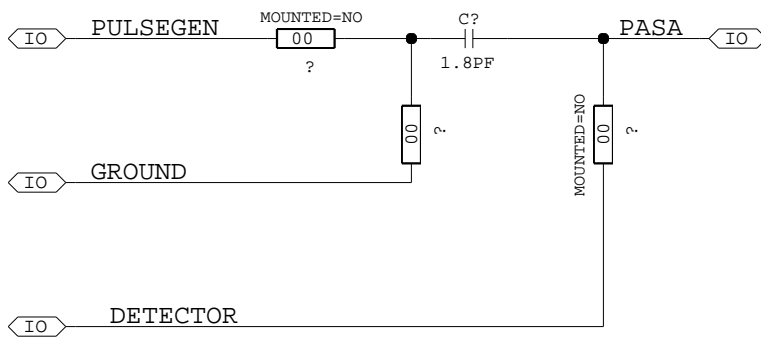
PROJECT: SALTRO ASIC test board

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Design by: DE GASPARI. M PCB by: NL DATE: 06/01/2011





Project file: SAltroTestBoard.cpm

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PROJECT: SALTRO ASIC test board



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MODULE: saltro_pasain

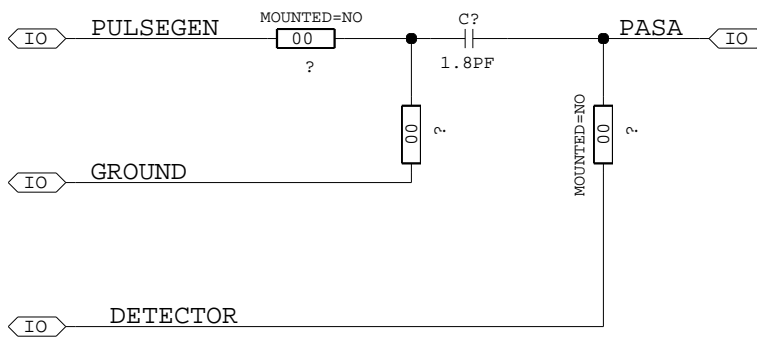
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Design by: DE GASPARI. M

PCB by: NL

DATE: 06/01/2011



Project file: SAltroTestBoard.cpm

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PROJECT: SALTRO ASIC test board



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MODULE: saltro_pasain

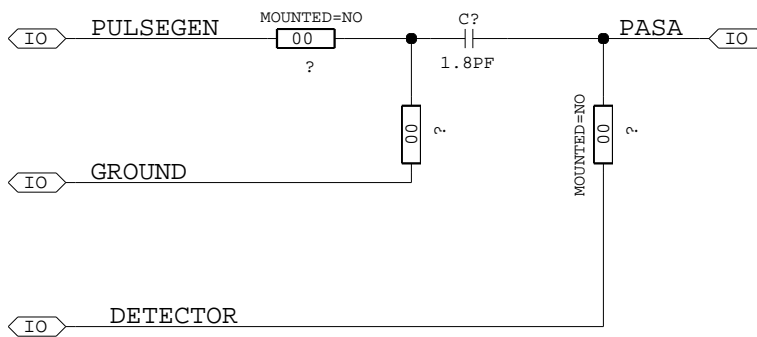
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Design by: DE GASPARI. M

PCB by: NL

DATE: 06/01/2011



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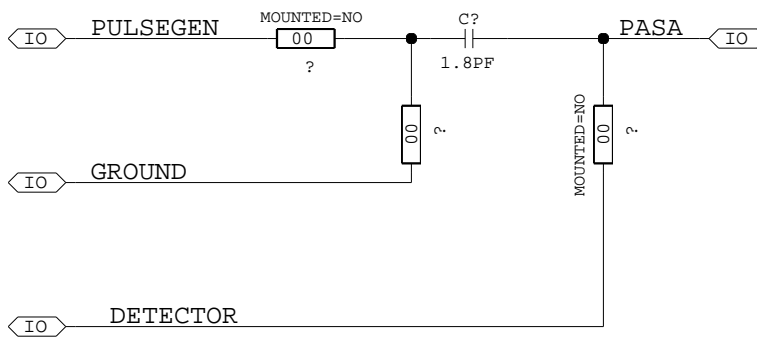
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PCB by: NL

DATE: 06/01/2011



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MODULE: saltro_pasain

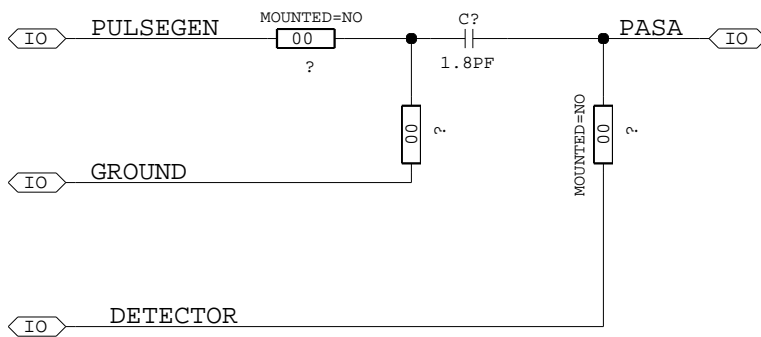
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DATE: 06/01/2011



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MODULE: saltro_pasain

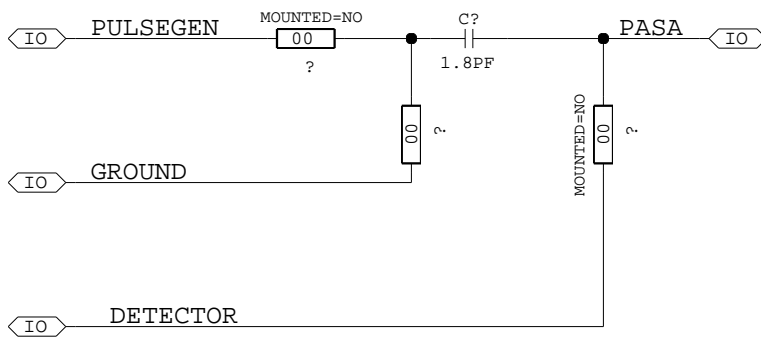
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LAST_MODIFIED=Mon Mar 28 17:35:29 2011

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MODULE: saltro_pasain

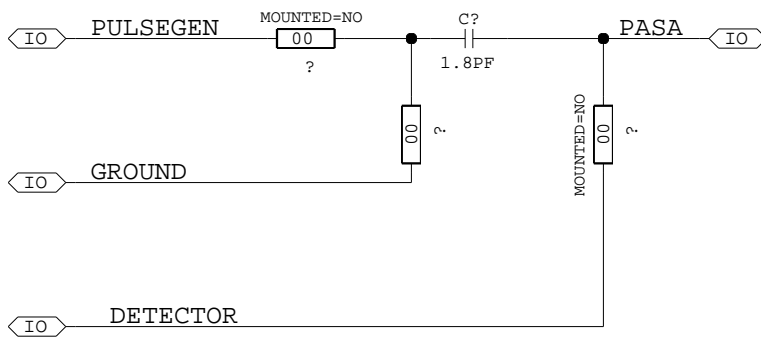
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MODULE: saltro_pasain

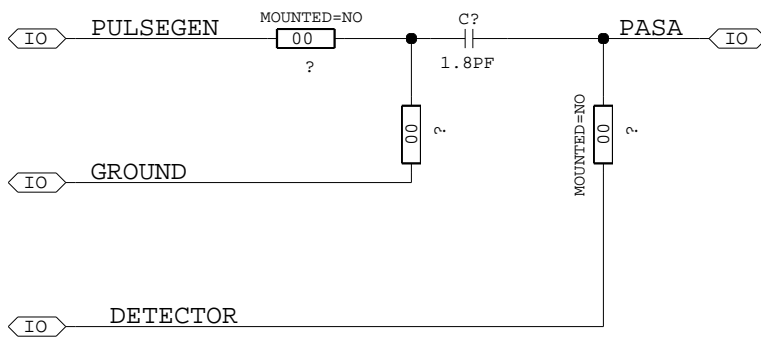
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MODULE: saltro_pasain

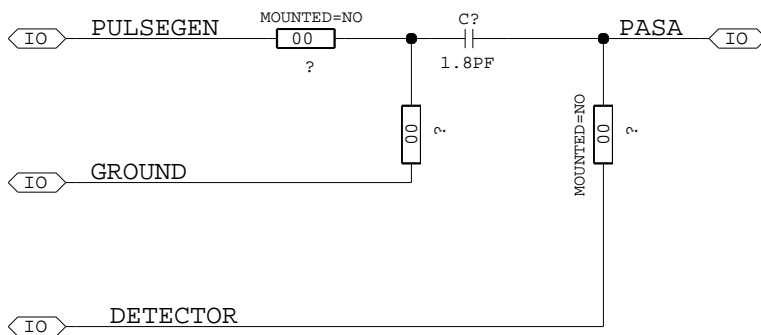
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MODULE: saltro_pasain

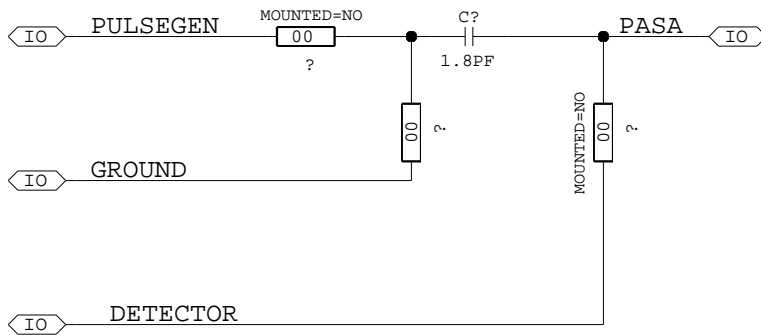
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MODULE: saltro_pasain

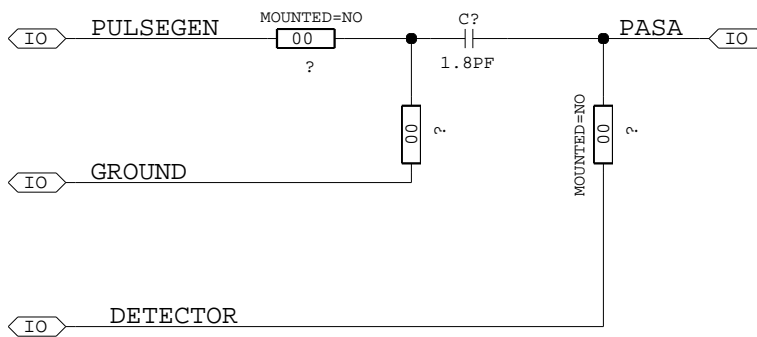
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MODULE: saltro_pasain

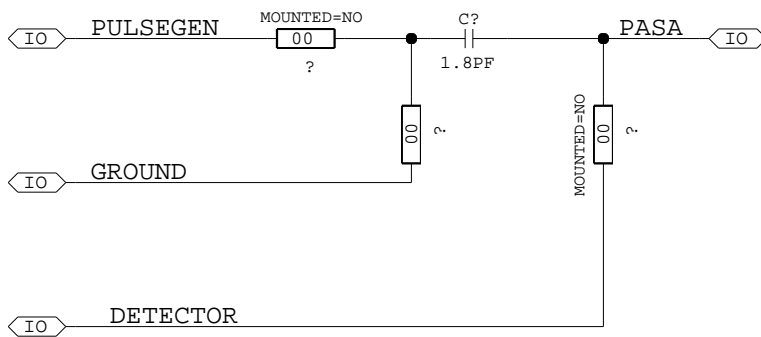
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MODULE: saltro_pasain

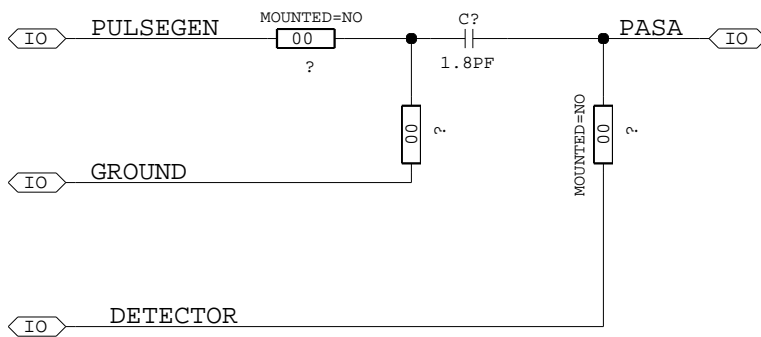
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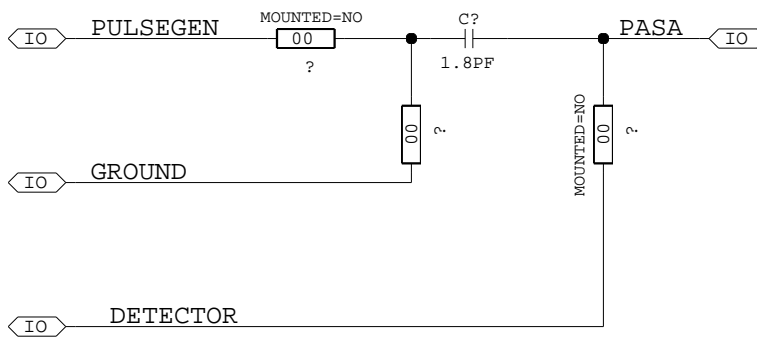
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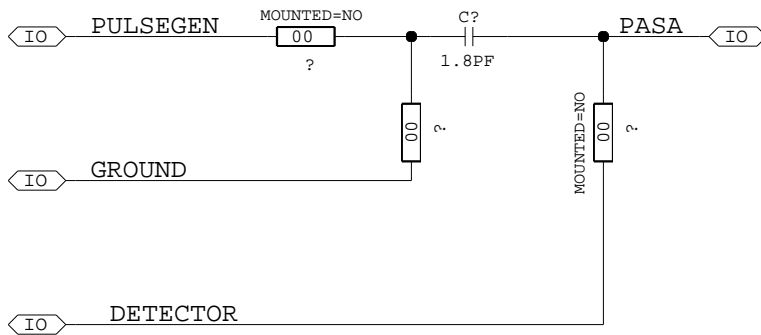
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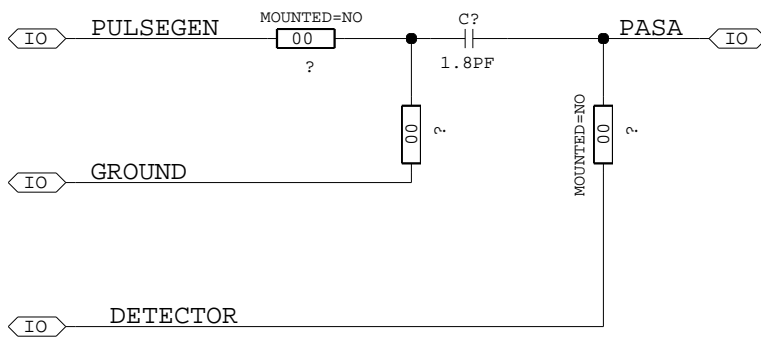
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MODULE: saltro_pasain

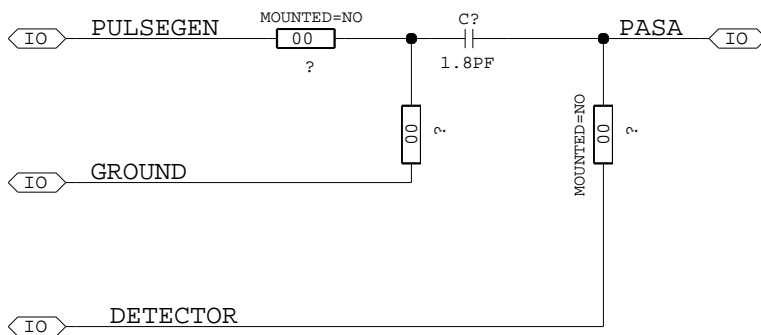
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Design by: DE GASPARI. M

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MODULE: saltro_pasain

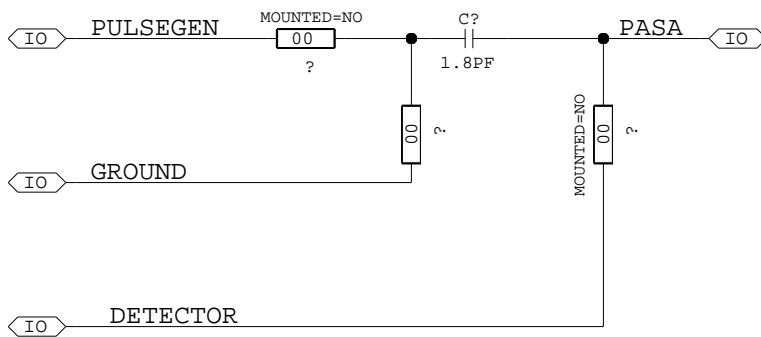
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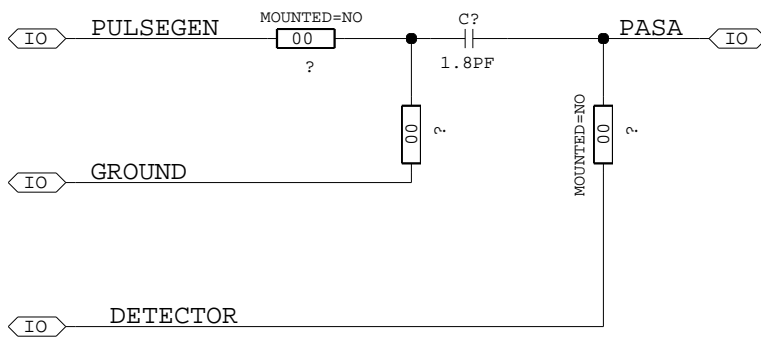
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MODULE: saltro_pasain

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