Mass test and calibration of SAMPAs

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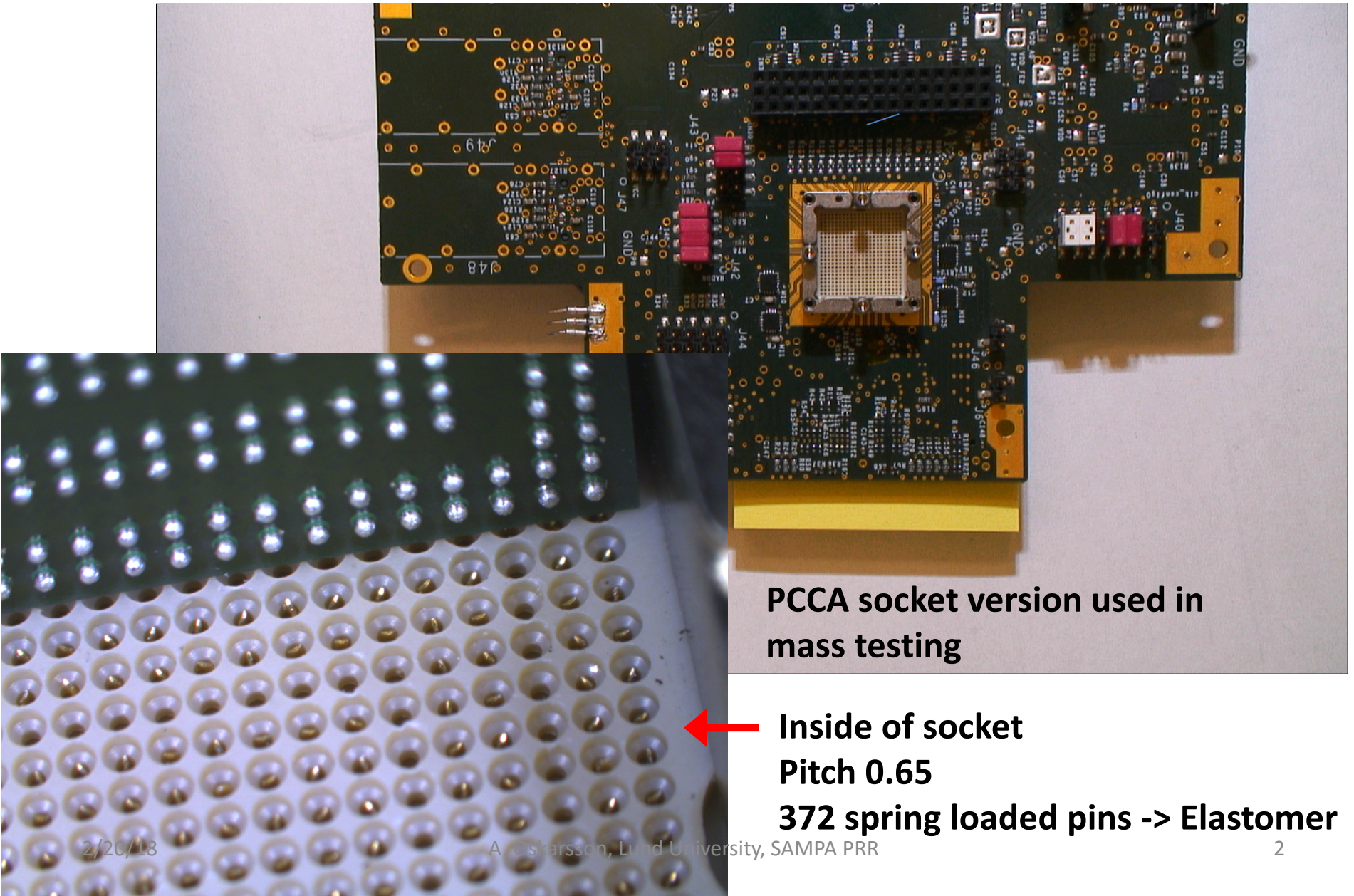
+ GBT/TRORC experts (Torsten Alt et al.) and
Experts involved in SAMPA-FEC and MuCh
Quite integrated with SAMPA characterization and TPC FEC development

These are some of the slides shown at SAMPA PPR in Feb 2018; familiar to Ken & Chuck, and also shown and discussed with sPHENIX team in Jan 2020

SAMPA test board with socket



PCCA socket version used in mass testing

Inside of socket
Pitch 0.65
372 spring loaded pins -> Elastomer

Test procedures in mass testing

Fab Tests DC

measure - DC internal reference voltages
currents to 5 power domains

Tests built into SAMPA

JTAG test – checks most digital IO
Memory test checks all memory cells
DFT test checks ~25000 flip flops

Data integrity

same checks as in final data taking (Sync)

External testpulses - remote control function generator (Tektronix AFG3000)
pulse every second channel. Bondwire and BGA substrate input.
crosstalk (shorts between channels)

Calibration

Taking calibration data for each channel
ADC – baseline/pedestal
Noise
Gain calibration
risetime-falltime

Robotic testing

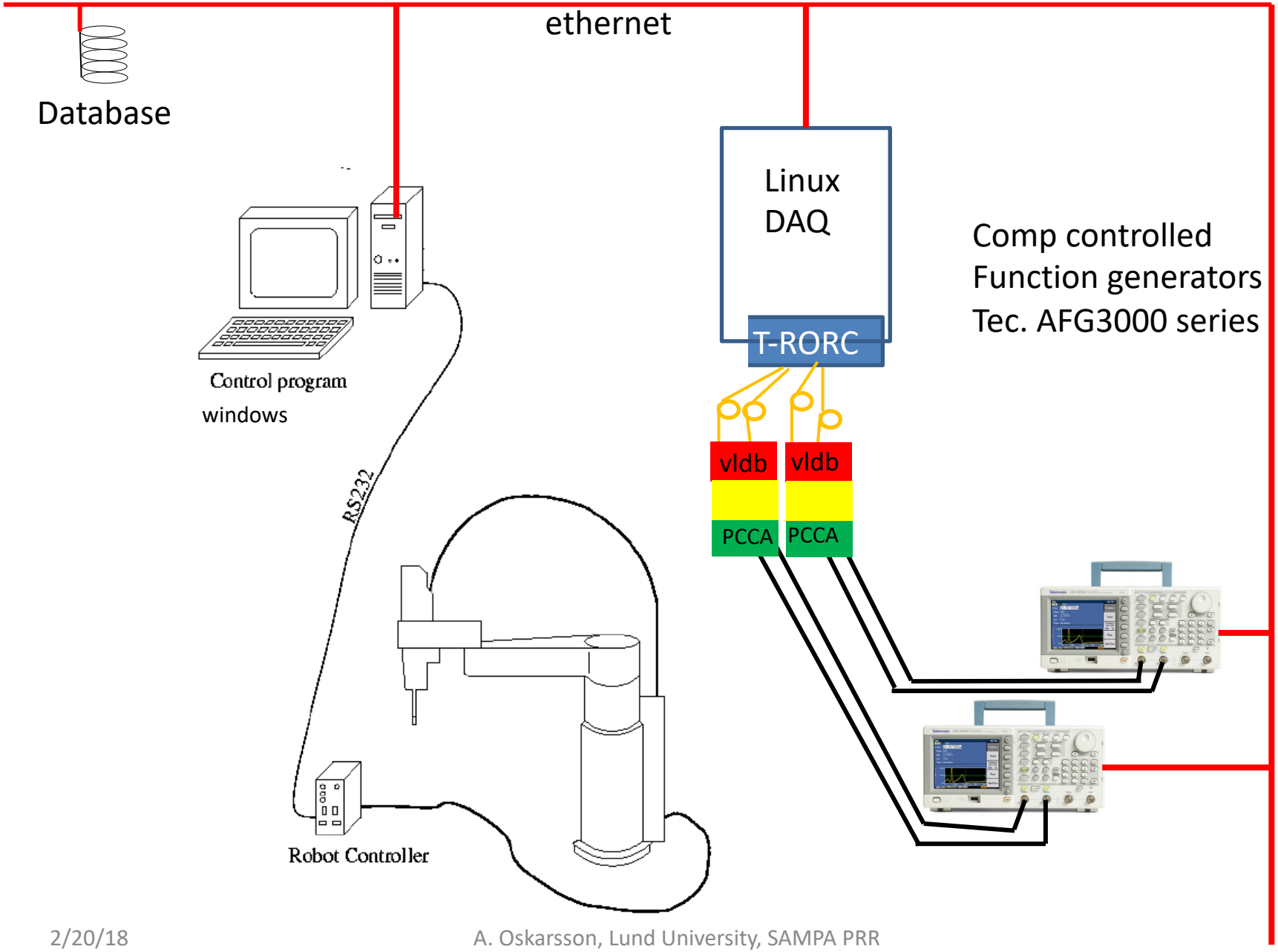
Robotic production testing in clean room (ISO7)

- automatic mass-testing 90k SAMPA V4 chips
- CHIP handling – chip sorting re-used
- New test card and readout

IMPORTANT. No manual handling of individual chips
Manual tray handling.

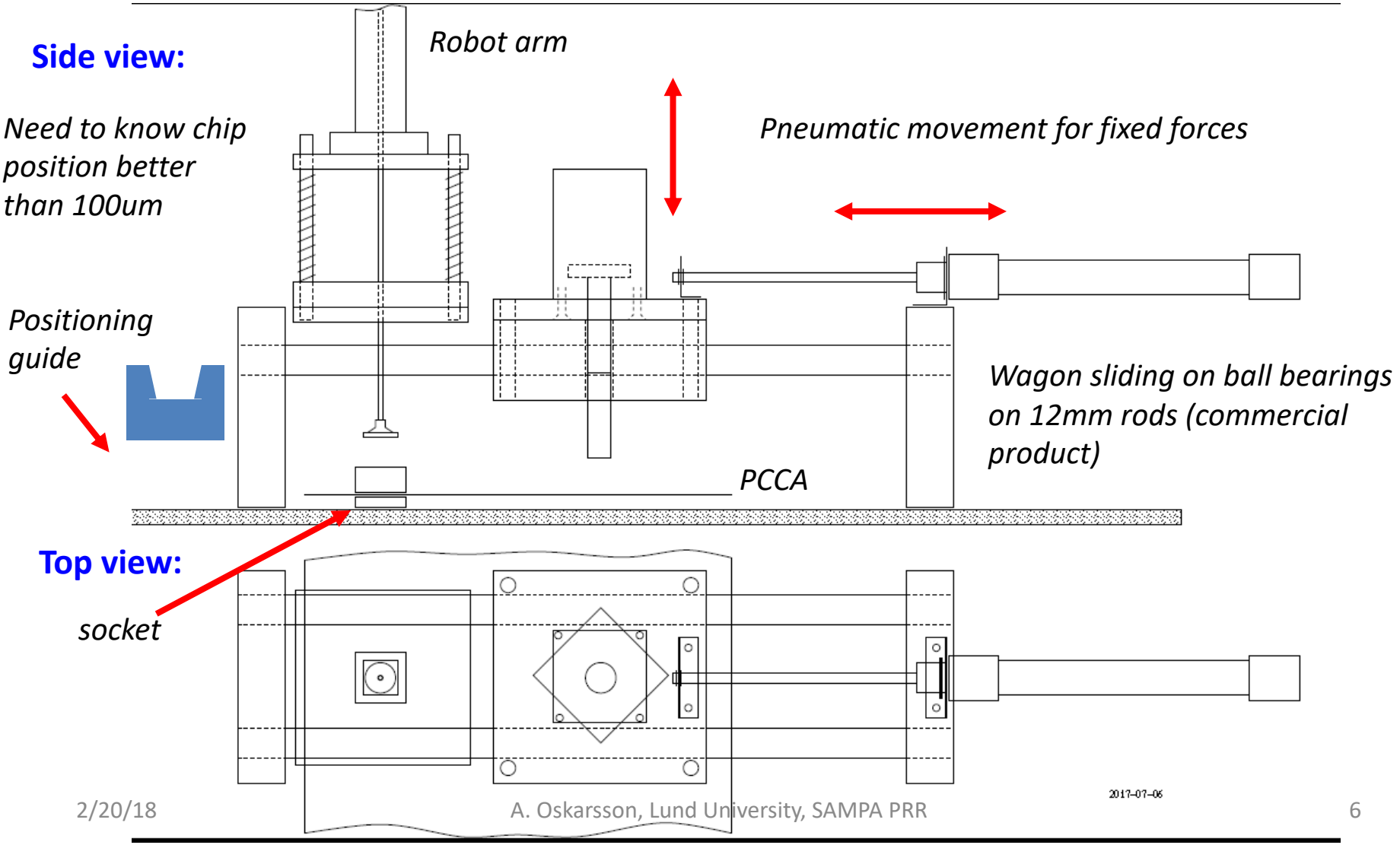
Video of robot in motion:
https://youtu.be/3tnqPbMWzqQ

Setup

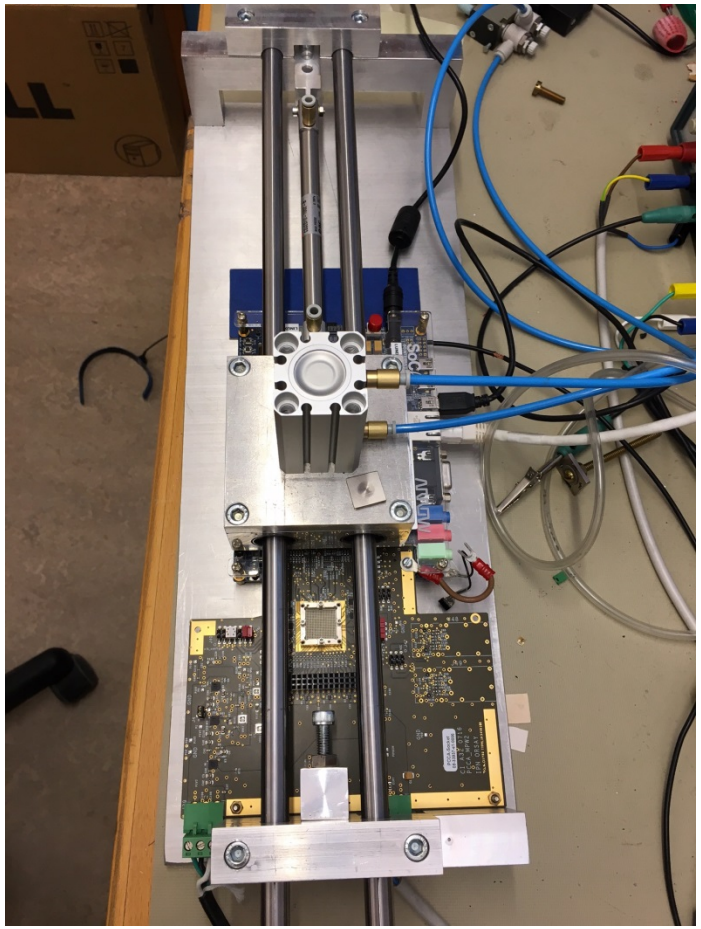

ethernet
Database
Linux
DAQ
T-RORC
vldb
vldb
PCCA
PCCA
Comp controlled
Function generators
Tec. AFG3000 series
Control program
windows
RS232
Robot Controller

Mechanics

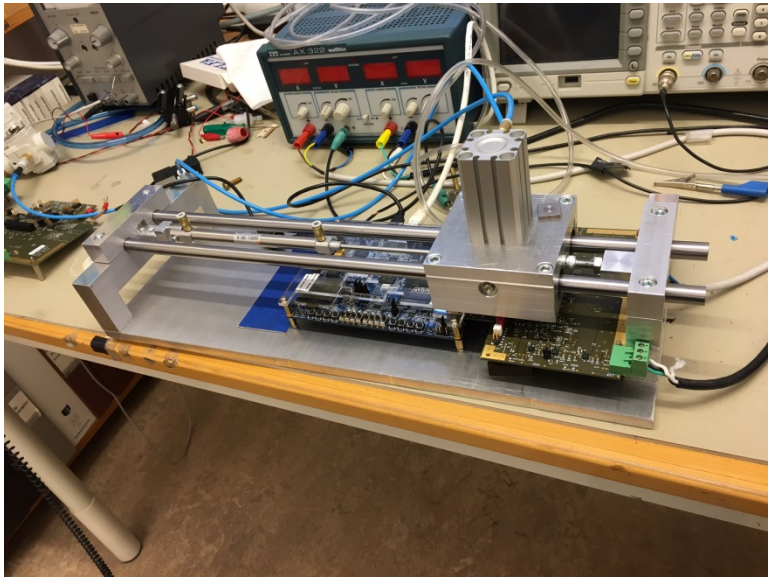
Tested the chip contacting in automatic handling. Works at 80N force (8 Kg weight)

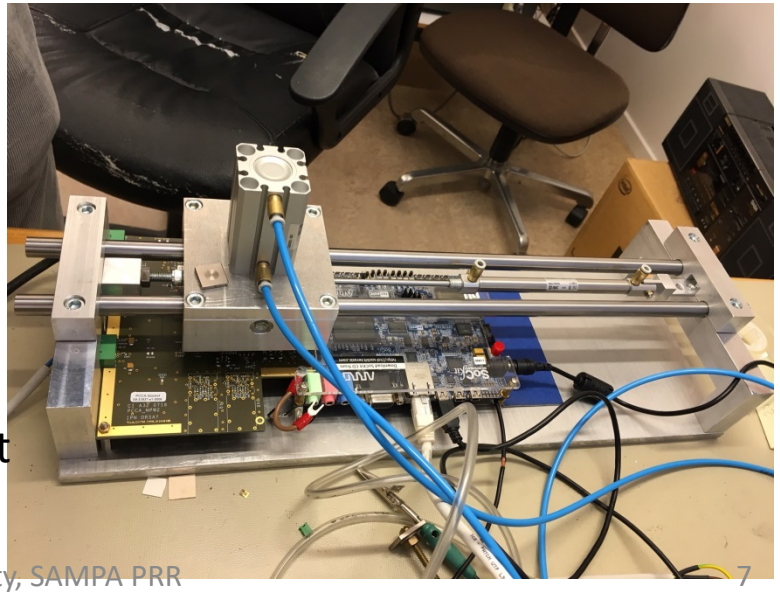


Open



Closed

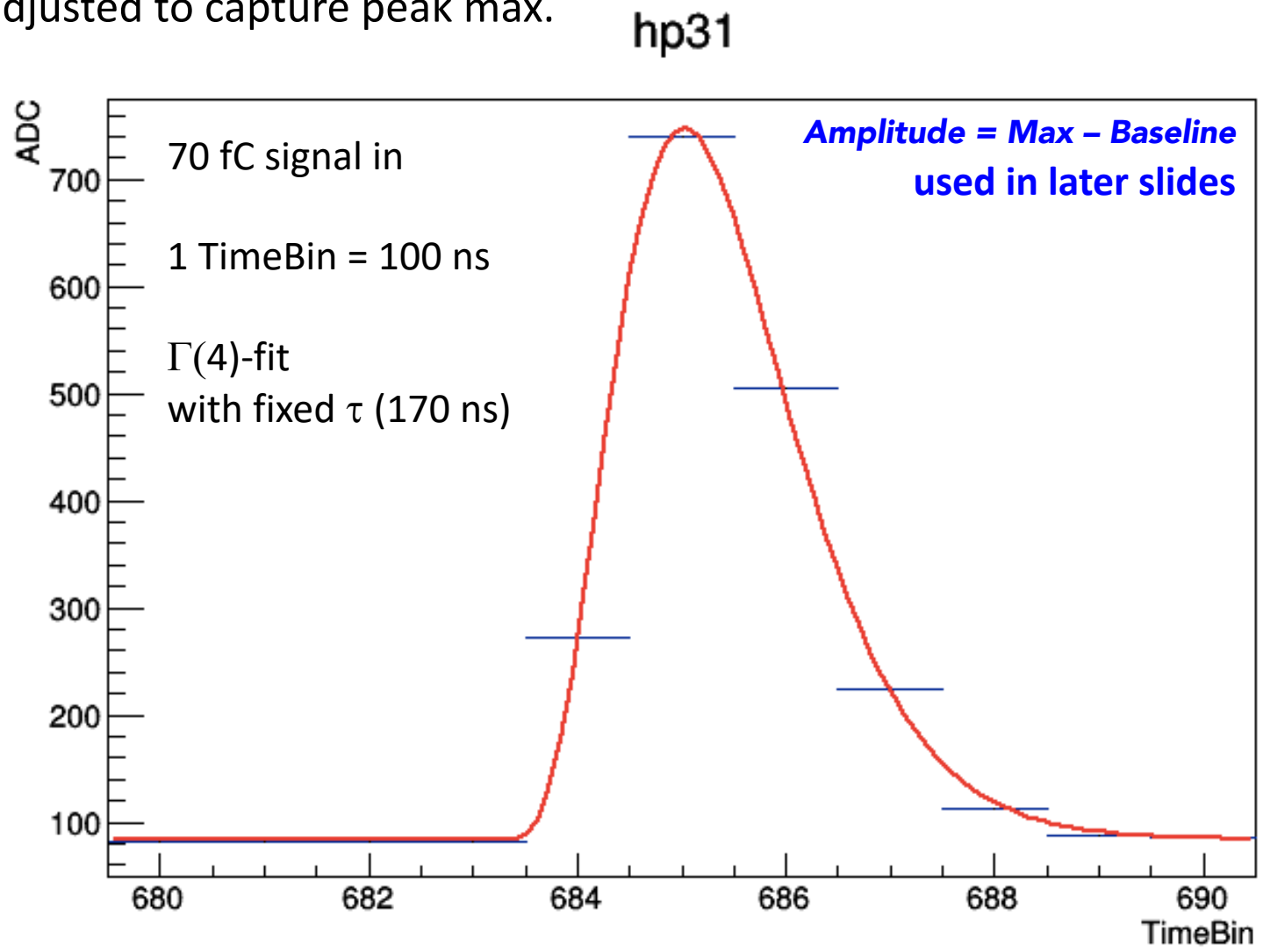




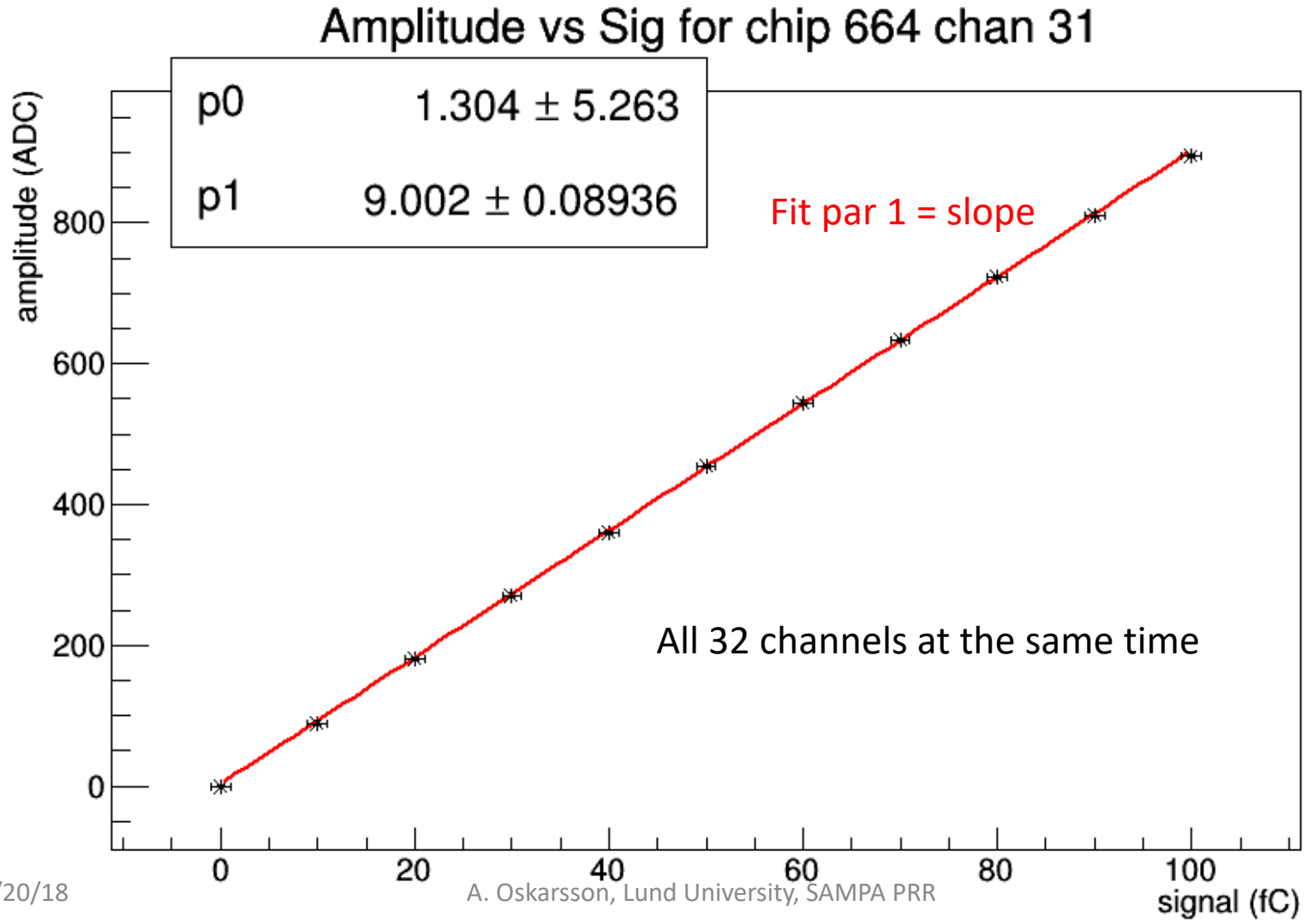
Comment AO:Will work on motion picture with robot next week

Gain calibration example (one channel)

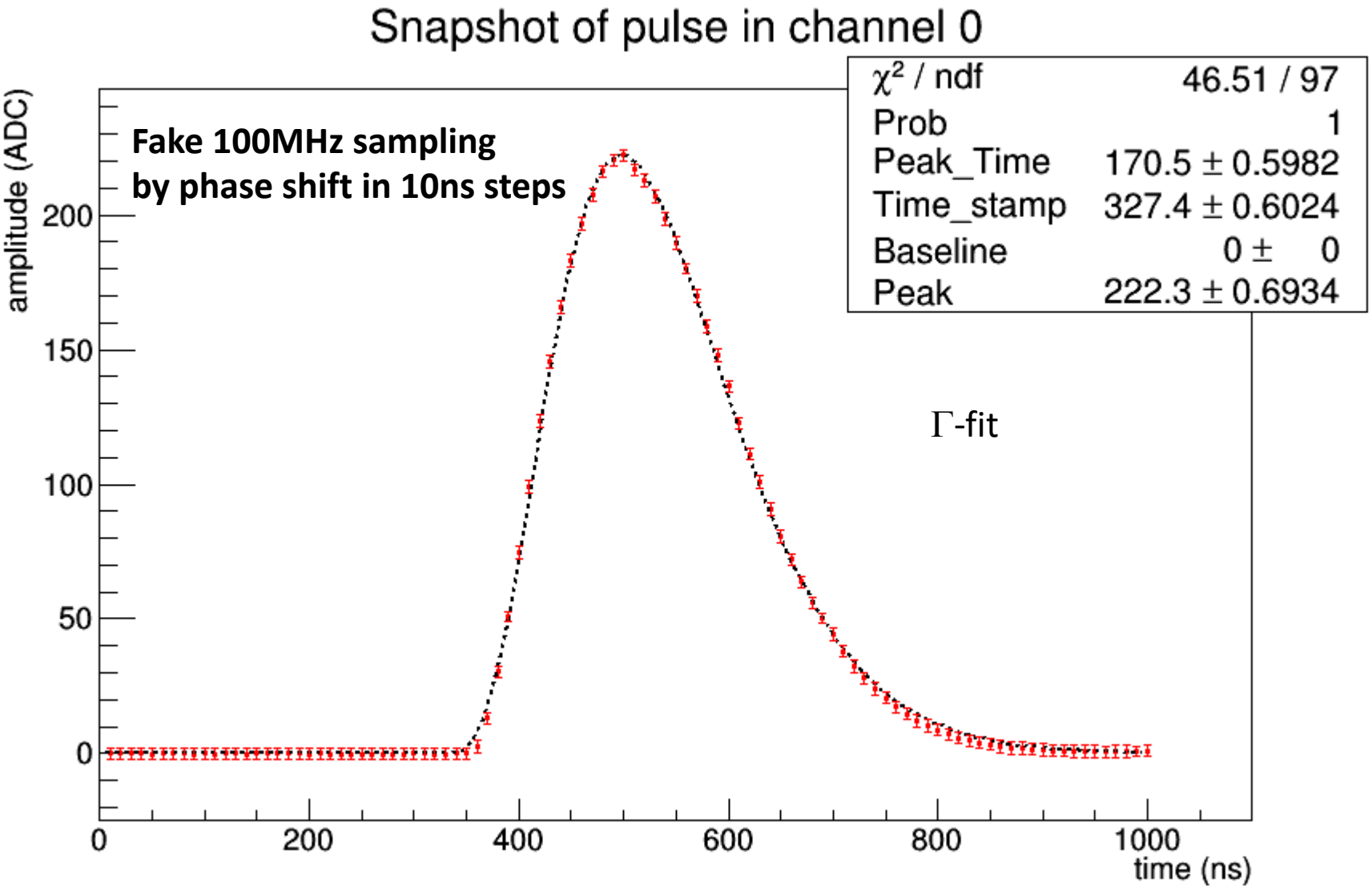
Testpulser synchronized with sampling clock.
Delay adjusted to capture peak max.



Calibration results for each chip and for individual channels



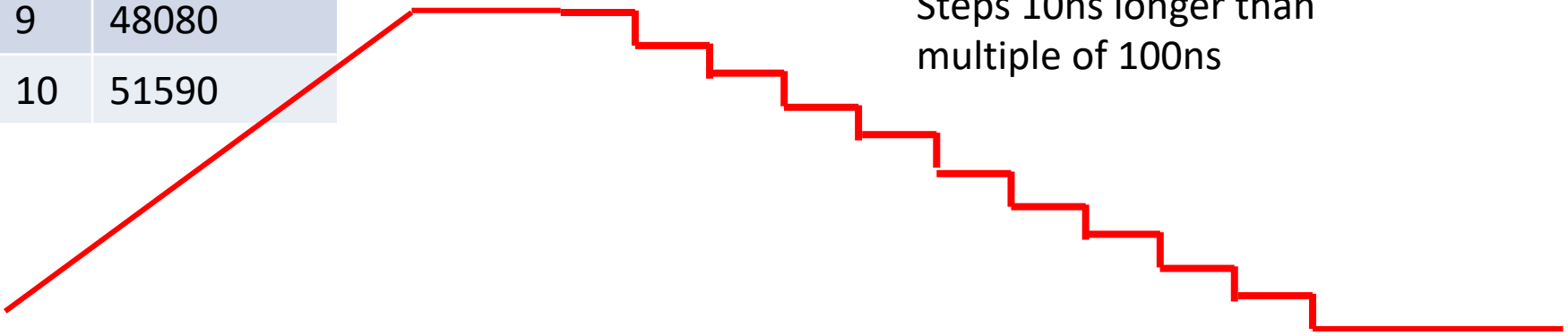
High resolution pulse sampling



Risetime, Falltime

pulse	Delay in ns
1	20000
2	23510
3	27020
4	30530
5	34040
6	37550
7	41060
8	44570
9	48080
10	51590

1 event is a pulse train of 10 pulses of same amplitude
Triggered by synchronized trigger pulse. 1000 events gives 1000 pulses on each 10ns sample



Steps 10ns longer than multiple of 100ns

Time sweep of pulse train

10MHz sampling, 100 microsecs full sweep

Induce opposite charge