27 May 2020 : Update Lund SAMPA V5 initial mass testing

Topics covered today:

- List of Checks
- V4 Production Statistics
- First V5 Testing Pass for 160 ns and 80 ns
- Plots/distributions for 160 ns and 80 ns
- Outlook

List of Checks 2

Checks and cuts for the bulk chip testing come in 2 main groups:

- Chip-level: most of these are straight-forward: – Sync, Memory, i2c, Jtag, DFT all simply have to work. Limits for reference voltages and currents are set to avoid shorts etc.
- Channel-level (analog info): here we have checks on Pedestal (Baseline), Gain, Rms (Noise), RiseTime and Xtalk. We are not so sensitive to Xtalk in our setup, and Noise is largely from the robot motor, rather than intrinsic chip noise.

I am not re-describing here how all the checks were done, but refer the sPHENIX folks to the discussions we had in early January - see also the Intro_SAMPA_PPR_Feb2018.pdf file in the same web-directory as this file.
The checks we do are basically identical to the procedure we followed for the SAMPA V4 ALICE TPC testing (same settings, calibrated injection board), except that in addition to the testing with 160 ns risetime, we also test with 80 ns risetime. (new configuration for sPHENIX with SAMPA V5).
We did also scan the Trigger Pulse delay values (end of April), and GBTx data alignment (on May 5). After the testing rounds described below, we shipped 3 trays of OK chips (378 chips) to BNL on May 13.

V4 Production Statistics

Summary from the testing the 90k+ chips for ALICE TPC + MCH tested in Lund from summer 2018 to summer 2019: Multiple errors can occur for the same chip

Station	**1**	**2**
nTests	43902	46981
nPass	35050 (79.84 %)	37283 (79.36 %)
nFail	8852 (20.16 %)	9698 (20.64 %)
Fail category		
Chip-level		
ACurr	1757 (4.00 %)	2033 (4.33 %)
Sync	529 (1.20 %)	644 (1.37 %)
RingOsc	426 (0.97 %)	564 (1.20 %)
i2c	341 (0.78 %)	492 (1.05 %)
Jtag	530 (1.21 %)	816 (1.74 %)
Mem	2622 (5.97 %)	3085 (6.57 %)
DFT	2423 (5.52 %)	2806 (5.97 %)
Channel-level		
PedAna	3936 (8.97 %)	4307 (9.17 %)
RmsAna	3966 (9.03 %)	4361 (9.28 %)
Gain	4799 (10.93 %)	5628 (11.98 %)
RiseTime	4413 (10.05 %)	4196 (8.93 %)
Xtalk	261 (0.59 %)	208 (0.44 %)
BitCheck	4237 (9.65 %)	3933 (8.37 %)

First V5 Testing Statistics, 160 ns

Summary from a round over the 980 chips tested with 160 ns configuration:
Multiple errors can occur for the same chip

Station	**1**
nTests	980
nPass	589 (60.10 %)
nFail	391 (39.90 %)
Fail category	
Chip-level	
ACurr	77 (7.86 %)
Sync	11 (1.12 %)
RingOsc	7 (0.71 %)
i2c	5 (0.51 %)
Jtag	8 (0.82 %)
Mem	67 (6.84 %)
DFT	48 (4.90 %)
Channel-level	
PedAna	209 (21.33 %)
RmsAna	292 (29.80 %)
Gain	214 (21.84 %)
RiseTime	235 (23.98 %)
Xtalk	24 (2.45 %)
BitCheck	210 (21.43 %)

Summary from a round over the 589(+2 retest OK) = 591 chips that tested OK with 160 ns configuration, in a follow-up pass at 80 ns: (we wanted to send Takao *et al.* chips somewhat urgently that tested OK for both 160 ns and 80 ns)

Station	**1**
nTests	591
nPass	475 (80.37 %)
nFail	116 (19.63 %)
Fail category	
Chip-level	
ACurr	5 (0.85 %)
Sync	0 (0.00 %)
RingOsc	2 (0.34 %)
i2c	0 (0.00 %)
Jtag	0 (0.00 %)
Mem	1 (0.17 %)
DFT	0 (0.00 %)
Channel-level	
PedAna	2 (0.34 %)
RmsAna	29 (4.91 %)
Gain	107 (18.10 %)
RiseTime	101 (17.09 %)
Xtalk	52 (8.80 %)
BitCheck	98 (16.58 %)

First V5 Testing Statistics Executive Summary 6

Before we look at the plots/distributions, let me give some comments on the testing statistics, and what we need to improve on.

- Main (digital, chip-level) errors all better or comparable to V4.
- Need to improve channel-level analog analysis: Ped, Rms(Noise), Gain, RiseTime, Xtalk, BitCheck. Large noise from robot motor appears to be a bigger issue at 80 ns than 160 ns, as could be expected.
- Need to adjust the current (ACurr) cut limits. The current values for V5 and V4 appear to not be exactly the same.
- We think that we should be able to get to a similar acceptable yield for V5 as for V4, after improvements, cut adjustments and possible repasses over chips with failed tests. Repasses were also done for the V4 chips. Our assumption is that if a test is OK, the chip is OK. (A failed test could be due to either the chip being bad, or the test setup/connection or analysis could be faulty)

Example Pedestal (Baseline), RMS (Noise) Analysis Plot 7

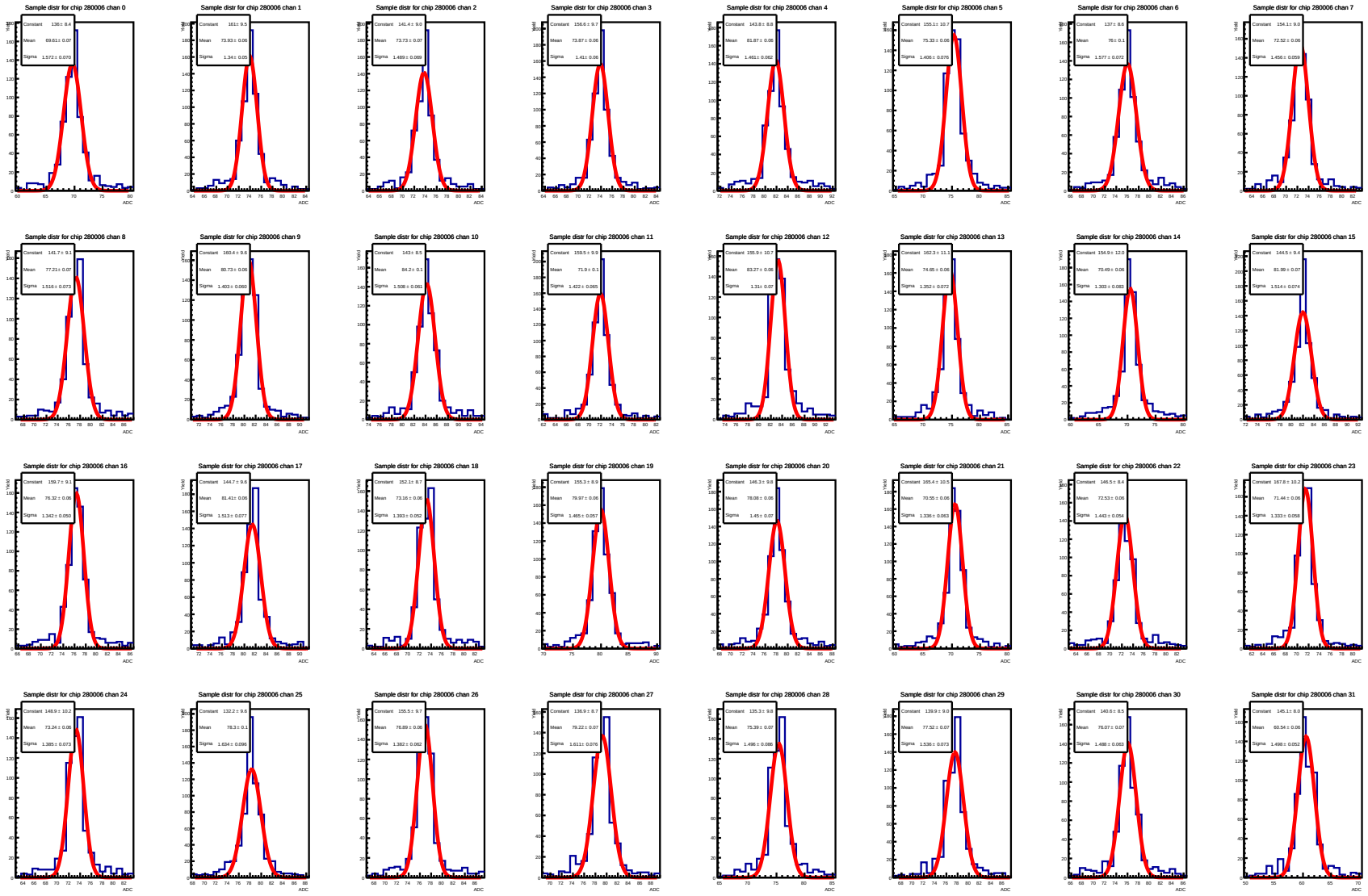


Figure 1: ADC distributions - Baseline Mean and RMS fits for one chip, at 80 ns.

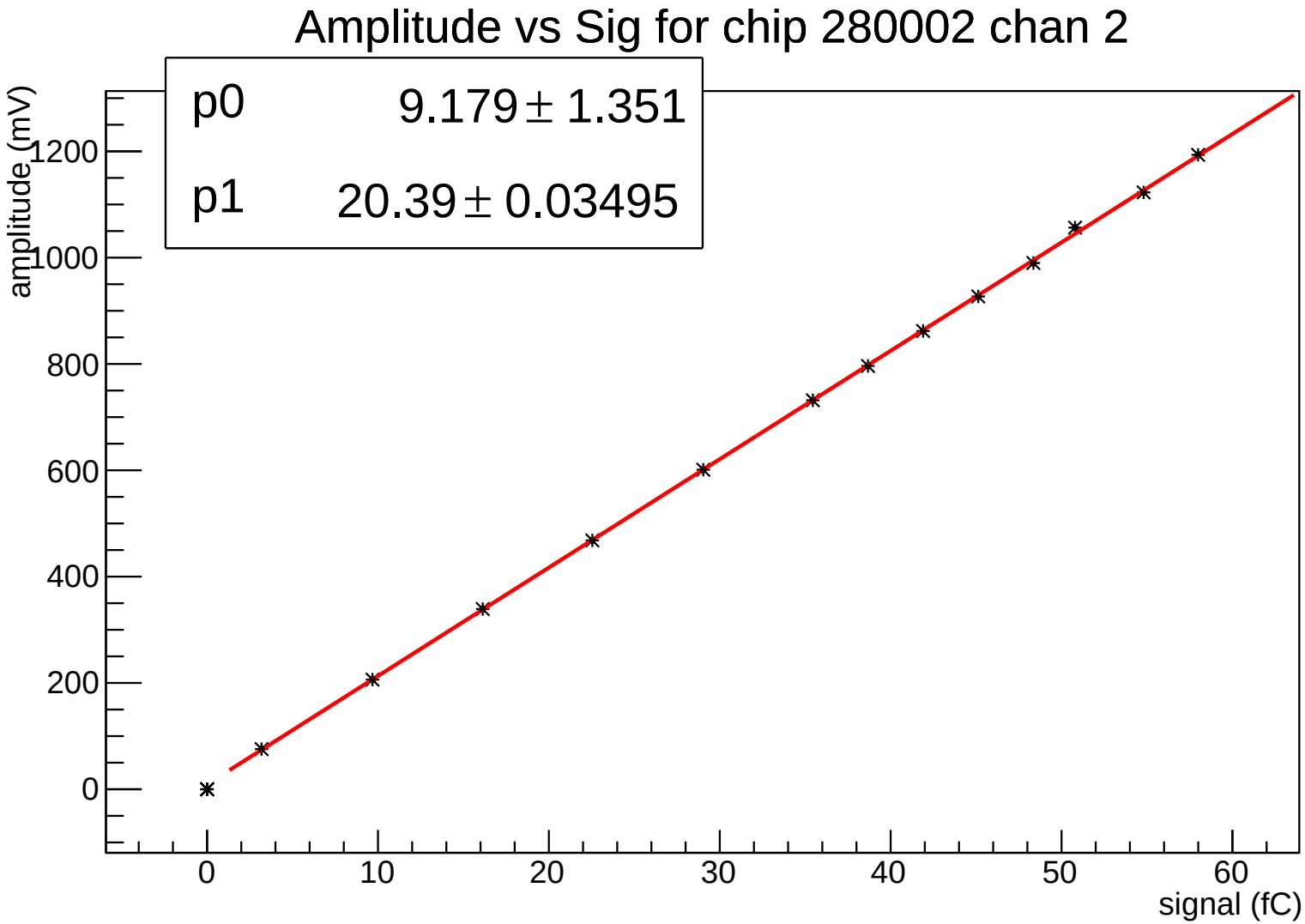


Figure 2: Example Gain Fit for one channel, at 160 ns.

Example RiseTime Analysis Plots

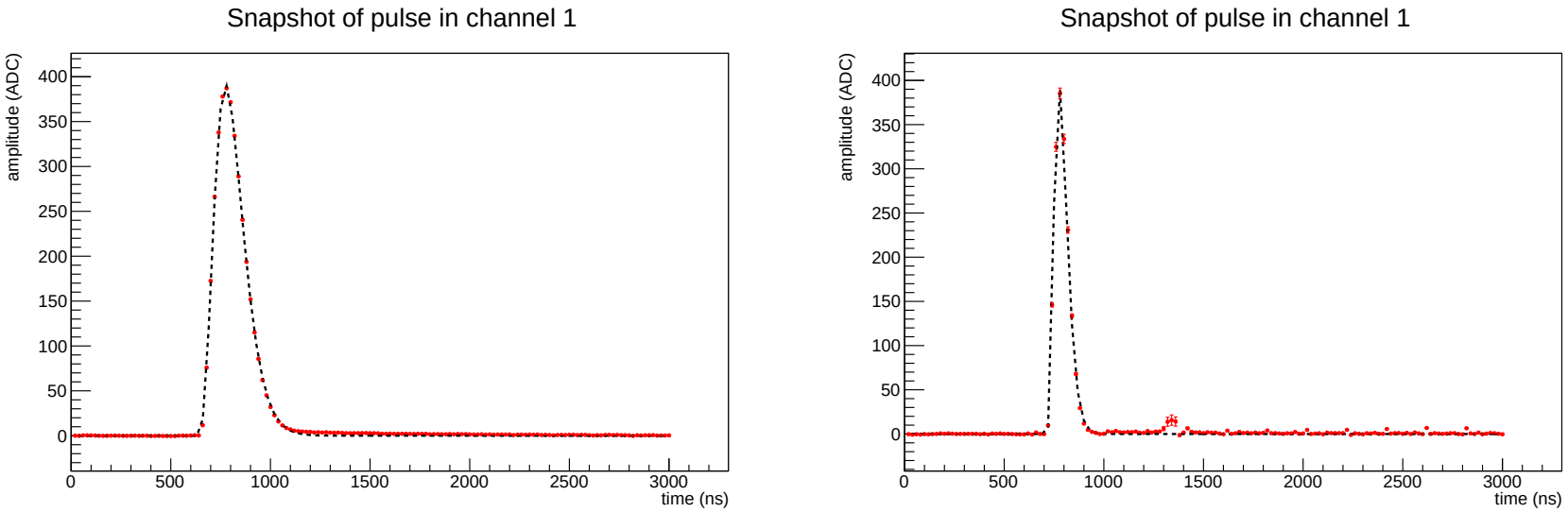


Figure 3: Signal shape with RiseTime function fits.
Left: 160 ns, Right: 80 ns.

Bulk Plot Section 10

Next plots are for all 980 chips for 160 ns, and from the re-pass at 80 ns for the subset that were OK during the 160 ns setting.

All plots are at 20 mV/fC settings. Plots with 30 mV/fC configuration are in the backup section at the end of these slides.

Pedestal (Baseline-Mean) distributions 11

Pedestals (baseline-mean) at 20 mV/fC setting info. Looking at collected data, without any input signal.
OK Cut: $40 < Ped < 110$ (ADC)

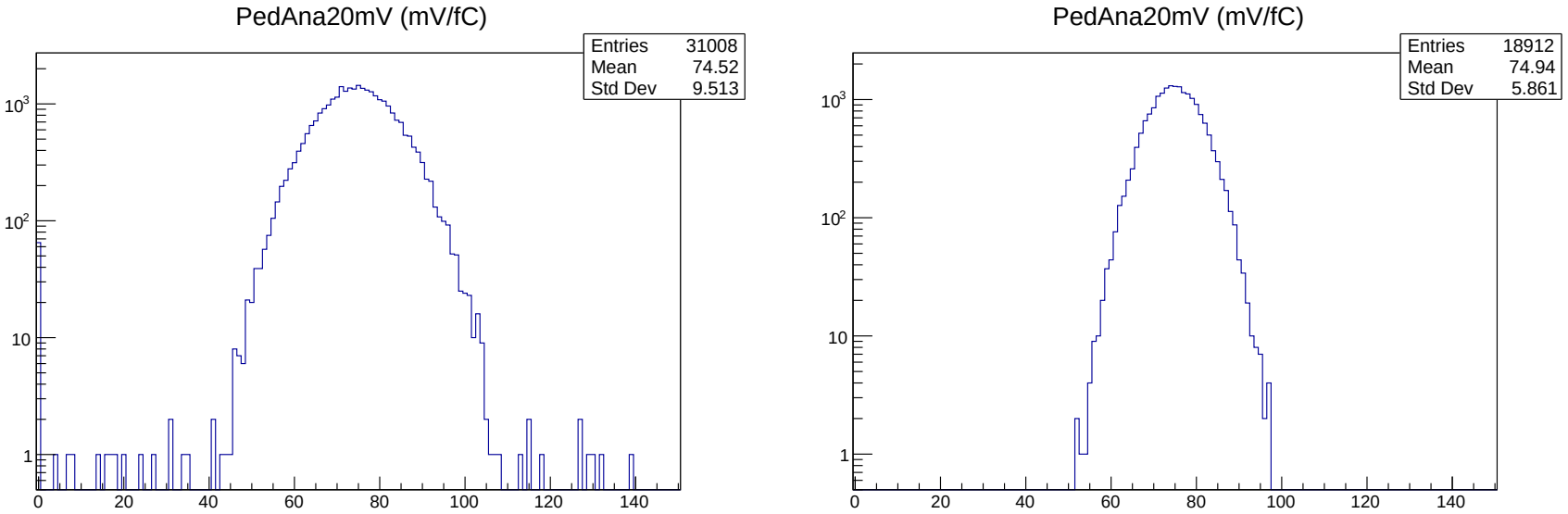


Figure 4: Pedestal at 20 mV/fC setting.
Left: 160 ns, Right: 80 ns.

Noise RMS (in ADC units) distributions

RMS (of Baseline) info.
OK Cut: $0.6 < RMS < 1.7$ (ADC)

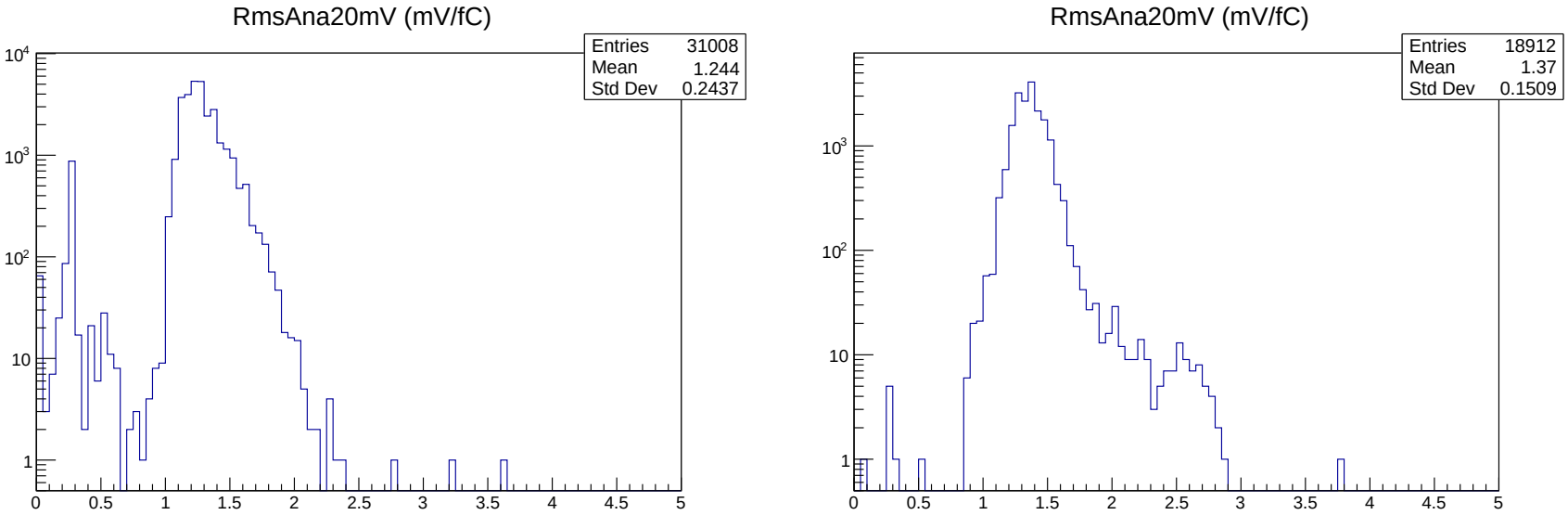


Figure 5: RMS at 20 mV/fC setting.
Left: 160 ns, Right: 80 ns.

We will investigate how we can improve the external noise situation with additional grounding/shielding.

Gain info - again, at nominal 20 mV/fC setting.
OK Cut: $19 < Gain < 23$ (mV/fC)

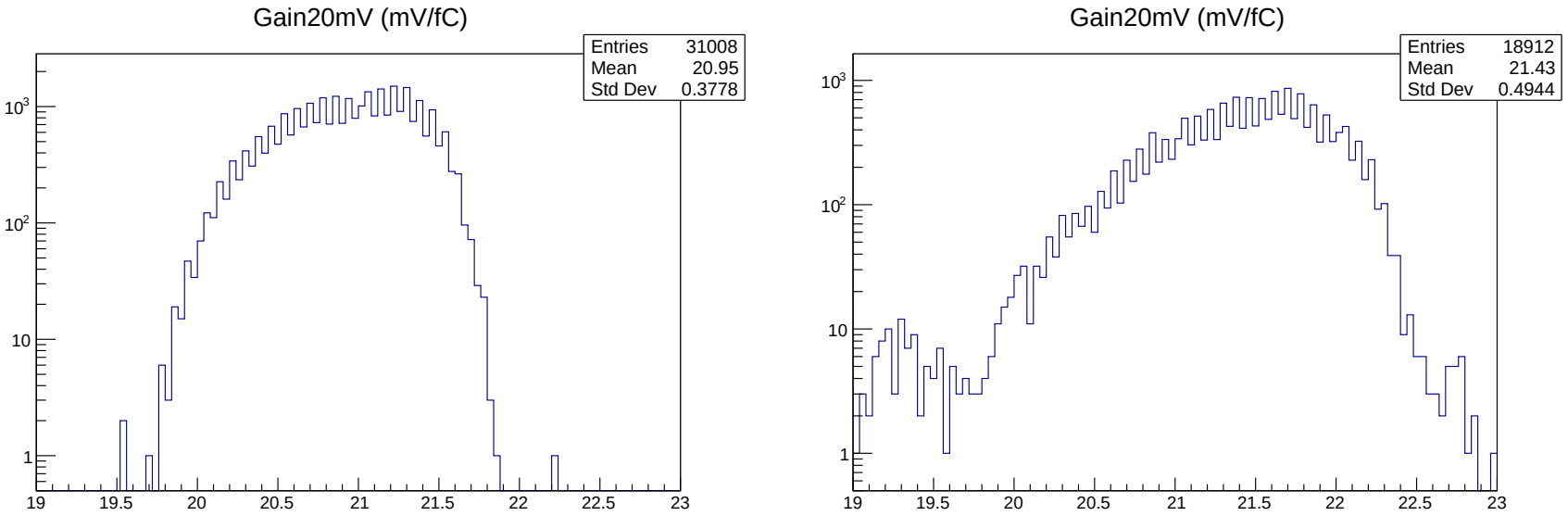


Figure 6: Gain at 20 mV/fC setting.
Left: 160 ns, Right: 80 ns.

RiseTime (in ns)

RiseTime info.

OK Cut: $135 < RiseTime < 155$ (ns) at 160 ns, or $55 < RiseTime < 75$ (ns) at 80 ns.

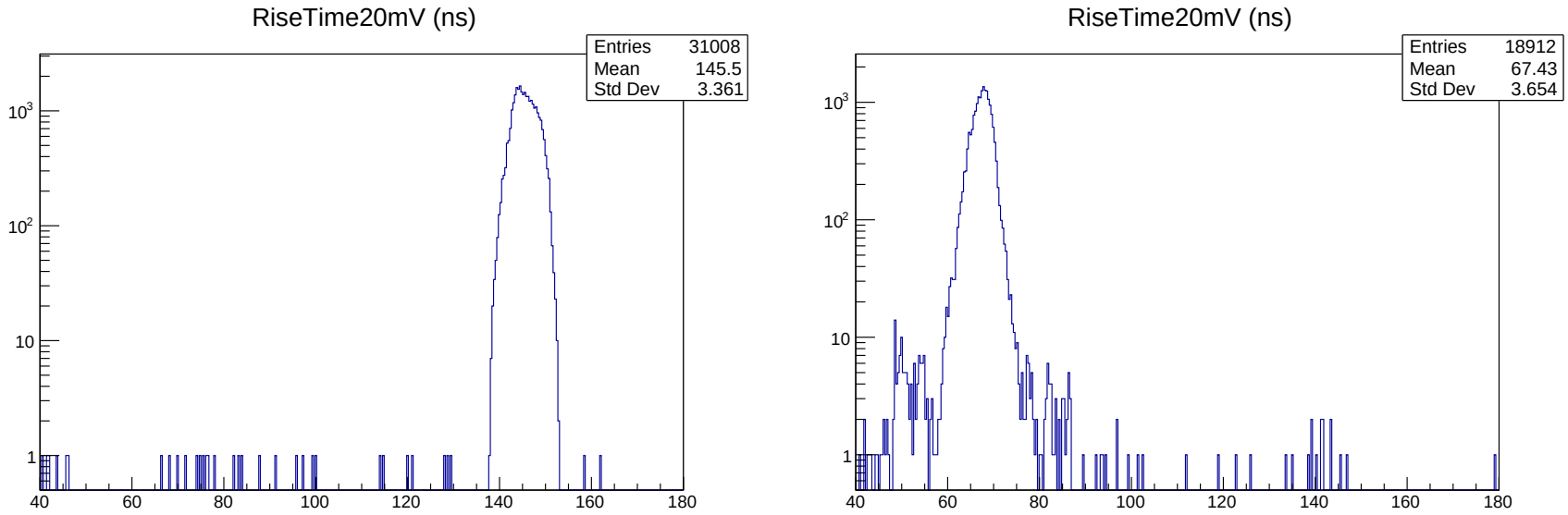


Figure 7: RMS at 20 mV/fC setting.
Left: 160 ns, Right: 80 ns.

Crosstalk-Even (fraction)

Crosstalk info.

OK Cut: $XTalk < 0.05$

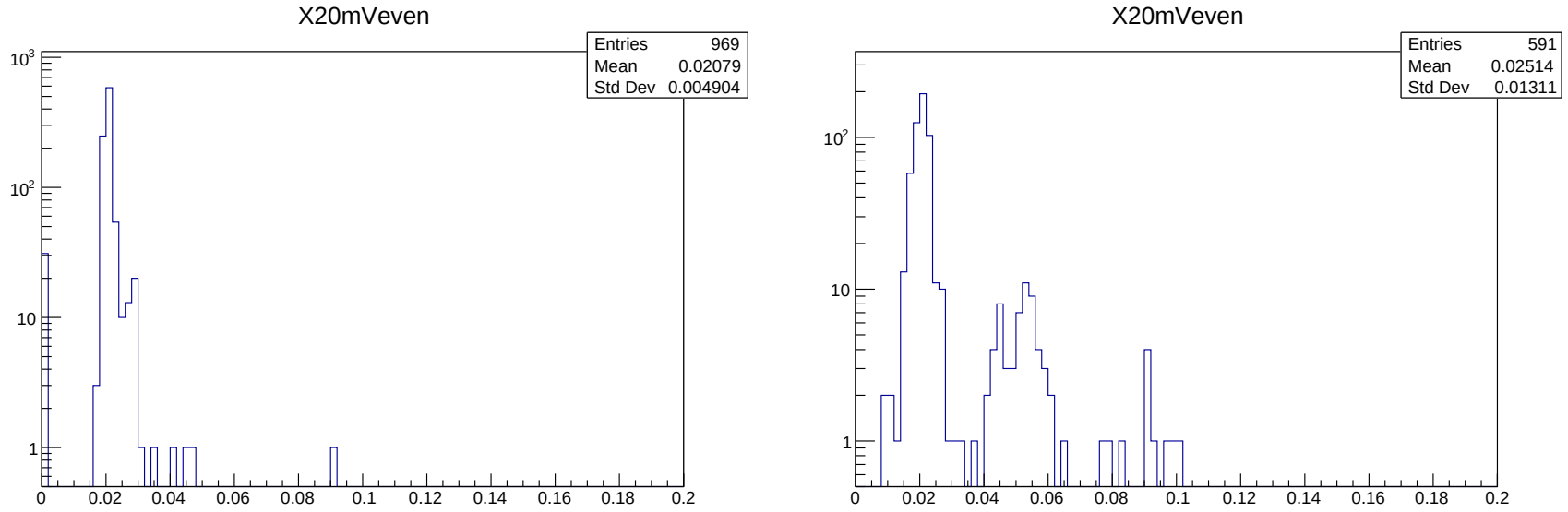


Figure 8: Cross-talk at 20 mV/fC setting.
Left: 160 ns, Right: 80 ns.

Waveform (ADC code vs Timebin) 160 ns - Motor Off

With robot motor off. ± 1-2 ADC counts around mean.

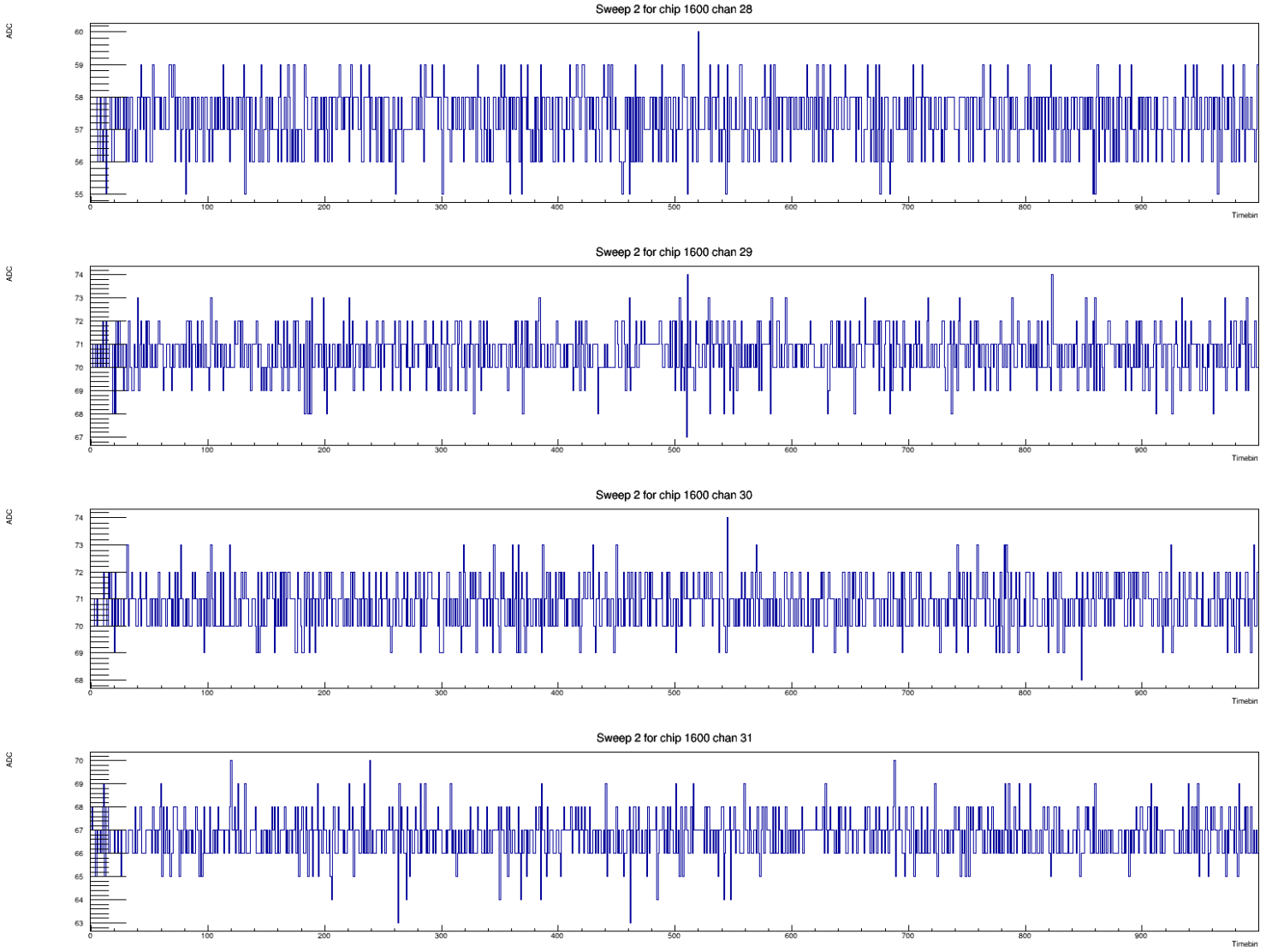


Figure 9: ADC code vs Timebin for 4 channels. Motor off

Waveform (ADC code vs Timebin) 160 ns - Motor On 17

With robot motor on. Coherent (for all channels) noise with up to 10 ADC count deviation from mean.

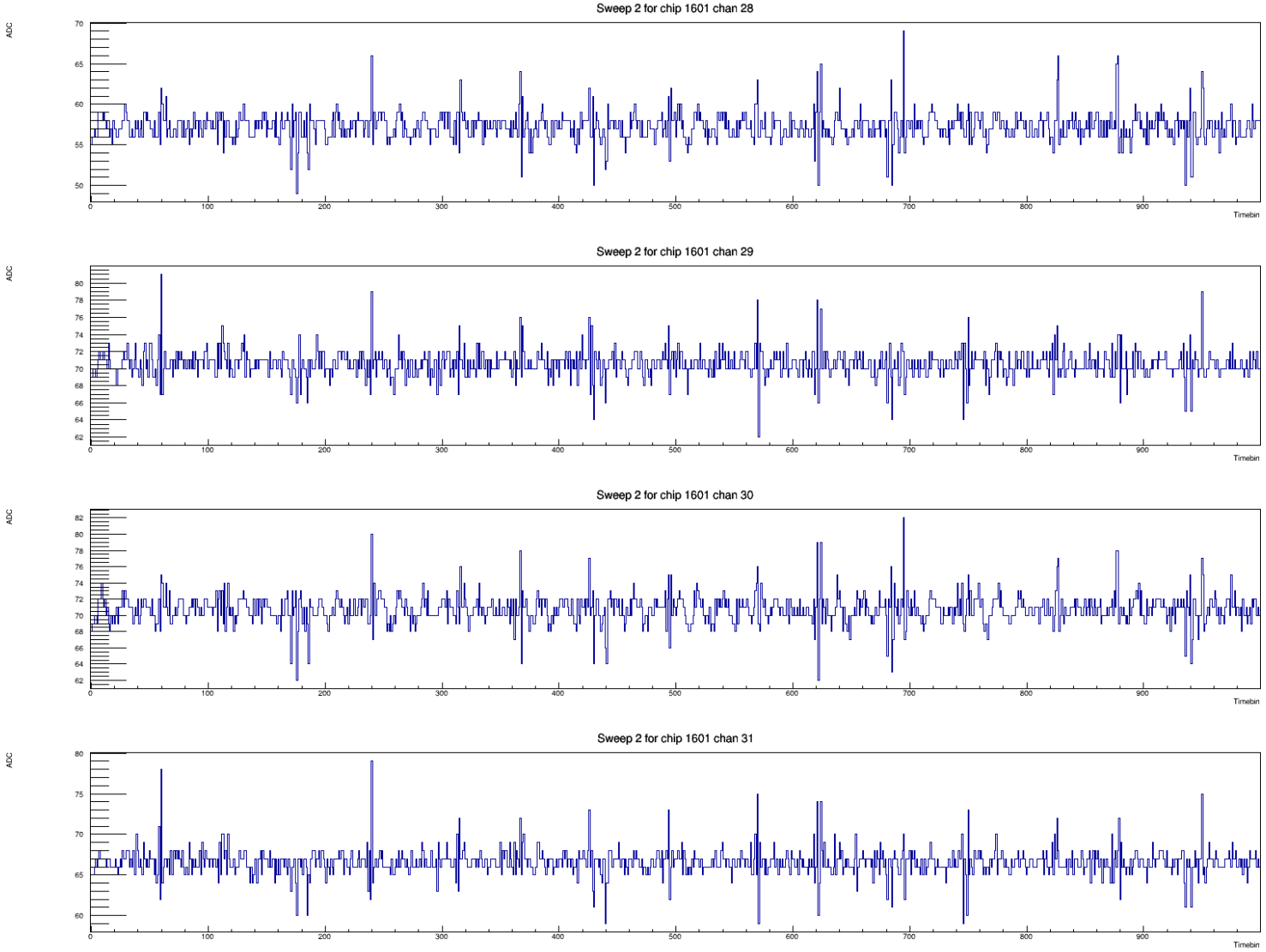


Figure 10: ADC code vs Timebin for 4 channels. Motor on

Waveform (ADC code vs Timebin) 80 ns - Motor Off

With robot motor off. ± 1-2 ADC counts around mean.

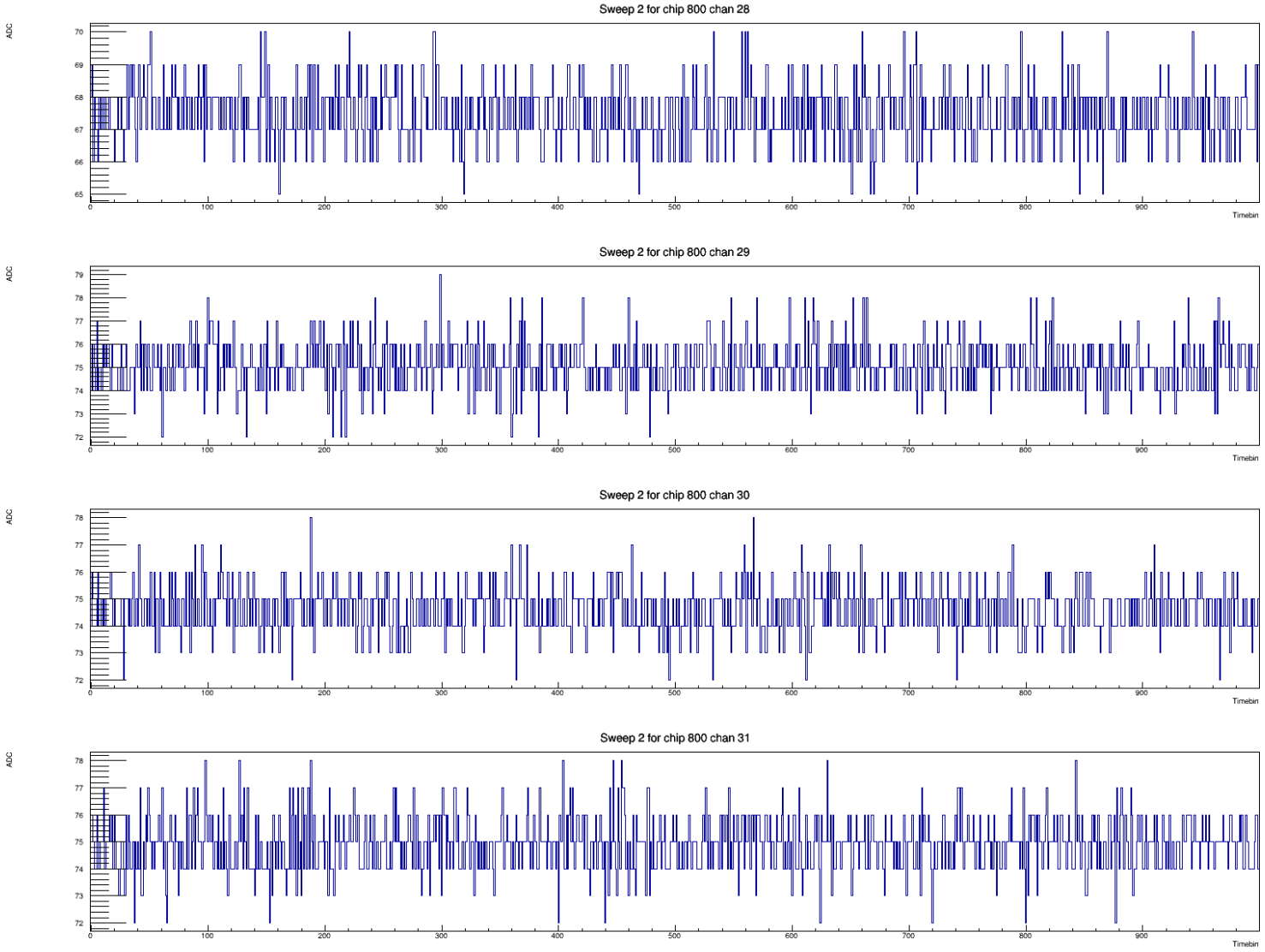
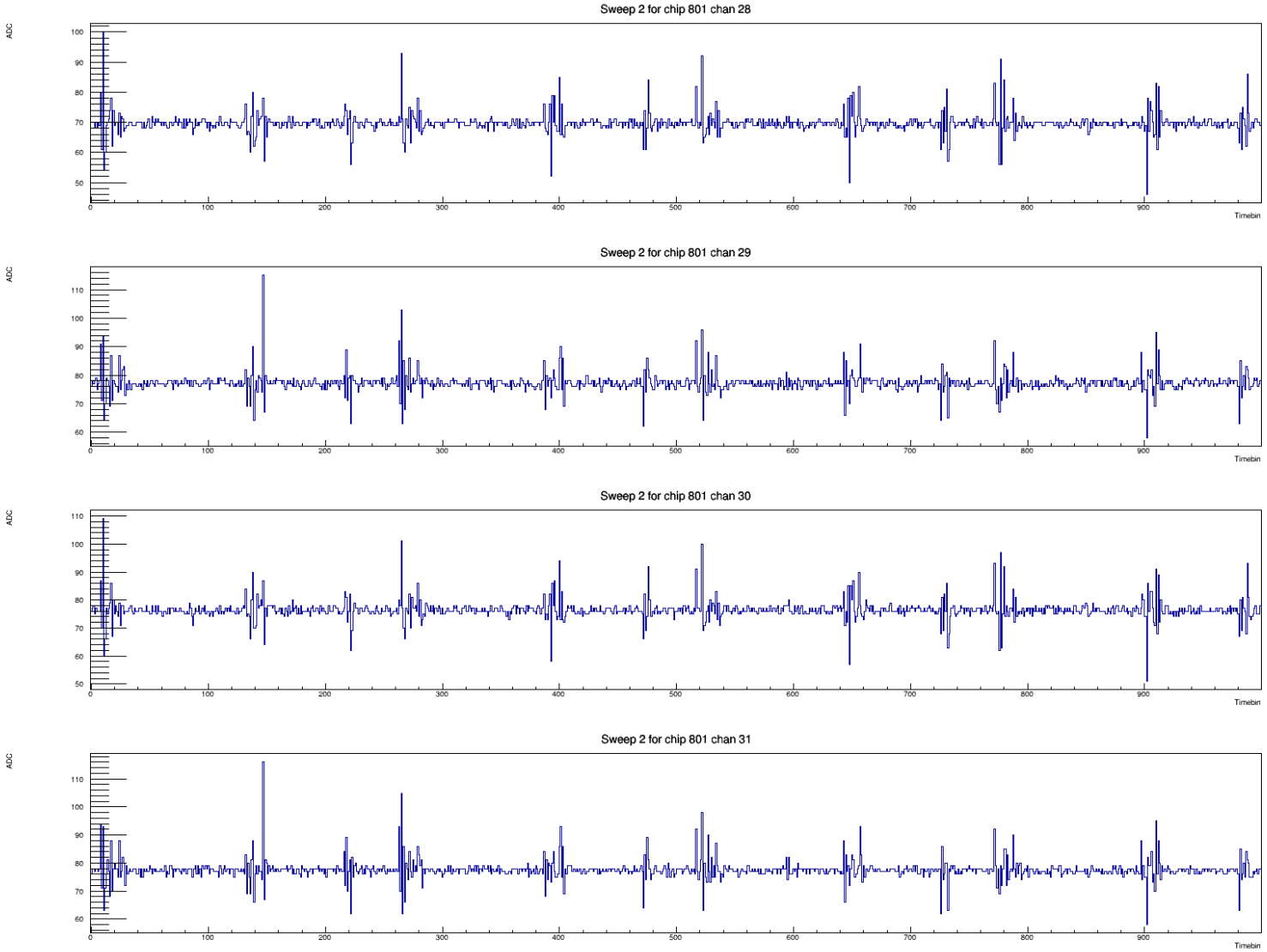


Figure 11: ADC code vs Timebin for 4 channels. Motor off

Waveform (ADC code vs Timebin) 80 ns - Motor On

With robot motor on. Signficantly more sensitive to external noise (robot motor) than at 160 ns setting.



Status and plan ahead

- Have gotten the initial rounds of V5 testing for sPHENIX started after cleanroom robot move, and sent 378 chips to BNL that passed tests at both 160 and 80 ns configurations. ($\sim$ 100 chips more than needed for the next few months).
- Need to improve noise situation in our setup and channel-level analog analysis: Ped, Rms, Gain, RiseTime, Xtalk, BitCheck. It is harder for us to determine (non-pedestal/baseline or rms) parameters at 80 ns than for 160 ns. If it was enough to qualify the chips at 160 ns configuration, we would be very happy... (Detailed chip categorization anyhow done at USP)
- Main (digital, chip-level) errors all better or comparable to V4.
- We expect that we should be able to get to a similar acceptable yield for V5 as for V4, after improvements, cut adjustments and possible repasses over chips with failed tests. This was also done for the V4 chips. Our assumption is that if a test is OK, the chip is OK. (A failed test could be due to either the chip being bad, or the test setup/connection or analysis could be faulty)
- Will continue to re-debug our setup to be ready to start with production testing in summer
- Will set up a reference tray for stability check
- Still work on noise and stability, and possibly getting both stations operational (may not need both for relatively small amount of sPHENIX chips)

Ped, RMS, Gain, RiseTime, Cross-talk Plots at 30 mV/fC setting info, followed by plots for current values.

Pedestal (Baseline) distributions

Pedestal (Baseline) at 30 mV/fC setting info:

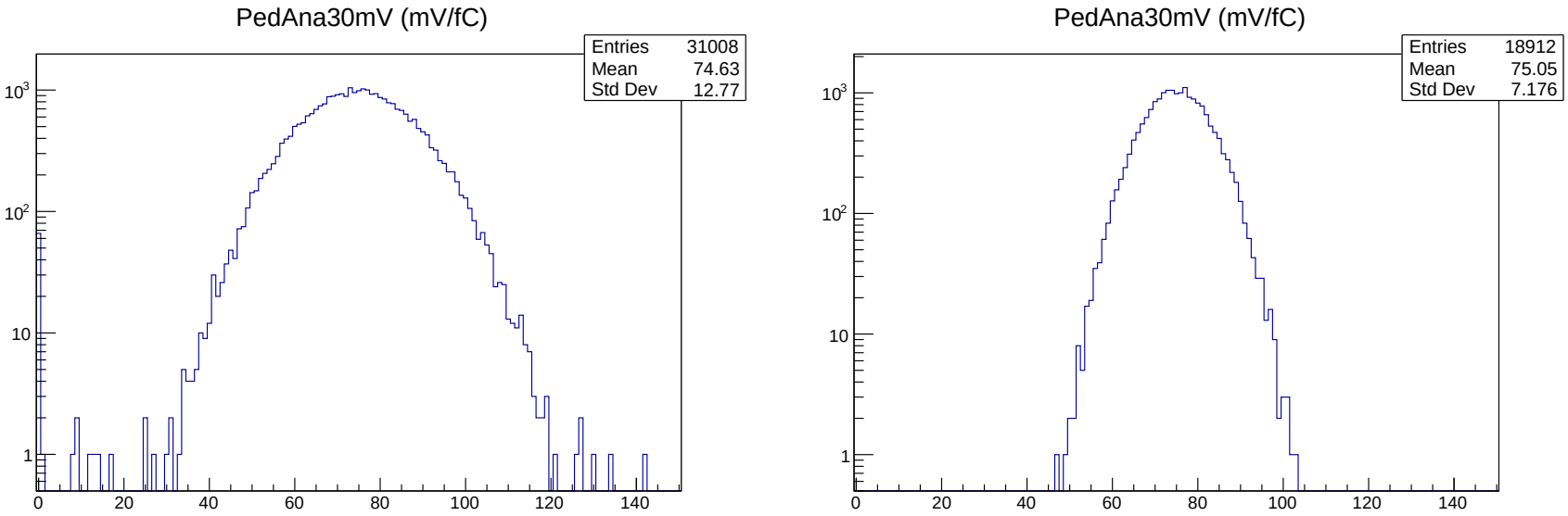


Figure 13: Pedestal at 30 mV/fC setting.
Left: 160 ns, Right: 80 ns.

RMS (in ADC units) distributions

RMS (Baseline Noise) info:

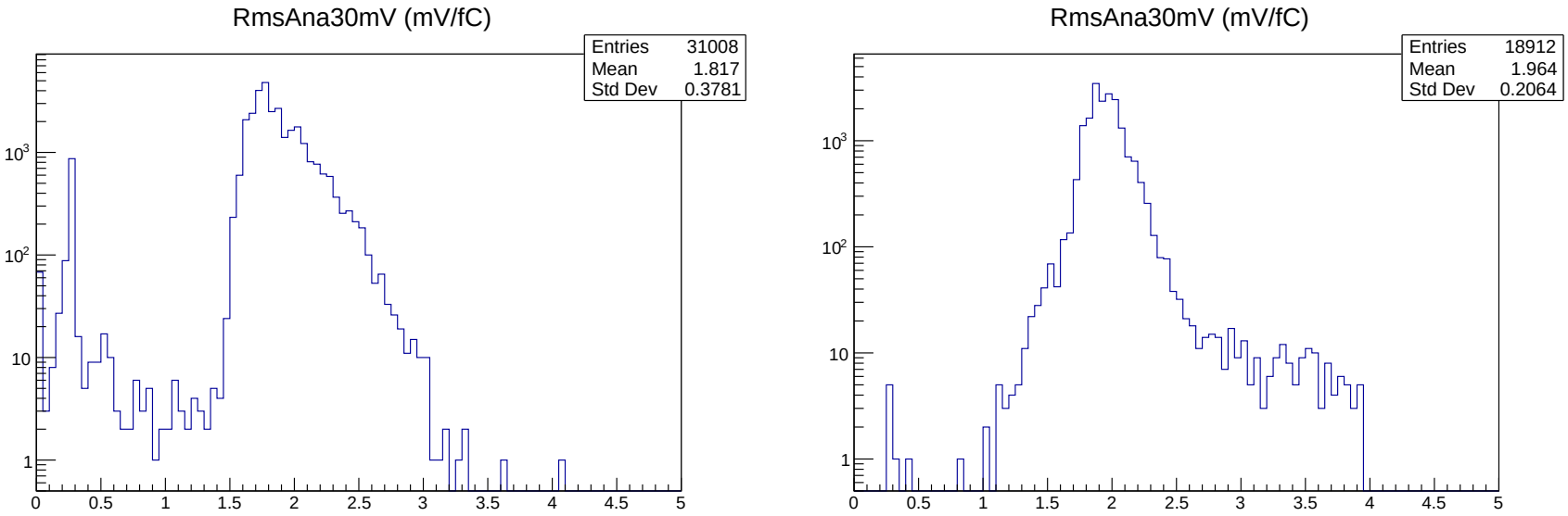


Figure 14: RMS at 30 mV/fC setting.
Left: 160 ns, Right: 80 ns.

We will investigate if we can improve the external noise situation with additional grounding.

Gain info:

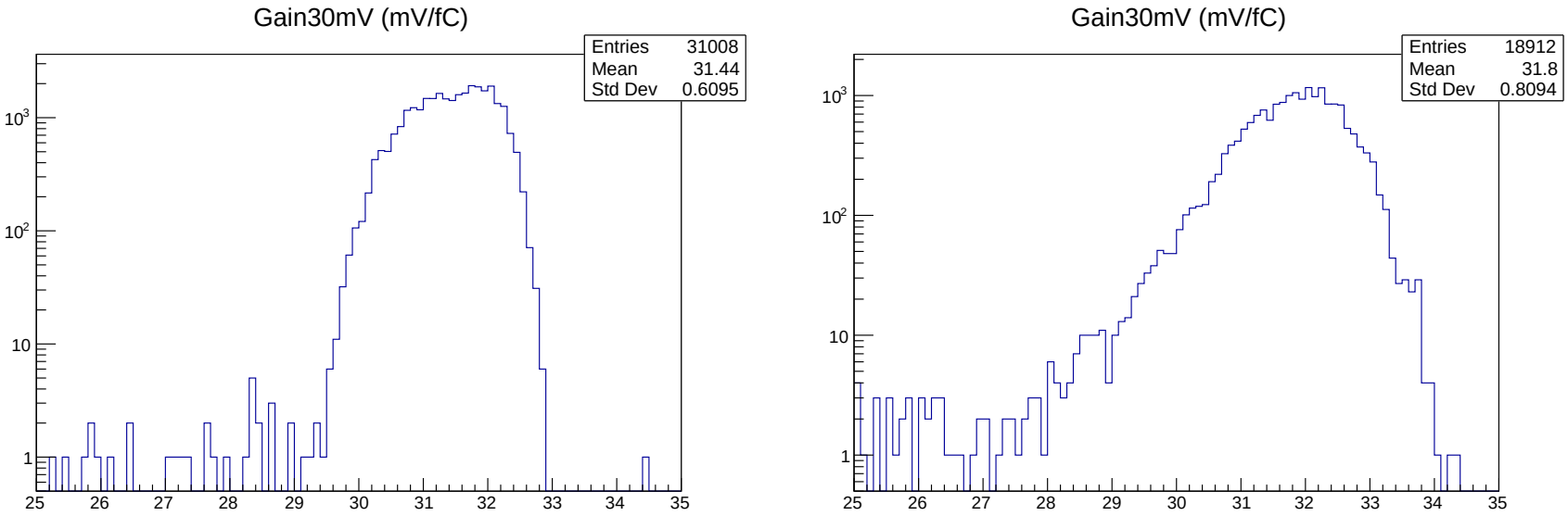


Figure 15: Gain at 30 mV/fC setting.
Left: 160 ns, Right: 80 ns.

RiseTime (in ns)

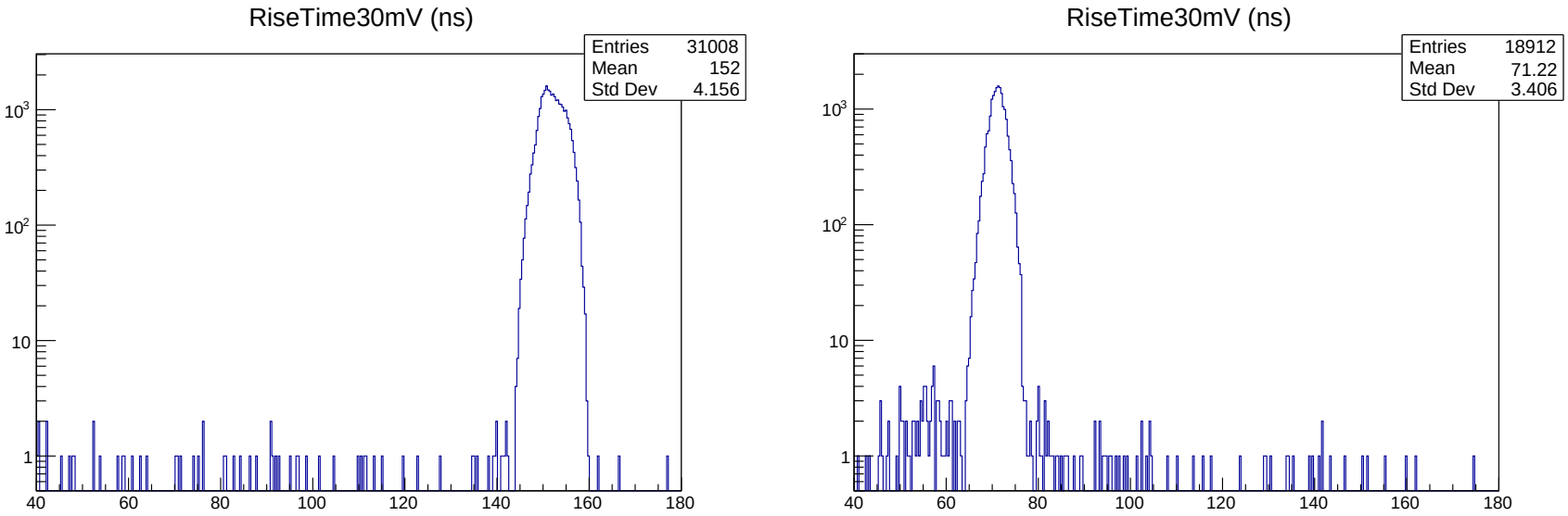


Figure 16: RMS at 30 mV/fC setting.
Left: 160 ns, Right: 80 ns.

Crosstalk-Even (fraction)

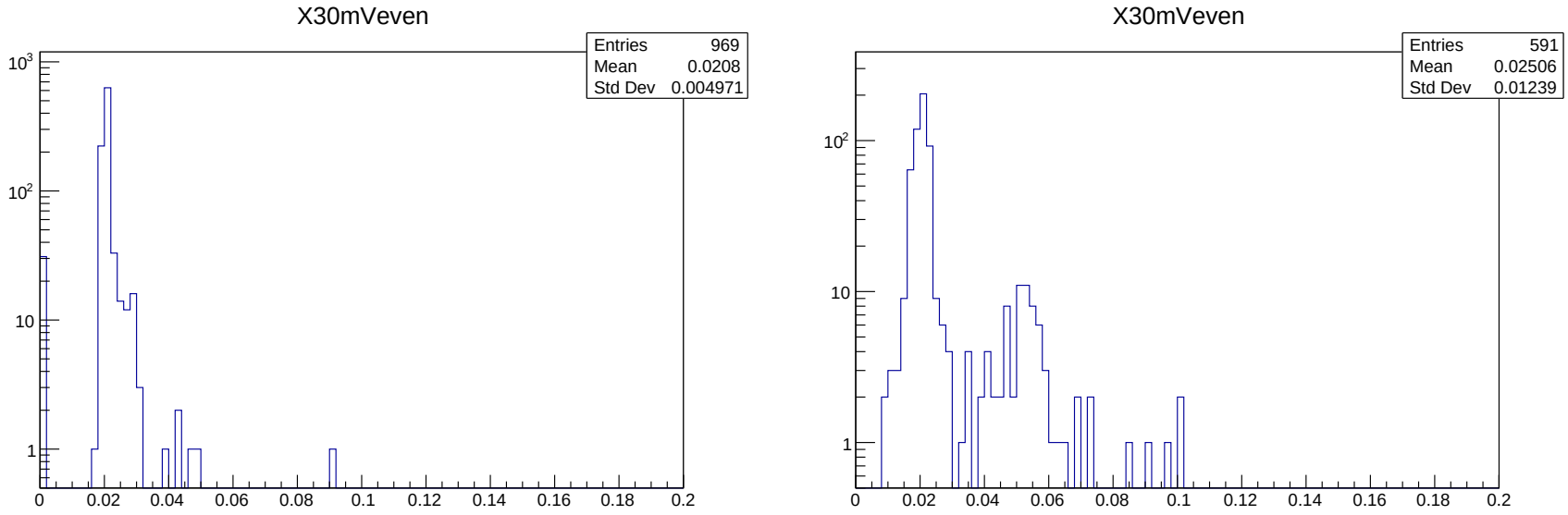


Figure 17: Cross-talk at 30 mV/fC setting.
Left: 160 ns, Right: 80 ns.

$FE1 - CURR$ Cut: min 75, max 100

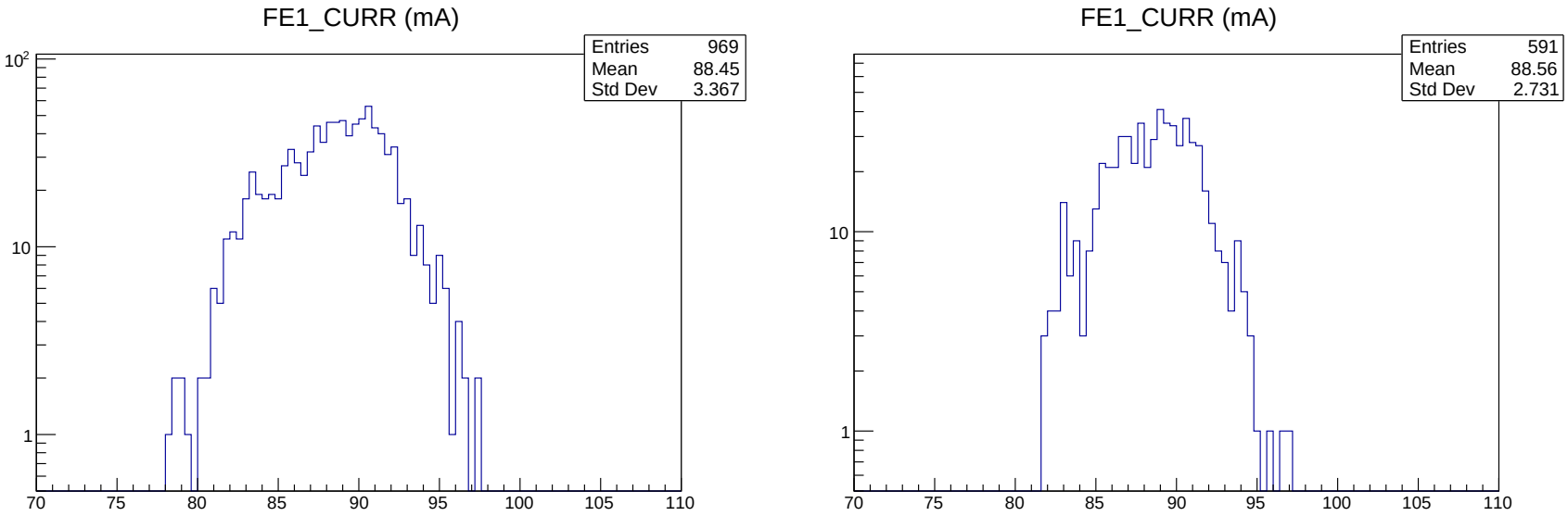


Figure 18: Current 0.
Left: 160 ns, Right: 80 ns.

$FE2 - CURR$ Cut: min 50, max 80

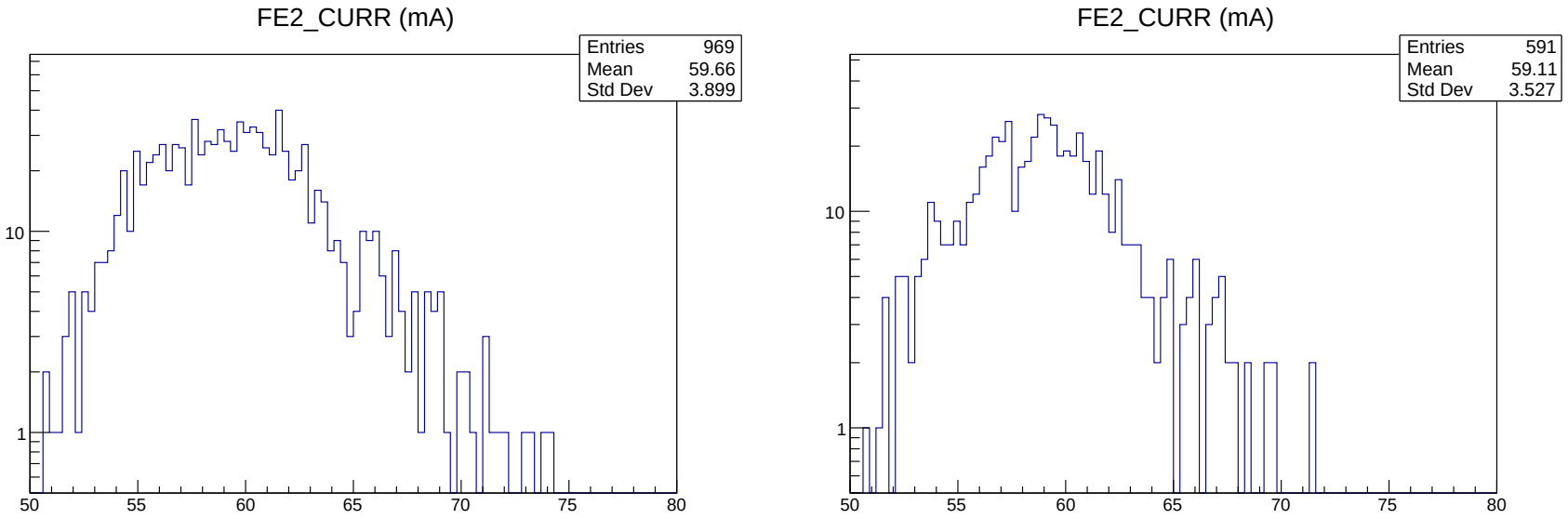


Figure 19: Current 1.
Left: 160 ns, Right: 80 ns.

$AD - CURR$ Cut: min 3, max 14

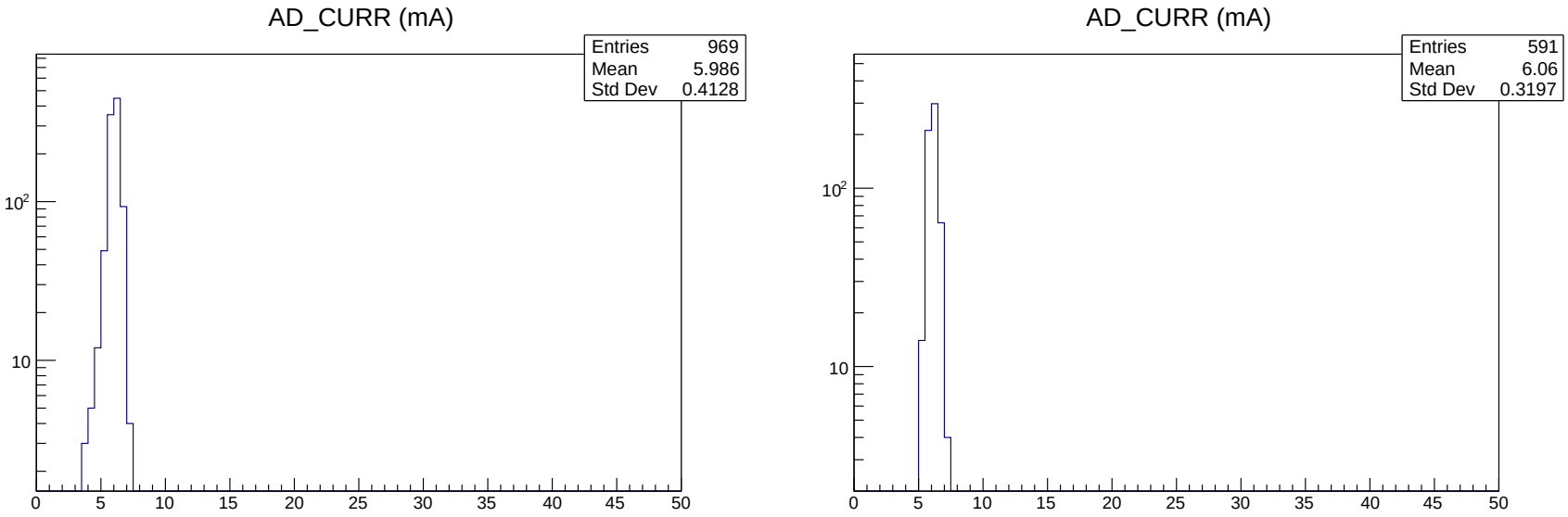


Figure 20: Current 2.
Left: 160 ns, Right: 80 ns.

$DR-CURR$ Cut: min 35, max 44

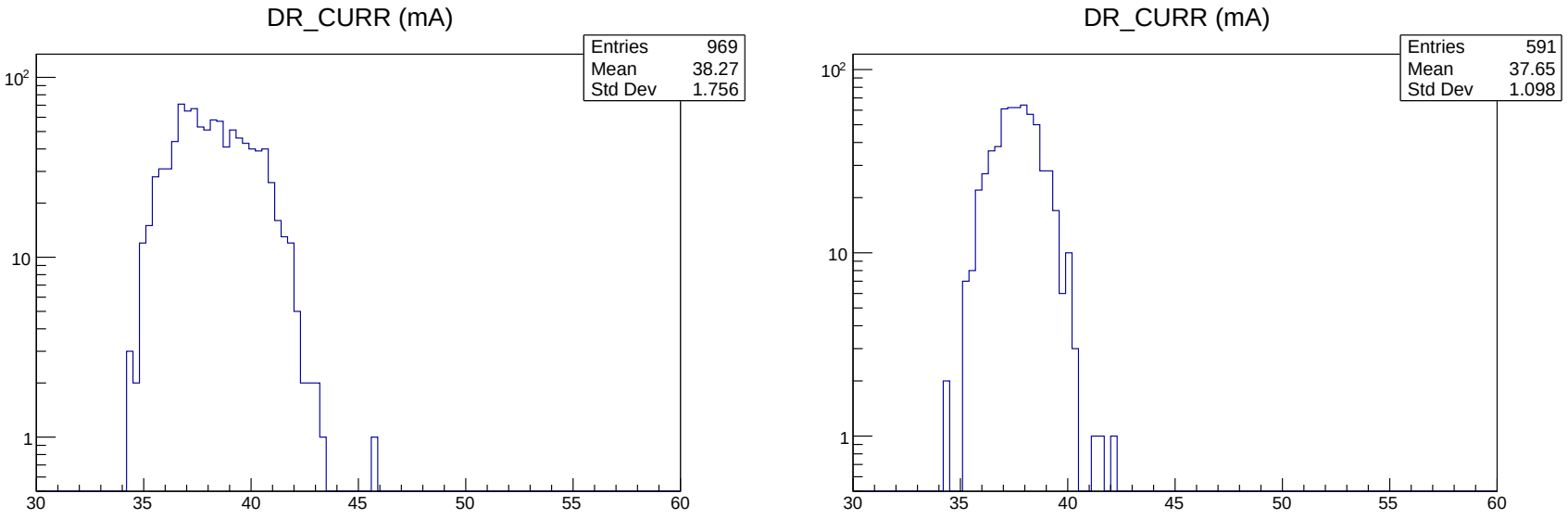


Figure 21: Current 3.
Left: 160 ns, Right: 80 ns.

$DG - CURR$ Cut: min 10, max 20

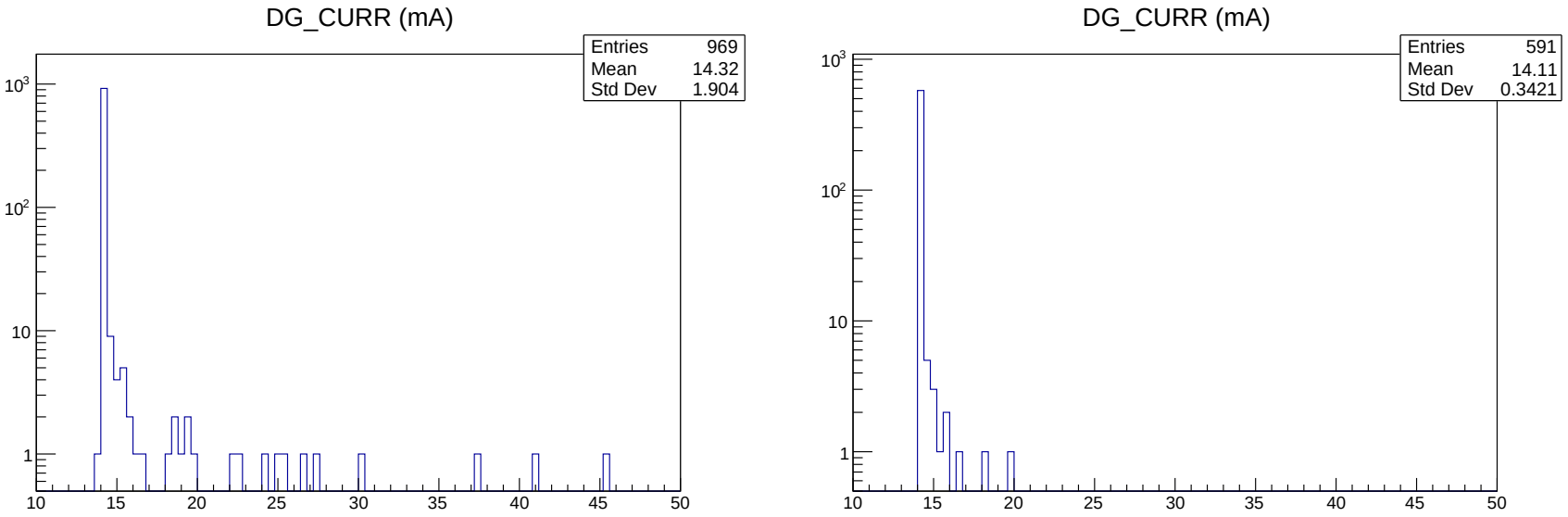


Figure 22: Current 4.
Left: 160 ns, Right: 80 ns.