Test results on V3 V4 from Lund

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All tests with socket PCCA and Sockit board readout.
1.244V supply
1.092V Vref
Default Bandgap trim setting 4. 770mV, 470mV and 620mV
20mV/fC if not said differently
10MHz sampling
DSP mode
11 elink mode

Score after 249 tested V3 and V4 SAMPA

judgement	V3	Fraction V3	V4	Fraction V4	Total V3+V4	Fraction total
Tested	136	100%	123	100%	249	100%
Dead ch. (zeroped) **1.9**	6	3%	6	4,8%	12	4,8%
Dead ch. (no signal)	4	4,4%	8	7%	12	4,8%
Jtag **1.10**	0	0	3	2,4%	3	1.2%
Memory error **1.7**	8	8,8%	5	4,1%	13	5.2%
DFT **1.11**	7	5,1%	9	7,3%	16	6,4%
Synch error **1.5**	0	0%	2	1,6%	2	0,8%
Inoperable (e.g short)	0	0%	3	2,4%	3	1.2%
Total faults	25	18,3%	36	29.1%	61	24.4%
correct double fault	22	16,1%	27	21,9%	49	19.6%

Dead ch (no signal) pedestal is OK but no response to testpulsing (like missing bondwire)

1.6. Data integrity best tested on FEC. Sockit not 100% stable readout.
But once synked, never losing synk

December 15, 2017: Lund update

In these slides, the folllowing items from Marco's list are included:

- 1.4: Bandgap voltages, V750 et al, many chips
- 1.8: Ring oscillation/Clock freq., many chips
- 1.13: Baseline info vs chan, many chips
- 1.14: Baseline noise at 0 pF and 0 Ohm, many chips
- 1.14: Baseline noise, variation with capacitance and resistor values, few chips
- 1.15: Crosstalk check, few chips
- 1.16-1.17: Gain variation with capacitance and resistor values, few chips
- 1.16-1.17, 16: Gain at 0 pF and 0 Ohm, many chips
- 21: Pulse shape, with varying delay between test pulse and sampling clock

Item 7, with pile-up saturation studies in separate file.

In the interest of time, put duplicates/extra plots in backup slides at the end.

1.4 : Bandgap voltages V3 and V4, many chips

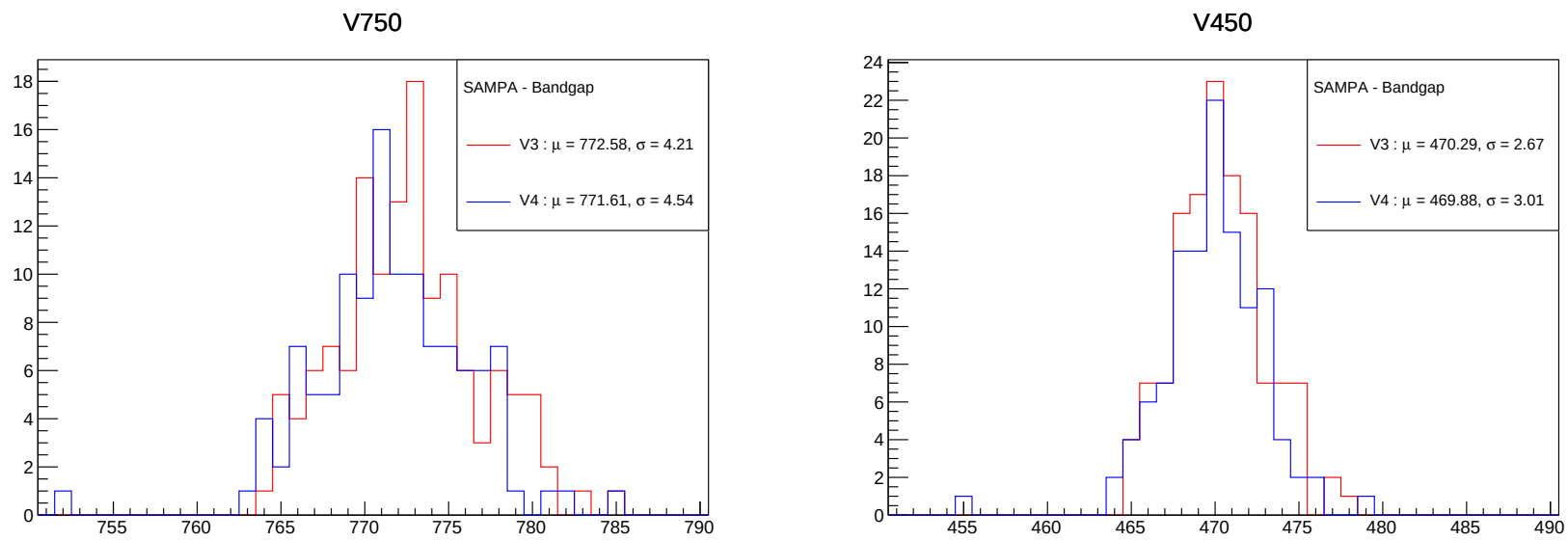


Figure 1: Bandgap voltages for V3 and V4 chips. V750 left, and V450 right.

1.4 : Bandgap voltages Differences V3 and V4, many chips 5

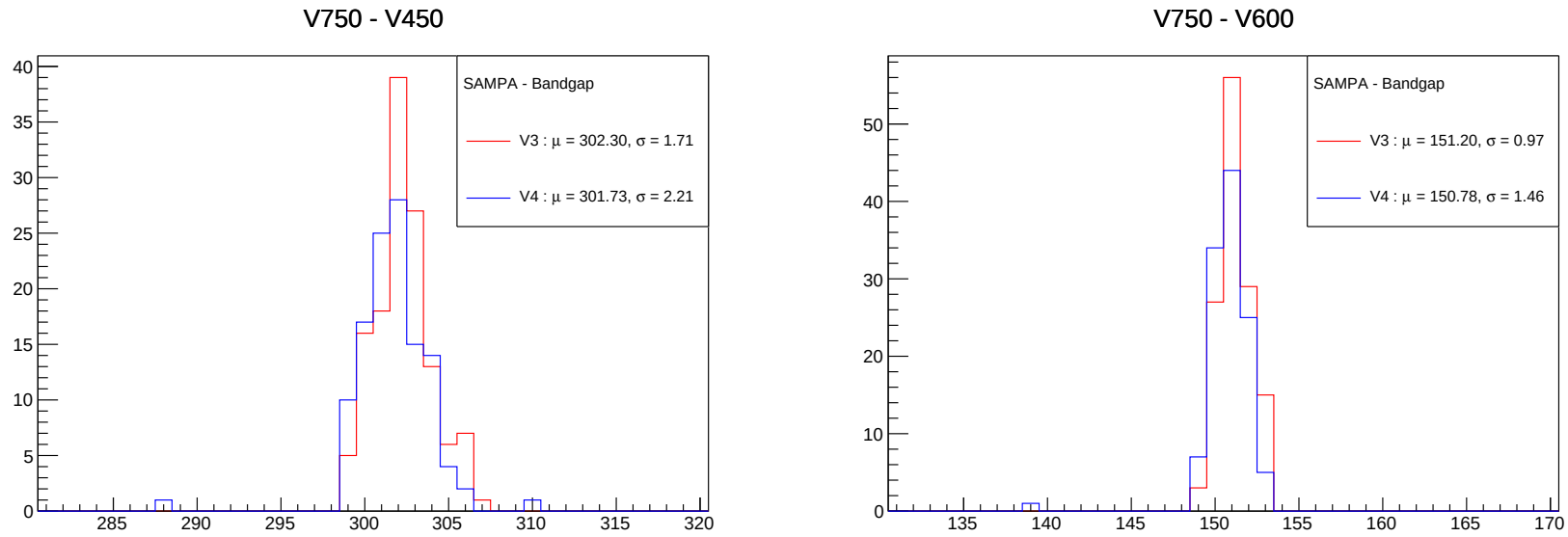


Figure 2: Bandgap voltages for V3 and V4 chips. V750 left, and V450 right.

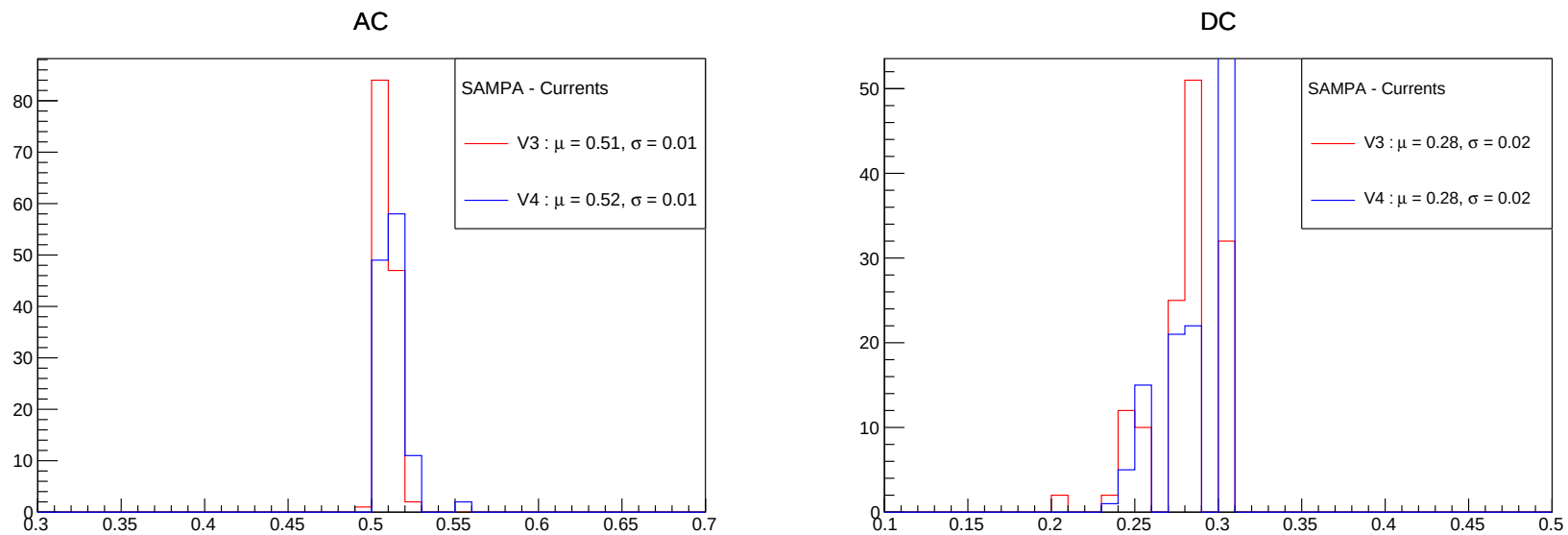
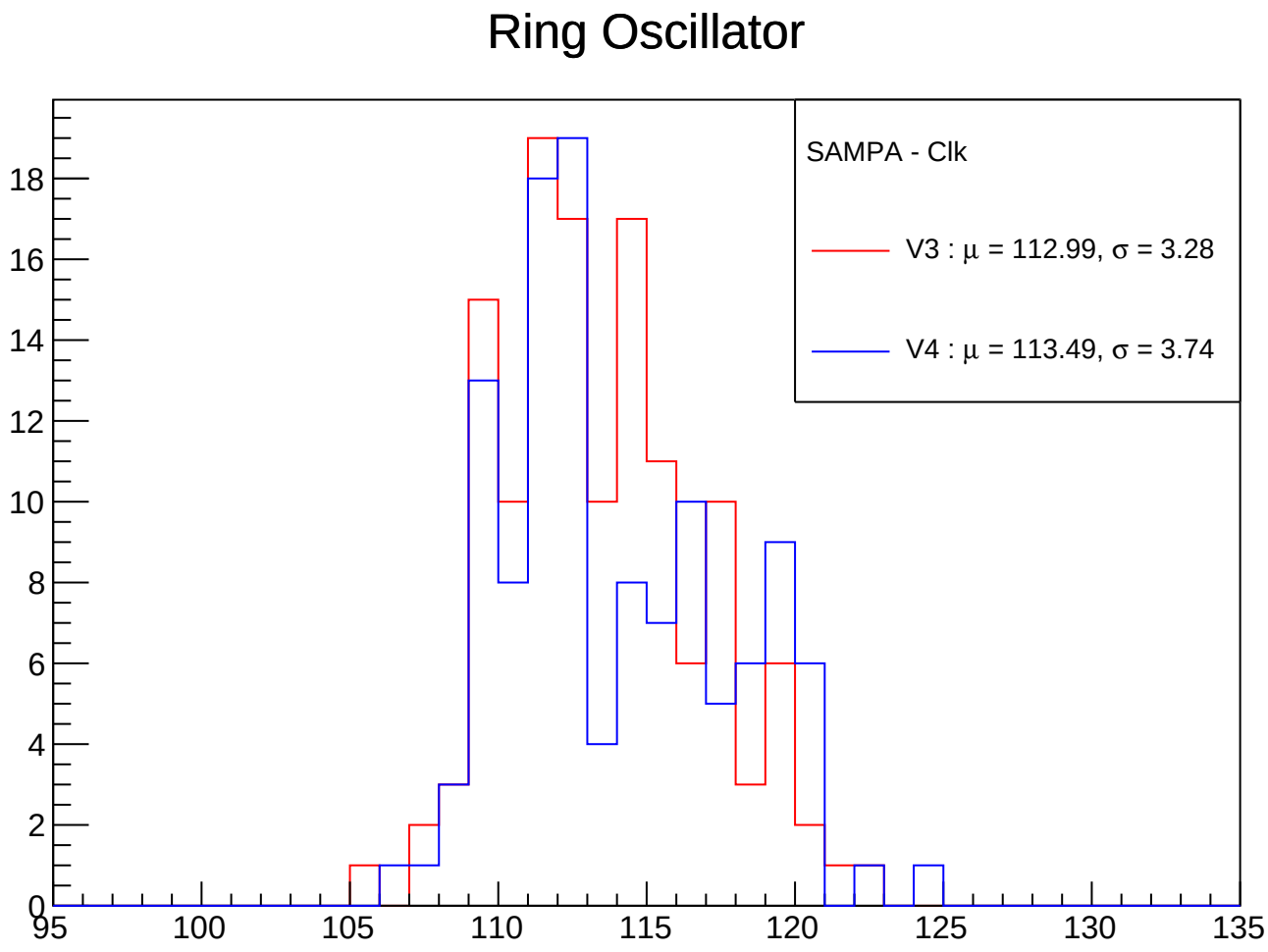


Figure 3: Bandgap voltages for V3 and V4 chips. AC left, and DC right.


Ring Oscillator
SAMPA - Clk
V3 : μ = 112.99, σ = 3.28
V4 : μ = 113.49, σ = 3.74
0
2
4
6
8
10
12
14
16
18
95
100
105
110
115
120
125
130
135

1.13 : Baseline V2 vs V3 vs V4, many chips, 1D

Baseline values for all channels for many V2 and V3 and V4 chips (at 0 pF and 0 Ohm):

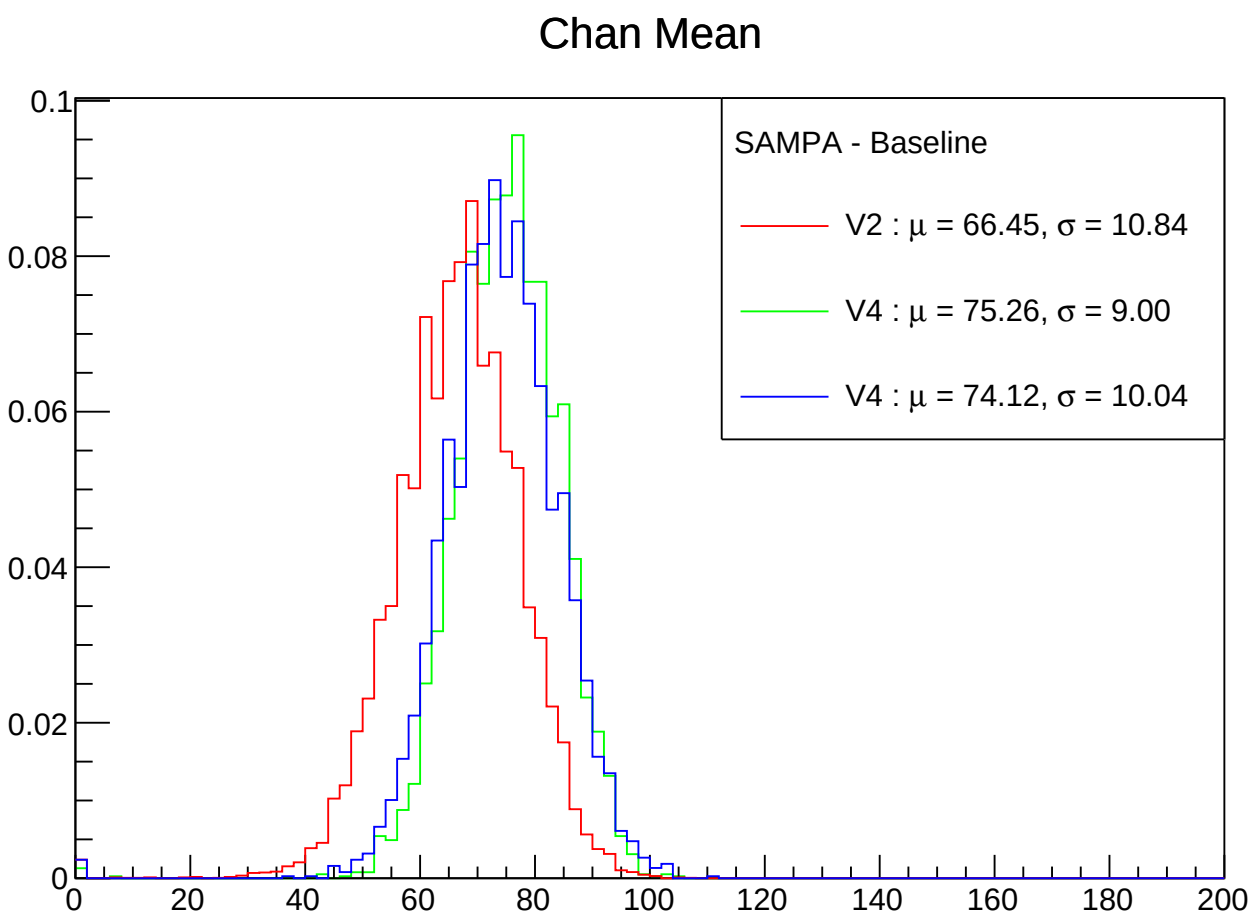


Figure 4: Baseline distributions for V2, V3, V4

1.13 : Baseline V2 vs V3, many chips, 2D

Baseline values as a function of chip number:

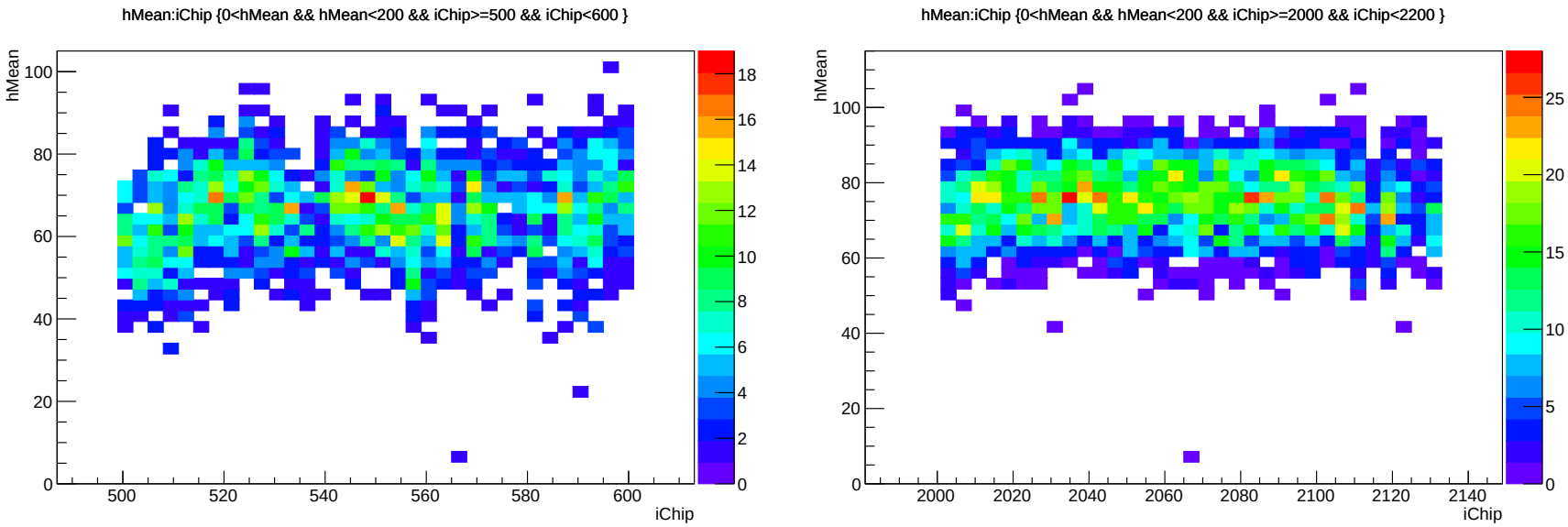


Figure 5: V2 on the left, V3 on the right.

1.13 : Baseline V3 vs V4, many chips, 2D

Baseline values as a function of chip number:
(looks like arger spread in baseline for V4 chips, but note different scale there were not any 0 channels in the tested V4 sample...)

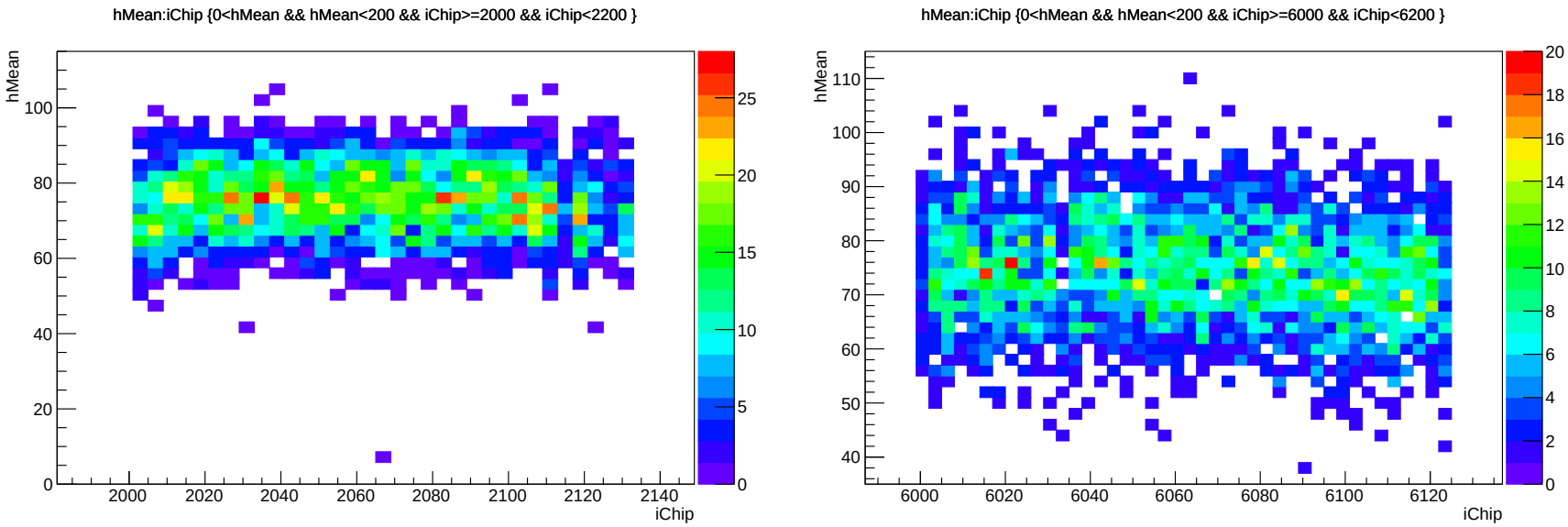


Figure 6: V3 on the left, V4 on the right.

1.14 : Noise V2 vs V3 vs V4, many chips, 1D

Comparing channels for many V2 and V3 and V4 chips (at 0 pF and 0 Ohm):
With ADC units on the left, and electron equivalents/estimate on the right.

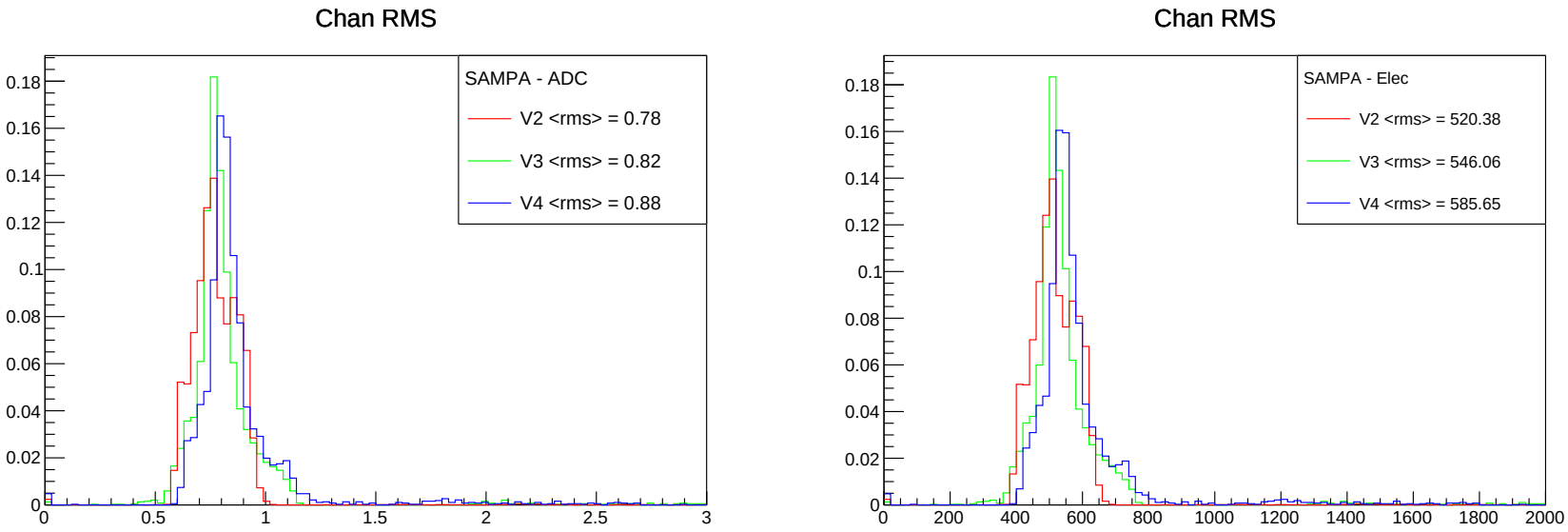


Figure 7: With ADC units on the left, and electron equivalents/estimate on the right.

1.14 : Noise V2 vs V3, many chips, 2D

Comparing channels for many V2 and V3 chips, 20 mV/fC settings: V2 on the left, V3 on the right.

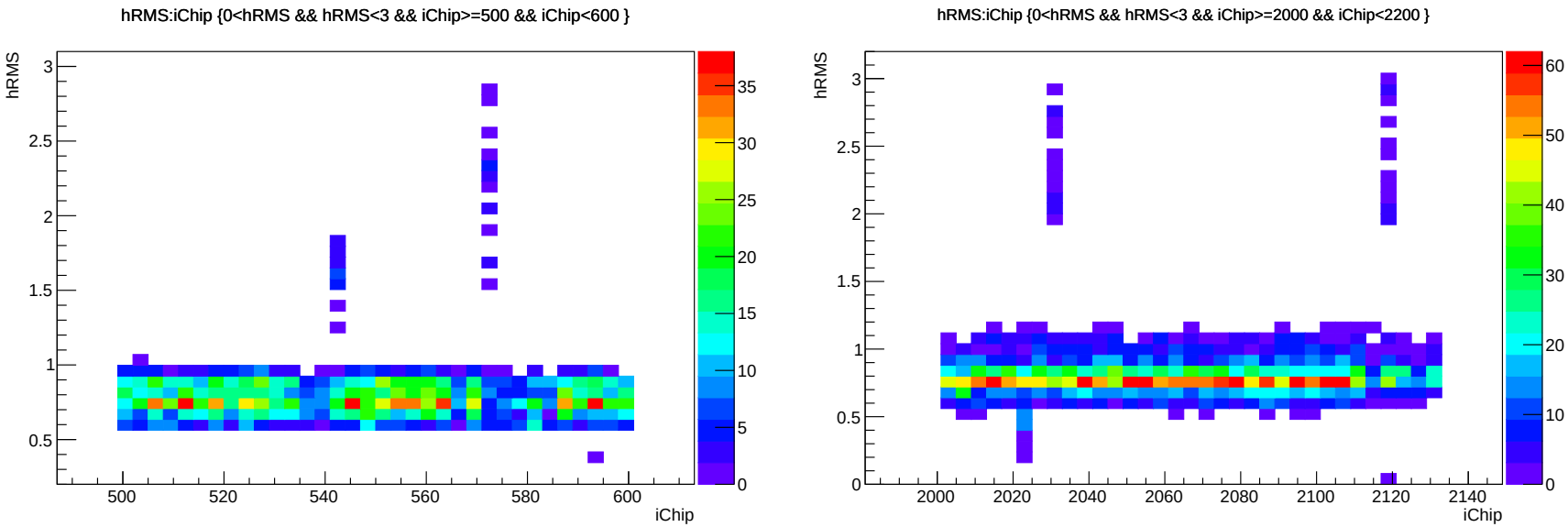


Figure 8: V2 on the left, V3 on the right.

1.14 : Noise V3 vs V4, many chips, 2D

Comparing channels for many V3 and V4 chips, 20 mV/fC settings:
V3 on the left, V4 on the right.

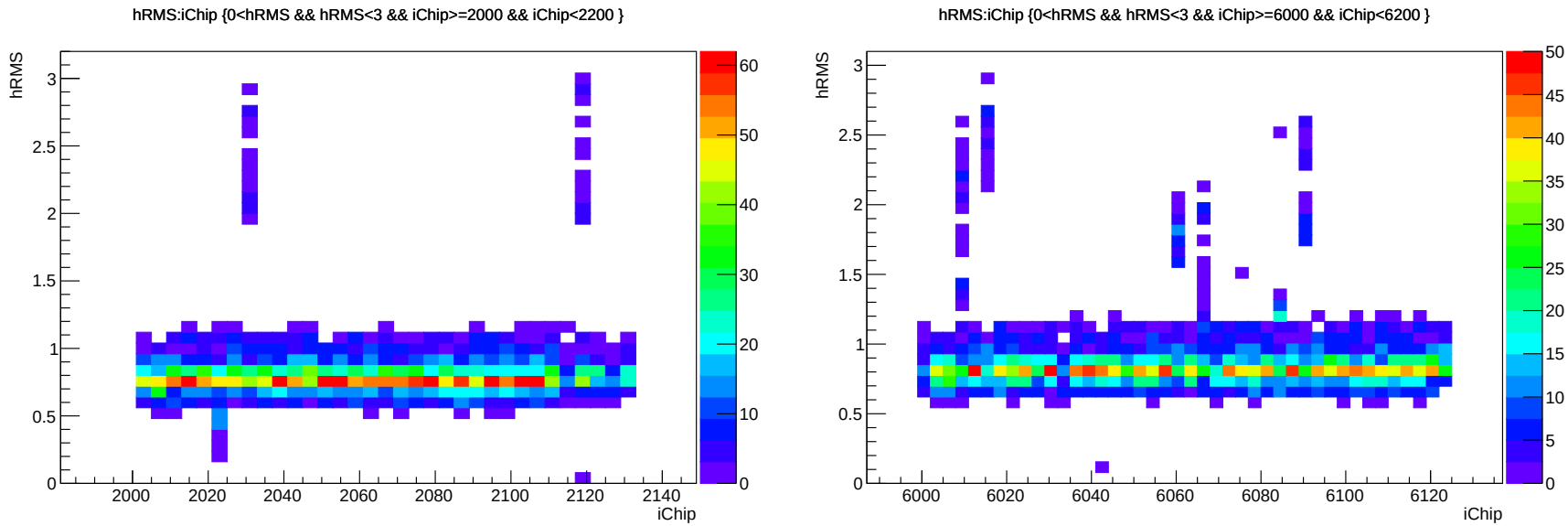


Figure 9: V3 on the left, V4 on the right.

A few noisier V4 chips, but could include some chips that also have other issues, or some spurious DAQ issues (?, to be verified/retested).

1.14 : V3 (chip #2128); Noise vs Capacitance (100 Ohm resistor)

(Already shown on Dec 7) One of 3 tested V3 chips : similar values as seen for V2 (18 pF value similar, 68 pF approx. 10% better for V3; other V3 chips more similar to V2 values).

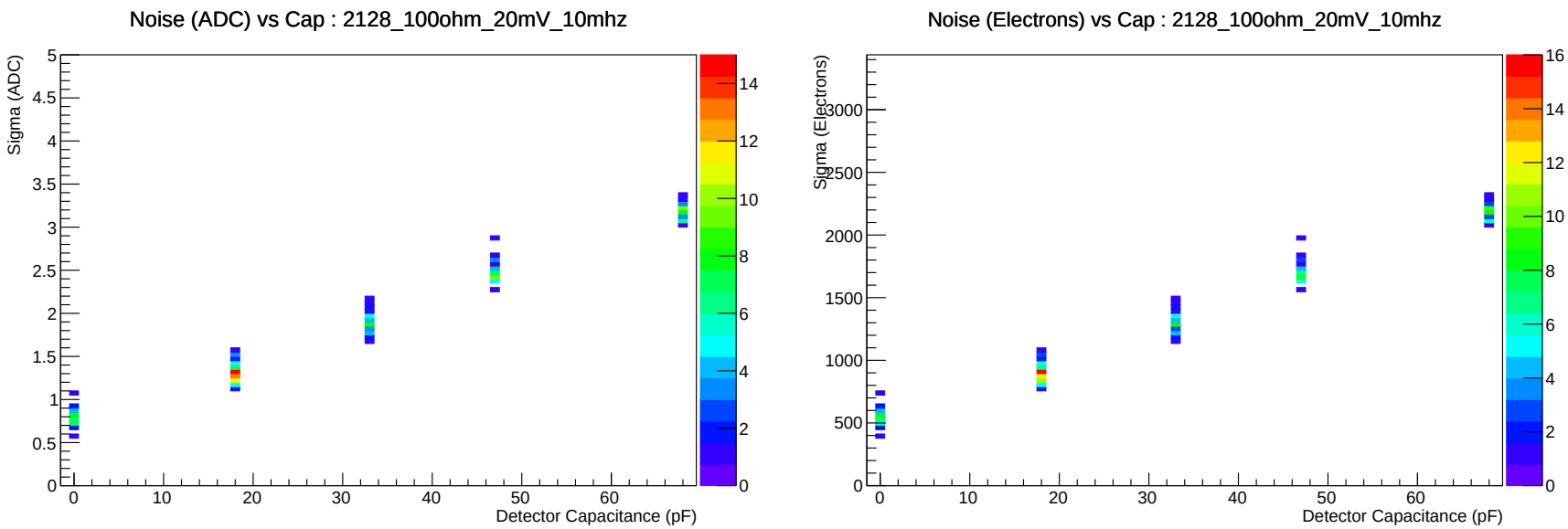


Figure 10: V3: with ADC units on the left, and electron equivalents/estimate on the right.

1.14 : V4 (chip #6115); Noise vs Capacitance (100 Ohm resistor)

(Already shown on Dec 7) One of 3 tested V4 chips : similar values as seen for V2 and V3

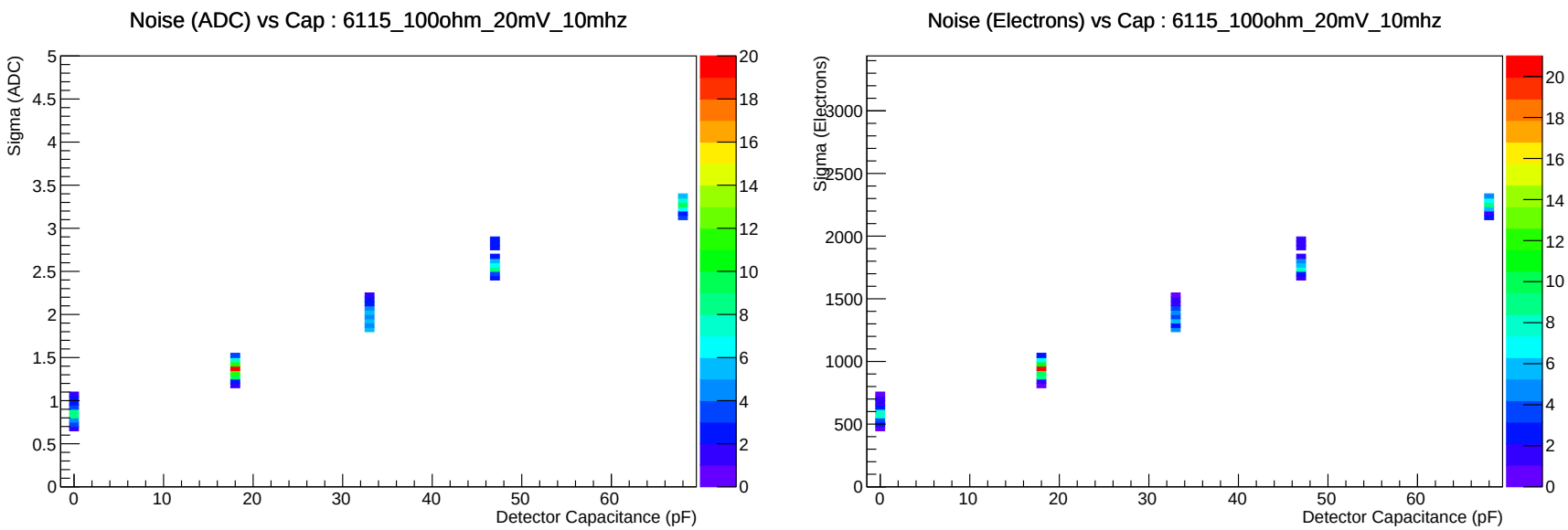


Figure 11: V4: with ADC units on the left, and electron equivalents/estimate on the right.

1.14 : V3 (chip #2128); Noise vs Resistor (0 or 18 pF capacitance)

(Already shown on Dec 7) One of 3 tested V3 chips : similar values as seen for V2

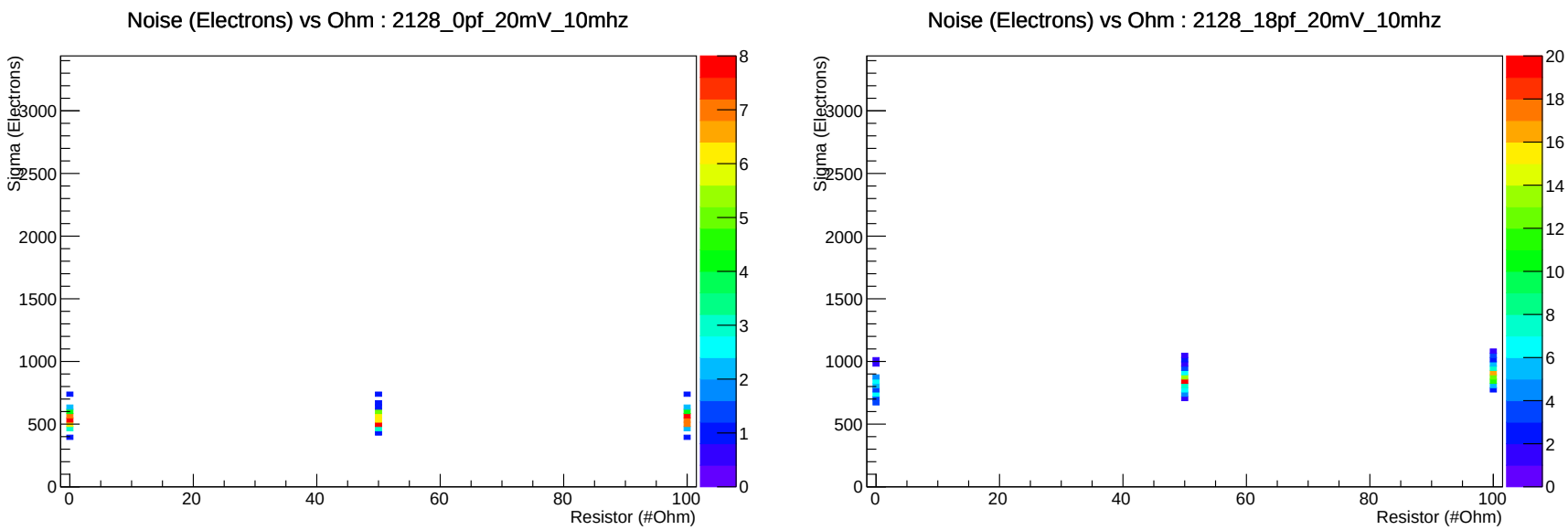


Figure 12: V3: 0 pF on the left, 18 pF on the right.

1.14 V4 (chip #6115); Noise vs Resistor (0 or 18 pF capacitance)

(Already shown on Dec 7) One of 3 tested V4 chips : similar values as seen for V2 and V3

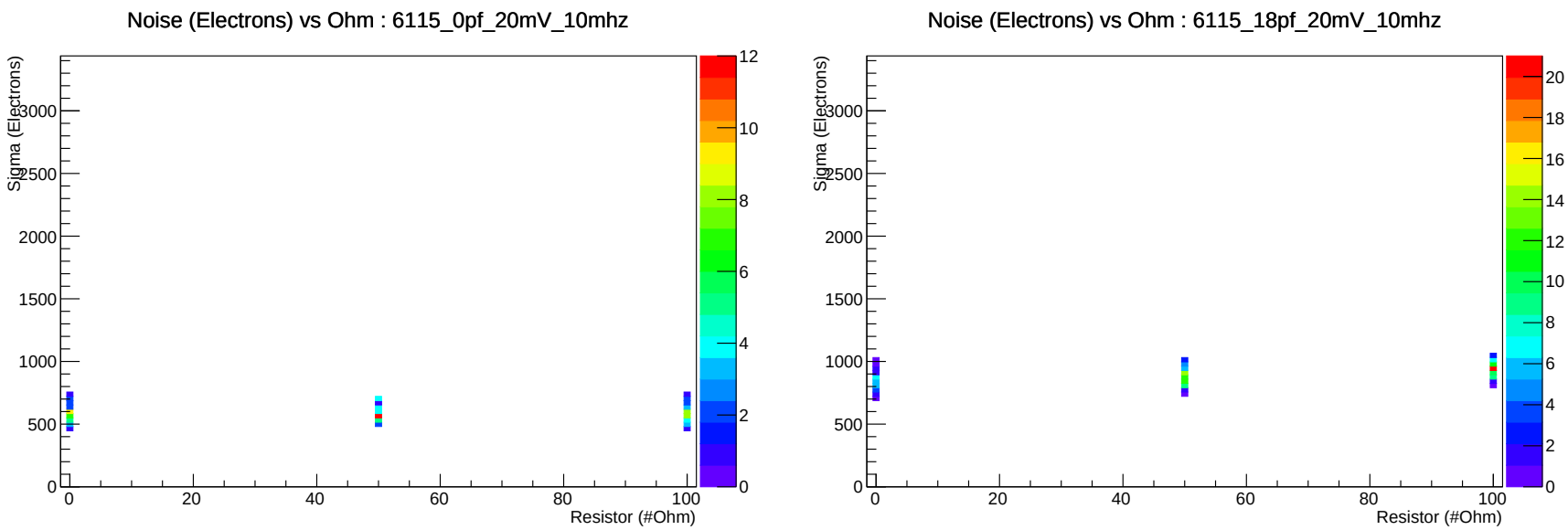


Figure 13: V4: 0 pF on the left, 18 pF on the right.

1.15 : V3; Crosstalk - pulsing Even channels

Pulsing Even channels, looking at Odd channels - see e.g. Aug 18, 2016 presentation at SAMPA meeting for more info on procedure.

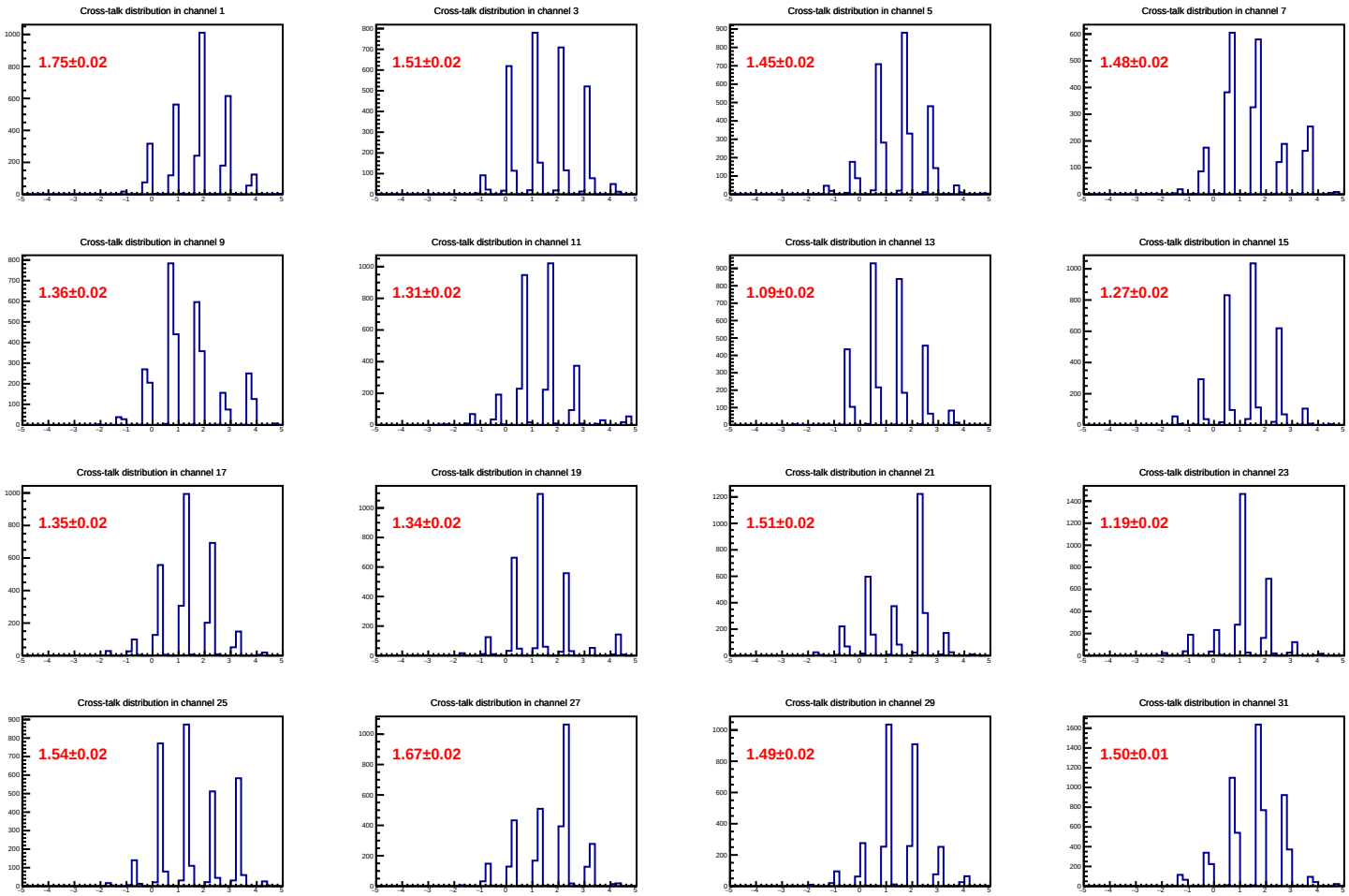


Figure 14: V3 Crosstalk

More plots in backup section, for V2, and pulsing Odd Channels.

1.15 : V4; Crosstalk - pulsing Even channels

Pulsing Odd channels, looking at Even channels

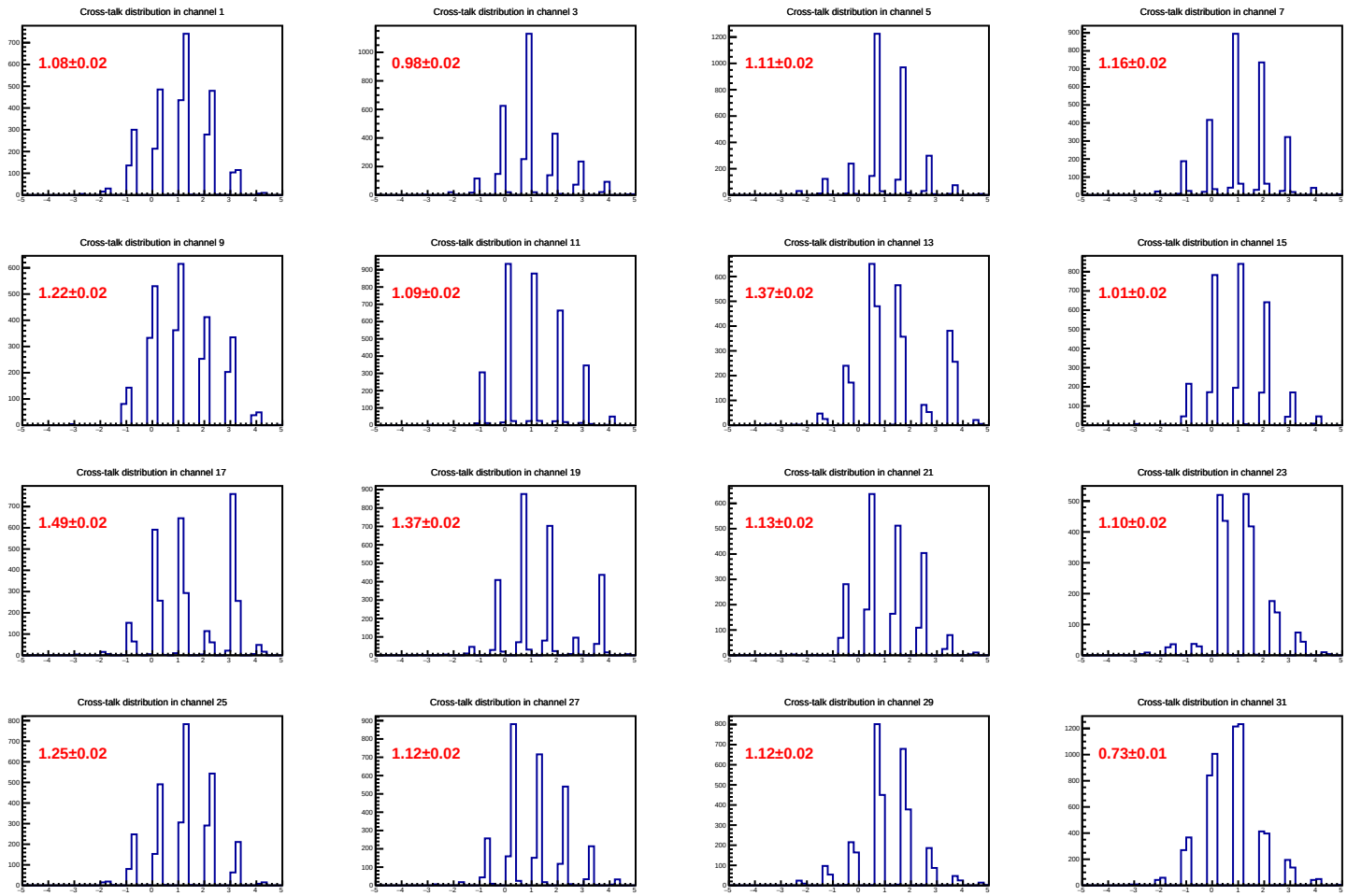


Figure 15: V4 Crosstalk

1.16 - 1.17 : Gain variation vs Capacitance and Resistor values

Channels for 3 V3 and 3 V4 chips plotted together; as usual here, 20 mV/fC settings used.

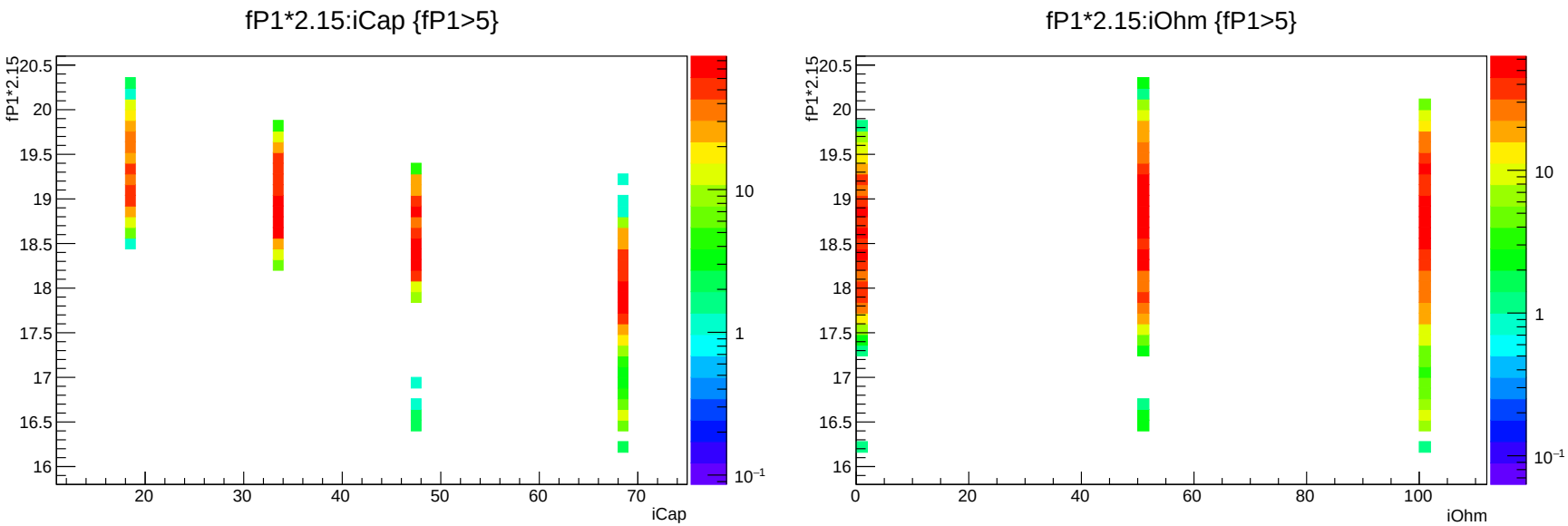


Figure 16: Gain vs Capacitance (left), and Resistor value (right).

Some reduction for larger detector capacitance, not much change vs resistor values.

1.16 - 1.17 : Gain V2 vs V3, many chips, 1D

Comparing channels for many V2 and V3 chips, 20 mV/fC settings (0 Ohm, 0 pF): V2 on the left, V3 on the right.

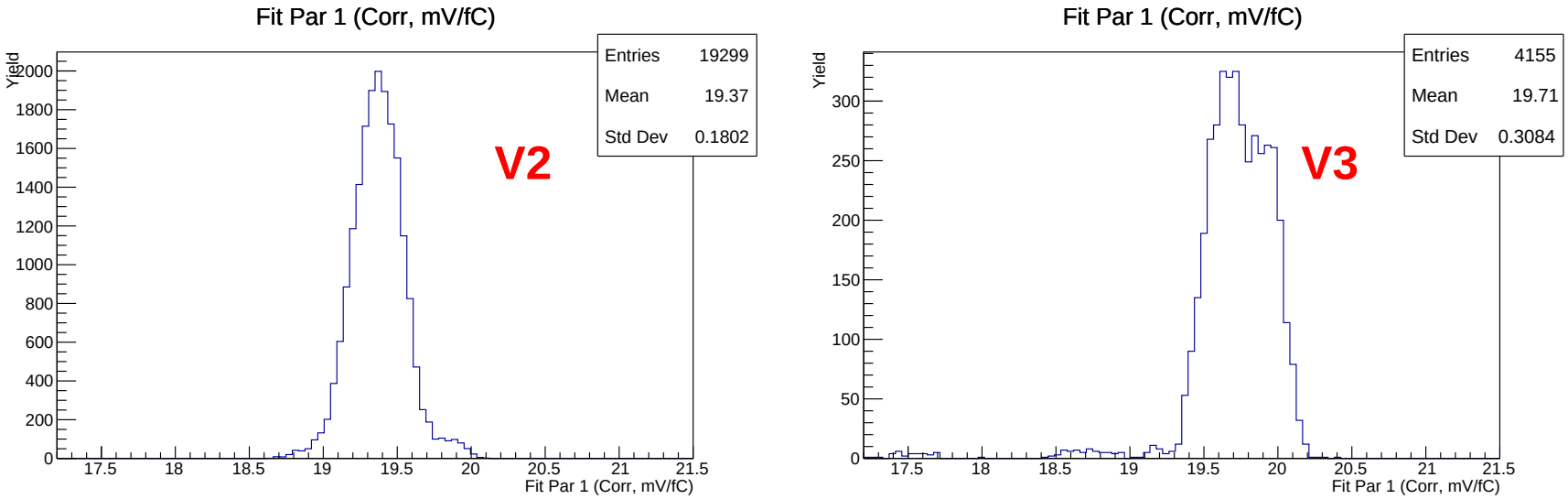


Figure 17: V2 on the left, V3 on the right.

1.16 - 1.17 : Gain V3 vs V4, many chips, 1D

Comparing channels for many V3 and V4 chips, 20 mV/fC settings: V3 on the left, V4 on the right.

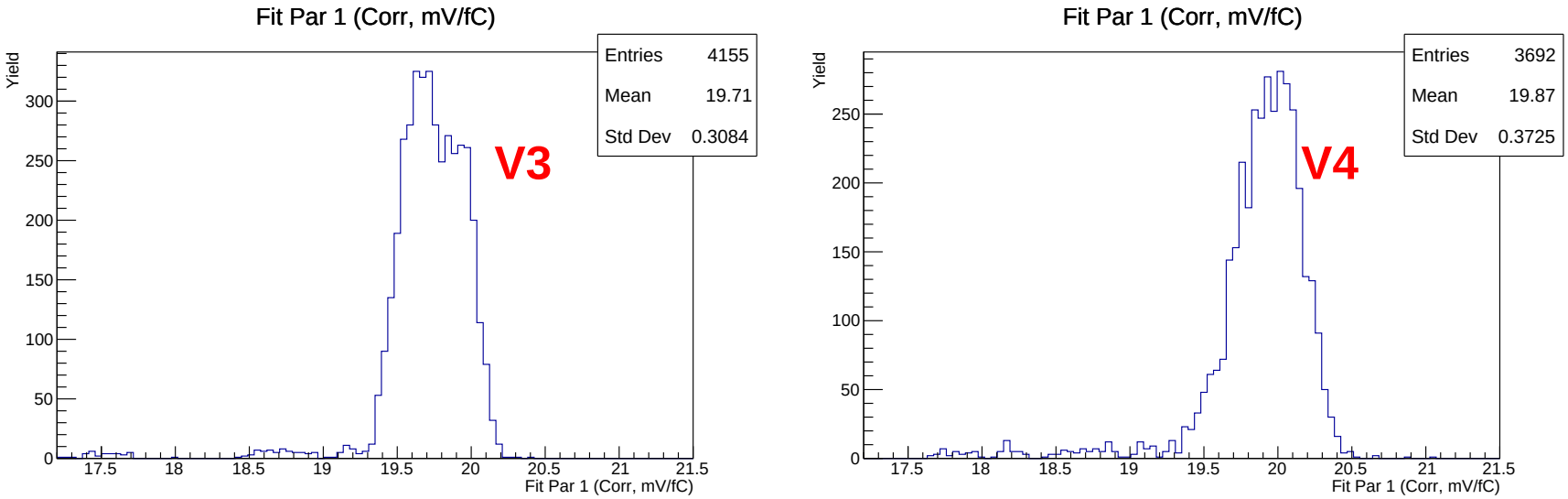


Figure 18: V3 on the left, V4 on the right.

1.16 - 1.17 : Gain V2 vs V3, many chips, 2D

Comparing channels for many V2 and V3 chips, 20 mV/fC settings: V2 on the left, V4 on the right.

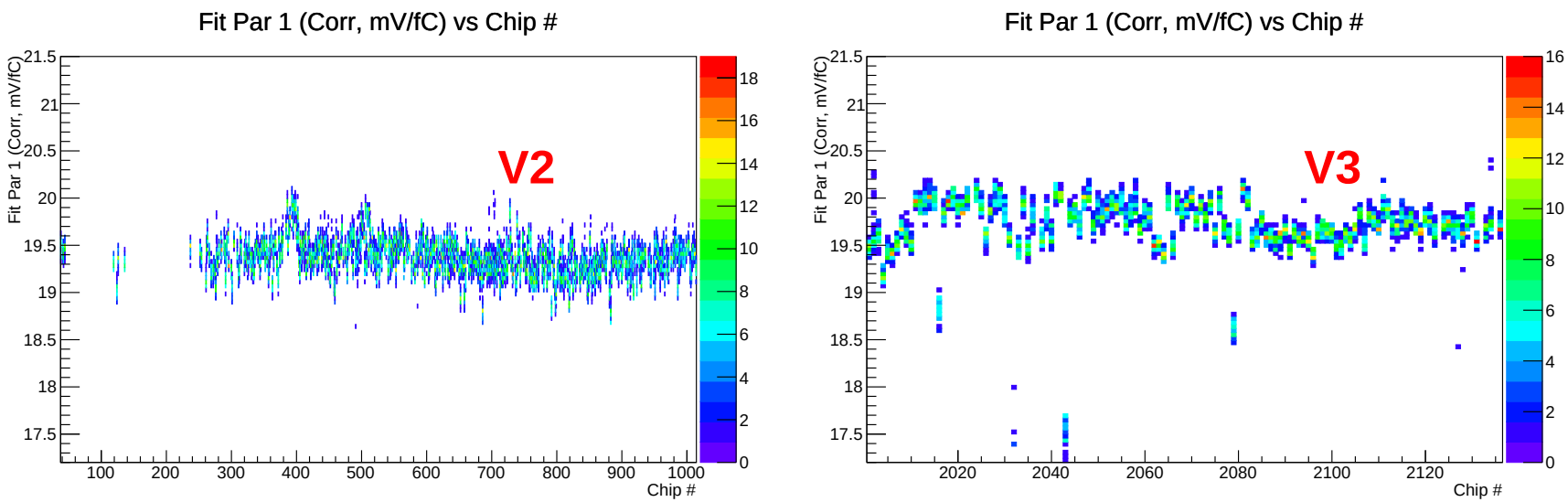


Figure 19: V2 on the left, V3 on the right.

1.16 - 1.17 : Gain V3 vs V4, many chips, 2D

Comparing channels for many V3 and V4 chips, 20 mV/fC settings: V3 on the left, V4 on the right.

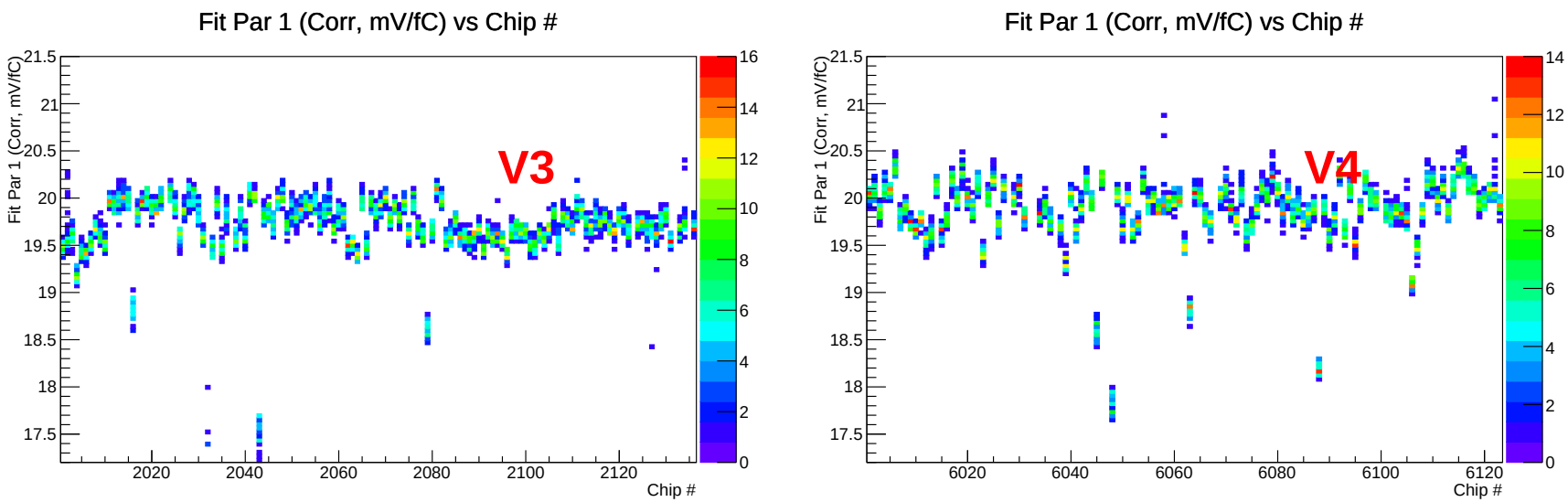


Figure 20: V3 on the left, V4 on the right.

21 : Pulse shape snapshot, V3 and V4

New procedure from Anders with several pulses in the same sweep, rather than many sweeps (events) in the procedure used for V2 studies. Faster, but need more delays between pulses for V3 to avoid pile-up/saturation issues(?).

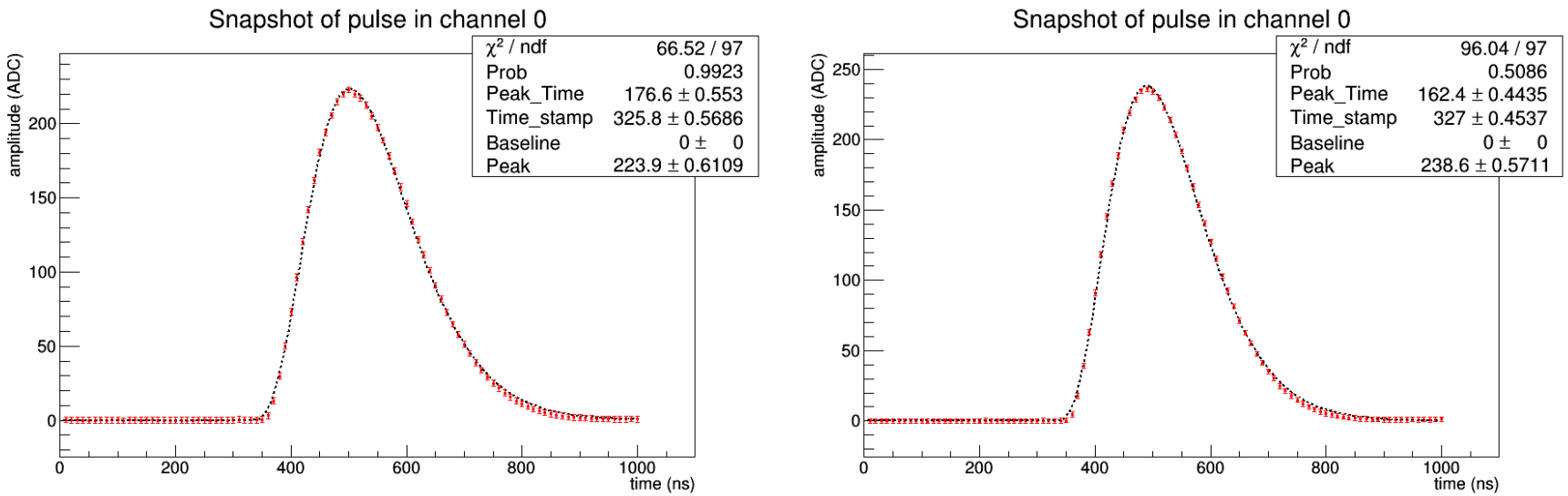


Figure 21: V3 on the left, V4 on the right.

Here we see Pulse shape snapshots for channel 0 for two chips.

21 : Pulse shape, V3 and V4

Here we plot the fitted rise times for all 32 channels in a chip together.

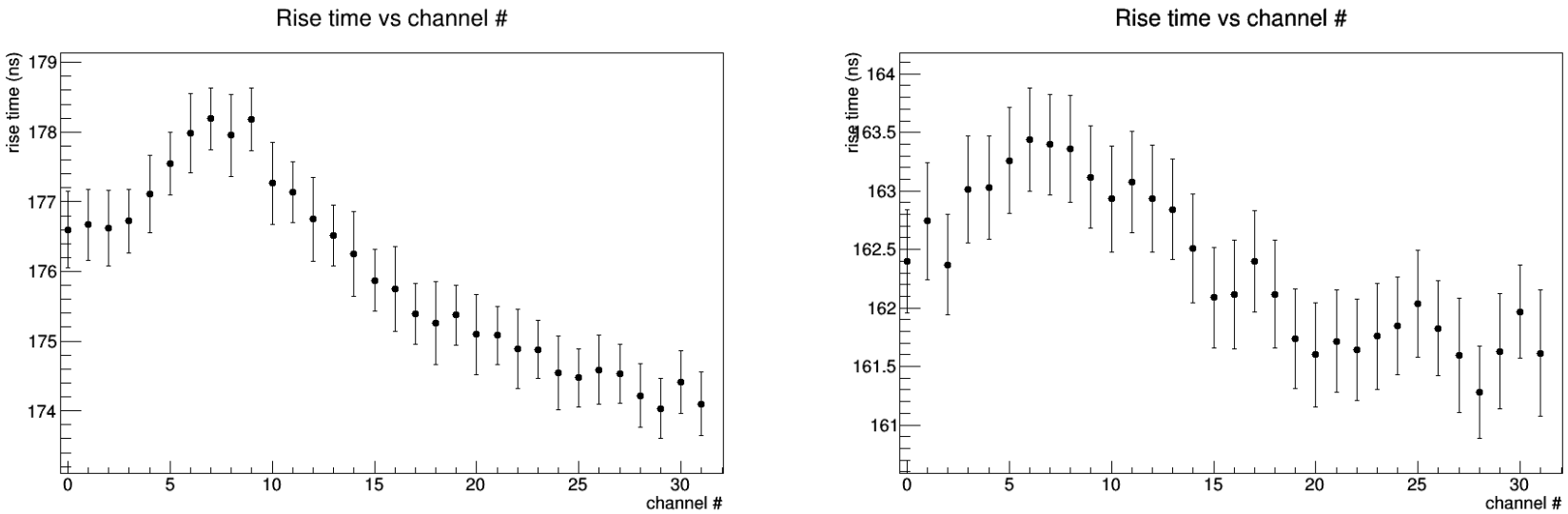


Figure 22: V3 on the left, V4 on the right.

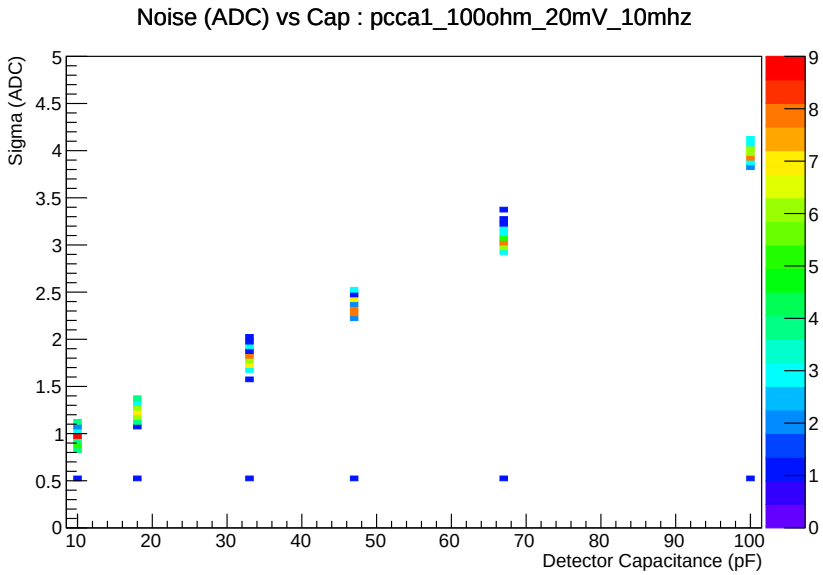
Interesting shape: channel-to-channel variations OK?

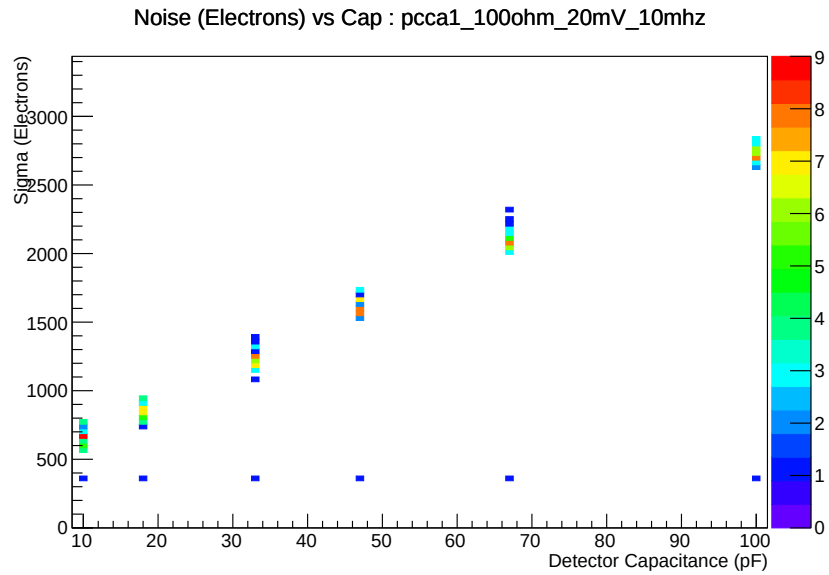
Summary / Outlook

- 1.4: Bandgap voltages, V750 et al, many chips - OK
- 1.13: Baseline info vs chan, many chips - OK
- 1.14: Baseline noise at 0 pF and 0 Ohm, many chips - $\sim$ OK
- 1.14: Baseline noise, variation with capacitance and resistor values, few chips - $\sim$ OK
- 1.15: Crosstalk check, few chips - *somewhat worse for V3 and V4 than for V2...*
- 1.16-1.17: Gain variation with capacitance and resistor values, few chips - OK
- 1.16-1.17, 16: Gain at 0 pF and 0 Ohm, many chips - OK
- 21: Pulse shape, with varying delay between test pulse and sampling clock - *channel-to-channel variations OK?...*

MPW2 = V2; Noise vs Capacitance (100 Ohm resistor) 29

First, a reminder for MPW2: we measure the sigma value in ADC and can convert that to an estimate of # of electrons, equivalent:

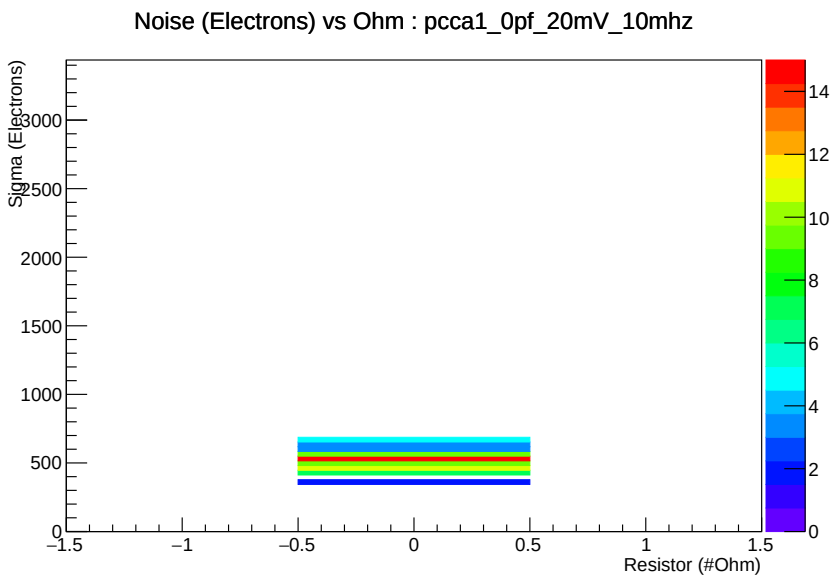


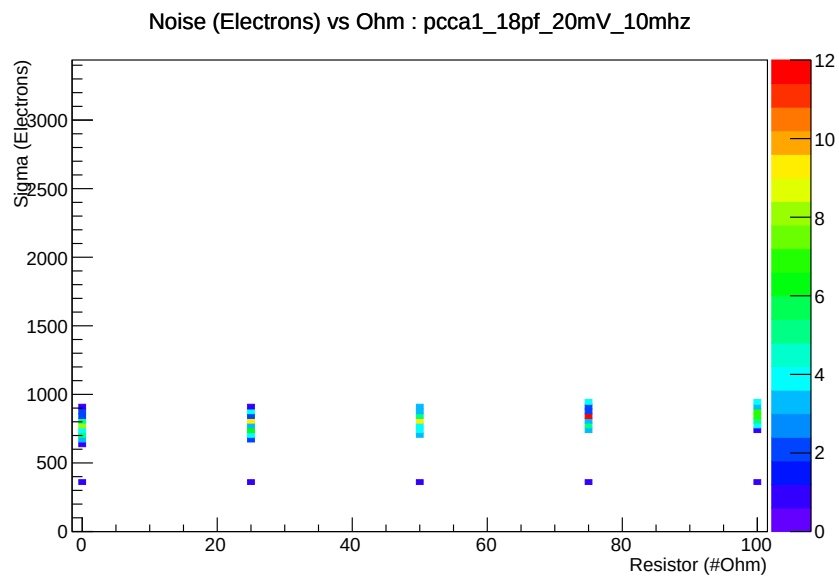


Show the values for all 32 channels in a chip. This V2 chip had one channel broken/unconnected.

MPW2 = V2; Noise vs Resistor value (for 0 pF and 18pF))

Next, let's also look at noise vs resistor value, for 2 different cap values (only show noise in electron equivalents) .

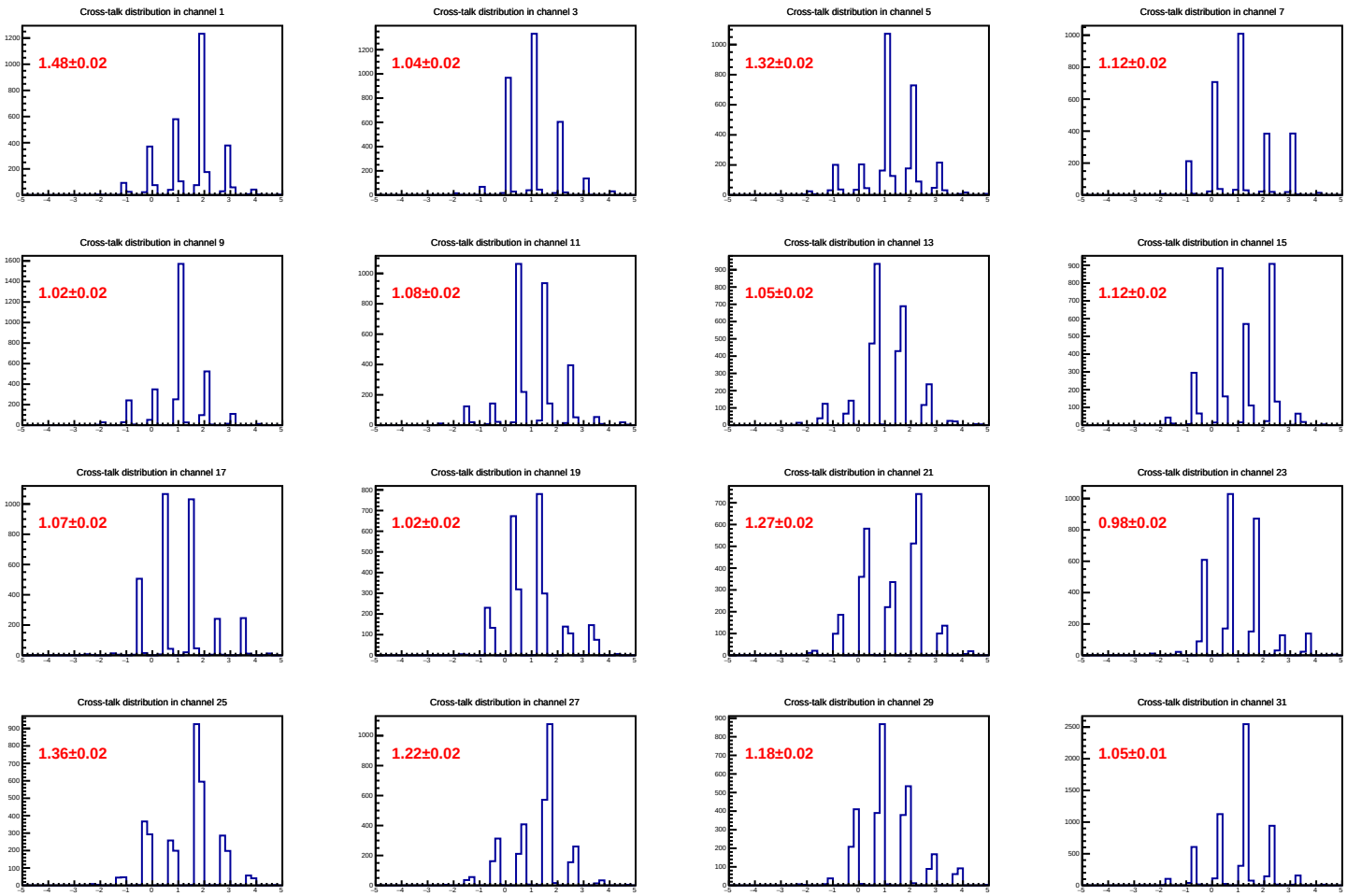




As expected, see differences between 0 pF vs 18 pF (scale in left vs right plot), but not much variation with resistor values (within right plot, perhaps ∼10% increase from 0 Ohm to 100 Ohm).

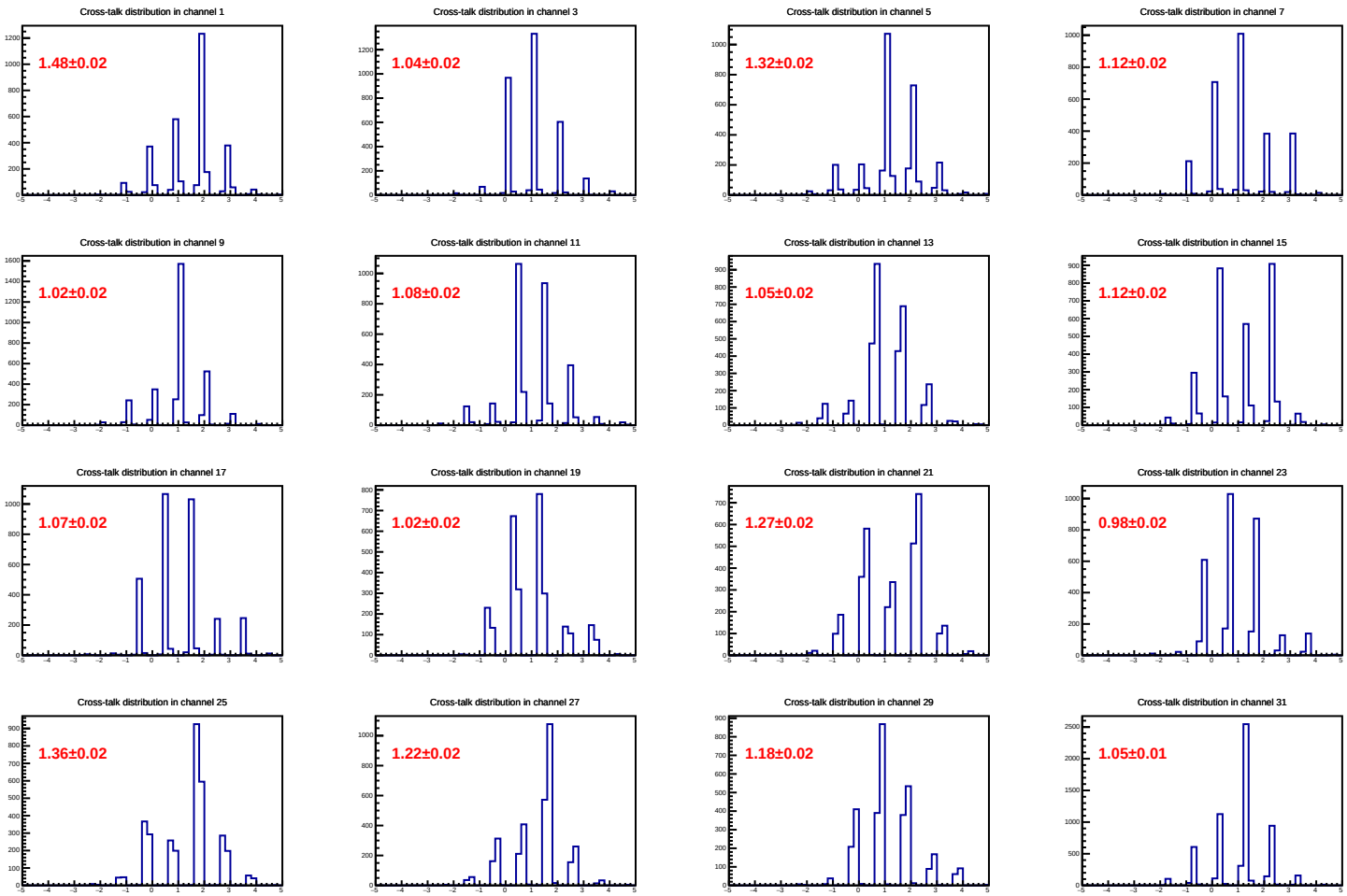
1.15 : V2; Crosstalk - pulsing Even channels

Pulsing Even channels, looking at Odd channels



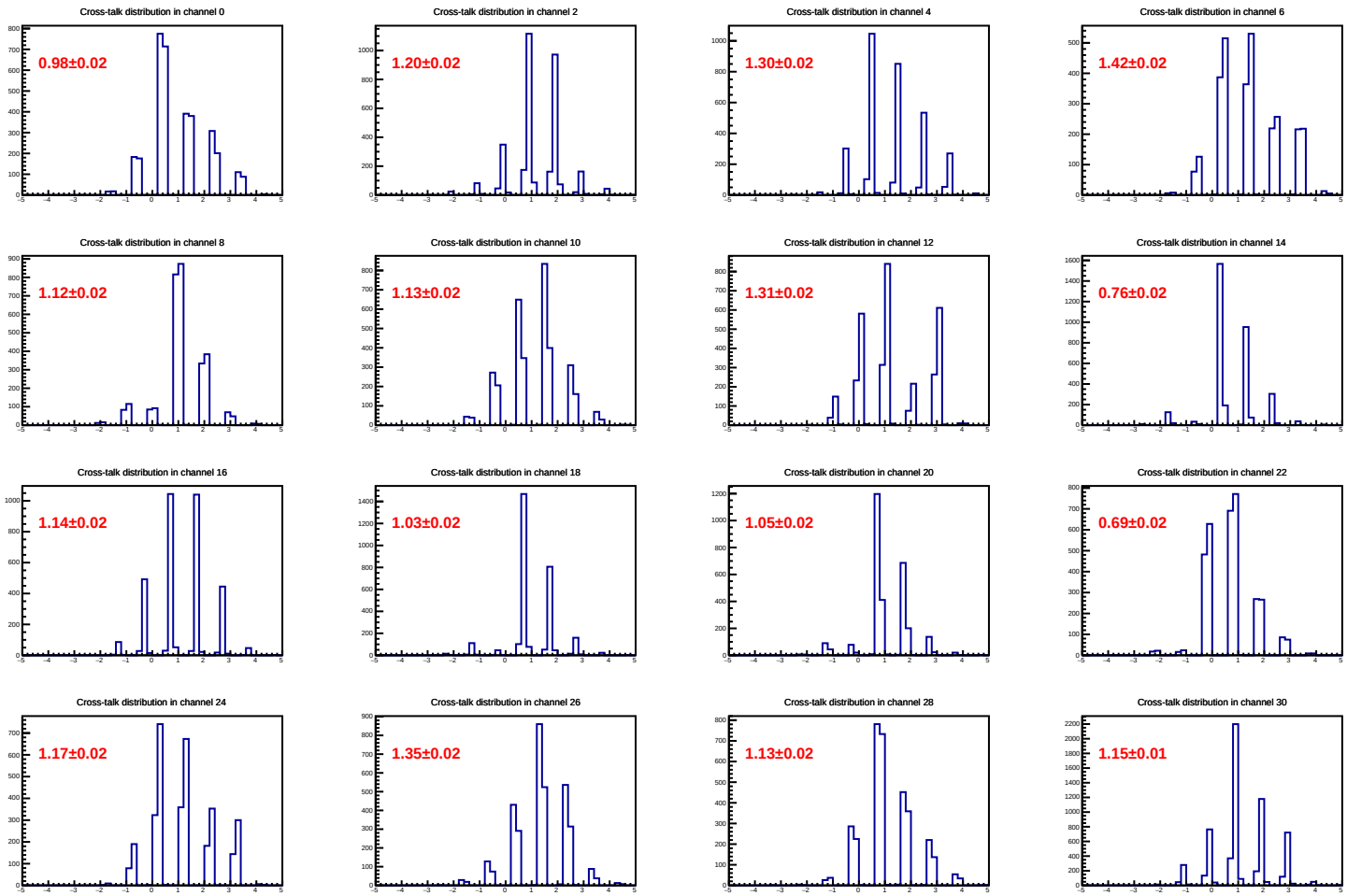
1.15 : V2; Crosstalk - pulsing Odd channels

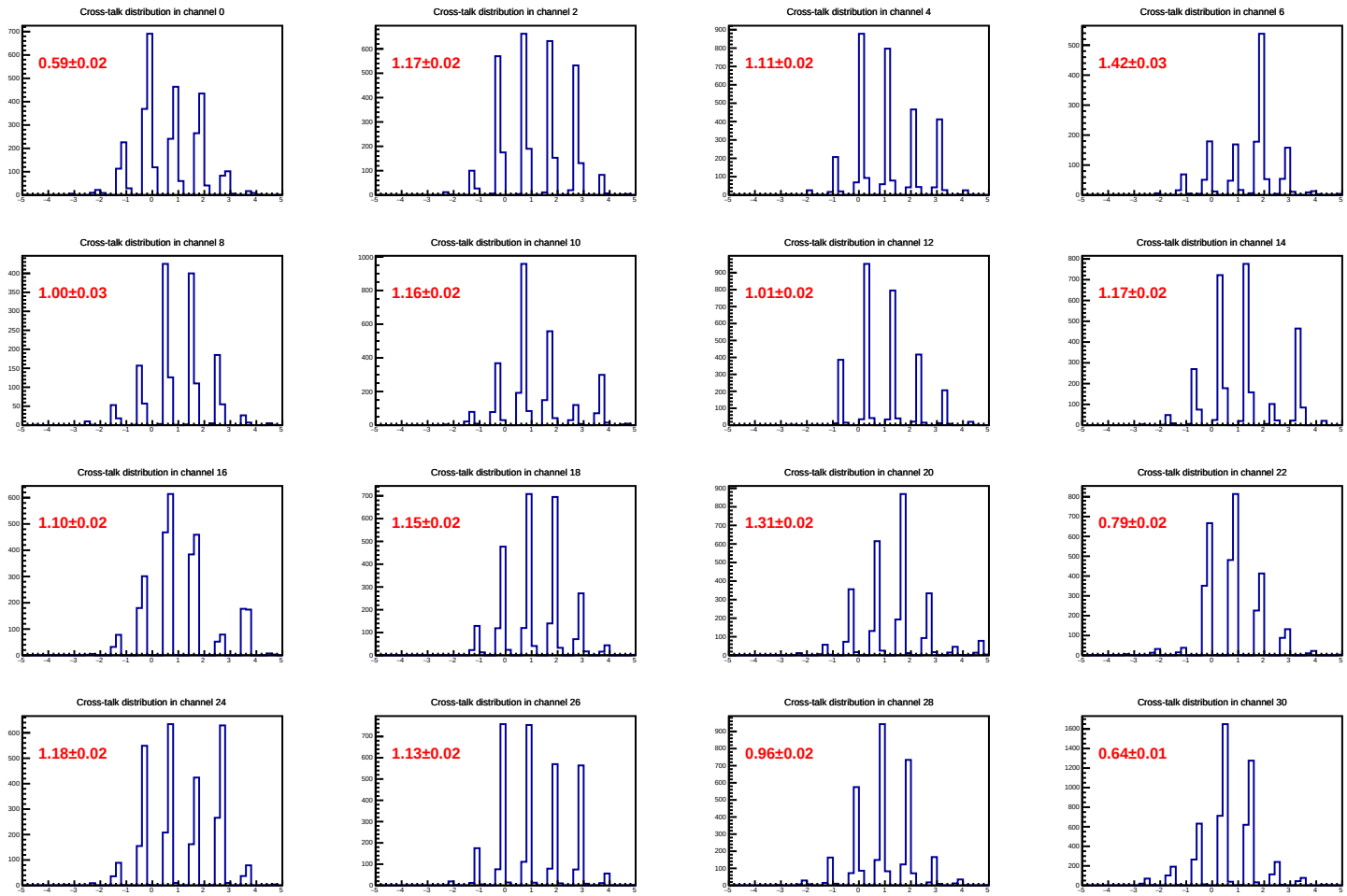
Pulsing Odd channels, looking at Even channels



1.15 : V3; Crosstalk - pulsing Odd channels

Pulsing Odd channels, looking at Even channels



1.15 : V4; Crosstalk - pulsing Odd channels

Pulsing Odd channels, looking at Even channels