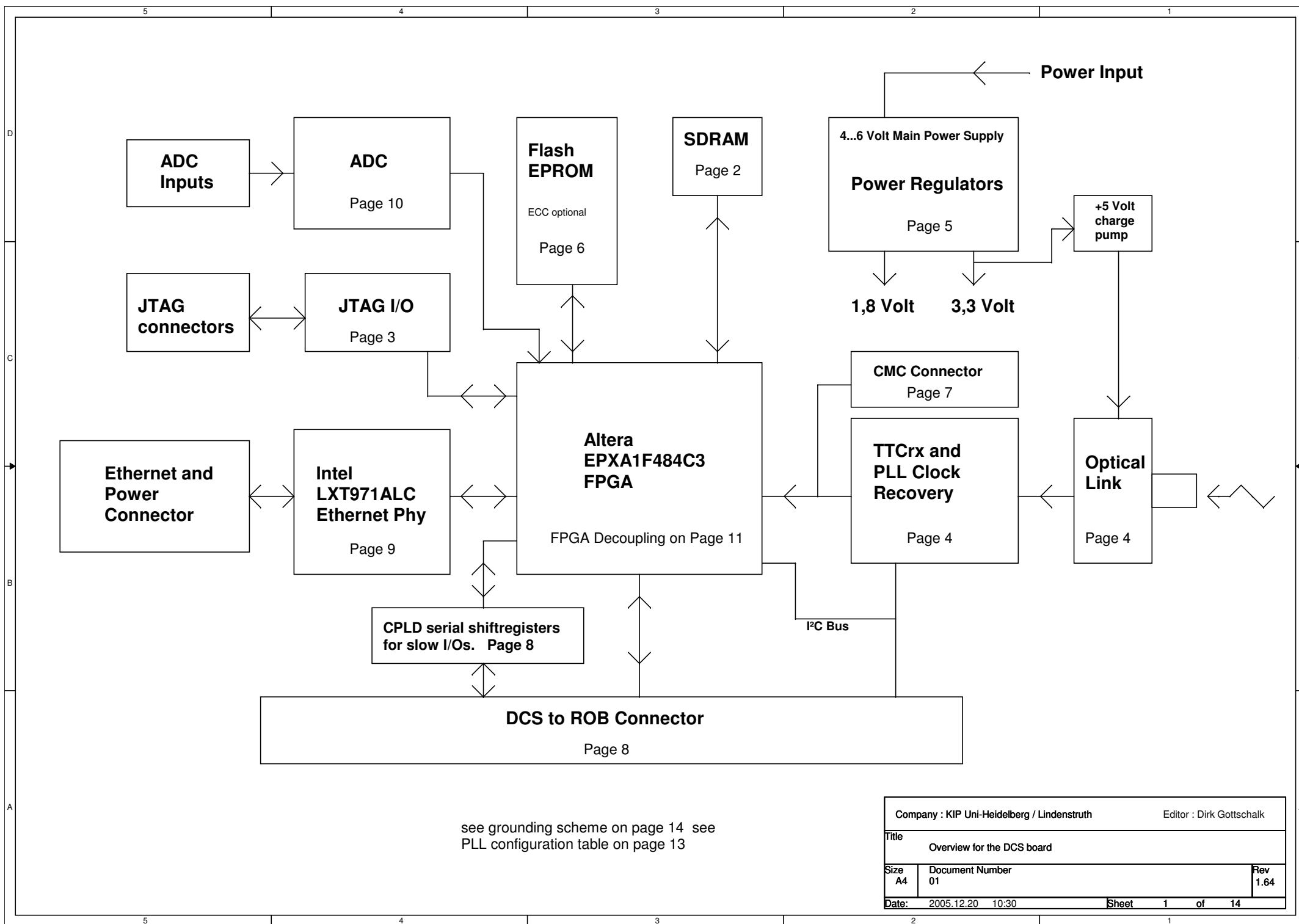
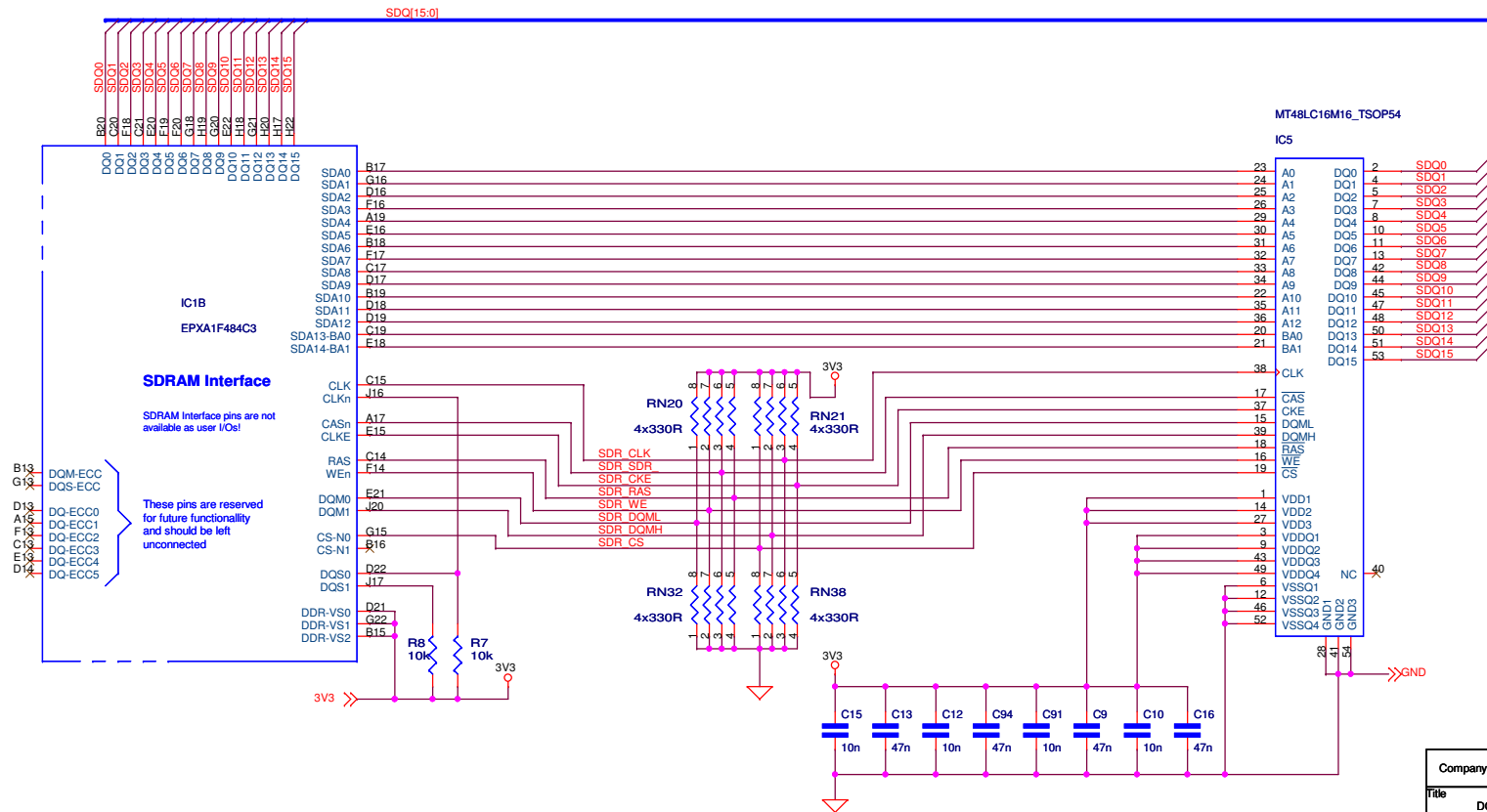




|                                             |                  |  |                          |   |       |
|---------------------------------------------|------------------|--|--------------------------|---|-------|
| Company : KIP Uni-Heidelberg / Lindenstruth |                  |  | Editor : Dirk Gottschalk |   |       |
| Title                                       |                  |  |                          |   |       |
| Overview for the DCS board                  |                  |  |                          |   |       |
| Size                                        | Document Number  |  |                          |   | Rev   |
| A4                                          | 01               |  |                          |   | 1.64  |
| Date:                                       | 2005.12.20 10:30 |  | Sheet                    | 1 | of 14 |



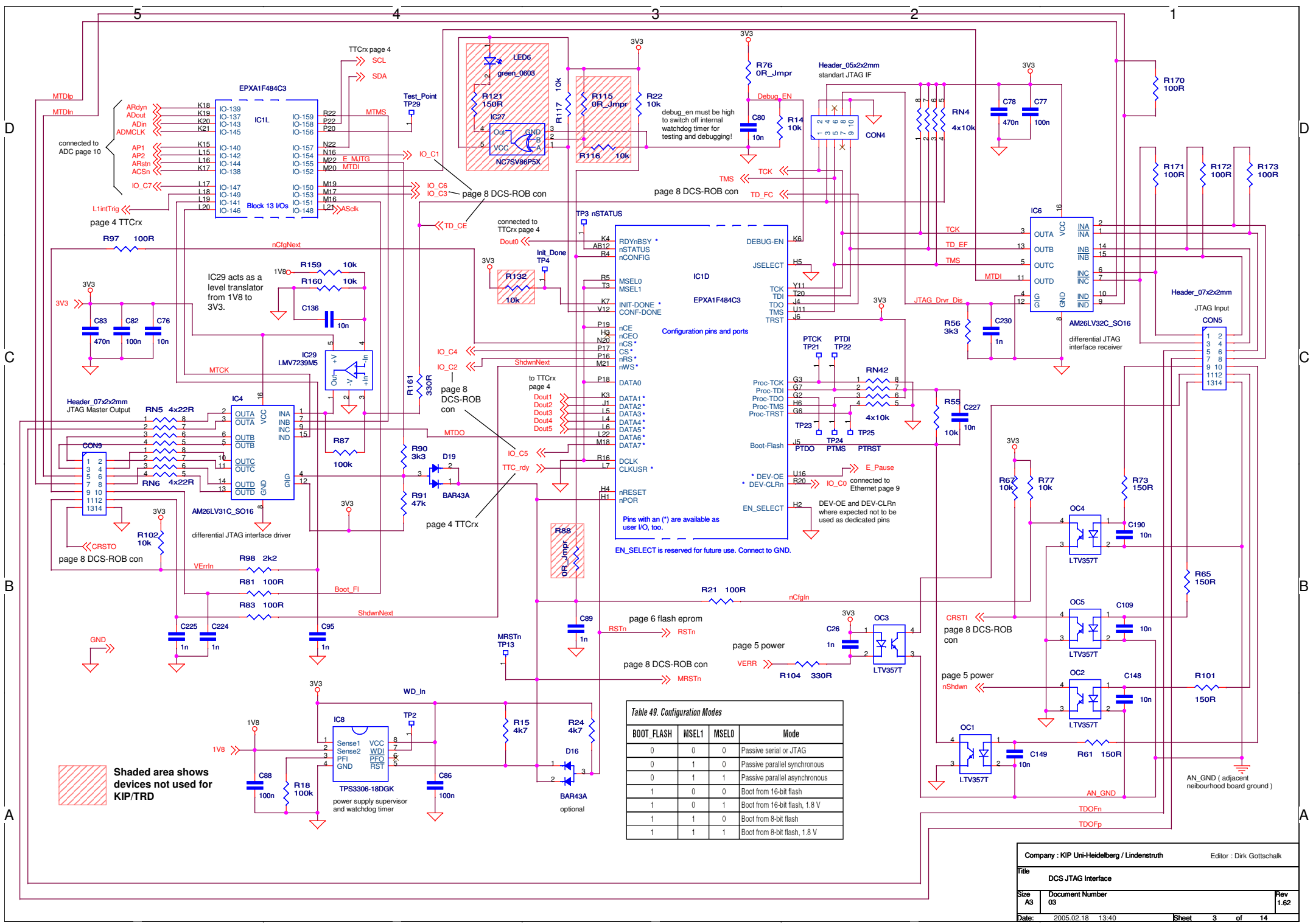


Table 49. Configuration Modes

| BOOT_FLASH | MSEL1 | MSEL0 | Mode                          |
|------------|-------|-------|-------------------------------|
| 0          | 0     | 0     | Passive serial or JTAG        |
| 0          | 1     | 0     | Passive parallel synchronous  |
| 0          | 1     | 1     | Passive parallel asynchronous |
| 1          | 0     | 0     | Boot from 16-bit flash        |
| 1          | 0     | 1     | Boot from 16-bit flash, 1.8 V |
| 1          | 1     | 0     | Boot from 8-bit flash         |
| 1          | 1     | 1     | Boot from 8-bit flash, 1.8 V  |

\*! keep this GND connection near/between TTCrx and IC28 !

Please see grounding scheme for PLL layout on page 12.

PLL frequency is defined by resistors R68, R99, R100, R105 and R107 to R110. If the voltage regulator shutdown feature is not needed the CPLD can configure the PLL via RN48 which otherwise is not populated.

Voltage regulator IC28 only used if low supply noise for PLL required.

connect capacitors C44, C50 and C56 as close as possible to PLL IC23!

Keep these signals as short as possible!

TPC PLL configuration table see page 13 !

TTCrx can shift Clock40Desn phase in 104ps steps between 0 and 25ns.

Shaded area shows devices not used for KIP/DCS

| Pin | HFBR-2316T | TRR-1B43 |
|-----|------------|----------|
| 2   | Out        | Outn     |
| 3   | VEE/GND    | Outp     |
| 6   | VCC        | GND      |
| 7   | GND        | VCC      |

AUX connector page 7

IC1H

EPXA1F484C3

Block 9 I/Os

|        |        |    |        |
|--------|--------|----|--------|
| BCnt0  | BCnt0  | L7 | BCnt0  |
| BCnt1  | BCnt1  | M7 | BCnt1  |
| BCnt2  | BCnt2  | G7 | BCnt2  |
| BCnt3  | BCnt3  | K6 | BCnt3  |
| BCnt4  | BCnt4  | M6 | BCnt4  |
| BCnt5  | BCnt5  | L6 | BCnt5  |
| BCnt6  | BCnt6  | J6 | BCnt6  |
| BCnt7  | BCnt7  | J5 | BCnt7  |
| BCnt8  | BCnt8  | L5 | BCnt8  |
| BCnt9  | BCnt9  | M5 | BCnt9  |
| BCnt10 | BCnt10 | L4 | BCnt10 |
| BCnt11 | BCnt11 | H6 | BCnt11 |

|           |           |     |           |
|-----------|-----------|-----|-----------|
| EvCntHStr | EvCntHStr | J7  | EvCntHStr |
| EvCntLStr | EvCntLStr | K8  | EvCntLStr |
| BCntStrb  | BCntStrb  | L8  | BCntStrb  |
| Brst2     | Brst2     | D12 | Brst2     |
| Brst3     | Brst3     | D11 | Brst3     |
| Brst4     | Brst4     | J11 | Brst4     |
| Brst5     | Brst5     | J10 | Brst5     |
| Brst6     | Brst6     | K11 | Brst6     |
| Brst7     | Brst7     | K9  | Brst7     |
| BrstStr1  | BrstStr1  | D10 | BrstStr1  |
| BrstStr2  | BrstStr2  | K12 | BrstStr2  |
| EvCntRes  | EvCntRes  | L9  | EvCntRes  |

|         |         |    |         |
|---------|---------|----|---------|
| BCntRes | BCntRes | M9 | BCntRes |
| AVDD0   | AVDD0   | G3 | AVDD0   |
| AVDD1   | AVDD1   | G2 | AVDD1   |
| AVDD2   | AVDD2   | G1 | AVDD2   |
| D_GND0  | D_GND0  | D6 | D_GND0  |
| D_GND1  | D_GND1  | D5 | D_GND1  |
| D_GND2  | D_GND2  | D4 | D_GND2  |
| D_GND3  | D_GND3  | D3 | D_GND3  |
| D_GND4  | D_GND4  | D2 | D_GND4  |
| D_GND5  | D_GND5  | D1 | D_GND5  |
| D_GND6  | D_GND6  | D0 | D_GND6  |
| D_GND7  | D_GND7  | D0 | D_GND7  |
| D_GND8  | D_GND8  | D0 | D_GND8  |
| D_GND9  | D_GND9  | D0 | D_GND9  |
| G_GND   | G_GND   | D0 | G_GND   |

ROB connector page 8

ROB connector page 8

ROB connector page 8

ROB connector page 8

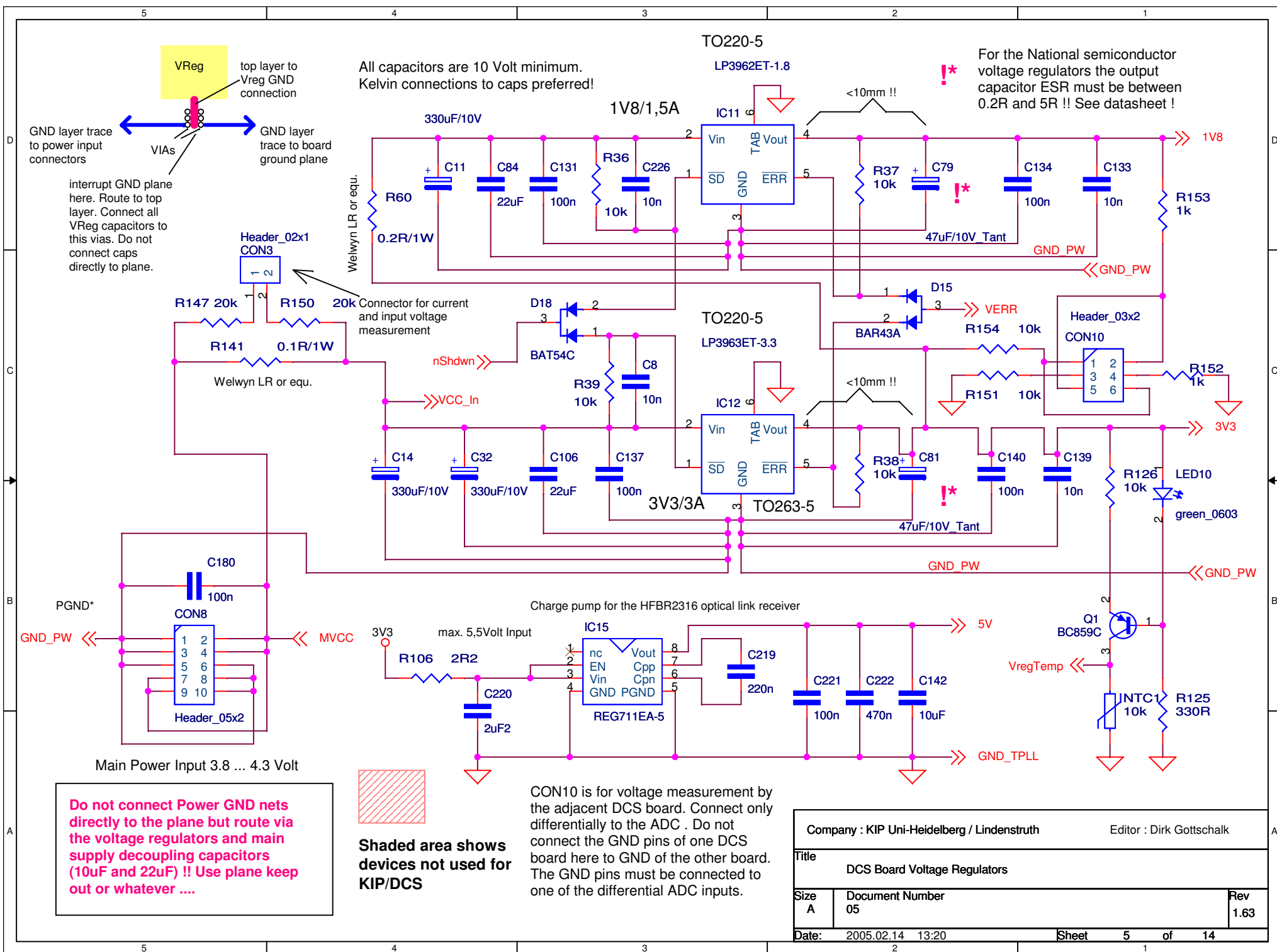
ROB connector page 8

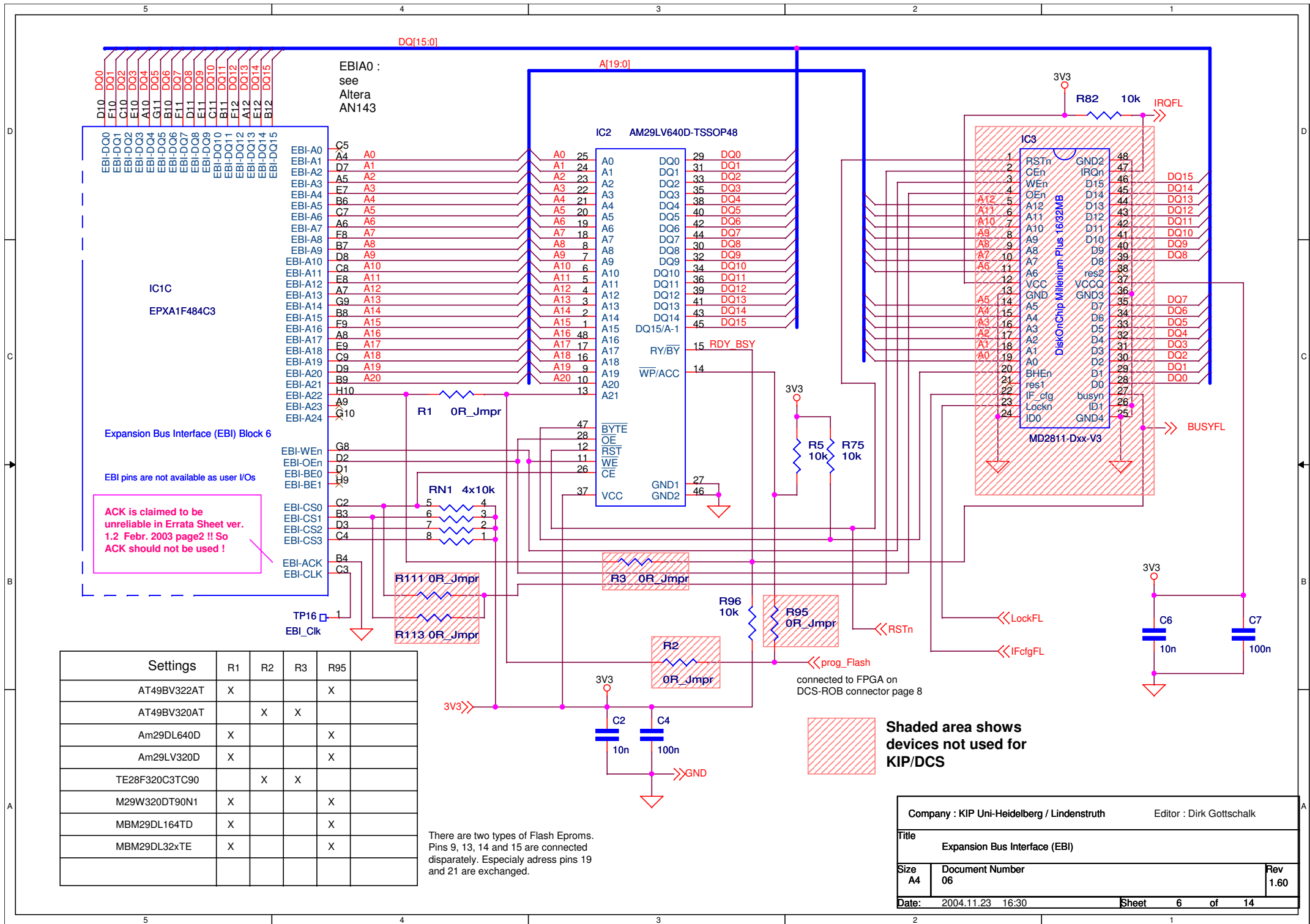
ROB connector page 8

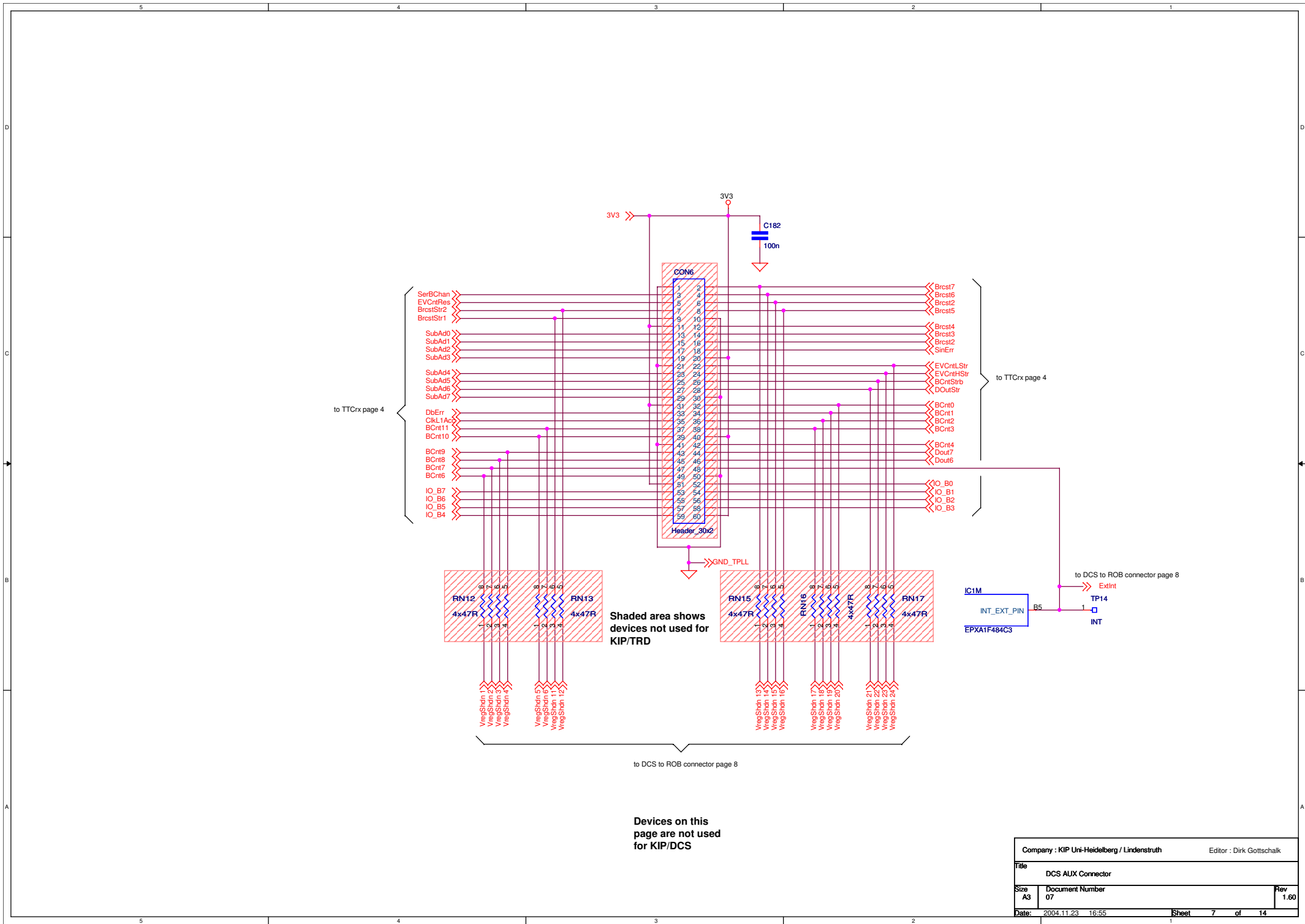
ROB connector page 8

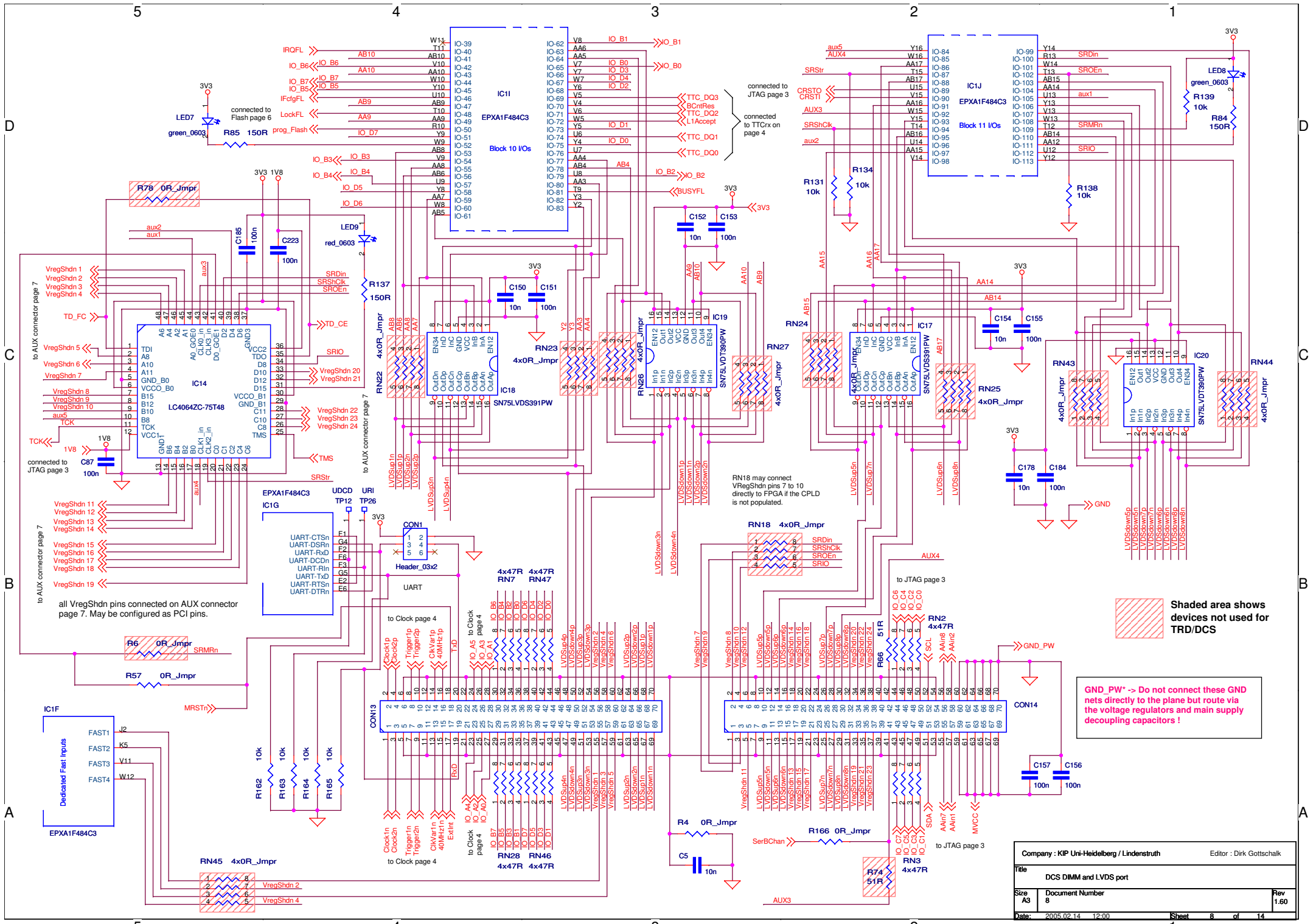
ROB connector page 8

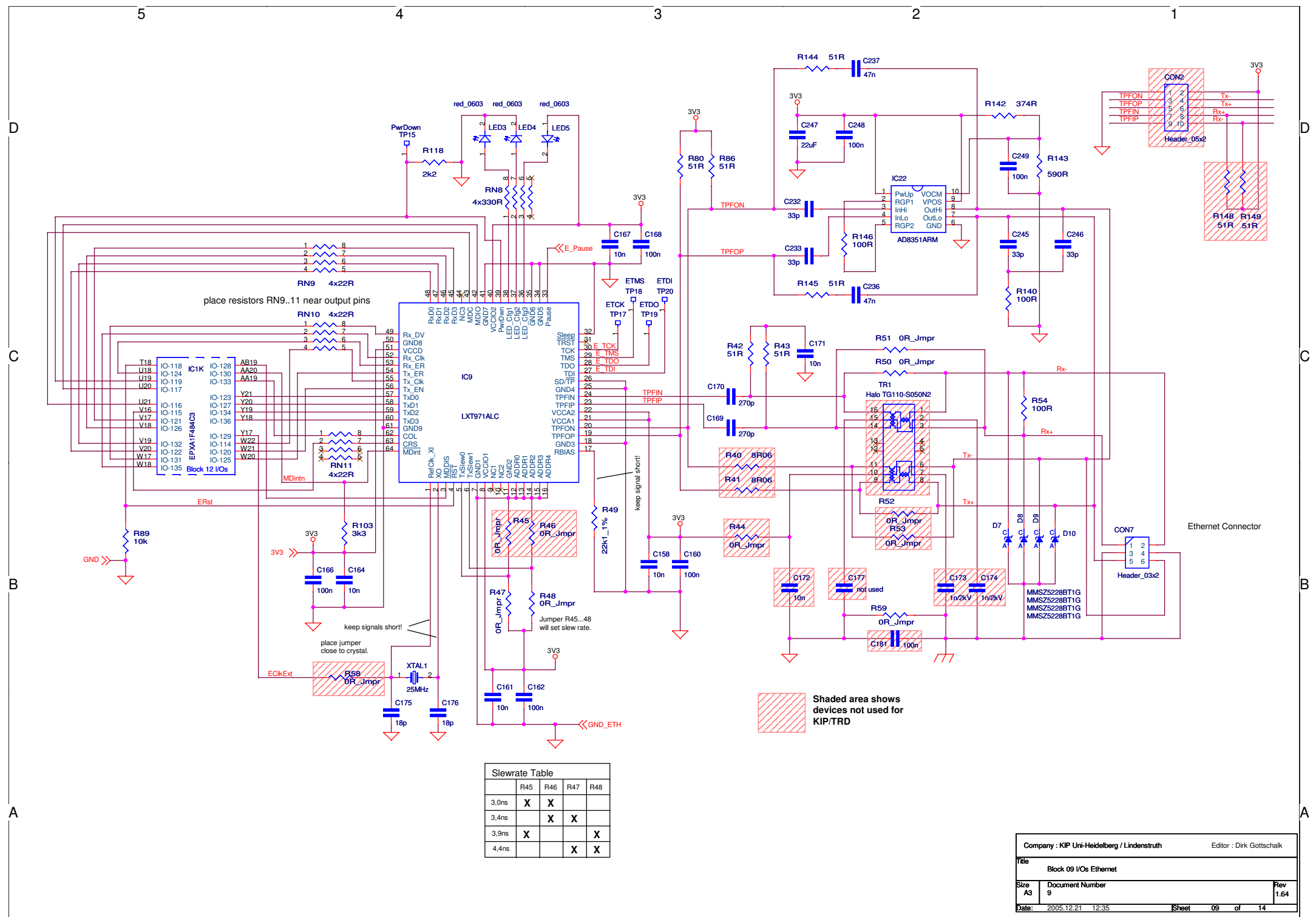
ROB connector page 8











shield signals AAin1 .. 4 with GND traces

To ROB connector page 8

keep all analog signals as short as possible

Place jumper R10 near to crystal. Keep trace short.

Populate R122 if AIN8 should measure voltage regulator temperature.

Keep this signals short!

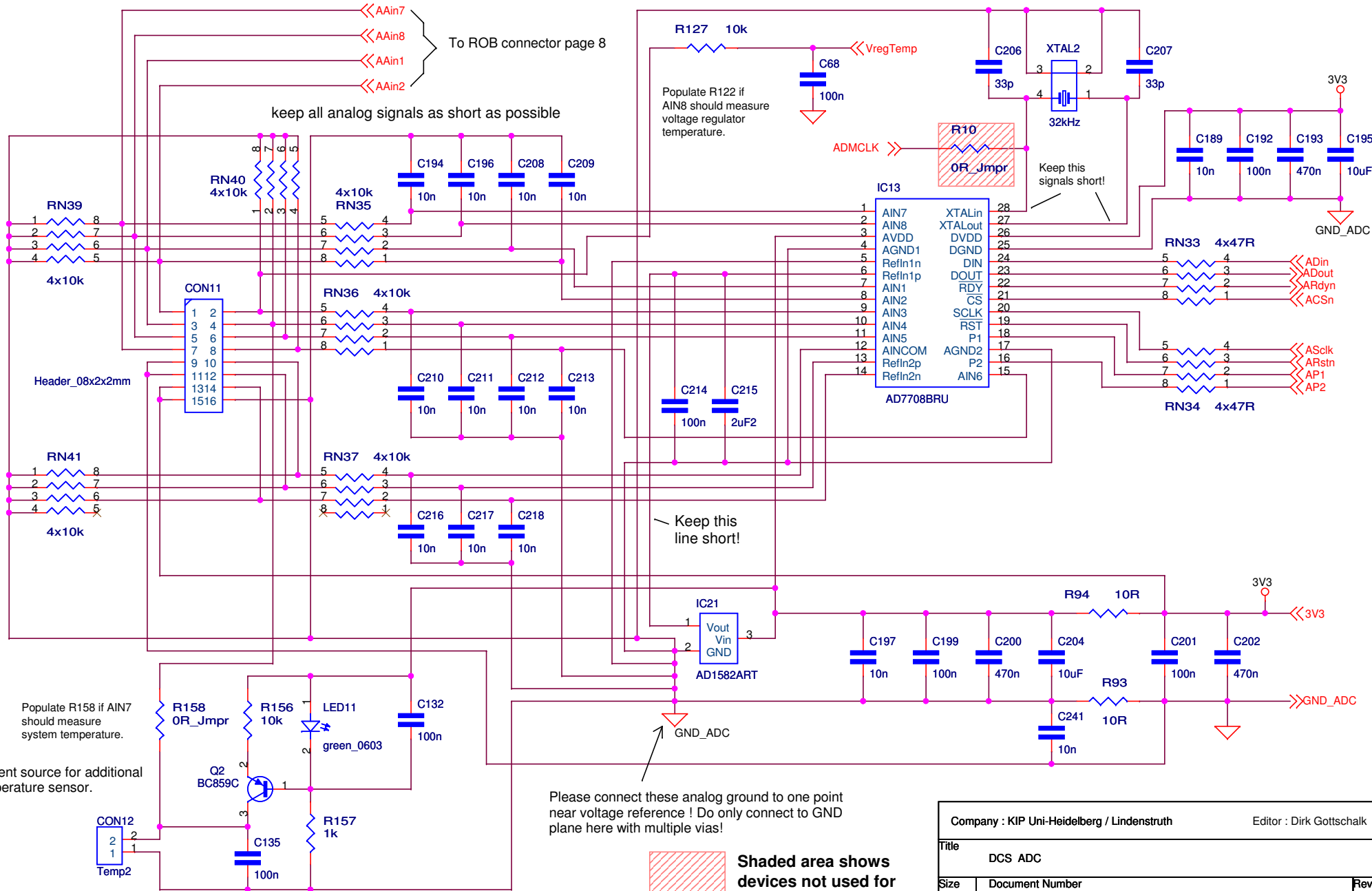
Keep this line short!

Populate R158 if AIN7 should measure system temperature.

Current source for additional temperature sensor.

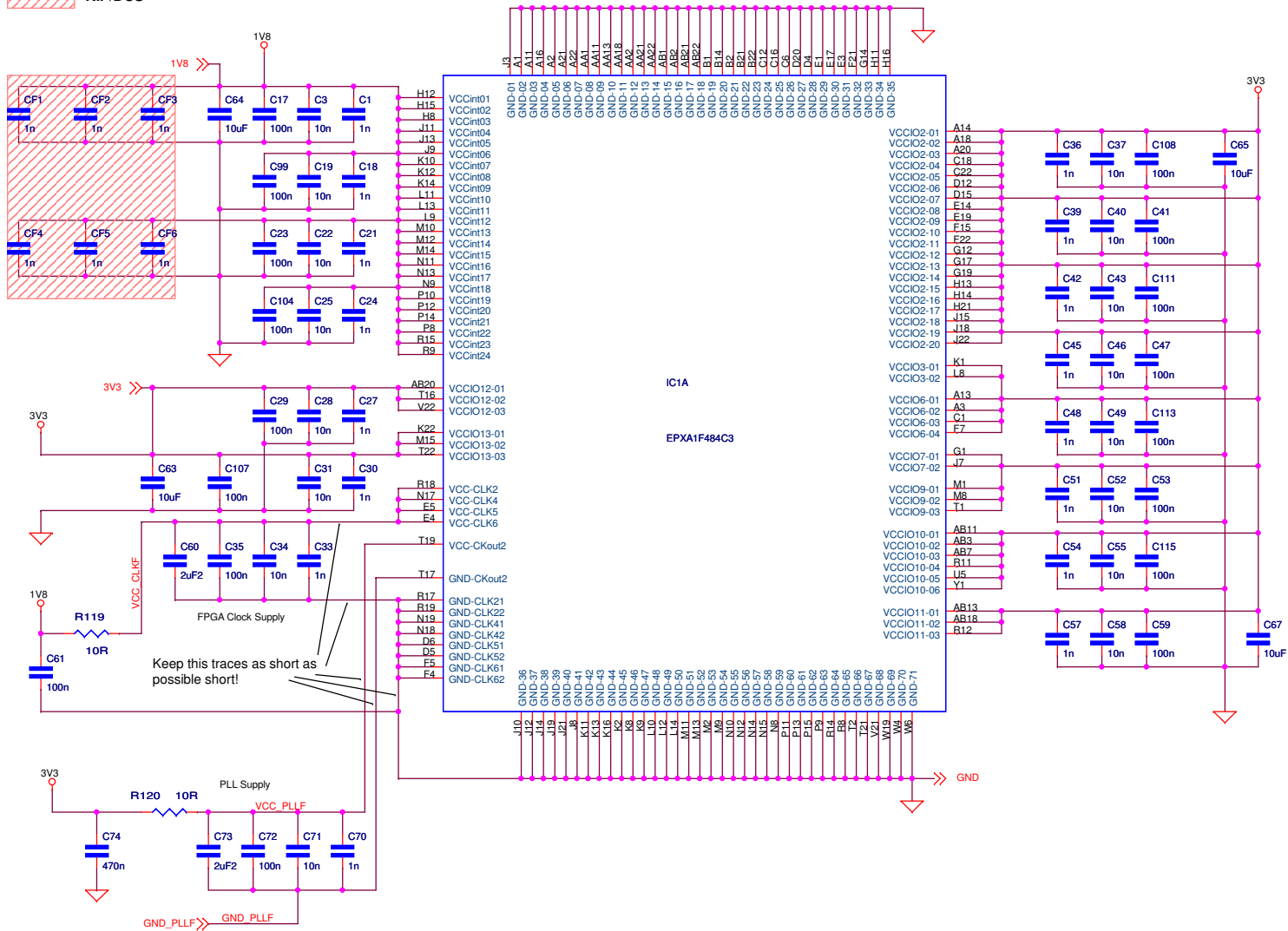
Please connect these analog ground to one point near voltage reference ! Do only connect to GND plane here with multiple vias!

Shaded area shows devices not used for KIP/DCS



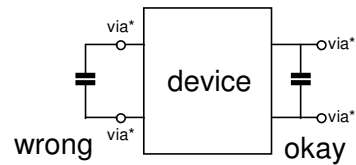
|                                             |                       |  |                          |       |             |
|---------------------------------------------|-----------------------|--|--------------------------|-------|-------------|
| Company : KIP Uni-Heidelberg / Lindenstruth |                       |  | Editor : Dirk Gottschalk |       |             |
| Title                                       |                       |  |                          |       |             |
| DCS ADC                                     |                       |  |                          |       |             |
| Size<br>A4                                  | Document Number<br>10 |  |                          |       | Rev<br>1.63 |
| Date:                                       | 2004.11.16 12:30      |  |                          | Sheet | 10 of 14    |

Shaded area shows devices not used for KIP/DCS



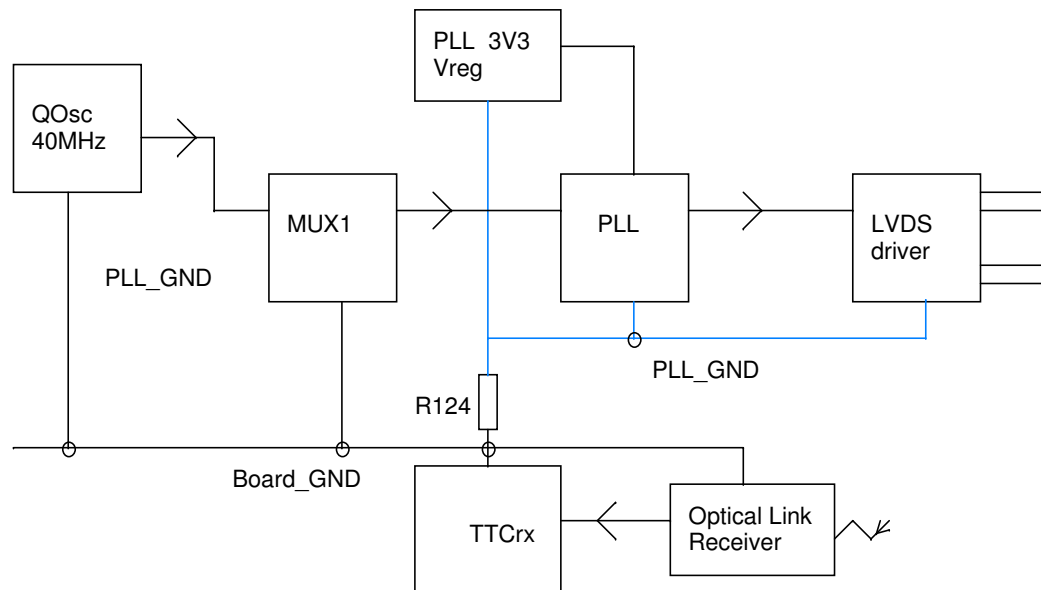
## Routing Hints for the DCS Board

Place 10nF and 100nF capacitors as close as possible to the devices. Place power vias as close as possible to the related decoupling capacitors not to the related device. This may not allways work with BGAs but should work with all non BGA packages. See picture.



\*via to supply or GND planes

## Grounding scheme for PLL, TTCrx and 120MHz LVDS driver



|                            |                       |  |                          |    |             |
|----------------------------|-----------------------|--|--------------------------|----|-------------|
| Wednesday 2003.12.17 10:10 |                       |  | Editor : Dirk Gottschalk |    |             |
| Title                      |                       |  |                          |    |             |
| DCS Board Routing Hints    |                       |  |                          |    |             |
| Size<br>A4                 | Document Number<br>12 |  |                          |    | Rev<br>1.60 |
| Date:                      | 2003.12.17 13:30      |  | Sheet                    | 12 | of 14       |

5

4

3

2

1

D

**PLL Configuration Table for TPC and TRD**

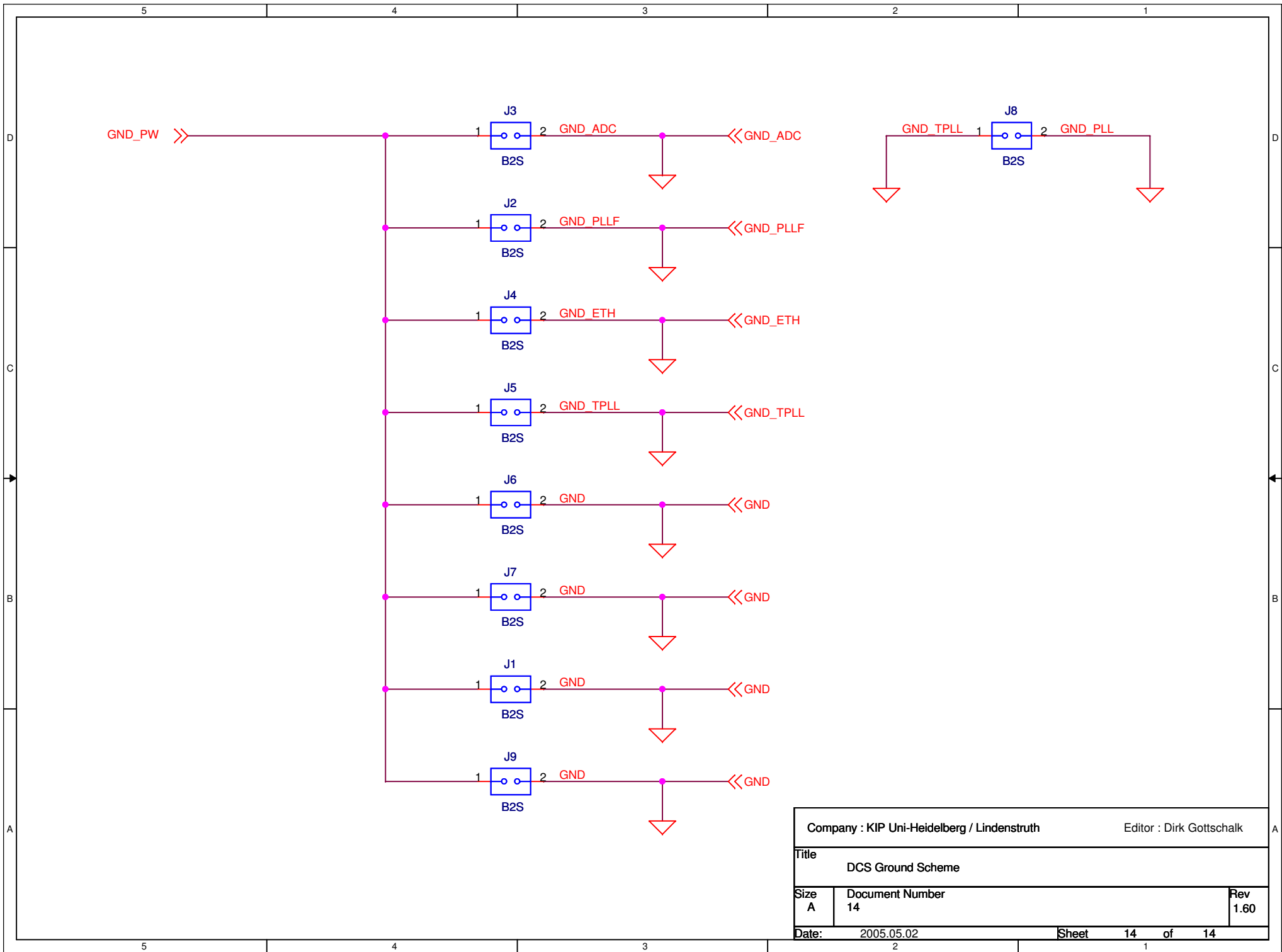
|                   | TRD       | TPC       |
|-------------------|-----------|-----------|
| default frequency | 120 MHz   | 40 MHz    |
| R68               | no device | 10k       |
| R99               | 0R_Jmpr   | no device |
| R100              | no device | no device |
| R105              | no device | no device |
| R107              | 0R_Jmpr   | no device |
| R108              | no device | 10k       |
| R109              | 0R_Jmpr   | 10k       |
| R110              | 0R_Jmpr   | 10k       |
| RN48              | no device | 4x0R_Jmpr |

C

B

A

|                                             |                       |                          |             |
|---------------------------------------------|-----------------------|--------------------------|-------------|
| Company : KIP Uni-Heidelberg / Lindenstruth |                       | Editor : Dirk Gottschalk |             |
| Title<br>PLL Clock Configuration            |                       |                          |             |
| Size<br>A4                                  | Document Number<br>13 |                          | Rev<br>1.61 |
| Date:                                       | 2005.05.02 10:00      | Sheet 13 of 14           |             |



|                                             |                       |  |                          |    |             |
|---------------------------------------------|-----------------------|--|--------------------------|----|-------------|
| Company : KIP Uni-Heidelberg / Lindenstruth |                       |  | Editor : Dirk Gottschalk |    |             |
| Title<br>DCS Ground Scheme                  |                       |  |                          |    |             |
| Size<br>A                                   | Document Number<br>14 |  |                          |    | Rev<br>1.60 |
| Date:                                       | 2005.05.02            |  | Sheet                    | 14 | of 14       |