Proposed prototype step, based on the 16 channel version of the S-ALTRO readout chip.

The Lund Group

Background:

Recent meetings within the LC-TPC and AIDA collaborations, in particular those specifically involving the electronic readout system for micropattern avalanche chambers (GEM and Micromegas) have brought a few crucial and also rather solid facts on the table. Motivated by this we have put together this proposal as start of the discussions how to proceed with the prototyping.

Some basic facts that we think are crucial: (please correct if we have misunderstood anything):

About Chips:

-a 16 ch S-ALTRO chip (S-ALTRO16) will be produced in an engineering run. If all goes well, there is a rather large number of chips (about 3000) available first quarter 2011.

-The 16ch S-ALTRO is compatible with the PCA16-ALTRO chip-set in terms of control and readout.

-A final 64ch version of the S-ALTRO is a very expensive step. For the time being there is no budget available for this.

About packaging:

-The decision about packaging is pending, except for a small number for characterization which will be packaged in LQFP176 (same as present ALTRO).This package has a footprint of 32mm*32mm. That is useful only for boards similar to the present FECs connecting to the pad board with cables. To repeat that step on large scale with S-ALTRO16 replacing the PCA16+ALTRO is not a big enough step forward for the next prototype.

- The area of the S-ALTRO16 die is about 50mm^2. The die will not be adapted for the smallest BGA packages which require bump bonding inside the package. Any other standard package will impose a severe limitation in pad size if we require that the electronics should fit behind the pads that it serves.

Other concerns:

-The overall budget with AIDA and other financial sources calls for low budget solutions.

-The whole chain, from pad to fiber will eventually be new, including the highly sensitive analog part. One can expect a need for many prototype steps on the electronics alone. An “all on one board” approach will inevitably be very expensive in prototyping. (see below)

-We judge that it will take several years until the 64ch version is available

-Due to the large threshold costs involved to obtain the 64ch chip some realistic intermediate prototype step should be taken with S-ALTRO16.

Goals with next prototype readout based on S-ALTRO16:

- the next prototype shall be made for pad panels fitting to the present endplate. The goal should be to equip 3-4 such panels.

- we should aim for realistic pad sizes. 1*4mm have been used as a smallest desirable size in the final solution. The present GEM prototype panels have pads with an area corresponding to about 1*6mm^2 pads. We consider this to be a realistic goal for a fully instrumented pad board.

- the issue of power pulsing should be prototyped

- cooling issues should be studied and developed and a final cooling solution should be prototyped.

- it should be as realistic as possible in terms of noise.

- the experience with the prototype shall provide safe input for the costly 64ch SALTRO development.

Some guidelines:

An important simplifying aspect for a prototype step based on the SALTRO16 chip is that this chip is compatible (in terms of signals and control) with the PCA16-ALTRO combination that is used in the present FEC-version. Thus it can be read out with the present board controller-ALTRObus-RCU system with small or no changes if we adhere to the modularity of 8*16=128 channels per board controller i.e. copy the present FEC modularity.

It has been a working assumption that in a final design all electronics will be placed on the top side of the pad board. There are many advantages in placing the board controller and maybe more (like LV-regulators and power switching) on one or two boards plugging onto the pad board which only houses the pads on one side and the SALTRO16 chips on the other. We list below some advantages with such a solution:

- trace routing from pads to SALTRO16 become simpler since translational routing will only be necessary at the edges of a pad board and not around non S-ALTRO parts in the interior of the module.

- with fewer components on the pad board we can use smaller pads.

- changes during electronics prototyping will be cheaper and easier to implement and test (a change in the digital part of the readout chain does not influence the expensive pad module and vice versa)

- the interface between the pad module and the controller/readout board is well defined

- it offers a good possibility to split design and fabrication responsibilities between several institutes

Further advantages of placing the non SALTRO functions on plug-in boards are:

- the trace routing on the plug-in board will be easier compared to the trace routing in case all the electronics would be placed on the pad board. The pad board will have fewer layers and thus becomes cheaper.

-analog and digital functions are well separated which makes it easier to optimize noise performance

- it moves heat away from the TPCendplate

- it facilitates service. A malfunction in the digital part of the readout chain (which kills a module) can be replaced without dismounting a module from the end plate. One may make a design so that one can isolate a bad S-ALTRO16 to prevent it from killing the whole module. The SALTRO16 is prepared for this to some extent. 16 (or even 64 in a final solution) dead channels are probably acceptable.

- By keeping the board controller, ALTRObus and RCU as they are we can wait until the DAQ of the LC experiment is fully specified before making large changes. Those specifications should only affect the plug-in boards and it is likely that the design of the pad boards can remain unchanged since the digital and analog parts are well separated.

More or less all of the above mentioned advantages for the prototype step with SALTRO16 are also valid for the final panel. Probably the serviceability stands out as the biggest advantage.

Problems with a full pad board with wire bonded chips!

If standard packages are too large and bump bonding cannot be used, we are left with wire bonding directly to the PC-board as the smallest outline solution. Let us now investigate what implications a solution with SALTRO16 chips wire bonded to the pad board would have.

The die size is about 50mm^2. 2 mm around the die for bondwires requires another 50 mm^2 and by adding area for passive components we end up with 160-200mm^2 for each chip serving 16 channels. So, one would need to have pads that are at least 1*10 mm^2 in size to match the area needed by each chip. This a bit too large to match the prototype goals.

An important complication is fabrication. To assemble a full pad board with several hundred wire bonded naked chips, of prototype quality and basically untested, means that one must expect 10-20 non working (assuming a yield of 95%) chips per board, which have to be identified and replaced. This is very hard to do and can only be done if testing a board with naked chips before sealing is an inherent design feature from the beginning. Even if that is possible, replacement of a bad chip is a compromise with fabrication quality. These problems can possibly be handled in a large scale final fabrication by testing on the wafer. An “on chip” analog test feature would improve the quality of the testing of the chip. Testing on the wafer for the small number of chips used in the prototyping is too expensive (too large setup cost).

So, these difficulties imply yet another solution at least for the prototyping.

A multichip module, FEC-MCM

We end up with the proposal to make a multichip module (MCM), with eight SALTRO16 chips wirebonded to a small pc-board. To meet the areal constraints, SALTRO16 chips have to be mounted on both sides of the board. That is possible since the MCM connects to the to the pad board by micro connectors of similar type as used for connecting the Kapton cables in the present EUDET system. Thus the MCM board is lifted up about 4.3mm from the pad panel allowing space for components on both sids of the MCM.

A very rudimentary CAD of such a module has been made , mostly in order to investigate the feasibility and to get some idea about the size. The drawing in fig 1 shows how components could be laid out on a 23.5 by 31.5 mm^2 PC-board. Proper design rules from the bonding company have been followed, external components are estimated to be the same as for the present PCA16+ALTRO, however choosing the smallest outline version. The only active components on the MCM-FEC are the eight S-ALTRO16 and two buffer chips for the clock distribution.

The signals from pads are brought to the preamp input of the SALTRO16, via 4 connectors, with 0.4mm pitch and 40 leads (32 signal plus 8 ground). The connectors have to be mounted with very high precision on the pad board and on the MCM module. (Possibly, two 80pin connectors could be a better solution than 4 connectors with 40 pins each).

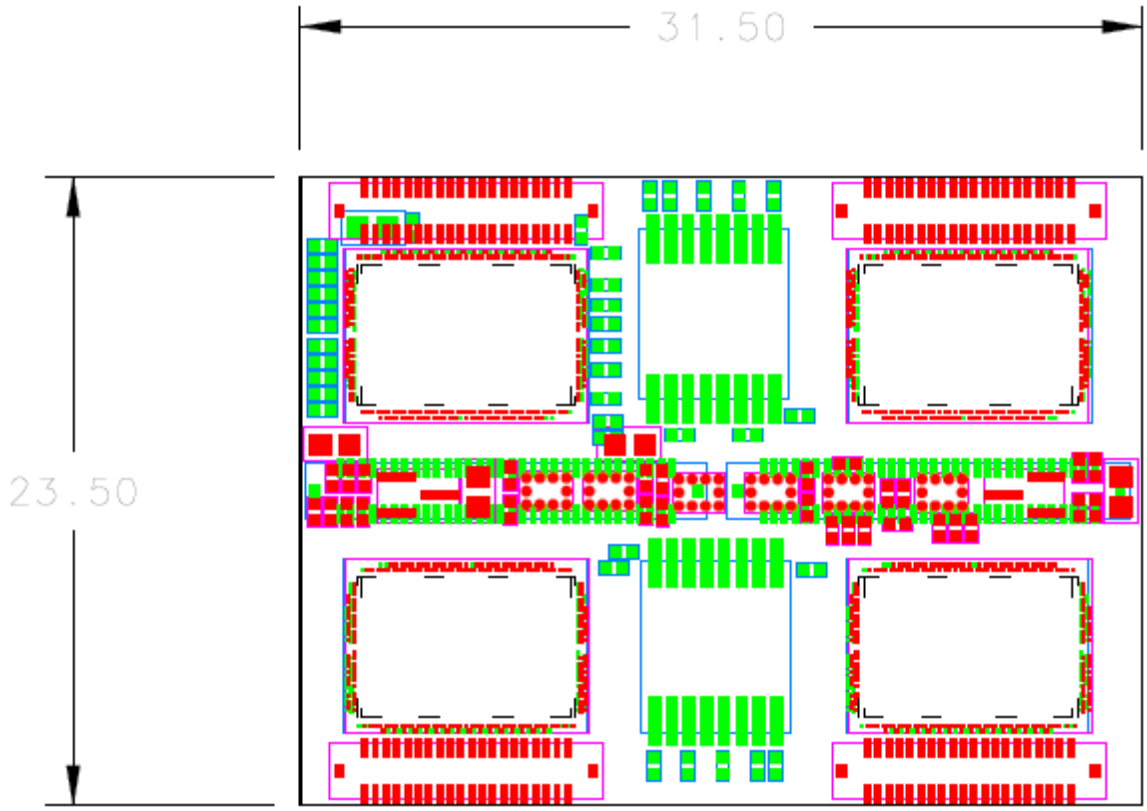


Fig 1a. *The FEC-MCM. Four SALTRO16 on the top side and for on the below side. Green colour refers to the top side and red colour to the below side.*

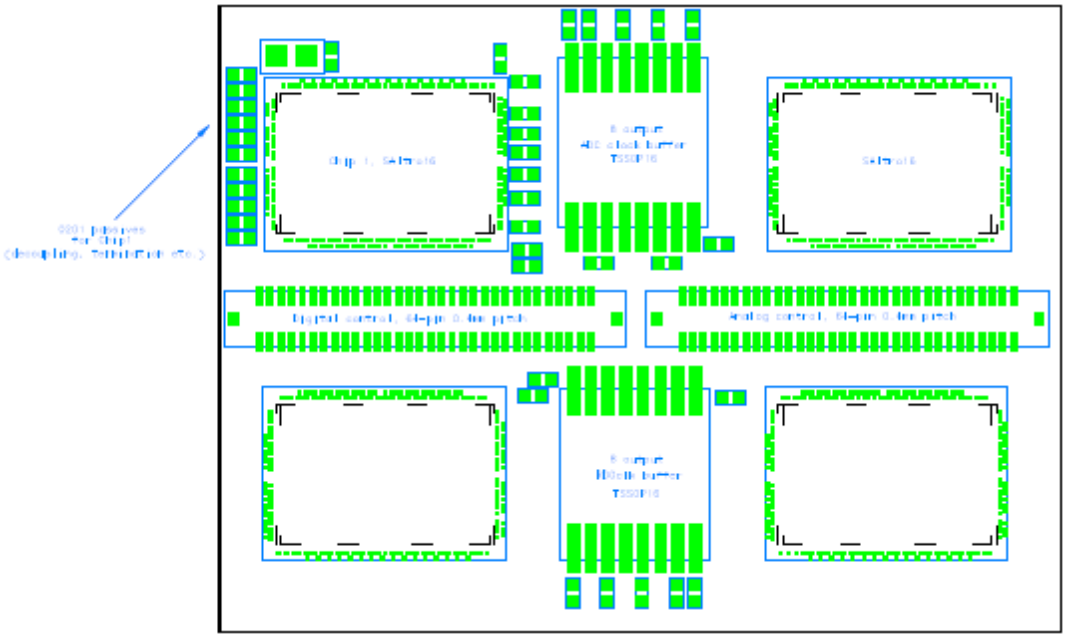


Fig 1b. *The FEC-MCM. Top side only. Two 60 pin connectors provide the connection to the digital readout, SALTRO16 control and LV supply .*

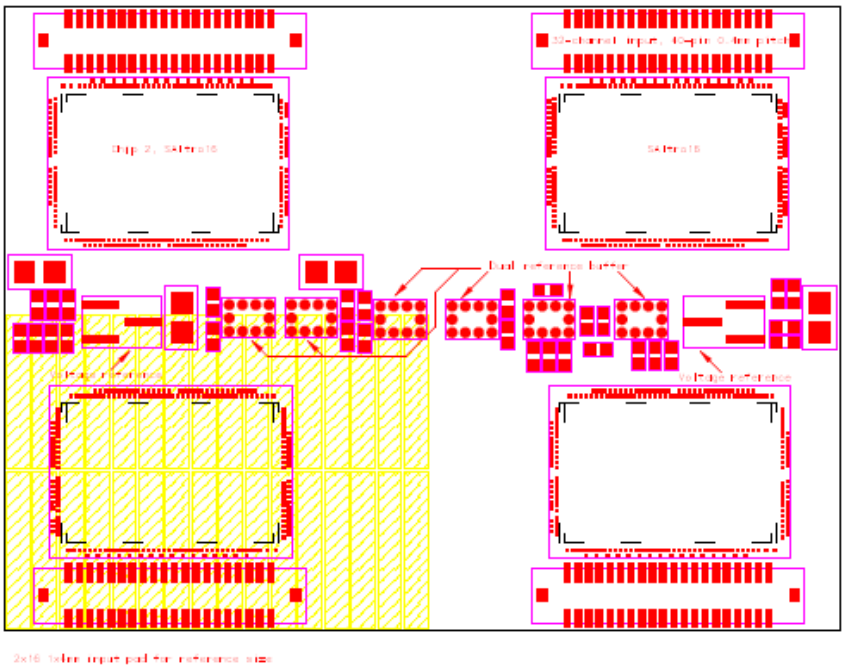


Fig 1c. *The FEC-MCM. Below side. 32 Pads with the size 1*6mm are indicated in yellow. i.e. the area served by two (above and below side) SALTRO16 chips. With 1*6mm pads the pad area of 32 pads is slightly larger than the area occupied by the associated electronics.*

FEC_MCMs placed on a panel of the LCTPC backflange

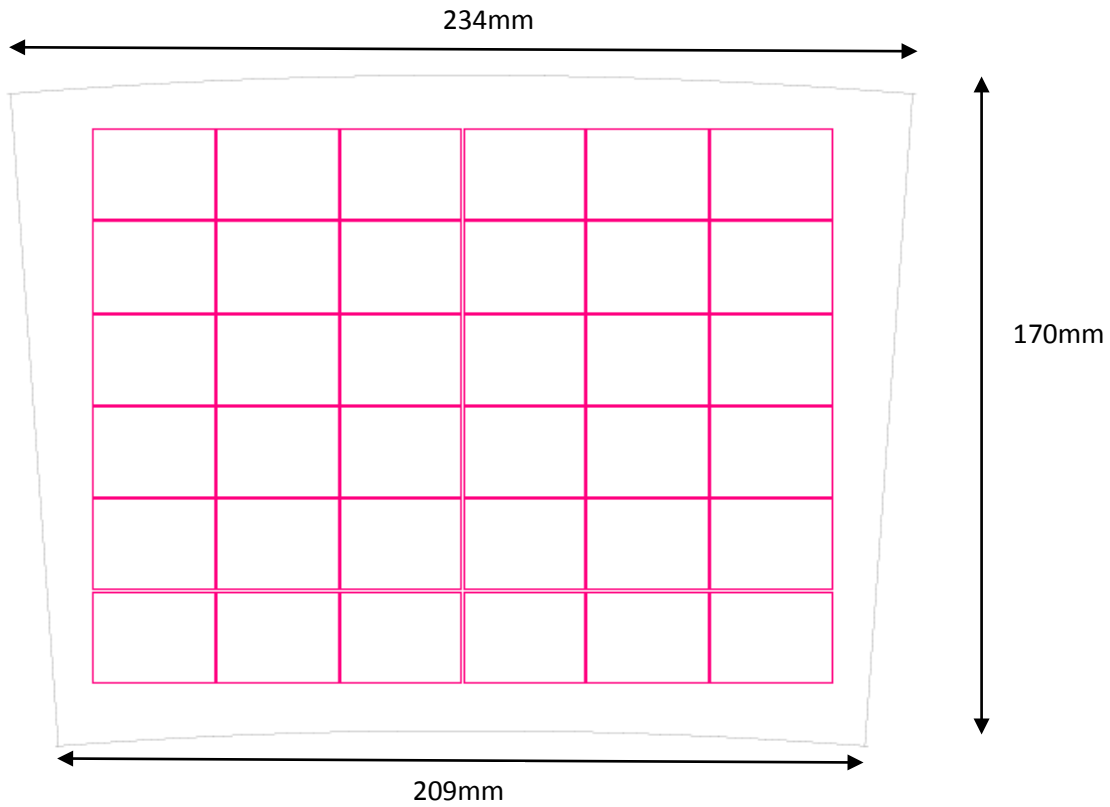
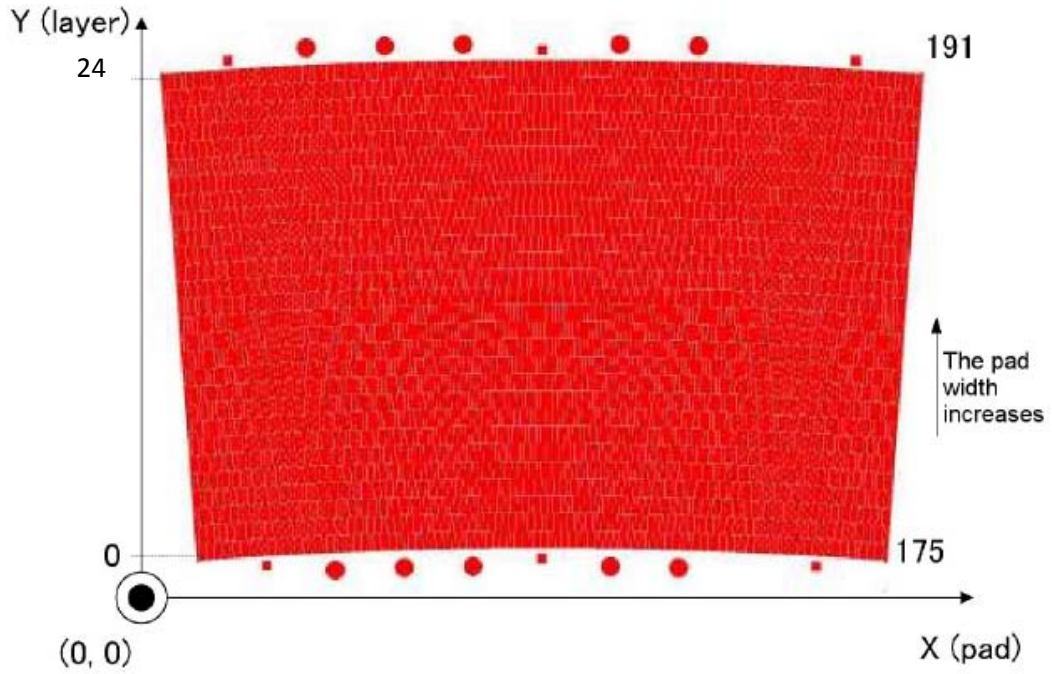


Fig 2. A matrix of 6 by 6 FEC-MCMs placed on a panel

Fig 2. shows the most reasonable placement is in 6 straight rows of 6 FEC-MCM's in each i.e. 36 FEC-MCM's in total. That yields 36*128=4608 channels in total. A placement following the curvature of the module will probably not increase the number of channels per panel much enough to motivate the drawbacks. .



layer	# of pads	Pad width (gap 0.1) (mm)	Pad length (gap 0.1) (mm)
24	**192**	**1.10**	**5.9**
23	**192**	**1.10**	**5.9**
22	**192**	**1.09**	**5.9**
21	**192**	**1.09**	**5.9**
20	**192**	**1.09**	**5-9**
19	**192**	**1.08**	**5.9**
18	**192**	**1.08**	**5.9**
17	**192**	**1.07**	**5.9**
16	**192**	**1.07**	**5.9**
15	**192**	**1.07**	**5-9**
14	**192**	**1.06**	**5.9**
13	**192**	**1.06**	**5.9**
12	**192**	**1.05**	**5.9**
11	**176**	**1.14**	**5.9**
10	**176**	**1.13**	**5-9**
9	**176**	**1.13**	**5.9**
8	**176**	**1.12**	**5.9**
7	**176**	**1.12**	**5.9**
6	**176**	**1.11**	**5.9**
5	**176**	**1.11**	**5-9**
4	**176**	**1.10**	**5.9**
3	**176**	**1.10**	**5.9**
2	**176**	**1.10**	**5.9**
1	**176**	**1.09**	**5.9**
0	**176**	**1.09**	**5.9**
sum	**4608**		

Table 1. *Pad sizes, following the pad layout used for the present Japanese GEMs but modified to the number of pads that could be read out by 36 FEC-MCMs*

The readout.

The readout of data from the FEC_MCMs can be done in different ways. The basic solution would be to keep everything as similar as possible to the present architecture. Later, depending on available resources, one can consider different levels of new development to make the solution more convenient and to include prototyping towards the final readout solution for the LC experiment.

The basic readout solution.

Evidently, the size of the FEC-MCM has to be kept at minimum. Thus one should place the board controller FPGA on a separate card which plugs into the FEC-MCM module. On the present FEC (ALICE/EUDET) the board controller, and the GTL chips send and receive data and control signals for 8 ALTROs on a FEC to/from the RCU on the 40 bit wide bidirectional ALTRObus. This is divided in two arms which each can handle 16 FECs. Access to the bus is via GTL driver chips, which requires 7 chips per FEC. The basic solution is to divide the present FEC, behind the 8 ALTROs and place all digital components for readout and control on a separate card, however retaining the architecture with 8 ALTROs as a unit.

The digital readout card

Presumably the most practical solution would be to have a common readout card for 6-8 FEC-MCMs, thus integrating the ALTRObus in the digital readout card. Two such cards (connected at one end), serving two FEC_MCM rows in fig 2, would replace one ALTRObus arm in the present design. The connection to the RCU could be made flexible by a short flat cable. Possibly, the connections between the FEC-MCMs and the digital readout card shall be flexible by short flat cables. If so, a single readout card could serve two FEC_MCM rows and the readout bus would be very short.

With 36 FEC-MCMs on a pad module, two RCUs would have to be used. With a cable connection from the readout card to the RCU, one of the RCUs could serve two FEC-MCM rows on the adjacent pad module.

Since programming of the preamp-shaper uses the board controller this functionality should also be placed on the digital readout card.

Development path for the readout card:

The main advantage with the basic solution for the readout is that it could be operational with minimal development efforts. Thus, test and optimization of the FEC_MCM could start in a fast and predictable way. The basic solution would probably become rather impractical if realized in full scale i.e. for reading out 12-16 FEC-MCMs through the same readout card. This is mostly due to the need of the bus translator chips (GTL circuits) which have to interface each FEC_MCM to the bus.

In the longer time perspective one should therefore work on a re-design of the readout architecture with the first purpose of removing the GTL circuits or at least reduce the number of them.

A more significant progression of the prototyping would be to use an FPGA board controller with a high speed serial output, maybe complemented with optical data transfer. One would then replace the readout card with just a card for the board controller and a serial link to a receiver card which interfaces to the RCU some distance away. That would add a large flexibility to the placement of the FEC-MCMs. Most importantly, one would also have taken a big step towards a final design.

LV and power pulsing

There is no room for LV regulators on the FEC-MCM. These have to be placed on a separate card which house the regulators and circuitry for the power pulsing. A suitable, very short connection to the FEC MCM has to be

chosen. The solution sketched in fig 1, using multiple pins of a micro connector for each LV and GND is can probably be done in a better way

Cooling

Placing the LV regulators and the digital readout and control of the front end electronics on separate plug in cards perpendicular to the FEC-MCM brings some of the heat off the detector backplane. It should be rather straightforward to provide additional water cooling (or other) to these cards. Cooling of the FEC-MCM may be harder but advantages are that the chips are lifted above the pad board so there is very little thermal contact to the TPC volume itself. But a scheme for cooling the electronics itself on the FEC-MCM board has to be worked out. In particular the confined space between the FEC-MCM board and the pad board could require special cooling attention.

Tentative work organization

An important advantage of the proposed prototyping is that it gives the possibility to split the design efforts on several institutions since the interfaces between the different parts are well defined. Since, the RCU can stay intact, everything that has been done so far for the EUDET project in terms of data archiving, monitor and control can be reused until new requirements are specified by the global design of the LC experiment

Pad panels

Design of pad panels can be done by those labs who have avalanche chambers to test. The critical interfacing to the FEC-MCM is of mechanical nature. Tolerances of connector placement are tight. Lund could do the pad board design if that is desirable

FEC-MCM

Lund has experience from the ALICE TPC and the EUDET project in working on the PASA-ALTRO and PCA16-ALTRO systems. CADding and prototyping of the FEC-MCM would suit us well. Lund has industrial contacts to fabricate the FEC-MCM .

The digital readout card.

Basic solution: The signal interface between the FEC-MCM and the RCU is straightforward as it is the same as in the present FEC design. Minor changes to FPGA firmware may be needed. A lab with competence in FPGA programming could contribute. Lund has the competence to CAD the board.

*Advanced solution*s: Again a work for an institute with competence in FPGA programming as it may also include modifications of the RCU firmware. Lund can do the CAD.

DAQ software for archiving, monitoring and control

Lund has done most of this in EUDET. Starting from there this could be suitable for contributions from all the involved institutions.

Summary.

The prototype plan we bring up to discussion has many attractive features we think. It is rather conservative, reducing risks. It provides a realistic prototype before taking the final expensive steps with the final 64ch chip.

A final solution for the LC-TPC, with a detachable multichip module with eight or sixteen 64 channel SALTRO

chips is an attractive alternative. It offers full repairability of the electronics, without dismounting pad boards from the TPC endplate. A realistic MCM prototype of this type , with LV-supply, board controller and optical output integrated on the MCM would be a natural development of the FEC-MCM prototyping. It can be done in a realistic way already with the 16-channel version of the chip. This would be a quite realistic prototype test in terms of electronics. The MCM-board would be somewhat larger than if the 64ch version SALTRO were used. Consequently, when tested on a pad board on the TPC, larger pads (or partial instrumentation of the pad board) will have to be used.

We also think that the proposal offers excellent possibilities for several institutes to work together and to use the available resources efficiently. Of course the costs must be evaluated before commitments can be made. Thus the discussion of who can do what is mostly to identify the necessary competences needed for different parts of the work.