Characterization of a compact, high resolution readout system for micro-pattern gaseous detectors

Master Thesis by: Liangliang Shi
Supervisors: Anders Oskarsson
Ulf Mjörnmark

Date: 24th, Jan, 2013

Abstract

A Linear e$^+$e$^-$ collider, either ILC or CLIC will be the next platform for high energy physics study to complement the LHC. Results discovered by LHC may need precision measurements before we can get full understanding of the physics. International collaborations are in the process to prepare both for the accelerator and for the experimental setup.

Time projection chambers as the main central tracking devices are used in various experiments. It provides good resolution for 3D track reconstruction. However, the large readout granularity needed to meet the resolution goals imposes stringent requirements on the readout electronics and the mechanical construction.

For the electronics, the requirements on miniaturization, the data volume and transfer bandwidth, temperature stability, power consumption and radiation hardness, high density of integration have to be driven to the technical limits and the detector development towards this is going on for the linear collider experiment. To meet these needs, S-ALTRO16 chip was recently designed and the first prototypes are available for characterization. It integrates the analog amplification part with the digitization and signal processing parts into a single silicon chip. In particular, maintaining the resolution while integrating a highly sensitive analog frontend with a digital part is an expected difficulty. In order to evaluate the possible effect on the resolution by this integration step we have performed the same (as far as possible) characterization of the existing readout system, where the analog and digital functions were implemented in separate chips (PCA16+ALTRO). In addition to performing the tests, the methodology for the test has to be developed.

In this thesis, the system noise issues are studied and measurements were done with the system. To better understand the system behavior, all the main functional components of the front end electronics were studied. To calibrate the system, it was studied how to best quantify the pulse amplitude when the sampling rate of the ADC is finite and the pulse is random in phase to the sampling clock.

Since the amplifier chip is programmable, in terms of input polarity, peaking time and conversion gain, this readout system can be used not only for a large variety of gaseous ionization chambers but also for a wider family of radiation detectors and other signal sources.

The main conclusion of the thesis is that the noise performance after the integration step, represented by the S-ALTRO16, is quite comparable to the performance before integration. The performance is close to the theoretical limit and we conclude that the integration has not resulted in any noticeable deterioration of the noise of the readout system.

Acknowledgements

Table of Contents

IV

Chapter 1 Introduction and the physics motivation for a Linear Collider

1.1 Introduction

This thesis deals with test and characterization of new readout electronics for radiation detectors. As many modern electronic readout systems for high energy physics experiments, it is based on application specific integrated circuits (ASICs) for the amplification and digitization of the detector signal. Two versions of the system were tested, one where the analog and digital functions are implemented in separate chips and the latest version where both analog and digital functions are integrated in the same chip.

Readout systems in high energy physics are normally designed for a specific detector. The ASICs used here have been made more versatile by a programmable preamplifier/shaper where polarity, peaking time and gain are selectable, resembling the multipurpose functionality of modular NIM electronics. Although this readout system is being developed for readout of large Time Projection Chambers (TPC) like the one planned for the future experiment at a linear collider, it has also a much broader potential use for compact readout of radiation detectors. In this project, the system has been studied mostly from this general point of view, independent of what kind of detector it may read out.

1.2 High Energy physics and the linear collider

Years after years, two "simple" questions bewildered human beings: What is the world made of? and how does it hold together? To figure out both puzzles, great minds have been working from individual thinking to large international cooperative projects such as LHC and its experiment until today and in the foreseeable future this trend will continue with e.g. the International Linear Collider, ILC.

Besides the well known origin of the word atom which is atomos in Greek, the ancient Chinese philosopher Zhuangzi also proposed: "Take half from a foot long stick each day, and you will never exhaust it in a million years". This shows that the ancient Chinese began to reflect on the origin of matter in a similar way as we do today, studying the matter structure like peeling an onion. Whether particles are divisible or not is a fundamental question to particle physics. Study of matter at shorter and shorter wavelength is thus a driving force behind particle physics experiments which goes hand in hand with the wish to produce new heavy particles as both require higher and higher energy collisions.

At the end of the 20th century the smallest building block of matter discovered was named the atom which implies indivisibility. Years later, when the concept of atoms was the general state of the art, it was found that the atom itself has internal structure and it is thus divisible (discoveries by Thomson in 1897 and Rutherford in 1909). Again when the concept of the atom as the smallest entity began to shake, it was found that the electron is stable. After several generations of experiments, people may still believe that certain particles are indivisible and today, no observations have been done which require any substructure of the quarks and the leptons for its explanation. Since the discovery of internal structure of nuclei, large numbers of composite particles were found. Questions

like how the constituents interact with each other came into consideration. Basically there are three sources that we can utilize to learn about this: scattering, decays, bound states.

Questions arise as how to produce such particles and detect them. The particles can be from cosmic rays like in the GAMMA project, man-made nuclear reactors like the Daya Bay reactor neutrino experiment, and various accelerators, like LHC. In general, both high mass particles and probing short distances need high energy particles. Various kinds of detectors are developed to fulfill the detection purposes.

1.3   The standard model

The standard model which is also referred as SM mostly formulated in 1970s can account for the experimental results very well. This model incorporates the fundamental building blocks: up, down, charm, strange, top, bottom quarks and electron, electron neutrino, muon, muon neutrino, tau, tau neutrino and gluon, photon, W&Z, Higgs boson. They can be grouped into fermions and force carriers which are bosons.

1.3.1   The Fermions

The fundamental building blocks of ordinary matter are the lightest fermions. They carry half-integer spin and they can be grouped into quarks and leptons. No two fermions can be described by the same quantum numbers in a system. This is called the Pauli Exclusion Principle. Quarks only exist in bound states but leptons can be observed as individual particles.

1.3.1.1   The quarks
The quarks come in three families. Their charges are fractions of elementary free charge.

Table 1.1 quark families [1]

Generation	Flavor	Charge	Mass
First	d (down)	- 1/3e	4.1-5.8MeV
	u (up)	2/3e	1.7-3.3MeV
Second	s (strange)	- 1/3e	around 101 MeV
	c (charm)	2/3e	around 1.27 GeV
Third	b (bottom)	- 1/3e	around 4GeV
	t (top)	2/3e	around 172GeV

For each quark, there is a corresponding antiquark with the same mass but opposite charge and other quantum numbers. Quarks can bind into doublets (quark-antiquark pair forming a meson) and triplets (three quarks forming a baryon).

1.3.1.2   The leptons
Leptons can be grouped into three families as well:

Table 1.2 the Leptons

Particles	Flavor			Charge
leptons	e	μ	τ	-e
	v_e	v_μ	v_τ	0e

Using the charge carried by the electron as the unit, leptons carry integral electric charge. The neutral leptons are called neutrinos, denoted by v with subscript to indicate to which family they belong.

1.3.2   The force carrier bosons

Bosons are the force carriers in the SM. Compared to fermions; they do not follow the Pauli Exclusion Principle. In the SM, a force or interaction between two particles originates from the exchange of boson force carriers. Three fundamental forces are incorporated in the model: weak, strong, electromagnetic forces while the fourth fundamental force, the gravitation is not part of the SM. The Gravitational force is extremely week on the scale of particle physics and it has negligible influence on particle physics phenomena.

The strong force is responsible for the quark binding to hadrons, and the force mediator is called gluon. The strong force acts on quarks but not on leptons. Electromagnetic interactions are common to our daily life, and it is responsible for the binding of electrons with nuclei and binding atoms together to bulk matter. Photons are exchanged to mediate the force. The electromagnetic force operates on charged particles. Weak interaction is responsible for the beta decay of radioactive nuclei. Weak interaction affects all the fermions i.e. both leptons and quarks regardless of whether they are charged or not. The mediators of weak interaction are the very heavy W and Z bosons.

Due to the different mass of each kind of mediator boson, the interaction range varies, from very short (about 10^{-18}m) for the weak interaction to infinitely long (however reduced with distance) for electromagnetic interaction.

Besides the bosons mentioned above, there is another one called the Higgs boson which accounts for the mass origin of the fundamental particles. Through interaction with the permeating Higgs field, fermions acquire mass. The Higgs boson is the fundamental component of this field. The Higgs mechanism itself does not predict the mass of Higgs particle. But through various constraints, it suggests that the mass should lie in the range from 114GeV to 250GeV. After years of efforts, the optimistic news came on July 4, 2012, when the LHC experiments ATLAS and CMS announced that an excess of events at a mass of approximately 125 GeV, with a statistical significance of five standard deviations above background expectations was observed, which is consistent with the Higgs particle but further tests are needed to confirm its existence and that it is really the Higgs particle either as it is predicted in the standard model or not.

1.4   Beyond the SM

Although the SM has been successful in explaining an enormous amount of experimental data to date, there are several important shortcomings as well. In the SM, gravitation is not incorporated. The mass of the neutrino is assumed as zero which is now well established experimentally not to be the case. The SM does not provide satisfactory answers to important astrophysical observations like dark matter and dark energy. Many arbitrary parameters should be explained. Problems like these should be solved before it can be called as a complete theory.

1.4.1   Super symmetry, SUSY

SUSY postulates fermion-boson symmetry. According to it, every boson has a fermion partner (identified by putting 's' in front of the name thus 'squark' 'selectron') and every fermion has a boson partner (identified by adding an suffix 'ino' to the existing name-thus 'photino', 'higgsino' etc). One obvious problem is that the pair partner should share the same mass. If so, it should have been observed already. So the symmetry we assumed should be broken. SUSY models have the potential to solve several important problems:

- It makes perfect convergence at the grand unification scale.
- It offers solutions to the hierarchy problem which is a severe one in SM.
- It provides the particle candidate for dark matter which is unexplained by standard model.

1.4.2   Grand unification

Electroweak unification is the first logical step; the next should be the incorporation of strong interaction. In such a Grand Unified Theory (GUT), all three different processes are unified as one process with single coupling constant. Since the coupling 'constants' are energy dependent, so it is tempting to assume that at some high energy scale, they may intercept.

1.4.3   Dark matter and dark energy

Evidence from independent observations like cosmic microwave background and supernova clusters etc show that dark matter and dark energy takes up 95% of the mass-energy content of the universe. Among the already known SM particles, it seems that none of them can be responsible for dark matter. If we assume the Newton's law is valid within the dimension of galaxy, based on the measured velocity of galaxy, we can gather the information about the mass of the cluster. This mass is much more than the visible stars in the cluster. It is surprising enough that there is hidden mass- dark matter within the cluster. And such dark matter requires weakly interacting and massive particle composites, otherwise it should have been observed. Although the SM does not provide any such candidate but in SUSY models, there exists such candidate particles. Meanwhile, we hope LHC or ILC should be able to produce 'pieces' of dark matter in the form of new massive particles.

For a long time, astrophysicists believed that the expansion of the universe would slow down due to the gravitational attraction of all matter. In 1998, Hubble Space Telescope observations of very distant supernovae showed that the universe was expanding with acceleration. This astonishing discovery again calls for new explanations. One of them is that there pervades dark energy in the universe. Such dark energy can counteract the effects produced by the normal gravitational forces so that we can explain why the universe expansion is accelerating.

So, conundrums are everywhere despite the outstanding success of standard model and there seems to be something beyond and it has so far been unreachable by laboratory

experiments. The situation is just like "As our circle of knowledge expands, so does the circumference of darkness surrounding it"-Albert Einstein.

1.5   Physics motivation of electron-positron linear collider (LC)

Compared to hadron collider, an electron-positron linear collider (named LC for short in the current context) features clean environment and precise control of initial state of the collision, which is suitable for precision experiments. By colliding elementary particles one avoids the complication that the properties of the individual partons in the hadron-hadron collision cannot be known on an event by event basis. With electrons one is also certain that the initial interaction is not via the strong force. The history of experimental particle physics repeats itself by approaching a new field with a hadron accelerator by which one can reach highest energies for exploration, followed by an e^+e^- accelerator for precision measurements. With LEP, the practical energy limit for a circular electron accelerator was reached. The limit is imposed by the losses due to synchrotron radiation.

Thus the international liner collider ILC and the compact linear collider CLIC were proposed to meet the energy frontier required by high precision measurement and TeV physics.

Precise measurement sectors are motivated mainly by [3]:
- properties of Higgs or unknown particles discovered by LHC
- interactions of top quarks, gauge bosons, and new particles
- New physics in TeV scale and better understanding of electroweak symmetry spontaneous breaking (EWSB) process.

Besides these potential precision measurements, the flexibility of LC program makes it convenient to study in either low energy range of 250-500GeV or in the high energy phase with$\sqrt{s}$ > 500 GeV. The low energy operation mainly driven by various threshold studies, while the high energy phase by physics beyond standard model.

Two options for the e^+e^- linear collider were proposed: the ILC project planned to use superconducting radio frequency acceleration cavities to provide accelerating power and CLIC utilizing separate driven high power beam which is a completely new accelerator technology. Although both of them are still dream projects, extensive collaboration worldwide has been started and this project is part of this development. The ILC technology is only feasible to reach up to 1TeV and beyond that, CLIC is needed. ILC is possible to construct with current technology while CLIC still requires substantial accelerator development.

With a Higgs mass at 125GeV/c^2 , it is seems that a first stage ILC is sufficient for the Higgs spectroscopy as part of the program. This is an important new aspect since starting of the accelerator in one initial stage with 250 +250GeV followed by an extension to 500+500GeV later on is very attractive.

1.5.1   Higgs physics

The observation of new boson particle which is compatible with a light Higgs boson of mass around 125 GeV puts science opportunities on the table:
- How does Higgs couple to itself and other elementary particles and what is the

mechanism.
- What are the properties of Higgs such as mass, width, spin, CP properties etc
- What is the origin of such particle or particles?

In the standard model, it accounts for the EWSB and the mass origin of the fundamental particles. So its properties need be measured precisely to compare with the SM predictions.

A linear collider, LC is the ideal solution for a Higgs factory. The main processes to produce Higgs in e$^+$e$^-$ collisions are Higgs-strahlung and the vector boson fusion process [2]: at the low energy phase of ILC the first process dominates while the second one becomes overwhelming as the √s approaches the high energy phase.
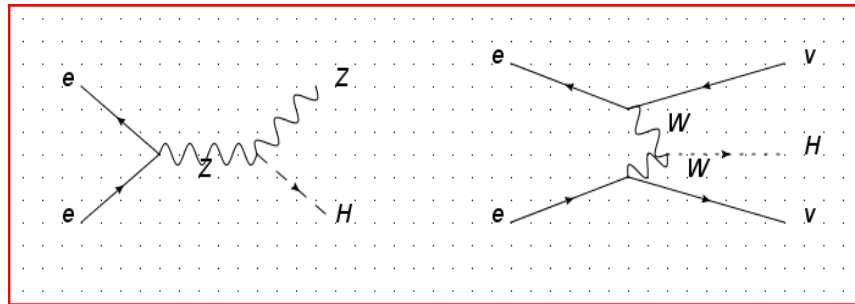

Figure 1.1 two main Higgs production processes where v denotes electron neutrino and the arrow notation used to denote the antiparticle.

Besides the two mentioned main production processes, rare processes such as $e^-e^+ \to t\bar{t}H$, $e^-e^+ \to ZHH$ and $e^-e^+ \to HH\nu_e\bar{\nu}_e$ can be studied as well. Such processes provide access to top quark coupling which is particularly large due to the large top mass and self coupling. The Higgs-strahlung process is suitable for model independent study because such events can be identified based on the electron positron pair with invariant mass of the Z boson. A number of interesting measurements can be done such as coupling constant of Higgs and Z boson, various decay modes etc [2].

As √s increases to around or greater than 500 GeV, Higgs production due to WW and ZZ fusion goes up as well. Under this situation, Higgs' coupling of W and Z can be measured with high precision. At LC, Higgs self-coupling can be measured in order to understand the Higgs mechanism. High precision coupling measurements can verify the prediction that coupling strength is proportional to the masses, which is a prediction from the Higgs mechanism.

Other properties like total Higgs width can be done based on the partial decay widths and branching ratio results. To complete the particle study, property measurements such as mass, spin and CP are accessible at ILC. Since EWSB is more sensitive to the behavior of Higgs, basic understanding of EWSB physics is also expected here.

1.5.2   Precision experiments

In principle the physics program at a linear collider is the same as at LHC, just with the special focus of precision measurements. The desired properties of the linear collider will ultimately be guided by the findings at LHC. One finding does already play a role and that is that the Higgs mass is reachable with the most modest type of linear collider i.e. a phase 1

ILC.

The demanding goals on precision can only be reached by new detector solutions and this project was done within the ILC-TPC collaboration which aims at a tracking detector by which about 10 times better momentum resolution than before can be reached. These properties also impose the requirements to the readout techniques which is the context of this thesis.

References

[1] Review of particle physics particle data group 2012

[2] Physics at the international linear collider preliminary version: draft 29, Nov, 2012.

[3] "The physics case for an e^-e^+ linear collider", ILC ESD-2012/4, CLIC-Note-949(July 30, 2012)

[4] "Precision measurements at the ILC", by T.K. Nelson, SLAC, Stanford, CA94025, USA.

Chapter 2 Time Projection Chamber and Readout system

In the first part of this chapter, the working principle of a time projection (TPC) chamber is given; The ALICE TPC readout system is presented to serve as a TPC readout system example in the rest of the chapter.

2.1 Time Projection Chambers

A Time Projection Chamber (TPC) provides the possibility of reconstructing many tracks per collision through the continuous tracking in 3D. The momentum measurement from a large number of coordinates measured along the track in a TPC has the potential of highest resolution. In the proposed LC project, a high resolution time projection chamber is used as the central track detector. To fully use the potential for high momentum resolution, a strong magnetic field and new micro pattern gas detectors have been adopted for the readout of the signal from the TPC. For the precision measurement, a high spatial resolution (<100 μm over 2-2.5 m drift distance under 3-5T magnetic field) is needed to meet the momentum resolution requirements. Parameters of vital importance for a TPC are: spatial resolution, momentum resolution, *dE/dx* resolution and nearby track resolution.

The main drawback of a TPC is that the long drift time makes it unsuitable at hadron colliders where low cross section phenomena require very high luminosity. For e^+e^- collisions the collision rate is low and the long drift time is less thus problematic. The same can be said for heavy ion collisions and the biggest now running TPC is that in the heavy Ion experiment ALICE at LHC.

2.1.1 Basic principles of a TPC

The TPC contains a large volume of sensitive gas which acts as ionization medium and provides necessary detectable track of liberated electrons. For a collider experiment, it has normally the shape of a hollow cylinder with the collision point at the center. At each end cap of the cylinder, there is a readout plane where the necessary amplification by avalanche chambers provides sufficiently large charge signal pulse for readout. In modern experiments, fast readout electronics is attached to the endplate so that data can be transferred to the DAQ computer array. The schematic view of a TPC is shown below figure 2.1. [1]

A high negative potential is applied on the cathode and the anode is at ground potential aiming for a uniform electric field. When an incident particle traverses the TPC volume, electrons are liberated due to ionization along the track. Such liberated electrons drift along the applied electric field towards anode plane. Normally a magnetic field is used to provide the track bending for the momentum measurement. The B-field is normally parallel to the E-field and it suppresses the transverse diffusion. Based on the measured radius of curvature of the track and the B field, information about the particle momentum can be obtained.
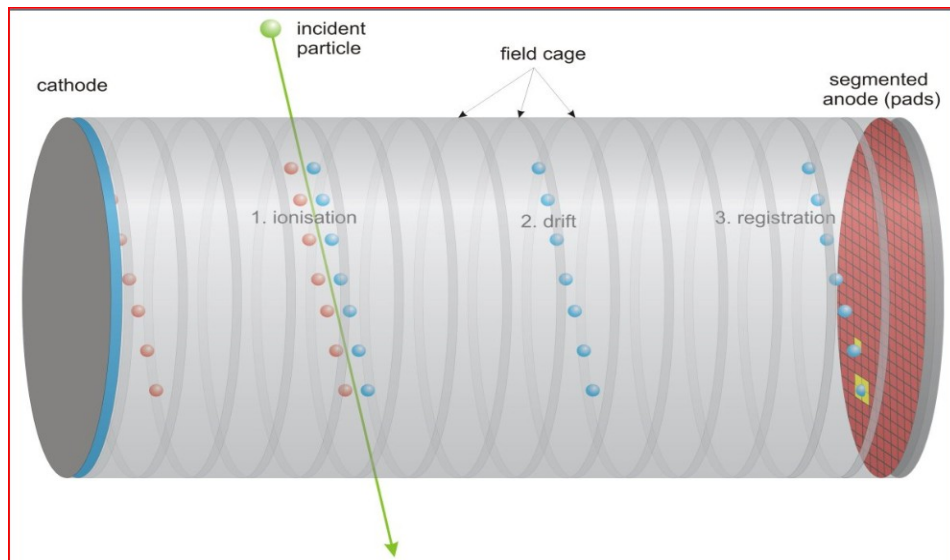
Figure 2.1 working principle of a TPC [1]

Normally, the primary electrons (the ones liberated by ionization) are too few for detection by electronics and thus an amplification process is needed in the readout chamber of the TPC. Large, stable, and proportional gains are desirable for a TPC and this can be obtained by the avalanche process through high electric fields in the gas. Suitable readout chambers can be Multi Wire Proportional Chambers (MWPC), Micro Megas and GEM etc. The amplified current signal is measured on the large number of small pads on the readout plane. The spatial coordinates of x-y (the plane transversal to the electric field) are given directly from the location of the pads on the readout plane and the z coordinates are obtained from the drift time between the passage of the incident particle and the pulse readout time on the pads.

The planned ILC TPC has physical size of 3.6m diameter and 4.3m outside length. Around one million pads (1mm×4-6mm) are needed on each end cap [3]. Since each pad has an individual readout channel, this puts extraordinary constraints on the compactness of the electronics as well as power consumption and of course the cost per channel.

2.2   ALICE TPC readout system [2]

The TPC is the main tracking device for heavy ions collision (Pb-Pb or PP) in the ALICE experiment at LHC. It is the largest TPC ever built and it is in operation since 2009. It has around 90m^3 volume and it is operated in a 0.5T magnetic field which is parallel to its axis. One vital design feature was to handle extreme multiplicity environment in heavy ion collisions at LHC energy. The detector gas used in the TPC is a mixture of Ne, carbon dioxide, and nitrogen. The readout chambers are based on the Multi-Wire Proportional Chamber (MWPC) with pad readout (557568 pad channels). The physical size is comparable to what an ILC-TPC is planned to have but the magnetic field is much weaker and thus the diffusion is large and thus ALICE cannot make use of very small pads. Thus an MWPC is adequate for readout in ALICE while the ILC-TPC with its higher B-field benefits a lot from readout chambers where the optimal pad size is substantially smaller.

The current signal induced on the readout pad in a wire chamber is characterized by a fast

rise time (few ns) and a long tail (hundreds of microseconds). As we mentioned, the TPC in ALICE works in high multiplicity environment, a pileup effect can be severe by these long tails. The readout electronics thus has been equipped with a tail cancellation feature which operates on the digitized information but the maximum allowed track density is limited by this and an avalanche chamber without such long signal tail would provide better performance in this respect.

The induced current signal pulses are transferred to 4356 front end cards (FECn, n indicates the card number) through flexible Kapton cables. The current pulse signal is converted into voltage pulse for digitization and post processing. The schematic of processing chain is shown below in figure 2.2.
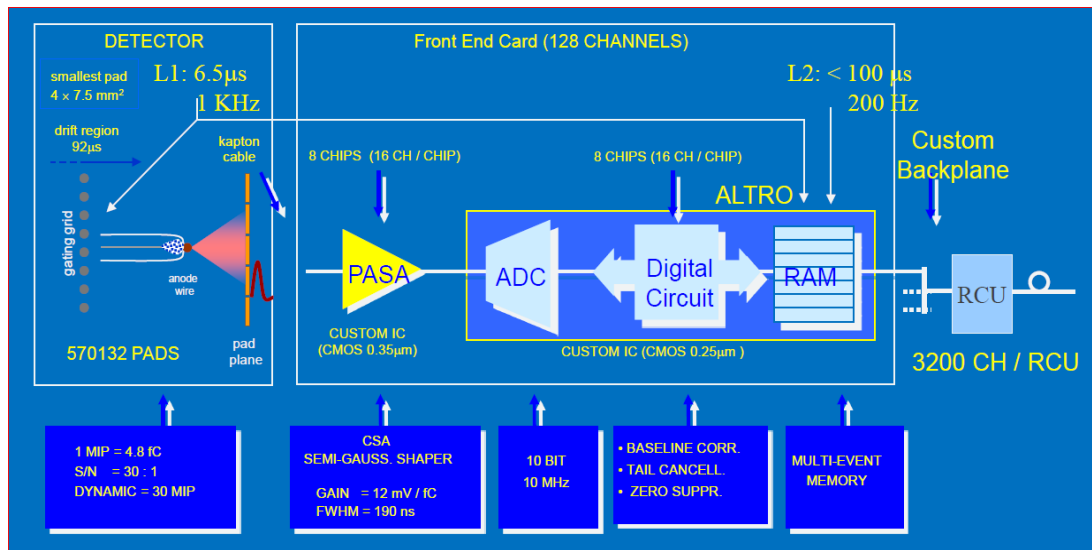

Figure 2.2 ALICE Front end electronics [5]

The new readout electronics used in this thesis is based on the ALICE TPC readout electronics. The analog part (the preamp/shaper) is however adaptable to many other types of gaseous readout chambers by being programmable.

A more detailed description of each block will be presented in chapter 6. The FECs are connected digitally to a Readout Control Unit (RCU) via 40 bit wide backplane bus. The RCU interfaces to DAQ computers, trigger and Detector Control system (DCS). The whole front end electronics has the ability of coping with extremely high data rates and the data throughout is around 750MB/event at an event rate of 1.4 kHz.

Charge collected on the pads of TPC is amplified by the PASA chip, and the differential output is fed to the Digital part (ALTRO chip). A Multi-event buffer was implemented in the ALTRO to minimize the dead time of whole system. Raw data is read out through optical link at 160MB/s. Basic readout block diagram is shown in figure 2.3.
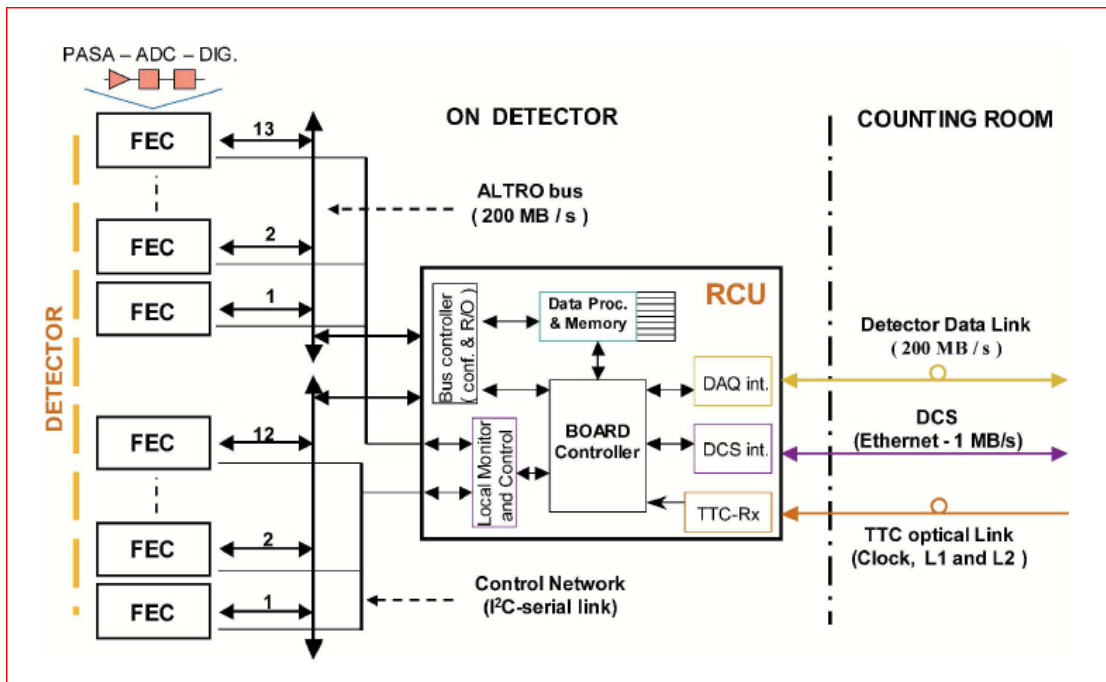
- 11 -

Figure 2.3 block diagram of a readout partition [2]

In summary, the whole system should work under high multiplicity, low power consumption and low radiation load etc. Especially, the readout electronics needs to be fit into the overall detector available space. Space constraints are not a large concern since the pad sizes are comparatively large in ALICE TPC.

References

[1] "www-flc.desy.de/tpc/basicstpc.php", Nov, 2012.

[2] "The ALICE TPC, a large 3-dimensional tracking device with fast readout for ultra-high multiplicity events" by J.Alme, etc. Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment. Volume 622, Issue 1, October 2010, page 316-367.

[3] "the international large detector: letter of intent", by the ILD concept group Feb, 2010. ArXiv: 1006.3396.

[4] "Micro pattern Gas Detectors", by Jochen Kaminski, 17th International Workshop on Vertex Detectors July 28-August 1, 2008.

[5] "The 16-channel Super-ALTRO Demonstrator", 19th, Nov, 2012, CERN.

Chapter 3 Noise analysis of the system

The chapter is divided into two parts: in the first part, general description of noise and a theoretical noise analysis are given; the system noise measurement is presented in the rest of chapter. Section 3.1 is about general description of noise. Noise analysis of the charge shaping amplifier and the ADC is given in 3.2. Measurement results are presented in section 3.3.

3.1   General description of noise

Noise is any undesired quantity added to the ideal signal which carries information. It obscures the signal that we can detect and thus it limits the resolution. Noise can be divided in intrinsic noise and external noise. The intrinsic property of randomness makes it impossible to predict the exact behavior but the average properties can be well described. In signal integrity perspective, it diffuses the signal in a random way. Statistical methods work in describing this effect. The Variance or the RMS value is the right one used frequently. In electronic systems, resolution itself is determined by the relative relation between signal variance and baseline variance. Basically, such noise is from internal processes of electronics in active and passive devices. External noise like pickup from the surroundings, such as digital clocks, RF radiation, grounding loops on the PCB and cabling etc is normally not random but is correlated to the external source, both in time and amplitude.

3.1.1   Electronic random noise

From Shockley-Ramo's theorem, current can be formed by a number of moving charges. In this physical scenario, only the instant velocity of charges and the number of charges are allowed to fluctuate. Thus these two statistically independent sources of fluctuation contribute to the current fluctuation.

The velocity fluctuation originates from thermal excitation which thus has the name thermal noise. Randomness of movement superimposed onto the average movement gives rise to such noise. **Thermal noise** is also called white noise since the power per unit bandwidth is constant at low frequencies. The power density can be expressed as follows:

$$\frac{dP_{noise}}{df} = 4kT \qquad (3.1)$$

, where the k is the Boltzmann constant, T the absolute temperature and f the frequency. Such noise is best demonstrated inside the ordinary resistor where aggregation of quantized electrical charge carriers moves randomly due to thermal excitation.

Fluctuations in the number of charge carriers come into the role when the numbers of charge carriers are injected into certain volume independently and randomly in space or time. **Shot noise** is present in PN junctions and it is proportional to the direct current. Its spectral noise current density can be expressed as:

$$\frac{d(i)^2}{df} = 2eI \qquad (3.2)$$

, where e is the natural electrical charge and I the DC current.

The third kind of inherent noise is called **flick noise** which exhibits 1/f dependence. It happens when the carriers are captured and released in a characteristic time interval (exhibits the so called 1/f dependence). One example of such capture and release mechanism is the extra energy states introduced by dangling bonds in semiconductor devices.

3.1.2 External noise (miscellaneous)

Although inherent electronic noise is key to limiting the circuit performance, the noise pickup from environment plays a vital role in most real applications as well. It modifies also the baseline and is then superimposed onto the real signal. Miscellaneous kinds of sources contribute to it, such as digital activity like ADC sampling clock, data readout clock, or surrounding RF radiation, transients between trigger and readout, grounding on the same PCB, signal coupling from neighbors, power lines etc.

For example, the ground is in theory assumed to be a perfect conductor. However, in reality, it shows finite impedance and can form certain loop or loops to couple additional signal to the original one. Thus grounding or not and how to ground are important aspects of the circuit design as well as to reduce the other contributions to the external noise to a minimum.

In summary, noise modulates the baseline where the signal sits on. In turn, the baseline fluctuation is superimposed onto signals that are being measured. In order to obtain high S/N ratio (signal to noise), it is natural to amplify the signal and reduce the noise at the same time. However, in a real situation, it is always necessary to make compromises between them. For radiation detectors with avalanche amplification or photomultipliers, the signal can be amplified without amplifying the noise. Thus such detectors are ideal for improving the S/N ratio.

3.2 Noise analysis of an amplifier

The typical signal is a current pulse from the avalanche readout chamber of the TPC. The whole front end electronics set-up is demonstrated in figure 3.1. The detector itself is a capacitive device denoted as C_d in the figure. The signal is coupled to the amplifier through Cc and Rs. The signal after the preamplifier feeds the pulse shaper with a peaking time chosen to reduce noise and accommodate the counting rate. In the case where an ADC follows, the shaper also serves for limiting the bandwidth to avoid aliasing. In the front end electronics, the noise is normally evaluated as the equivalent noise charge (ENC), which is defined as the noise charge in units of electron charges when the S/N ratio is 1.

The noise estimation of such system can be fully described by a noise voltage source and noise current source. The noise voltage source can be from the thermal resistive components such as input resistors, resistive bias network or internal components of the amplifier. With the generally accepted assumption that the input device dominates the noise and the power consumption of the charge sensitive amplifier, noise can be expressed based on the discussion in the previous section.
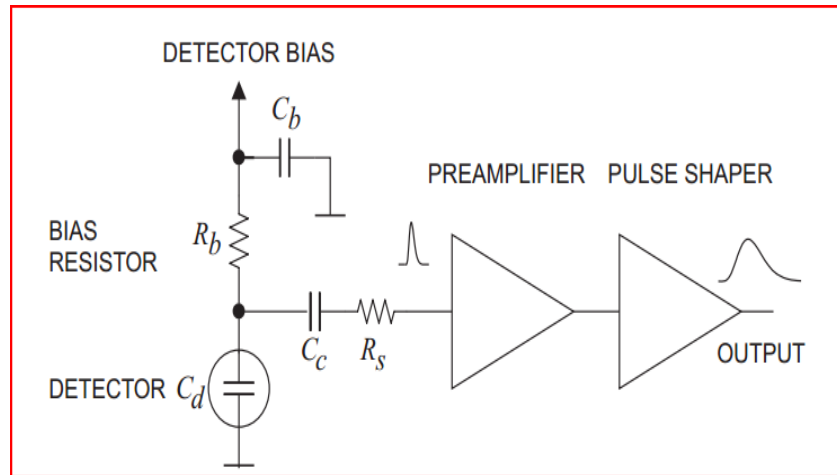
Figure 3.1 typical detector front-end electronics [3]

The output from the charge amplifier feeds to the pulse shaper ($CR-RC^4$ semi-Gaussian shaping). The transfer function in Laplace space can be expressed:

$$H(s) = \left[\frac{s\tau_0}{1+s\tau_0}\right]\left[\frac{A}{1+s\tau_0}\right]^4 \qquad (3.3)$$

, where τ_0 is the time constant for both CR and RC blocks, A is the DC gain of the integrator. The total RMS noise can be evaluated from the integral:

$$V_{noise} = \int_0^{+\infty} |v_o(j2\pi f)|^2 |H(j2\pi f)|^2 df \quad (3.4)$$

, where $|V_o|^2$ is the noise power density from the output of charge amplifier (CSA) evaluated in frequency domain. The noise circuit model of the CSA (named PASA which is the predecessor of the PCA16 chip studied in this thesis) can be found in [2], which is reproduced here for convenience:
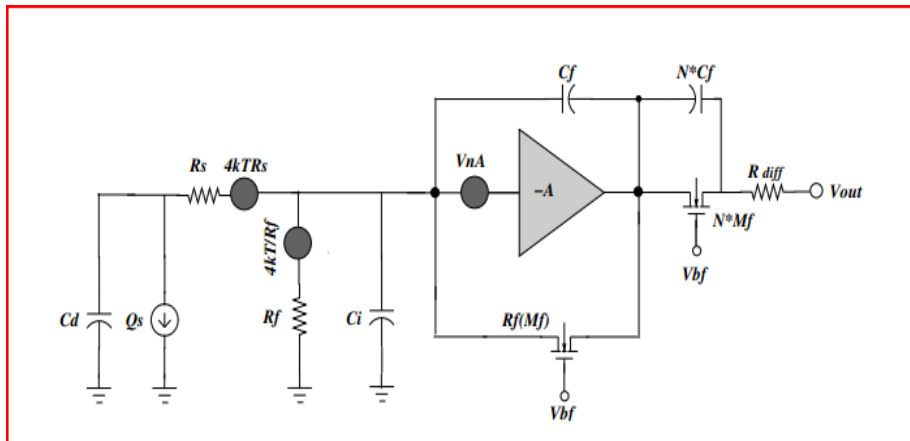

Figure 3.2 noise equivalent circuit of PASA (excluding pulse shapers)

Four major noise sources are considered here: 1. thermal noise from ESD resistive components; 2. Thermal noise from the feedback transistor (which works as resistor here to modify the time constant of feedback); 3. Channel thermal noise; 4. 1/f noise of the input transistor. Since the four mentioned noise sources are statistically uncorrelated, the total RMS noise can be expressed as quadratic summation of these four contributions (the expression can be deduced from [4] or found in [2] (there are mistakes in the paper for Eq.3.5 and 3.6 which I have corrected here)):

- 16 -

$$ENC_{R_s}^2 = 4kTR_s \frac{C_T^2 B(\frac{3}{2}, n - \frac{1}{2})n}{4\pi\tau_s q^2} (\frac{n!^2 e^{2n}}{n^{2n}}) \quad (3.5)$$

$$ENC_{R_f}^2 = \frac{4kT}{R_f} \tau_s \frac{B(\frac{3}{2}, n - \frac{1}{2})n}{4\pi q^2} (\frac{n!^2 e^{2n}}{n^{2n}}) \quad (3.6)$$

$$ENC_{th}^2 = \frac{8}{3}kT \frac{1}{gm} \frac{C_T^2 B(\frac{3}{2}, n - \frac{1}{2})n}{q^2 4\pi\tau_s} (\frac{n!^2 e^{2n}}{n^{2n}}) \quad (3.7)$$

$$ENC_{1/f}^2 = \frac{K_f}{C_{ox}^2 WL} \frac{C_T^2}{q^2 2n} (\frac{n!^2 e^{2n}}{n^{2n}}) \quad (3.8)$$

where k is the Boltzmann constant, T is the absolute temperature, n the order of shaper network, R_s the input resistive components connected in series, C_T the total capacitance at the input, $B(k,j)$ is the Beta function, τ_s peaking time, R_f the feedback resistor, gm is the trans-conductance of input MOS transistor, K_f is the 1/f noise coefficient related to the CMOS process used, C_{ox} the gate oxide capacitor and W, L is the gate width and length of the input transistor respectively, q is the natural electric charge. From equation 3.5 to 3.8, it is clearly shown that the parameters we can control are: the total capacitance, temperature, peaking time, while other parameters are fixed when the chip has been manufactured.

Based on the calculation results in [2], it is shown that Eq. 3.5-3.8 contribute to 343, 92, 174, 4 ENC electrons respectively in PCA16.
Total noise can be expressed as:

$$ENC_{tot}^2 = ENC_{R_s}^2 + ENC_{R_f}^2 + ENC_{th}^2 + ENC_{1/f}^2 \quad (3.9)$$

And the total *ENC* from random intrinsic sources gives around 395 electrons. It should be noted that I have not full control over all the process dependent data input for the calculation so these absolute values have to be interpreted with caution although they agree well with the measured results.

3.3 The resolution in the Analog to Digital converter, ADC

Besides the PCA16 chip, another key component is the ADC in the ALTRO chip. Noise sources associated with the ADC are input referred noise due to thermal noise of physical devices, quantization noise due to the finite resolution of the ADC and distortions due to the aliasing sampling etc. All of these account for quoting the effective number bits instead of nominal value. Detailed definition of the ADC and various concepts can be found in ref.[5]. According to equation 74 in [5], the noise from the discrete ADC scale can be evaluated in (LSB):

$$ADC_{noise} = \frac{FSR}{2^{ENOB}\sqrt{12}} \quad (3.10)$$

, where *FSR* stands for the full input scale, *ENOB* the number of effective bits. Take the ENOB value as 9.7 and we obtain a noise from ADC is 0.355 ADC counts. If we assume the noise from PCA16 and ADC is statistically independent, the total noise in ADC counts can be calculated as 0.481 ADC counts (LSB) at 12mV/fC conversion gain and 120 ns peaking time.

Various kinds of noise sources contribute to the final measured RMS noise of the system. However we assume that the digital signal after ADC coding is invulnerable to noise. Generally speaking, this features one big advantage once the signal has been digitized in any kind of modern digital electronics application. Careful attention should be paid to large systems, since rare bit changing events may happen in particular if the electronics is placed in radiation environments. Various kinds of error checking and correcting mechanisms should be implemented to avoid them.

3.4   RMS Noise measurements on the front end card

The noise was measured as the RMS of pedestal values, i.e. the DC level corresponding to no input signal. During each noise measurement, 300 events of 1000 samples each were taken and the RMS value was calculated. To reduce the noise from the environment, all 128 input channels of FEC77 were situated inside a grounded metal box acting as a Faraday cage. The box shields very effectively against external pickup from the environment. Such external pickup is particularly problematic when the front end card was connected with long Kapton cables for signal input. The shield box did not play any important role when the front end card is empty loaded, i.e. without the Kapton cables. A sample pedestal run result is presented in figure 3.3 (FEC77 empty loaded and situated inside the shielding box).
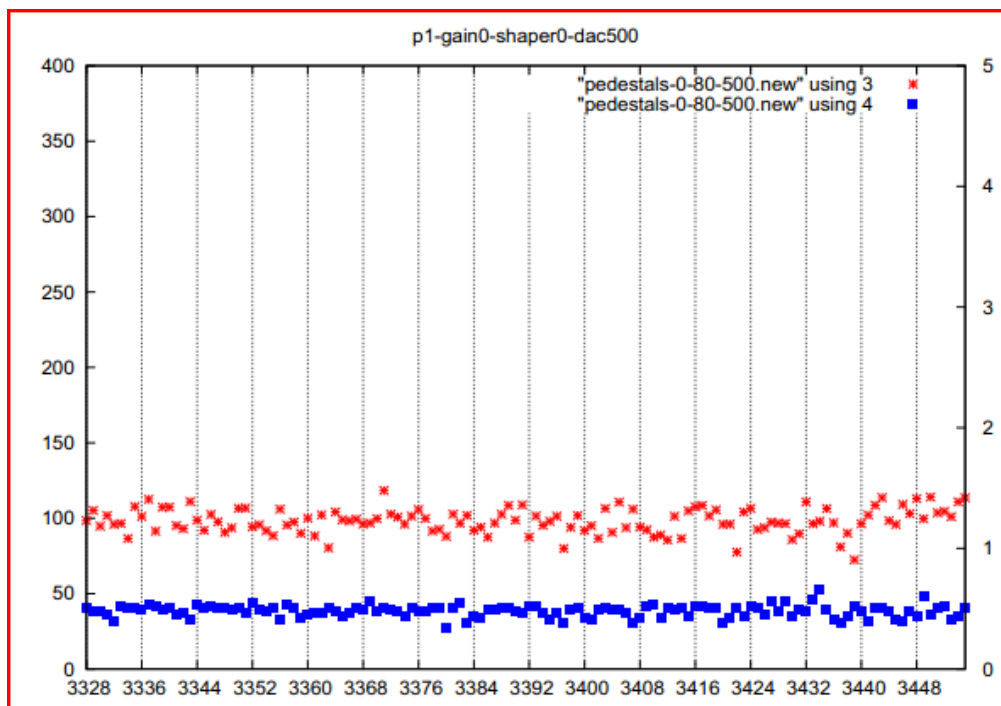

Figure 3.3 RMS noise and pedestal distribution gain@12mV/fC, peaking time: 120ns

In figure 3.3, the x-axis is the channel number corresponding to 128 channels on FEC77. The left y-axis is the mean pedestal value (red asterisks), and the right y-axis represents the RMS noise (blue squares). Peculiar points are due to the bad connection or variation from channel to channel. Figure 3.3 shows the best case in terms of noise among various configurations. The worst case is shown below in figure 3.4 for illustration.
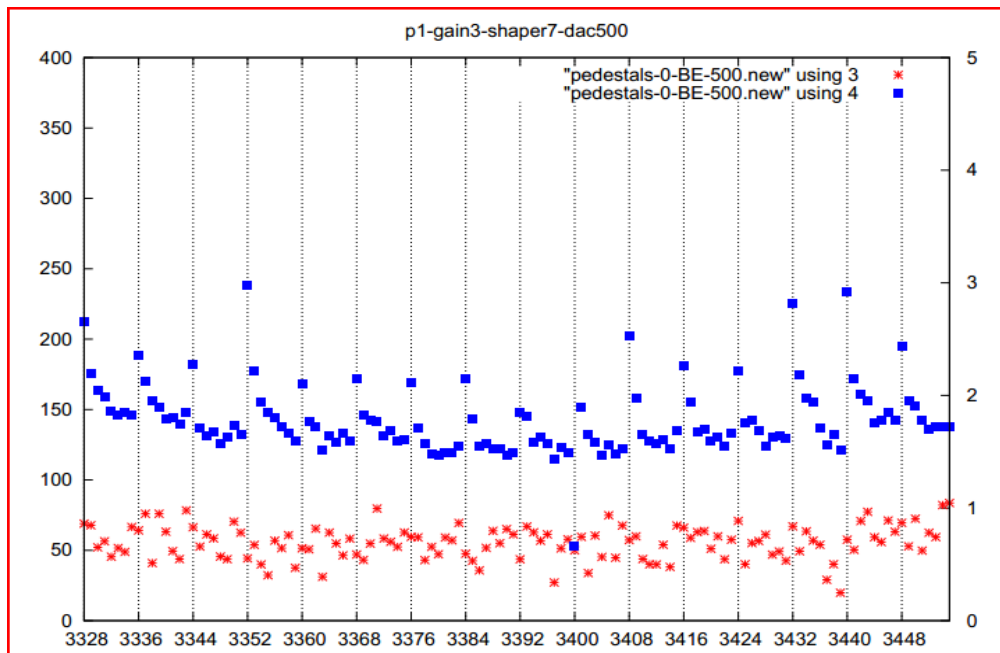
Figure 3.4 RMS noise and pedestal distribution gain@27mV/fC, peaking time: 30ns connected with Kapton cables.

Generally, the system noise increases as the conversion gain increases when measured in ADC counts. In the units of ENC it should be the same as long as the amplifier noise is considered. When the FEC77 card is empty loaded and the system noise is evaluated by the unweighted average (the explanation will be given below) of all 128 channel values, it shows 0.456 ADC count noise at 12mV/fC and 0.744 ADC counts at 27mV/fC in contrast.

As we discussed in the previous sections (Eq. 3.5-3.8), the noise level depends on the resistors and capacitors connected, which contribute to the values of R_s and C_T respectively. Such issues were investigated with a protection card (the card was designed for testing different kinds of input protection, thus the name). Various configurations were produced on this protection card (0, 24, 50, 200, 900 ohm for addition to R_s and with 0, 33, 66, 100, 133pF for C_T). The protection card used for this purpose is shown in figure 3.5. The system noise versus both capacitance value and resistance are plotted in figure 3.6 and figure 3.7 respectively.
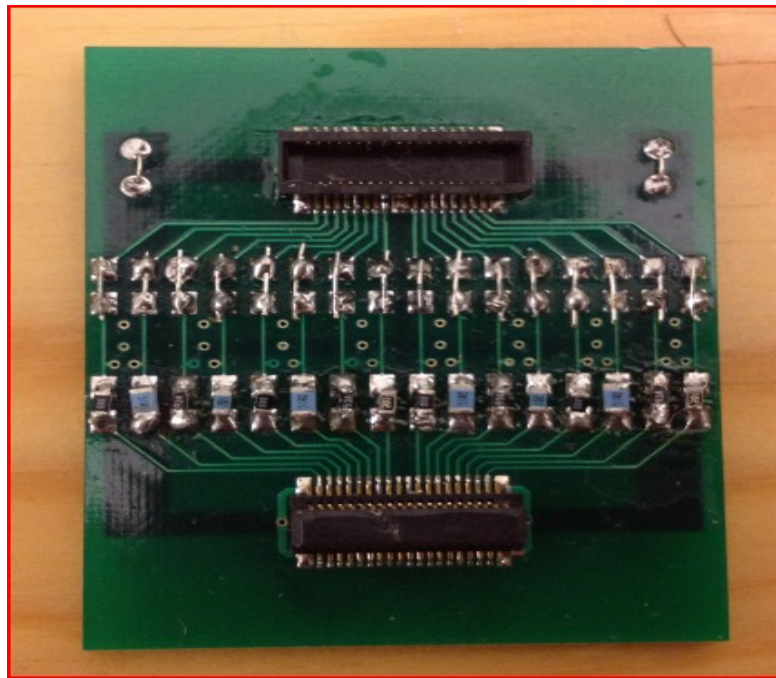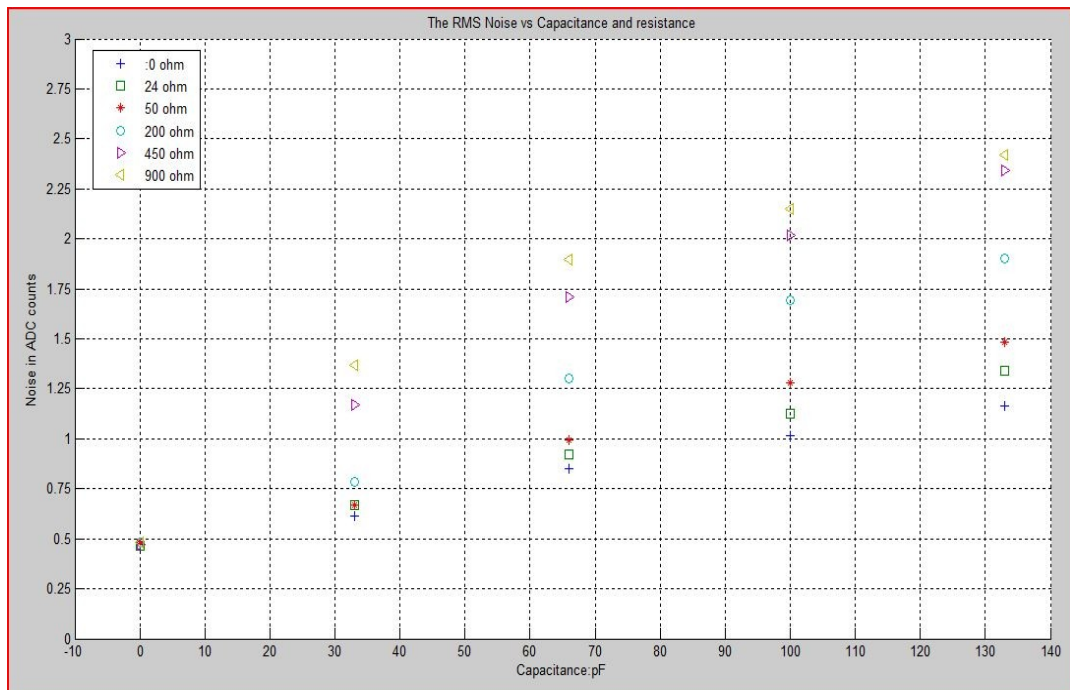
Figure 3.5 protection card

Figure 3.6-1 system noise versus capacitance (noise measured in ADC counts)
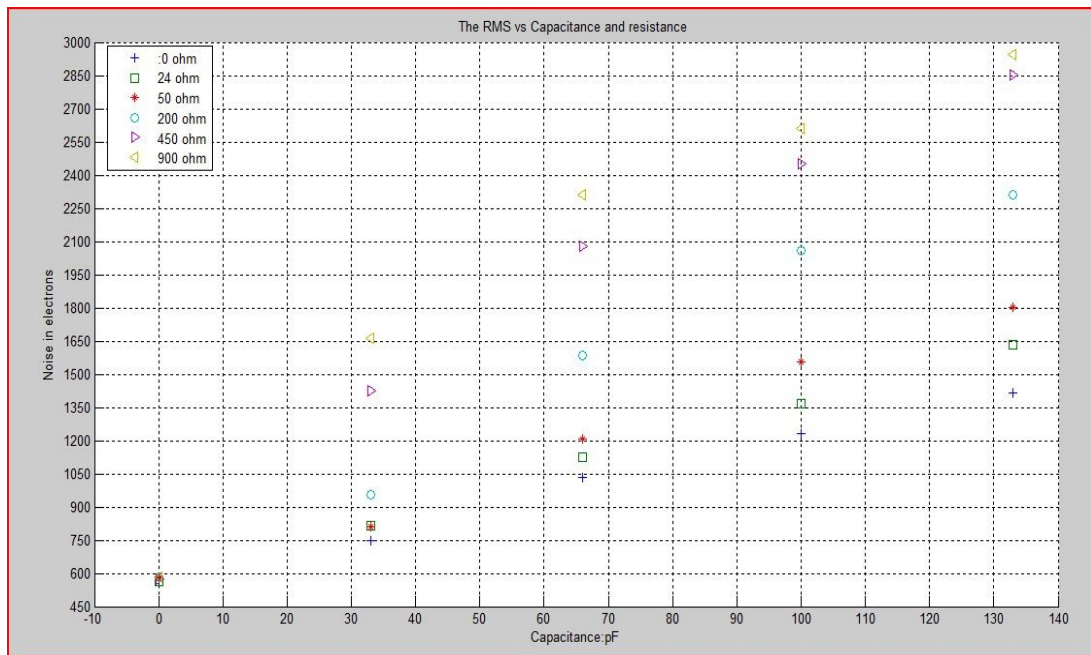
Figure 3.6-2 system noise versus capacitance (noise measured in ENC electrons)

As we can see from figure 3.6, the system noise increases approximately linearly with the capacitance. It can be explained from the Eq. 3.5 and 3.7. Both of them are the major contributors to the system noise which depends approximately linearly on the total capacitance. For the fixed capacitance, the system noise increases with the resistance accordingly which is reasonable based solely on Eq. 3.5 where an increase with a sqrt (R_s) dependence is expected. At the point 0pF and 0 ohm (note that this is for external additional components), it shows the system noise around 0.456 ADC counts which verifies our calculated result 0.481. Based on the noise level we get with Kapton cable connected to the amplifier input, an equivalent capacitance of the cable around 30pF can be obtained through interpolation in figure 3.6.
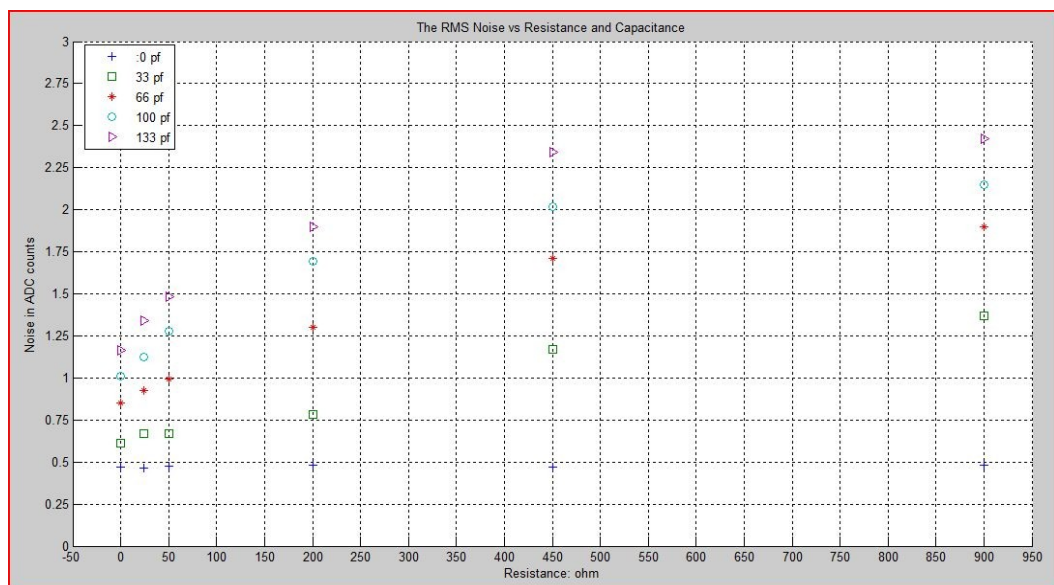

Figure 3.7-1 System noise versus resistance (noise measured in ADC counts)
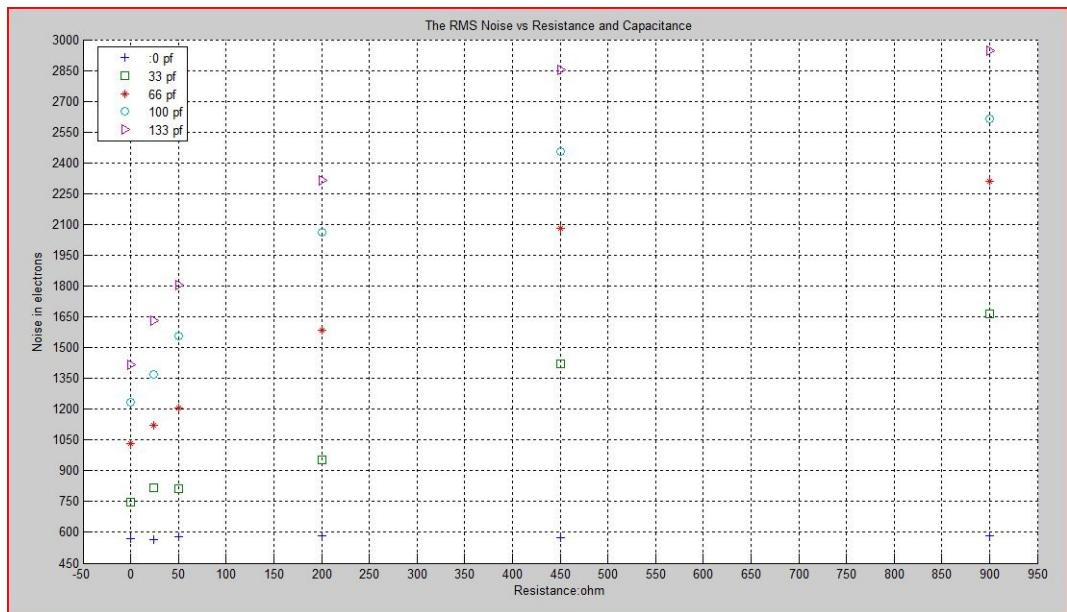
Figure 3.7-2 system noise versus resistance (noise measured in ENC electrons)

Another key role in the system noise is the temperature. One piece of TGP hyper heat conductive graphite was attached between the PCA16 and the ALTRO chip. It features 1000-1700W/m-K (several times better than copper). It shows around 0.15 ADC counts reduction in noise compared to the card without such material. Heat is equilibrated between two chips and is more efficiently cooled away by the much larger surface exposed to convection air flow for cooling. Figure 3.8 shows the material set-up. The material is marked with red ink. A special purpose of this test was also to study if the extremely good heat conductor (whose electrical properties were unknown to us) would transport external noise from the digital ALTRO chip to the analog inputs of the PCA16. This was evidently not the case and the conclusion was that the material can safely be used for cooling purposes.
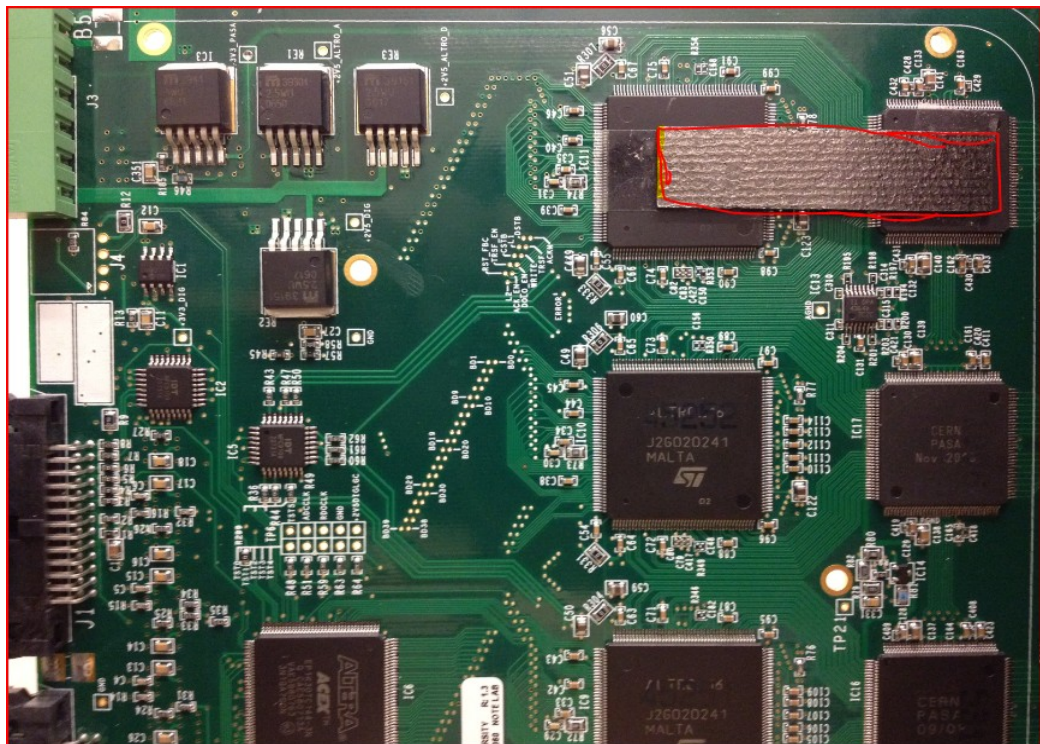

Figure 3.8 hyper heat conductive graphite

In figure 3.3, one may ask whether the noise level depends on the channel as observed in the protection card. It shows higher noise level for channels (ch3328, ch3336, ch3344 etc) near to ground route which can be observed more clearly in figure 3.4. Obviously there are patterns every eight channels. It can be seen that the outermost two channels in figure 3.5 sit on top of the copper ground in the Kapton cable. This ground is evidently noisy and one can see from the time structure of the noise that it comes from the digital activity in the ALTRO chip. The same question arises for the whole card. In order to study this, 128 data sets were collected with the FEC77 empty loaded. Each of the data set of channel number versus noise is fitted linearly. 128 slope values are added together to get the mean value. It shows zero mean slope value within the accuracy of 0.01%. One sample fitted plot is presented in figure 3.9.
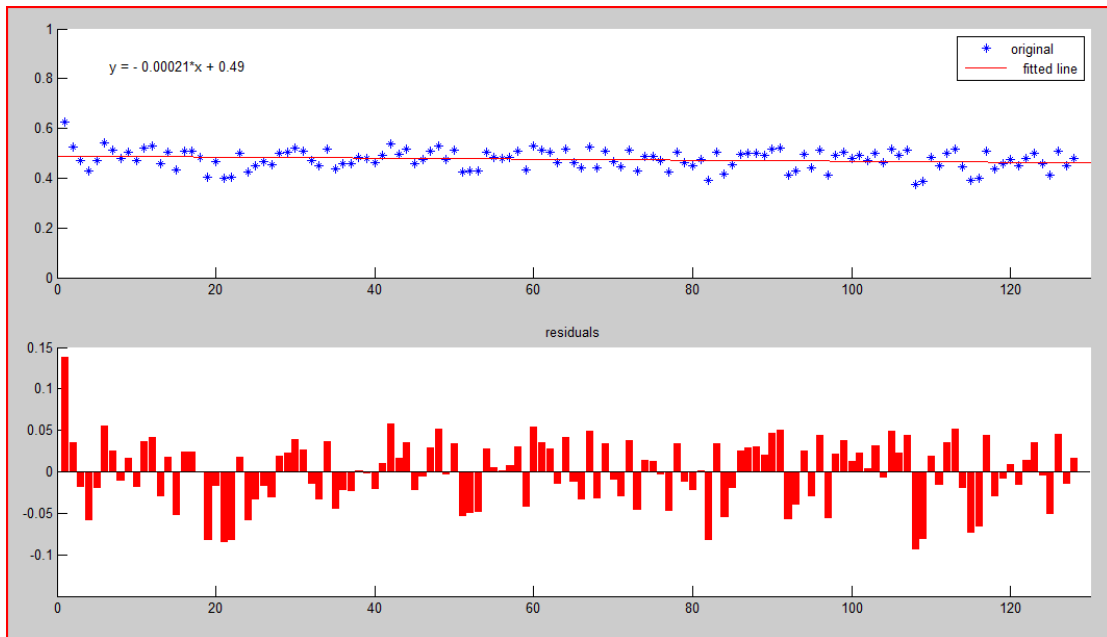

Figure 3.9 sample rms noise fit versus channel number. The noise values are in ADC channels.(12mV/fc,120ns)

So the system noise shows no systematic trend on the FEC card level.

In summary, the system noise depends on temperature, resistors and capacitors connected. It shows more sensitive to the capacitance since it depends linearly from Eq3.5, 3.7, and 3.8. Measurements reveal that there is no systematic behavior on the board level. Normally the noise decreases (evaluated in ENC) with conversion gain as the ADC noise is the same for all gains. The peaking time affects the noise in the way indicated by Eq.3.5, 3.6, and 3.7 i.e. longer peaking time gives lower noise.

Various kinds of capacitors within pF scale were used for calibration purpose. The nominal value and its tolerance claimed by the producer are not adequate for calibration purpose. It becomes necessary to know the value as well as one can achieve. Two indirect measurements on the capacitors used for calibration are presented in the appendix 1.

3.5   Summary

The noise level limits the resolution of a system. Normally a system works under comprises

based on various noise considerations. Thermal and device noise contributes dominantly in our system. Total load capacitance and resistor account for the large part of system RMS noise as we analyzed. Since the Kapton cable contributes to the total capacitance a lot (in the noise term, around 40%), it will be removed from the future readout system as we will discuss in chapter7.

Because the front end electronics contains the charge sensitive amplifiers, normally we need a coupling capacitor to couple signal to inputs. Such capacitance introduced is key to our calibration purpose. The test results and description of the calibration are presented in chapter 6.

References

[1] "Design of analog CMOS integrated circuit" by Behzad Razavi, first edition, ISBN-10:0072380322

[2] "The pre Amplifier shaper for the ALICE TPC detector" by H.K. Soltveit etc. Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment. Volume 676, 1 June 2012, pages 106-119.

[3] "Review of particle physics" by Particle Data Group, Particle detector at accelerator from particle data group. Section 31.8: Low-noise electronics. 2012, article 010001 in volume 86 of Physical Review D.

[4] "Low-noise wide band amplifiers in bipolar and CMOS technologies", by Z.Y. Chang, W.M.C Sansen, Kluwer Academic publishers, 1991

[5] IEEE standard 1057-2007

Chapter 4 The DAQ system

In this chapter, a short description about the Data acquisition system (DAQ) is given both in software and hardware. In the section 4.1, a short introduction is given. The hardware description is given in section 4.2, and software description is presented in another separate section. The chapter ends with beam test setup at DESY with pictures and final remark.

4.1   Introduction

The DAQ system is based on ALICE TPC system. It aims at a general purpose readout system for radiation detectors and the main components consist of front end card (FEC), readout control unit (RCU) and two LINUX PCs. The FEC is connected to the readout control unit through a backplane, where it has 32 slots to hold 32 FECs which communicate with the RCU on a 40 bit wide parallel bus. The acquired data is transmitted through optical fibers at 200MB/s to the Data Readout Receiver Card hosted by the DAQ computer through a PCI adapter card. One switch provides the local network for DAQ devices, and the other serves the interface to internet connection. The experimental setup block diagram is showed in figure 4.1.
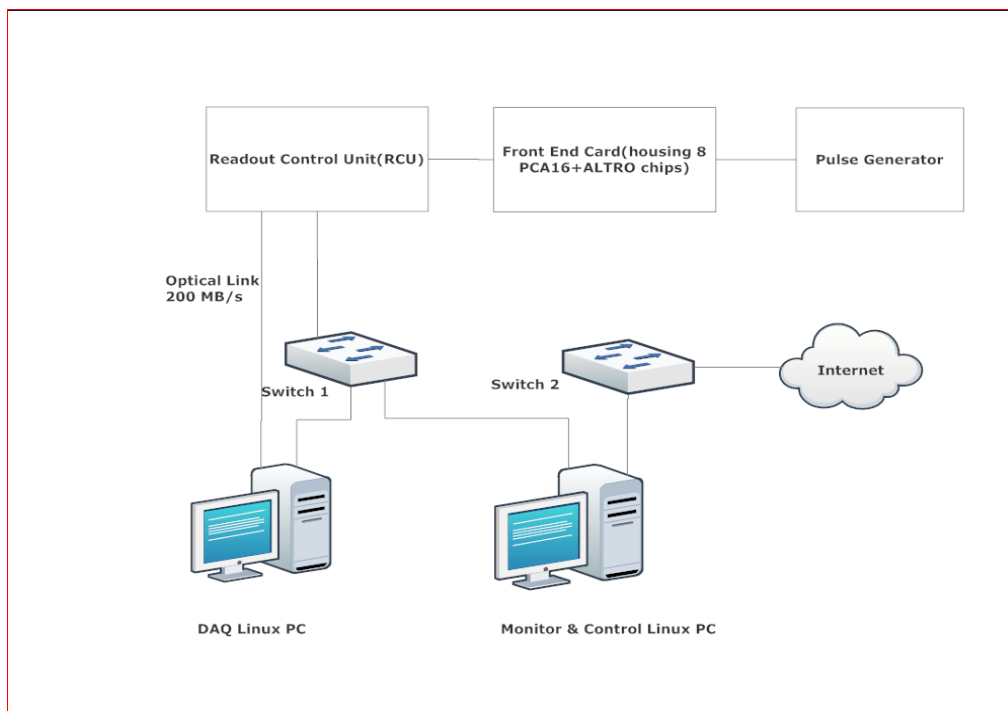

Figure 4.1 system block diagram

In the current project, it serves the test setup for the FEC77 (77 the number of the card). Such setup is a general purpose readout system in the sense that it can handle different pulse signals from various kinds of detectors (sources). This flexibility is achieved by the programmability of the PCA16 chip.

4.2   Hardware setup of the system

The hardware system consists of one FEC, backplane, Readout Control Unit (RCU), one PC

used as DAQ computer, one PC as monitor computer and cables (fibers) for data transfer for uploading and downloading, one AFG signal generator, and four low voltage power supplies to provide power for both RCU and FEC. The overview of system is showed in figure 4.2.
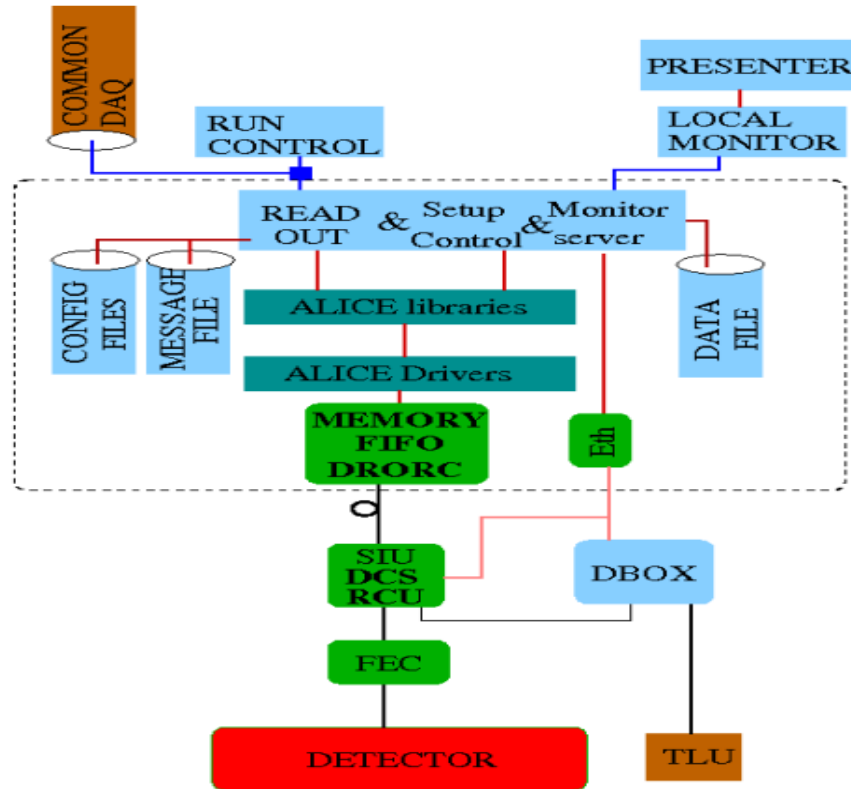

Figure 4.2 overview of the DAQ system [1] (the detector and TLU were replaced by a pulse generator in our test)

The main components of the system are briefly described in the following:

- ✓ **FEC**

   One FEC contains 128 channels which are well isolated from each other. 8 PCA16 and 8 ALTRO chips are hosted on each board. The charge signal from a detector sensor pad is coupled to the input of a PCA16 channel. The charge pulse is converted to a voltage to get amplified, shaped for the fully differential ALTRO input. The following ALTRO chip undertakes the digitization and processing task. More detailed description is given in chapter 6.

- ✓ **RCU**

   The RCU controls the readout from the FECs via 40 bit wide backplane bus. The initialization and monitoring of FECs are also accomplished here. It further packages the data collected from the FEC and send them through an optical link to the DAQ computer.

- ✓ **DAQ and monitor PC**

   The data readout receiver card is placed inside the DAQ computer. The main task for DAQ computer is to acquire data sent from optical link. The monitor computer is used for local control, monitoring and result presenting. The two computers are connected within the same LAN. The control & monitor computer also has a DHCP

server to serve the IP address for local devices connected if necessary. Both of them are running on the Linux system.

✓ **Trigger and signal input**

In our experiment setup in the laboratory, the trigger and input signal generation is done by a two channel pulse generator. Channel 1 is used as the trigger source for the system. Channel 2 is used for the pulse signal to mimic the induced detector signal.

4.3   Software setup of the system

The software system is divided into different blocks: the data taking block, monitor block, data presenter & analysis block and blocks that interface between them. The data taking block includes the driver and libraries for DRORC and a C program called readout program for the readout of the front end electronics and data storage.

The data presenter & analysis block contains a presenter (written in ROOT and C++) and a graphic user interface written in Java. Both of them are shown in figure 4.3 and figure 4.4.
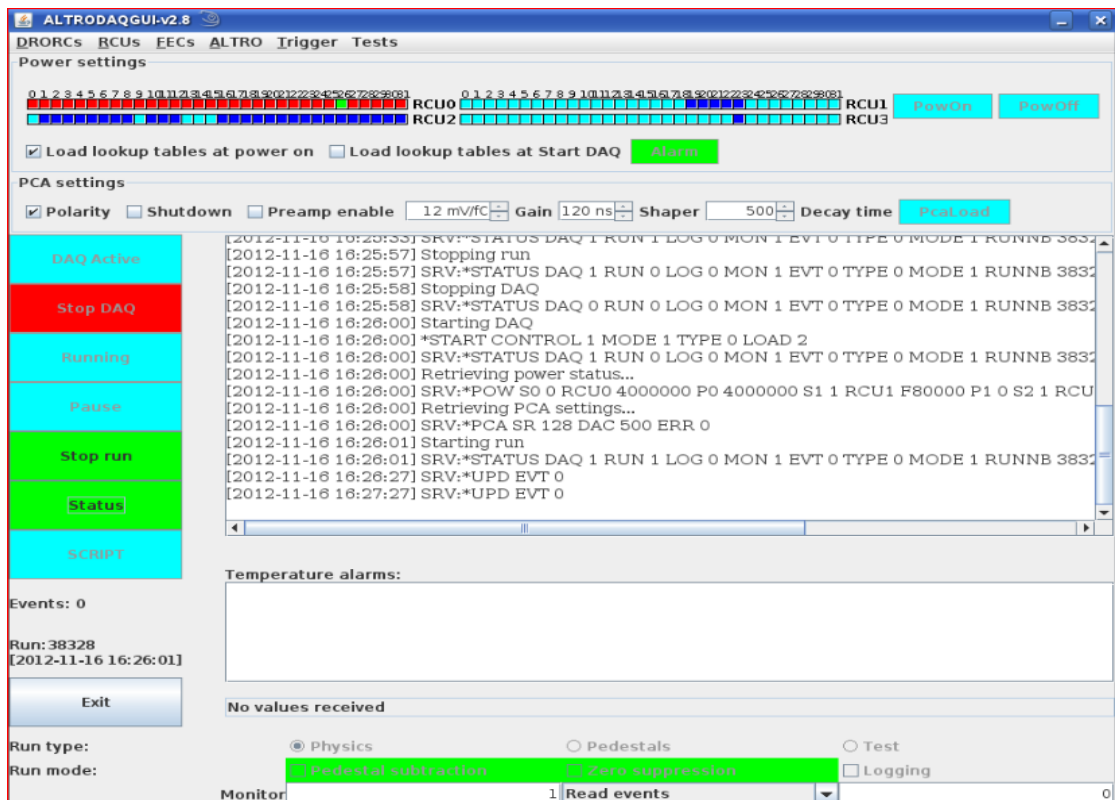

Figure 4.3 DAQ panel for run control and detector control, mainly PCA16 settings.
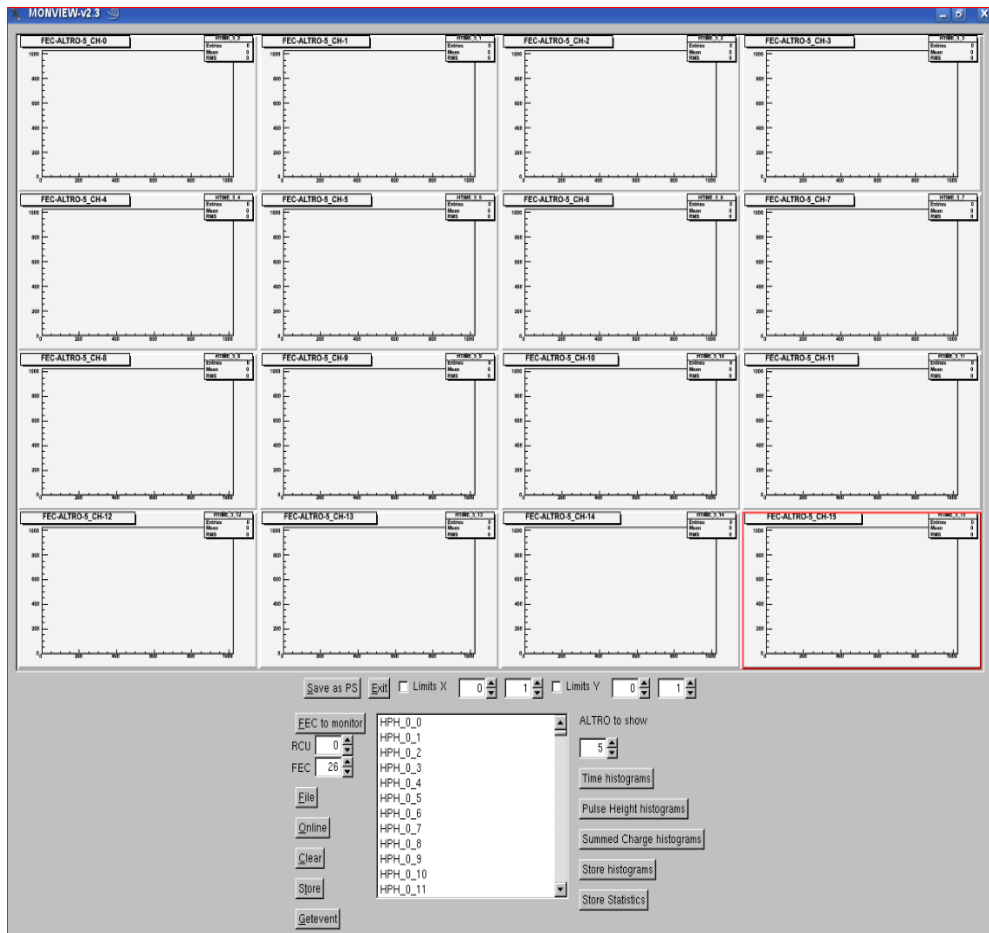
Figure 4.4 presenter interface

The interface module includes one server program called ilcserver and one monitor program called "monhandler". The ilcserver is the interface between control GUI and the readout program. Its main task is to decode the package received from readout program and interpret the text command received from control panel. The ilcserver is able to connect to one or more user interfaces.

The monitor program communicates by text commands and messages with the monhandler (a thread started by the readout program). It can also read data from files for playback purpose. The readout program sends an event to the monitor program when it gets a request for a new event. The monitor program fills histogram and stores them in root format.

The presenter program can display various kinds of histograms created by the monitoring task as mentioned above. Such histograms include pulse height, ADC counts versus time, Max ADC COUNTS versus channel (top three most frequently used) etc. It can request a new event from the monitor thread started by the readout program through the monitor program. Data flow and commands are shown in figure 4.5.
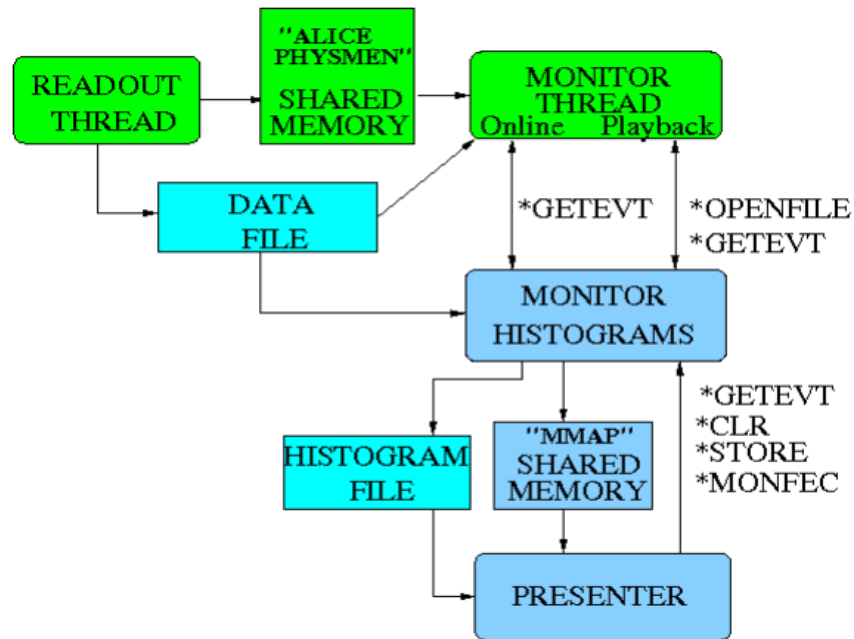
Figure 4.5 command and data flow in the monitoring system [2]

The GUI program is the control interface between the user and the system. Basically, it can be divided into four functional blocks: control block, configuration block, monitoring block and mode selection block. In the control block, one can power on/off the FECs, start and stop the data taking, execute a script etc. In the configuration block, one can change the settings of the FEC such as polarity, preamp enable, peaking time, gain, and decay time of the PCA16. It is also possible to set the parameters for zero suppression and the number of pre and post samples to be used (meaning of these ALTRO parameters are detailed in chapter 6). The monitoring block contains the function of temperature monitoring and a place for displaying text regarding as the system status. The system is able to work within three different modes which can be set through the GUI interface. These three modes are:

- ✓ **Physics**: for normal data taking, in this mode the readout program configures a physics trigger. The normal pulse histogram can be displayed. Pre and post samples around pulse can be set. The pedestal subtraction and zero suppression for data reduction purpose can be done too.
- ✓ **Pedestals**: Pedestals are calculated in this mode. The pedestal values are used for pedestal subtraction when doing physics run. In each configuration setup for PCA16, such pedestal run should be done. It has to be repeated on a regular basis and whenever the pedestals are expected to have changed. Pedestal itself contains the information about environment of the signal will be acquired (described in detail in chapter6).
- ✓ **Test:** for the expert to test memory or registers and data transfer.

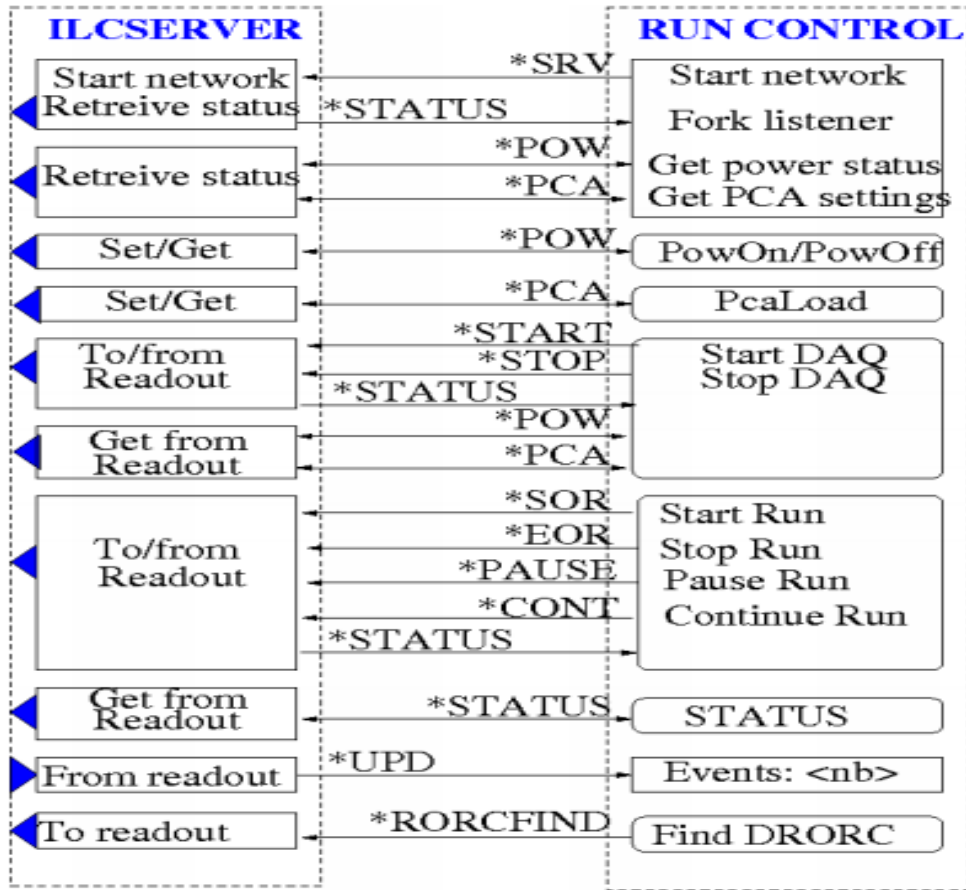Figure 4.6 shows the communication between GUI program and ilcserver.

Figure 4.6 Control GUI communications with the ilcserver [3]

4.4 Beam test setup

In this section, a summary of beam test setup at DESY in Hamburg is given. The purpose of the test was to study the performance of readout chambers (GEM) for the LC TPC (prototype). In the setup, two rows of FECs were used. At the beam test, the trigger was formed by scintillators and was distributed to two RCUs. FECs with temperature sensors were mounted at every fourth FEC position. The whole electronics was cooled with compressed air to provide suitable working conditions for the electronics. In contrast to the single FEC readout system used for the work in this thesis, the readout at the full scale beam test setup requires flexible Kapton cables to connect to the detector. All low voltage cables (for powering up electronics) were mounted in two aluminum rings to provide the needed mechanical stability. The system was controlled in a hub 10 meters away. The pictures of the real setup are shown below.

Figure 4.7 FECs connected to TPC

Figure 4.8 FECs fully connected with RCU and LV-power

In conclusion, such setup as in figure 4.7 fulfills current measurement task for about 5000 channels of TPC readout with GEMs.

References

[1] "http://www.hep.lu.se/eudet/daq/doc/overview-v4.0.pdf"
[2] "http://www.hep.lu.se/eudet/daq/doc/presenter-v2.2.pdf"
[3] "http://www.hep.lu.se/eudet/daq/doc/gui-v2.8.pdf"

Chapter 5   Amplitude estimation due to phase shift of sampling ADC

As we will see in chapter 6, the output pulse from analog amplifier is characterized by a real value function known as Γ_4 function. The amplitude of the pulse represents the charge dumped into the input of the charge amplifier. Thus it is important to calibrate the system, i.e. to determine the relation between the amplitude and the input charge. The digitization of the analog pulse and the phase shift between the ADC sampling clock and the pulse arrival time makes the calibration a non-trivial problem.

5.1   The mathematical description of the pulse

Pulses from various detectors are analog in nature and can be described as real value functions. Each kind of detector is characterized by a family of functions with several free parameters. In our case, the pulse shape can be written analytically in the form of:

$$v(t) = Baseline + Ae^4 \left(\frac{t - t_0}{\tau} \right)^4 e^{-4\frac{t - t_0}{\tau}} \qquad (5.1)$$

Where *Baseline* is the zero level (also called pedestal) from where the pulse grows, A is the amplitude, t_0 is the starting time of pulse and τ the peaking time. Figure 5.1 shows one pulse, simulated with Matlab with *Baseline*=0 and normalized amplitude. Other parameters can be read from the figure:
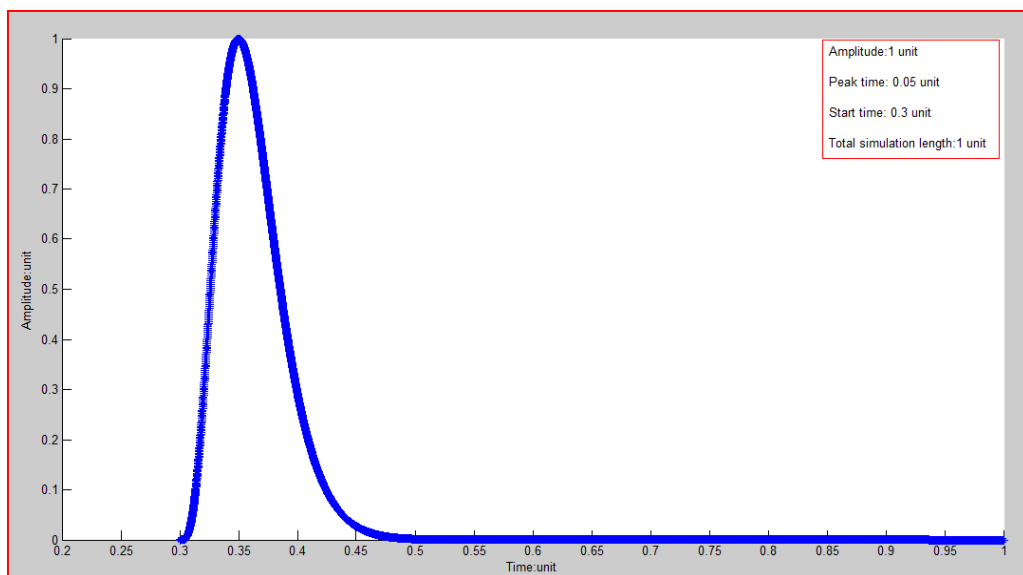

Figure 5.1 Pulse described by formula 5.1

Any pulse, continuous in time can be viewed as being sampled in an infinitesimal step or equivalently at an infinite high sampling clock rate. According to Nyquist-Shannon sampling theory, the sampling clock frequency is not necessarily infinitely high in order to retrieve the complete information from the original pulse. Such finite samples used to describe a pulse can be viewed in high dimension [3]. Therefore, a continuous time pulse can be represented in an infinite dimension space as a point. If we use N samples from such pulse to represent the pulse, it can be viewed as one point in such N dimensional space.

Due to phase shift we can get a set of samples, which can be represented in N dimensional space as the same number of points. Such different points in higher dimension space have the same pulse identity in the time domain. Based on the sampling theory mentioned

before, we can safely draw the conclusion that, there must be invariant properties associated with these points in higher dimensional space. A detailed description of this idea can be found in [1] and [3]. These points in N dimensional space are from now on denoted as representative points since they represent the pulse. Representative points in higher dimensional space can be fitted as we do curve fitting in lower dimensional space. The fitted curve is called representative curve. As the phase shift happens more and more, we can acquire more representative points in high dimensional space. Any invariant property associated with our fitted curve can be used as the parameter estimation of the pulse through tuning of the coefficient.

In the current case, we fit representative points with a "line" in such hyper space. It can be simply expressed as:

$$\sum_{i=1}^{n} a_i s_i = A$$

(5.2)

Where n is the number of samples we will use, and a_i is the coefficient which will be determined from simulation, A is the normalized amplitude. When the error associated with A exceeds a predefined value, more As can be chosen to reduce the error. Such segmentation handling is similar as we approximate a curve using segmented straight line.

Due to the phase shift, the real peak value is always hidden from the obtained digitized values (sample values). In a real experiment we cannot expect the same pulse occurs even twice. In our current case, trying to calibrate the amplifier response by constant standard pulses, we should measure the same amplitude every time if the sampling frequency were infinite since the pulse is provided from a high quality signal generator. Thus we can get a large number of identical events, and the maximum value of such digitized pulses can be picked out to get the statistical distribution of maximum sampled values. Better understanding of such distributions can also be used to correct the data in a statistical sense.

5.2   Simulation with Matlab

A detailed algorithm description and motivation for the simulation can be found in [1] and [3]. Here I only mention the necessary points in order to present the simulation and specifically chosen parameters are also mentioned. In figure 5.2, the hidden peak problem is demonstrated.
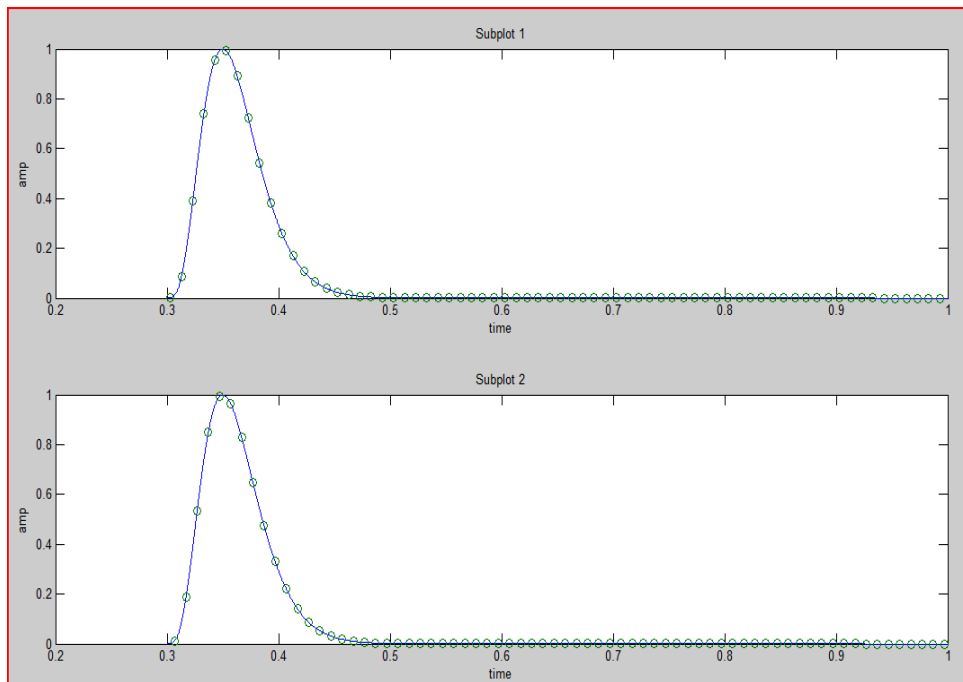
Figure 5.2 hidden peak problem due to asynchronous sampling clock with signal starting time. In the upper panel, the phase shift is chosen as 0.03 units, and sampled at 0.01 intervals. In panel 2, the phase shift is 0.07 at the same sampling rate.

In the following simulation, 1 unit duration is sampled at 100 0000 intervals to simulate the analog pulse. Such pseudo analog pulse is called the pulse later on. We will sample the pulse at 0.01 units so that every step still has 10000 samples inside to suppress the side effect of such pseudo analog pulse. The phase shift is simulated in a small step (0.0001 unit) shifted from the starting of the pulse within one sample interval (0.01 unit). The amplitude error (taken as the deviation of highest sample value from the true amplitude) with regard to phase shift is plotted in figure 5.3.
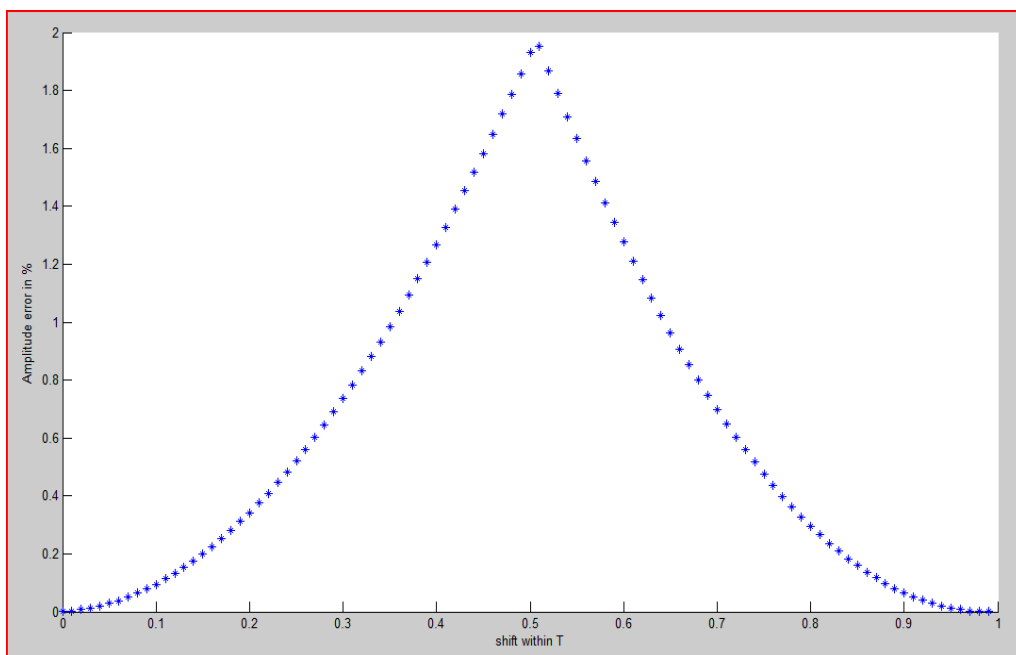

Figure 5.3 amplitude errors as a function of sampling phase shift (in fraction of a sampling period T).

As we can see from figure 5.3, the error in percent can be around 2% before we use any

algorithm to estimate the amplitude in this simulation. It should be noted that the magnitude of the error depends on the sampling rate relative to the rate of change of the voltage of the pulse. In this simulation of principles, the sampling interval is about 10% of the FWHM of the pulse. In our measurements reported in chapter 6 the sampling intervals are about 4 times longer and thus the maximum error is much larger than 2%.
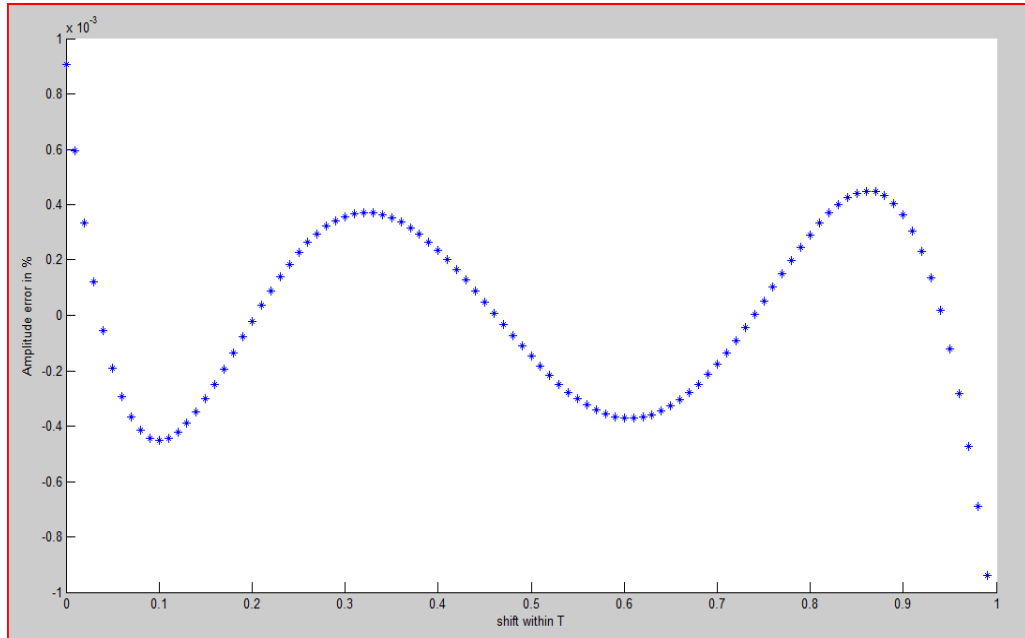

Figure 5.4 estimated amplitude error versus phase difference. 5 samples used to estimate the error.

Compared with figure 5.3, the amplitude residual error is greatly reduced when we use the estimation algorithm based on equation 5.2. The maximum error is below 0.001% in absolute value. It shows that the maximum errors happen around the phase shift 0 and 1. Since we employed the same settings to obtain both figures, the distribution can be roughly understood by that the optimal curve tries to fit all the representative points including the points around peak error in figure 5.3. So the maximum error happens in phase shift 0 and 1 roughly in figure 5.4.

Based on the coefficients matrix, we think that the amplitude estimation can be done with desirable precision. Since in reality it rarely happens that pulses have the same shape or parameters more precisely, the best case is that pulses come from the same family and the parameters vary a little. Therefore, the knowledge of the amplitude estimation versus parameters variation should be obtained. In our case, totally four parameters namely baseline, amplitude, peaking time, starting time, should be taken into consideration. The baseline is stable (see chapter 6) and can be subtracted so it plays no role in the estimation. Amplitude is not a problem either, because the samples obtained are proportional to the normalized one. So the relative error should be the same, but the absolute error can be proportional to the amplitude (bear in mind the maximum ADC counts is 1023). The sensitivity of estimation to other parameters like starting time, peaking time should be well investigated. In fact, the effect of the parameter starting time shift can also be understood by the phase shift in figure 5.4 if we keep the sampling clock fixed this time. Finally, only peaking time shift needs carefully study. Figure 5.5 shows the amplitude error versus shift in peaking time.
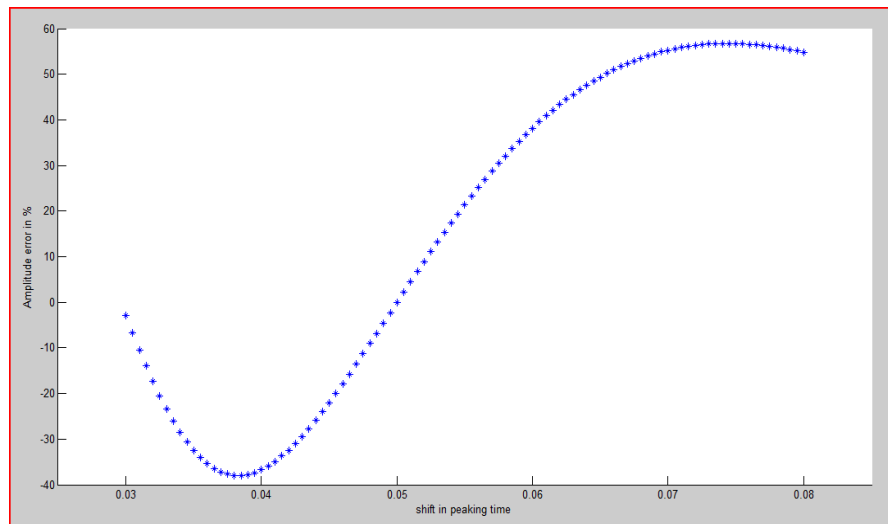
Figure 5.5 estimation errors versus variation in peaking time

From figure 5.5, the coefficients matrix cannot work with pulse with different peaking time. In other words, the matrix has little knowledge about the pulse family. So rescaling the data set is necessary to gain better estimation. From the other point of view, it also shows there is certain variation range if we relax the error requirements.

Basically, there are several ideas can handle this problem. Firstly we can try to find invariant of the pulse family so that every family member can transform to a standard pulse in order to use the computed coefficients matrix. But such transform should be invertible so that right amplitude can be obtained. Secondly, instead of transforming to a standard pulse, we can build a library of pulses where each of them associates a set of coefficient matrix. The estimation of amplitude can be based on such searching library to find the right matrix to compute. Thirdly, we don't need a library explicitly but we could build the knowledge of pulse family into a neural network which can handle such problem elegantly. One drawback with such method is that it needs more computation power and cannot be used as online data analysis when the occupancy of signal is very high.

In the following part, the amplitude estimation task will not go further here in those ways proposed above. A method based on the statistics of maximum sampled values of each sampling cycle is utilized. One point would be mentioned here that in real research experiment, this method cannot be a valid way to estimate amplitude. Because normally such maximum sampled value distribution is not available. However, it can still be used as an assistant way to correct the data in a statistical sense. For the current calibration purpose (topic in chapter 6), this is a valid way since such maximum sampled value distribution is available as standard pulses come from the pulse generator.

In the section 5.3, the simulation and real data distributions are presented and analyzed.

5.3   Maximum sampled value distribution

The simulation is based on the pulse described in previous sections. During every sampling cycle, the maximum sampled value is recorded. In the first place, the distribution is obtained when the samples are from an ideal pulse (there is no noise to the signal). During the second part, additive white Gaussian noise is added to the signal to simulate the signal in reality. Finally the real maximum sampled value distribution is presented.

Since the sampling period relative to the pulse duration determines the width of the maximum sampled value distribution. In figure 5.6, the maximum sampled value distribution is presented at different sampling period. The following sampling periods are based on 1/2, 1/4, 1/6, 1/8 of the pulse FWHM. 1/4 of FWHM is close to the situation when the PCA16chip is in the 120ns peaking time setting and the ADC sampling is done at 20MHz. To simplify the computation the starting time of pulse is fixed at 0, and the peaking time 0.05. So the result simulated pulse is expressed as:

$$v(t) = e^4 \times (\frac{t}{0.05})^4 \times e^{-4\frac{t}{0.05}} \qquad (5.3)$$

Other parameters are the same as before.
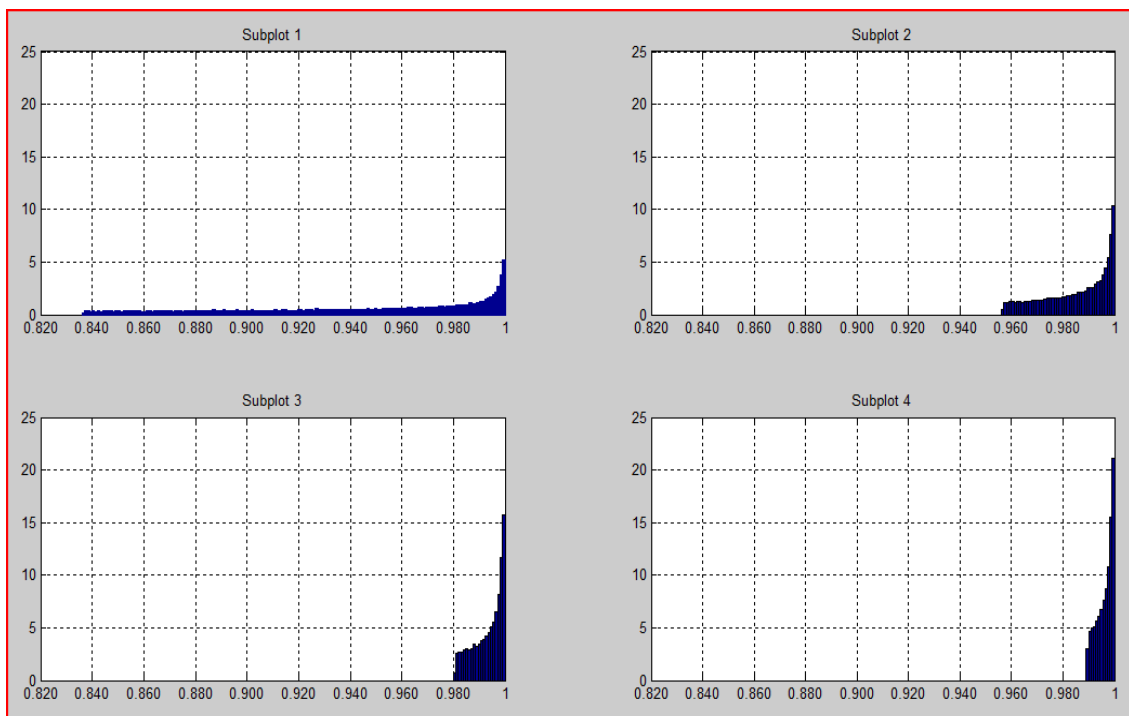
Figure 5.6 maximum sampled value distributions at different sampling rate. All plots are normalized to the same scale for comparison visually. The *x* axis is the normalized amplitude; *y* axis is the frequency in %.

In figure 5.6, the sampling frequency increases from subplot 1 to 4. It is obvious that the maximum sampled values are squeezed into a small fraction (i.e. becomes more accurate) as the sampling frequency increases. This effect can be understood both qualitatively and quantitatively. As the sampling period decreases, the resolution to find the peak value also increases, thus the obtained amplitude values are more accurate. On the other hand, the lowest boundary of such distribution (the lowest amplitude value in the distribution) can be calculated from two points between which the time interval equals the sampling period but gives the same pulse height at both points. One way to explain the distribution is: assuming we can project the time onto the pulse curve, the places where equal distance interval at curve has larger time projection should get more chance to be sampled. Since we assume the time shift within one sampling period is uniformly distributed in our simulation (i.e. all phase shifts are equally probable), the result is reasonable. This explanation is also confirmed in figure 5.12 from the observation of real data. Here it is motivated to use the value that happens most frequently as the estimation of peak value if we ignore the quantization error due to sampling.

In the following part, additive white Gaussian noise is added to the ideal pulse curve to simulate the real situation. The motivation here is to check how well the maximum sampled value distribution can survive under such conditions.

For the comparison with figure 5.6, the same parameter set is chosen. And the result noise pulse is presented in figure 5.7. The result maximum sampled value distribution is presented in figure 5.8.
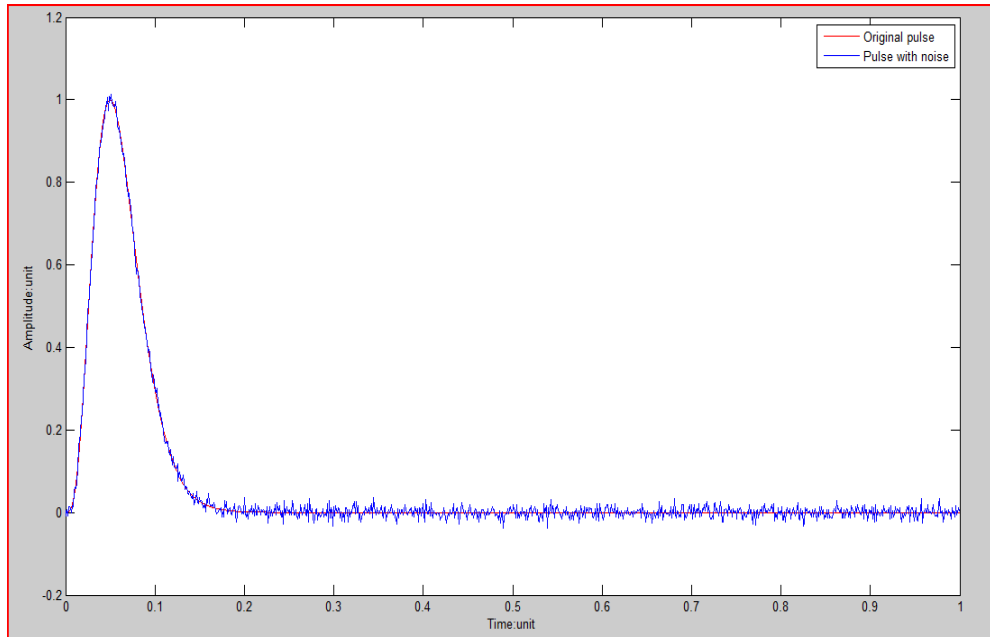

Figure 5.7 Pulse with additive white Gaussian noise. The signal to noise ratio is set to 25 dB for demonstration purpose.
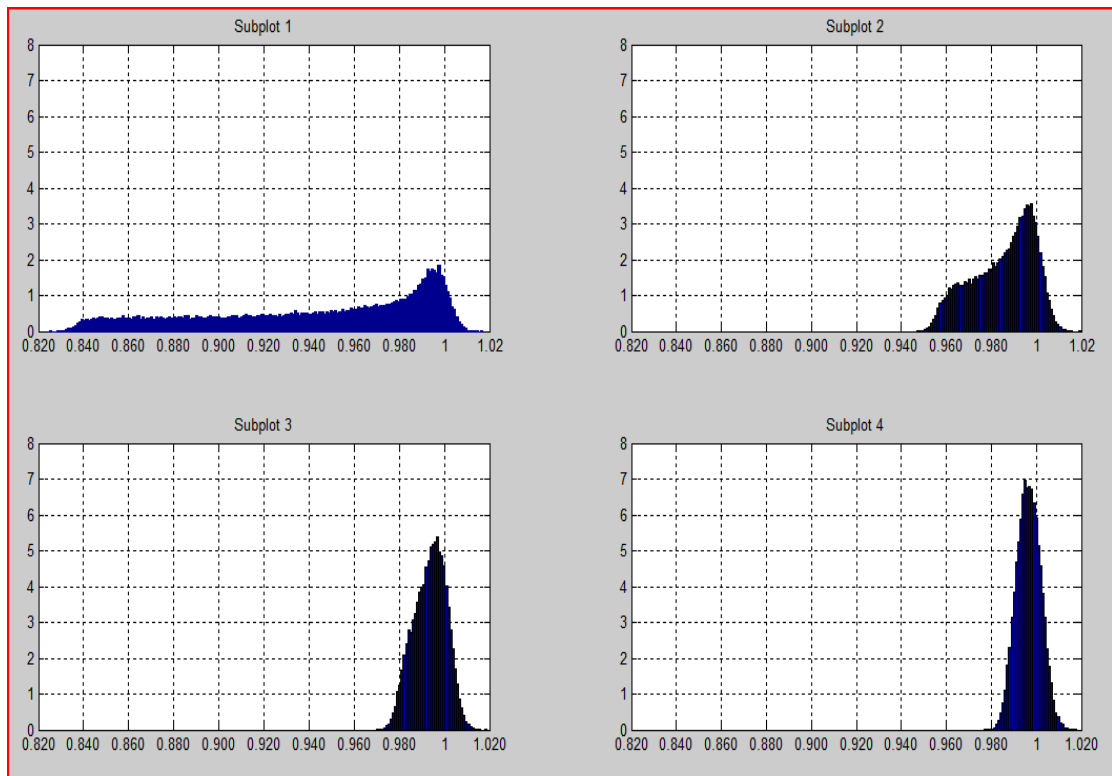
Figure 5.8 maximum sampled value distribution with noise superimposed onto the pulse (SNR 33dB).

- 40 -

In figure 5.8, the same tendency as figure 5.6 is observed from subplot 1 to 4. As the sampling frequency increases, maximum sampled values are squeezed into a smaller fraction in the normalized scale. In figure 5.8, the maximum sampled value distribution approaches Gaussian distribution. It is reasonable since we are sampling the noise intensively. The ideal maximum sampled value distributions in figure 5.7 are diffused by noise in figure 5.8. Under this situation, the real peak value can be obtained by the mean value of such distribution however shifted to smaller value from the real amplitude. The maximum sampled value distribution when we increase the signal to noise ratio is showed in figure 5.9 and figure 5.10. The real data is shown in figure 5.11 for comparison.
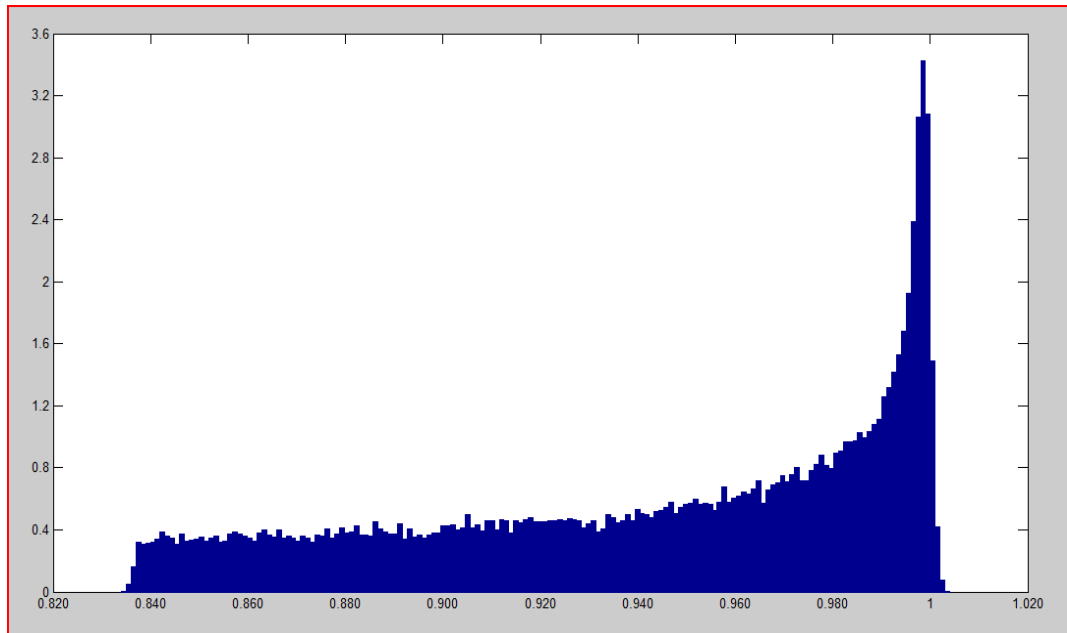

Figure 5.9 maximum sampled value distribution with 45 db signal to noise ratio. The sampling step is 0.4 FWHM.
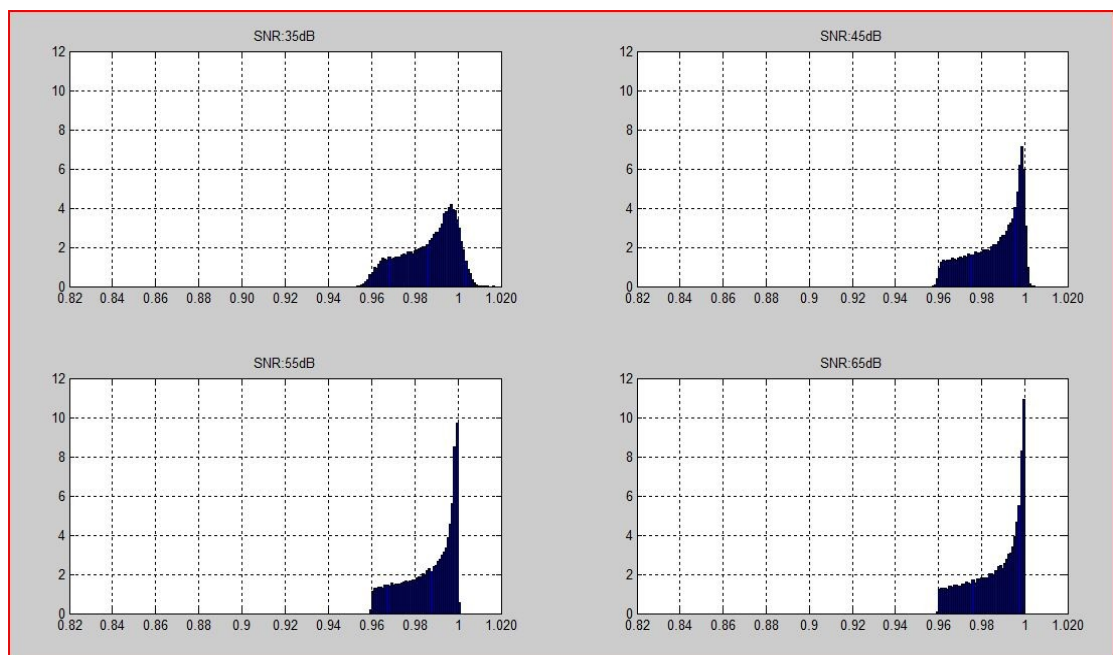

Figure 5.10 maximum sampled value distribution with different SNR. The sampling step is 0.24 FWHM.

From figure5.10, it is shown that the distribution approaches the ideal one as the SNR increases. The steep edge is smeared out by the noise at lower SNR which corresponds to the bad noise situation.
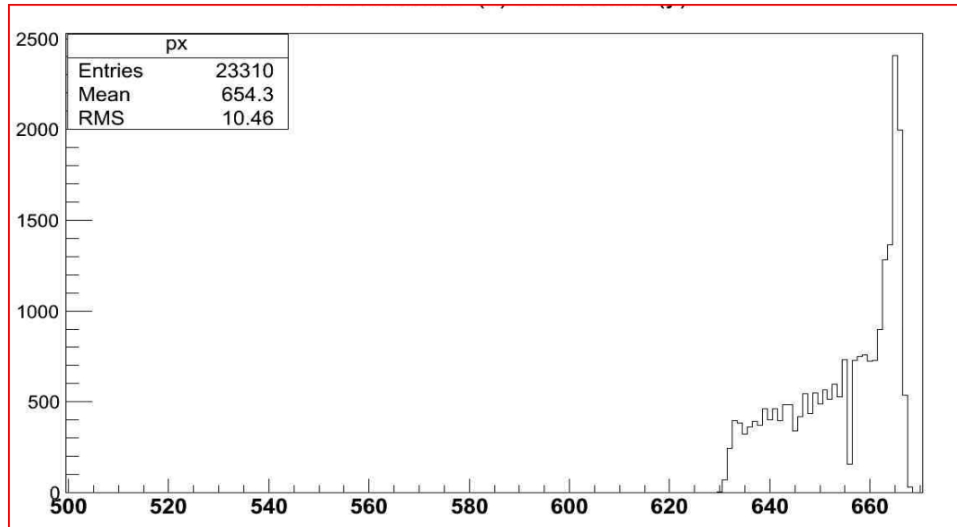

Figure 5.11-1 maximum sampled value distribution from experiment data, sampling clock 20MHz.around (1/4 FWHM)
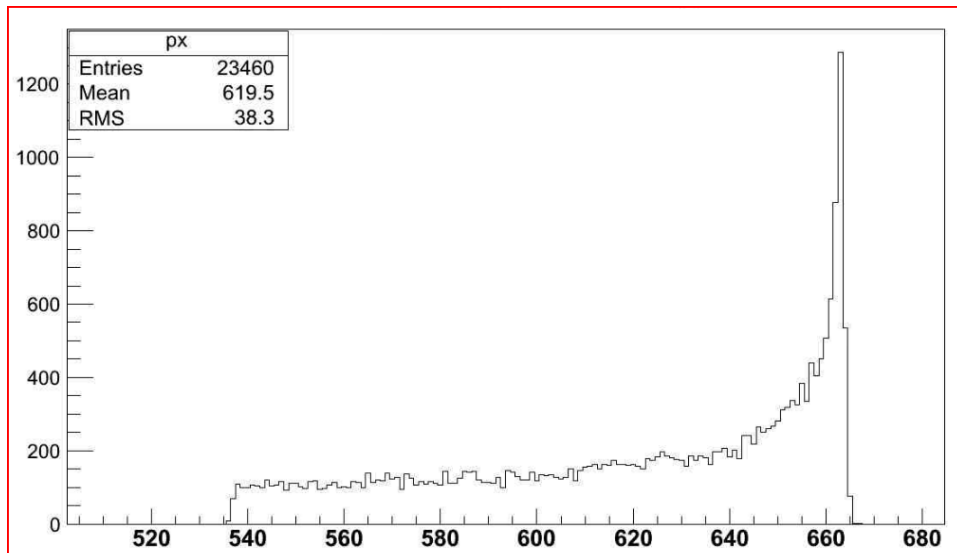

Figure 5.11-2 maximum sampled value distribution from experiment data, sampling clock 10MHz. (around 1/2 FWHM)
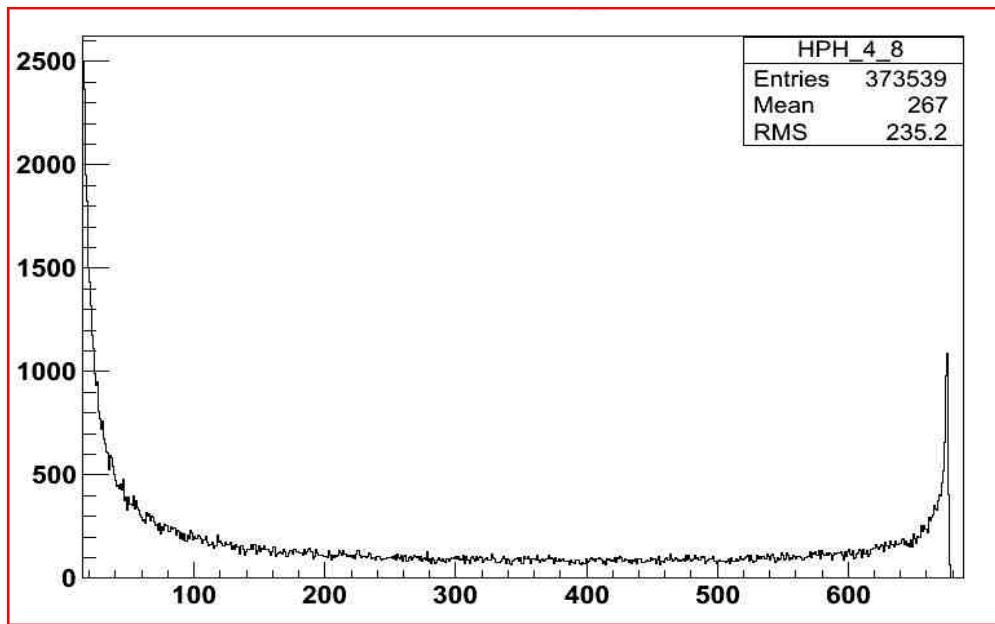
Figure 5.12 sampled pulse value distribution from experimental data, sampling clock 10MHz

Distribution plots from the laboratory measurement confirm our simulation results. So we can safely use the value happens most frequently as the hidden peak value in maximum sampled value distribution. The error associated with this is around 0.1% which is better than the estimation from directly normalized integral of each histogram where the error is around 1%. One final remark about figure 5.12, here the y axis is the number of entries and the x is ADC value. The data is from the same channel as in the figure 5.11(chip4 channel 8). One difference from other maximum sampled value distribution figures is that it is sampled values distribution. In fact, the maximum value of such distribution can get is around 30000. In order to demonstrate the peak around amplitude 680, Y axis is truncated. Two peaks can be easily explained based on the explanation in section 5.3. The distribution can be understood by that the sampling step is large enough to cover the whole pulse duration and the distribution itself is maximum sampled value distribution in this sense.

5.4   Conclusion and future

In this chapter, the amplitude estimation problem due to phase shift between ADC clock and pulse signal is addressed in several ways. Although the piece-wise linear filter method is promising, the sensitivity to peaking time and the difficulty to estimate in real case limits its application in the current scope. Several alternative ways are suggested to solve it. Here the promising candidate is neural network which has "memory" of pulse family if the training data set is carefully designed. And itself recovery ability is another attraction to real experiment application where abnormality results from irradiation or other sources. Finally, we conclude with the use of highest frequent sampled value from the maximum sampled value distribution for the amplitude estimation which will be utilized in chapter 6.

References

[1] "a fast and precise peak finder for the pulses generated by the future HEP detector", by V. Buzuloiu, CHEP'92, Annecy, France –pages 823-827.

[2] ROOT tutorials from CERN.

[3] "Real time recovery of the amplitude and shift of a pulse from its samples", by V. Buzuloiu, CERN-ECP/94-21, 8 December 1994.

[4] "Fitting function to noisy data in high dimensions", by Jerome H.Friedman, SLAC-PUB-4676 July 1988.

Chapter 6 Characterization of the PCA16-ALTRO system

This chapter is about characterization of the front end card (FEC) which carries the PCA16 and ALTRO chips. A general description of the FEC is given in the first place. The PCA16 and ALTRO chips are described separately. Various kinds of measurements are presented in the third section. The chapter concludes with a short summary.

6.1   Front end card-FEC

Front end electronics generally features low noise and high resolution. In our lab, the FEC is a general purpose readout system. Compared to its ancestor which is used in the ALICE experiment, the programmability of gain, polarity, peaking and decay time are new features in the amplifier chip. One front end card contains 8 charge sensitive amplifier chips (the so-called PCA16 chip) and 8 ALTRO chips which correspond to 128 readout channels. An FPGA works as the board controller. Each pair of chip (one PCA16 and one ALTRO) has 16 channels operating in parallel. Some steering parameters are common to all channels of a chip, others are individually controlled.
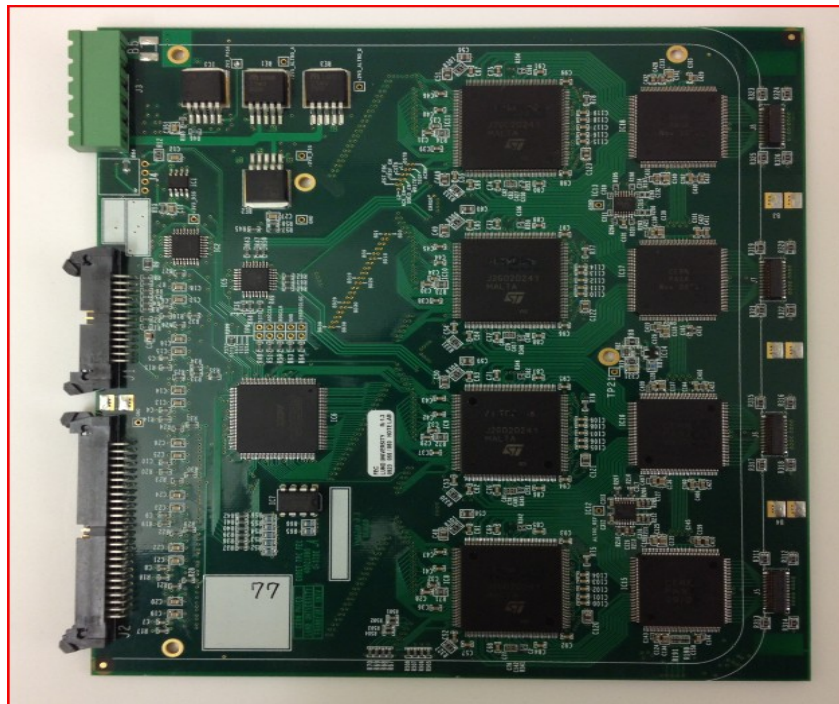

Figure 6.1 Front end card-top side

On the right hand side from figure 6.1 are the connectors for the input signals, the left side power supply connector and data bus connectors. The PCA16 is mainly an analog chip which is in charge of amplifying and shaping the signal. Digitization and digital signal processing are accomplished in the ALTRO chip.

6.1.1   The PCA16 chip

The PCA16 is a single end input, fully differential output chip. It is the analog part of the data readout chain as described in Chapter 2. The programmability enables it to work under different configurations which are summarized in table 6.1. Besides the

configuration options provided in table 6.1, it is also possible to bypass the shaper block to connect the outputs of the preamplifier to the ALTRO directly. The chip has 16 identical channels and each channel consists of one charge sensitive amplifier, followed by pole-zero cancellation network, semi-Gaussian CR-RC network and common mode feedback block. It has an impulse response function in the Γ_4 functional form as we discussed in previous chapter. The differential output from a PCA16 channel, as observed on the oscilloscope is seen in fig 6.2.
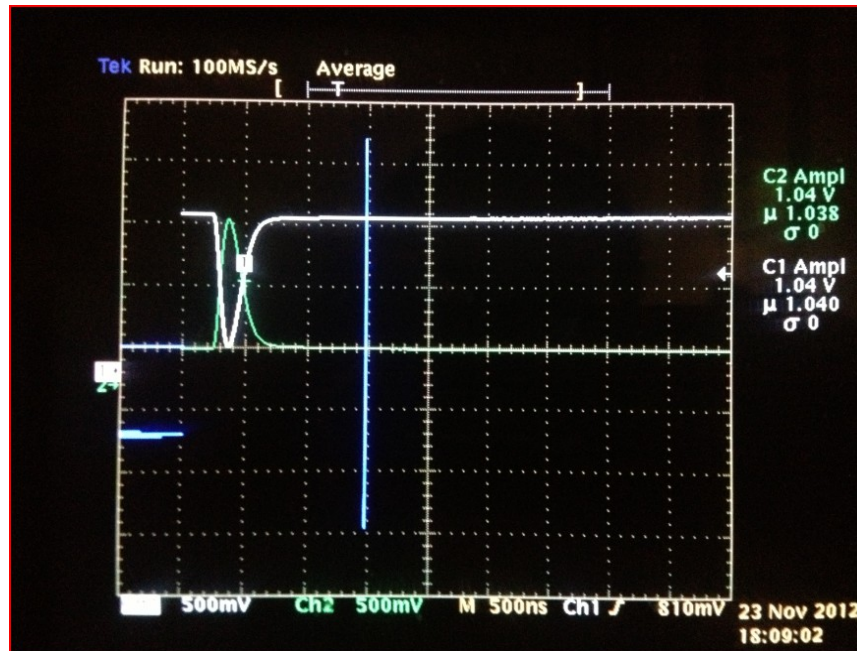

Figure 6.2 PCA16 differential output

As we can see, the pulse rises up in a short time and returns to baseline without undershoot. A brief discussion of each block is given in below:

Table 6.1-1 Different configurations (In shaper mode)

Polarity	Positive(MWPC-like signal)		Negative(GEM-like signal)	
Gain(mV/fC)	12	15	19	27
Peaking time(ns)	30	60	90	120

Table 6.1-2 Different configurations (in preamplifier mode)

Polarity	Positive(MWPC-like signal)		Negative(GEM-like signal)	
Gain(mV/fC)	5.25	5.5	5.8	6.5
Peaking time(ns)	10	30	60	80

6.1.1.1 Charge sensitive amplifier (CSA)

Normally the signal formed by the GEM-detector is a weak charge pulse with extremely short width within nanosecond scale. Such signal can be detected with operational amplifier mode integrator based on one feedback capacitor. It integrates the weak charge and converts it into a voltage signal for further processing. The charge is integrated in the

feedback capacitor (420fF [3]) (also the charge it detects) and then it can be dumped through the feedback resistor (10MΩ [3]), which is regulated by the self adaptive bias network. The feedback path provides a discharge time constant of 4.2 microsecond which dominates the tail of output pulse from charge sensitive amplifier (CSA). The value is a compromise between noise and counting rate considerations. However, this block in the amplifier causes: 1.undershoot which shifts the baseline thus causing false estimation of pulse amplitude 2. Longer decay tail due to dominant pole from the feedback path (about 4.2μs) which limits the counting rate capacity.
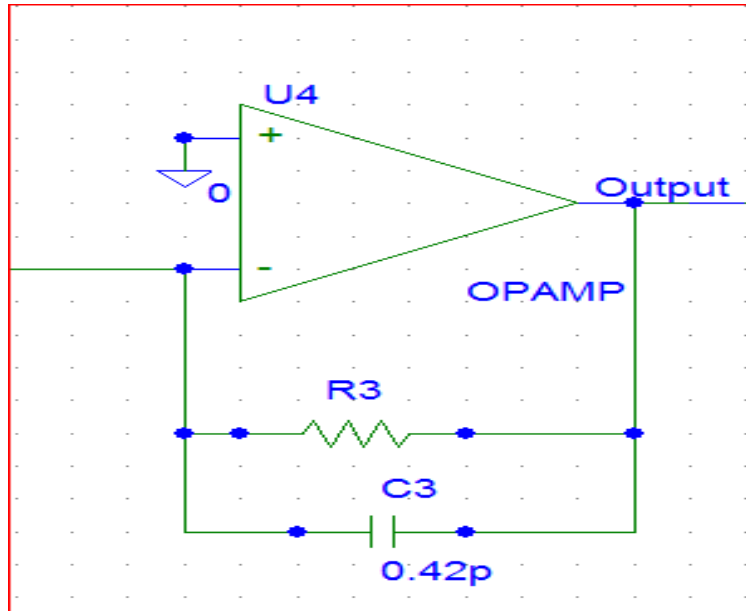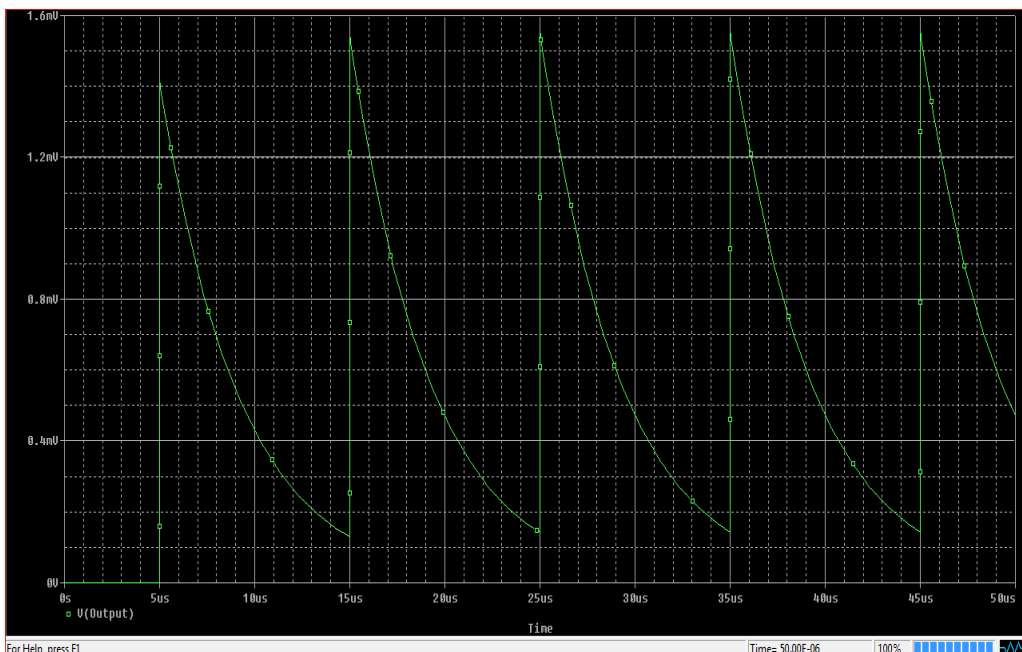

Figure 6.3 CSA schematic circuit

Fig 6.4 pulse output from CSA and pileup effects. Simulated by Pspice with delta like current pulse input.

6.1.1.2 Pole-zero cancellation

Due to the long tail output from CSA in fig 6.4, the output pulse rides on the previous one which results in pileup effect. A pole-zero cancellation network is needed to cancel one

dominant pole from the CSA. The resistor used in this network is regulated by the same self-adaptive bias network as the feedback resistor so that the cancellation circuit is able to cancel the pole exactly and dynamically.

6.1.1.3   Semi-Gaussian CR-RC circuit

The pulse after pole-zero cancellation circuit is fed to the Semi-Gaussian CR-RC network. Through such CR-RC filtering, the noise and pulse width can be reduced in a satisfactory way through proper choice of the order of the shaping filter. By using an operation amplifier to implement CR-RC like circuit, the signal to noise ratio and pulse width can be reduced further compared to normal CR-RC circuit. The whole circuit is a 4th order shaping amplifier. It consists of two second order bridged-T filters and each one of them introduces two poles and one zero. In the first filter block, a voltage follower is combined with the filter in order to minimize the variations of DC level of its output due to variations of process parameters, operating conditions etc [6]. The outputs of both the first filter and the voltage follower are fed into the input of differential inputs of the second filter. Together with the first filter, they provide a semi-Gaussian CR-RC filtering block. Pulse output from this stage is narrowed and the signal to noise ratio is set optimally. Besides the blocks mentioned above, other blocks are also needed to stabilize the system.

In summary, the output of PCA16 is fully differential and ready for ADC inputs in ALTRO chip.

6.1.2   The ALTRO chip

The ALTRO is a mixed signal processing chip integrating 16 identical channels in one single chip. Each channel operates concurrently and independently to process the analog pulse from corresponding channel of the PCA16 mentioned above. A simplified processing chain is shown in figure 6.5 [4]
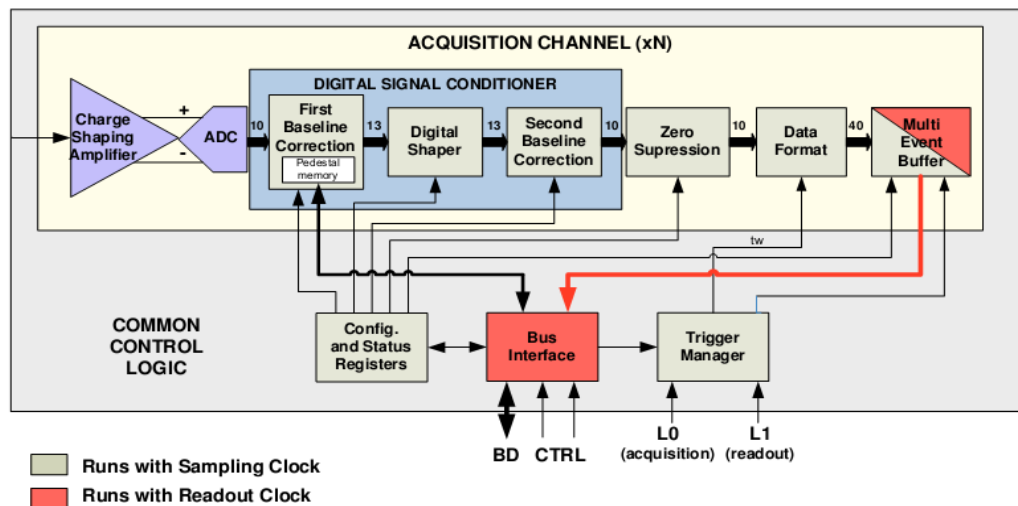

Figure 6.5 processing chain of ALTRO chip [4]

When the L0 trigger is received, the user defined number of samples (1000 maximum) are acquired and processed. The acquisition is frozen and ready for readout when the L1 trigger arrives. The data stored in data memory will be overwritten otherwise if no L1

trigger arrives. Data can be readout based on another clock which is independent of ADC's sampling clock. In the following, a description of each block along the processing chain is given. Emphasis and detailed description is given to the blocks used in the thesis. Only concise description to dummy blocks is presented for the purpose of completeness. Since all the 16 channels are identical, the following description corresponds to one channel. Basically the processing chain can be divided into analog to digital conversion block (including ADC), digital processor block (BSCI, TCF, BSCII, ZERO SUPPRESSION, DFU) and memory block (Multi-Event Buffer).

6.1.2.1 The ADC

It quantizes the analog pulse by sampling the voltage at times defined by the sampling clock and outputs binary codes for processing and storage. It works under 20MSPS with 10 bit precision.
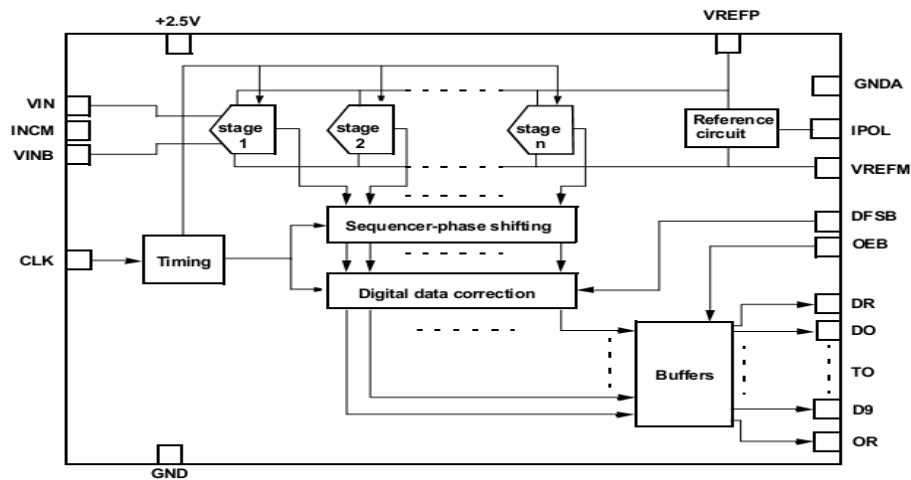

Figure 6.6 Block diagram of TSA1001 pipeline ADC [5]

It is based on the TSA1001 IP core from ST Microelectronics [1]. Nine 1.5 bits stages as showed in the block diagram comprise the pipeline and overall 10 bit ADC precision is obtained. To recover from the conversion delay due to each stage, a sequencer-phase shifter is implemented. The output bits from shifting block are ready for digital data correction and finally the 10 bits are extracted [5]. A reference circuit based on band-gap generator is used to generate internal reference voltage for each stage.

This commercial ADC can work in different configurations. For FEC77 under test, the differential input configuration is implemented. The difference between inputs of VIN and VINB is measured, while the common mode signal is rejected. Several key parameters are defined as follows:

$$Dynamic\ Range = [VREF_{BOT} - VREF_{TOP}; VREF_{TOP} - VREF_{BOT}] \qquad (6.1)$$
$$Conversion\ Gain = 1024/(Dynamic\ Range) \qquad (6.2)$$
$$ADC\ Count = (vin\text{-}vinb) \times ConversionGain + 512 \qquad (6.3)$$

The dynamic range is defined from the difference between $VREF_{BOT}$ and $VREF_{TOP}$ to the difference between $VREF_{TOP}$ and $VREF_{BOT}$. The output full code range is from 0 to 1023.

6.1.2.2   First baseline correction: BCSI

The main purpose of this block is to prepare a stable baseline where signal pulse sits on for the tail cancellation in the next step. The targets to be removed can be the DC level, low-frequency spurious waveforms, systematic perturbations from trigger etc.

The low frequency signal can be in the range of kilohertz, which is almost constant within time window during one event. Such perturbation is corrected by a self calibrated circuit. It tracks the signal outside the time process window calculating the cumulative average continuously until L0 trigger arrives. The average is subtracted from the pulse signal within the sampling time window.

Systematic perturbations (i.e. in specific samples of each event) can be removed based on the memory of systematic pattern stored in a dedicated pedestal memory. During acquisition, such pattern can be either subtracted from the signal samples or performing response equalization between channels. This memory can also be used as an injection pattern for the test purpose without pulse input. Namely, it can work under three different modes: subtraction mode, conversion mode and test mode.

After this stage, a more constant baseline is achieved, though the complex tail of pulses is still present (in the MWPC readout case) and perturbations due to non-systematic effects still exist which motivate the implementation of the following functional blocks.

6.1.2.3   Digital shaper: TCF

As mentioned above, in the conventional multi-wire proportional chamber, the signal produced due to the movement of positive ions is characterized by a complex long tail. In this or similar cases, the tail should be removed otherwise the pileup effect would be dominant enough to bury useful physical information and make the data reduction block inefficient.

This digital shaper is implemented by 3 first order IIR filters in cascade where each IIR has its own pole and zero corresponding to two user programmable coefficients. In total six configurable coefficients provide the power of filtering a wide range of tails with desirable precision.

Ideally the pulse signal after this block, the pileup effect should be removed effectively. One should however remember that the tail is still present on the analog pulse and in the case that a pileup pulse saturates in the amplifier the information about the second pulse may be distorted. This problem can only be handled by proper matching of the dynamic range and gain of the system. The non-systematic perturbations cannot be removed until now which makes the baseline correction II necessary before zero suppression can take place. In the thesis project, this module is not used.

6.1.2.4   Second baseline correction: BCSII (Dummy)

Compared with BCSI, this correction is applied within a time window so as to remove the non-systematic perturbations involved. Such function is based on a Moving Average Filter. It performs in two phases: generation of the acceptance window to perform averaging of

the baseline; the second, the correction based on the average result obtained from the first phase. A double threshold scheme following the slow variation of the signal is implemented to calculate the sample average. If there exists a fast variation in the signal, such scheme guarantees the exclusion of the average calculation which is given by the following equation:

$$y(n) = \frac{1}{M} \sum_{k=0}^{M} x(n-k), M = 1,3,5 \, or \, 7 \quad (6.4)$$

In the second phase, the baseline is corrected by subtracting the average calculated in the first stage. The data after this block is ready for reduction namely zero suppression.

6.1.2.5 Zero suppression

One intuitive and simple data reduction scheme is the removal of data samples which are too close to zero or below certain threshold since these points contain no essential information. Samples below a user defined threshold are considered as noise and would be discarded before being stored in the event buffer for readout to the DAQ computer. One shortcoming of such pulse detection scheme is that it is sensitive to the random noise which happens to be higher than the threshold. To avoid using an unnecessarily high threshold, a glitch filter is implemented for checking consecutive number of samples above the threshold. To avoid the digital truncation, user defined pre and post samples also collected below the threshold which are adjacent to the real pulse. Fig 6.7 shows a schematic how the zero-suppression works.
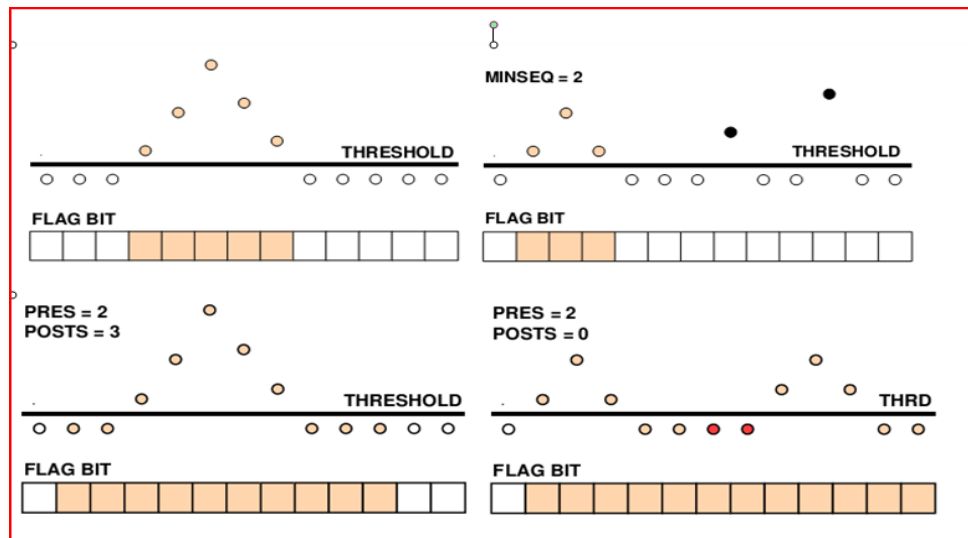

Figure 6.7 the zero-suppression scheme [4]

The obtained pulse data after zero suppression should be combined with extra time information since the time information from the sample sequence is lost because of the removed zero samples. The time information is coded in one extra 10 bit word. Because the data word is also 10 bit, to further distinguish the time word and data word, another 10 bit word containing number of samples is needed.

After zero suppression, the data volume can be only 5% of the one without zero-suppression during test in the worst case. Two extra words mentioned above are inserted in the data format unit.

6.1.2.6 Data Format Unit

This unit performs insertion of the extra two words as mentioned above and hardware information etc into a set of 40 bit words. The time stamp specifies the time distance between last sample of the cluster and the trigger. The data formatting procedure is shown below:
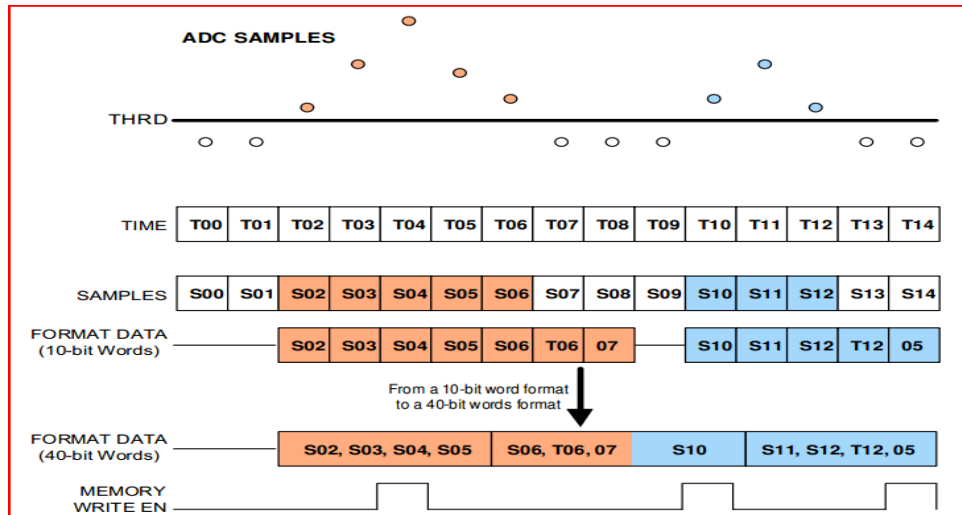

Figure 6.8 Data formatting procedure [4]

After formatting, the 40 bit data is ready to move to event memory for shipping to DAQ computer.

6.1.2.7 Multi-Event Buffer

Collisions happen randomly in time. To even out the data load on the readout chain a buffer mechanism can reduce the dead time of the readout electronics to a certain extent. For gaseous detector, the dead time has two main contributions: one is due to the drift time and the other is the readout electronics. The buffer memory is 1024 times 40 bits wide, which can be divided into number of blocks (4 or 8 blocks). Each event data stream can be written into the next available block or read from the current block, which depends on the available instructions from the RCU.

In all, besides these functional block mentioned above, the whole ALTRO chip works under two independent clocks: a slow clock (20 MHz) for ADC and processing units and a faster clock (40MHz) for readout.

6.2 Measurements on a FEC

On the FEC77, PCA16 and ALTRO are separate chips. This makes it possible to observe the analog pulse between the two chips and measurements become possible. For one channel, the connection between the PCA16 outputs and the ALTRO chip ADC inputs is as figure 6.9:
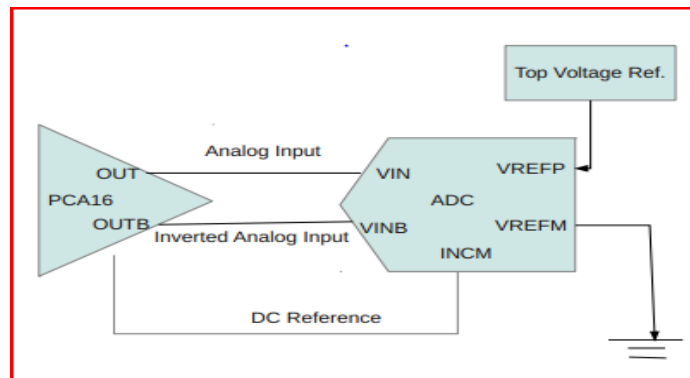
Figure6.9 PCA16-ADC configuration for one channel (the DC reference is common to all channels in a chip).

The measurement and analysis is divided into PCA16, ADC, and the combination of the two.

6.2.1 Measurements on the PCA16 chip

From equation 6.1-6.3, we can observe that the ADC value depends on various DC reference levels such as $VREF_{TOP}$ and $VREF_{BOT}$ etc. The stability of such levels (or the difference between such levels more precisely) becomes more important when different configuration is chosen for PCA16. The result is presented in the plot below with different configurations. The X axis code is based on different configurations. The Y axis is the real measured value in volt. For example, the first bit is set as polarity, the second Preamp output enable, the third bit as peaking time, and the left two bit as conversion gain. If the code is 11100, it means polarity is 1, pre amp enabled, any peaking time, 12 mV/fC conversion gain. The translation table is shown in table 5.2.

Table 6.2 translation table for fig 6.10 (Preamp enabled means the output is from the preamplifier; preamp disabled means the chip is in shaper mode i.e. the output pulse is the output of the shaper)

| Binary codes	00100	00101	00110	00111
configuration	Polarity=0 Preamp disabled 12mV/fC	Polarity=0 Preamp disabled 15mV/fC	Polarity=0 Preamp disabled 19mV/fC	Polarity=0 Preamp disabled 27mV/fC
Binary codes	10100	10101	10110	10111
configuration	Polarity=1 Preamp disabled 12mV/fC	Polarity=1 Preamp disabled 15mV/fC	Polarity=1 Preamp disabled 19mV/fC	Polarity=1 Preamp disabled 27mV/fC
Binary codes	01100	01101	01110	01111
configuration	Polarity=0 Preamp enabled 5.25mV/fC	Polarity=0 Preamp enabled 5.5mV/fC	Polarity=0 Preamp enabled 5.8mV/fC	Polarity=0 Preamp enabled 6.5mV/fC
Binary codes	11100	11101	11110	11111
configuration	Polarity=1 Preamp enabled 5.25mV/fC	Polarity=1 Preamp enabled 5.5mV/fC	Polarity=1 Preamp enabled 5.8mV/fC	Polarity=1 Preamp enabled 6.5mV/fC
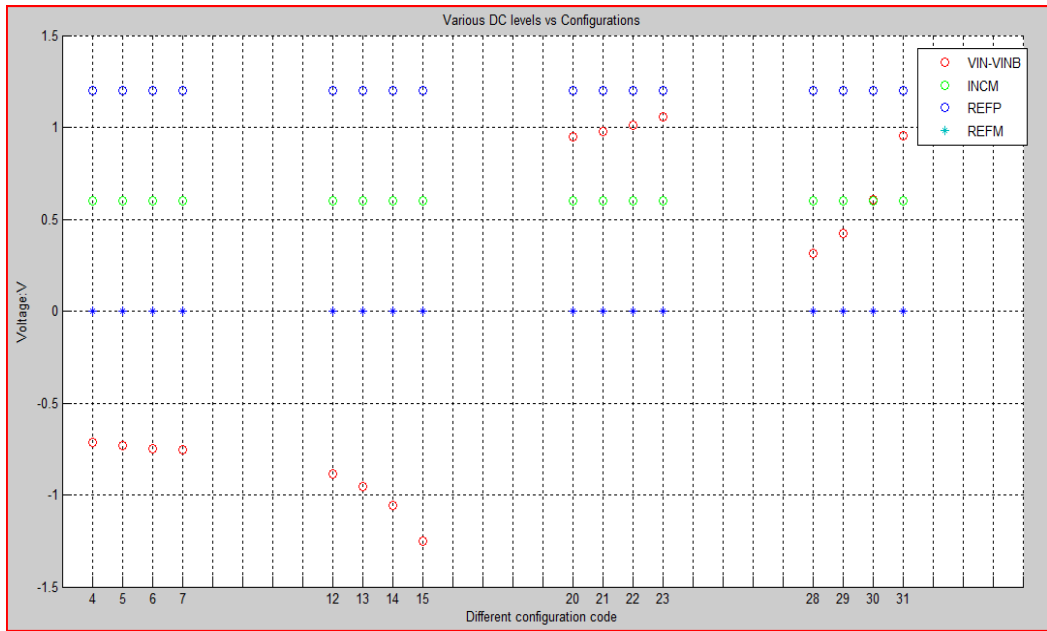
Figure 6.10 DC levels for different configurations

From figure 6.10, it is clearly seen that the INCM, REFP, REFM levels are constant across the different configurations within the error imposed by the digital multimeter. The difference between VIN and VINB (without signal) varies from one configuration to another. Comparing the configuration 12-15(01100-01111) to 4-7(00100-00111), it is clear that the level gap becomes wider when the preamp is enabled. The same conclusion can be drawn when one compares 28-31(11100-11111) to 20-23(10100-10111). The variation is within 0.15V when the preamp is not enabled when one examines the configuration with settings 4-7 or settings 20-23. However, it varies more than 0.5V when the preamp is enabled. It is reasonable since the gain varies from 5.25 mV/fC to 6.5mV/fC if the preamp is enabled. Ideally, the difference between vin and vinb should vary proportionally with the gain change in order to keep the linearity of the PCA16. Figure 6.11 and figure 6.12 show this behavior:
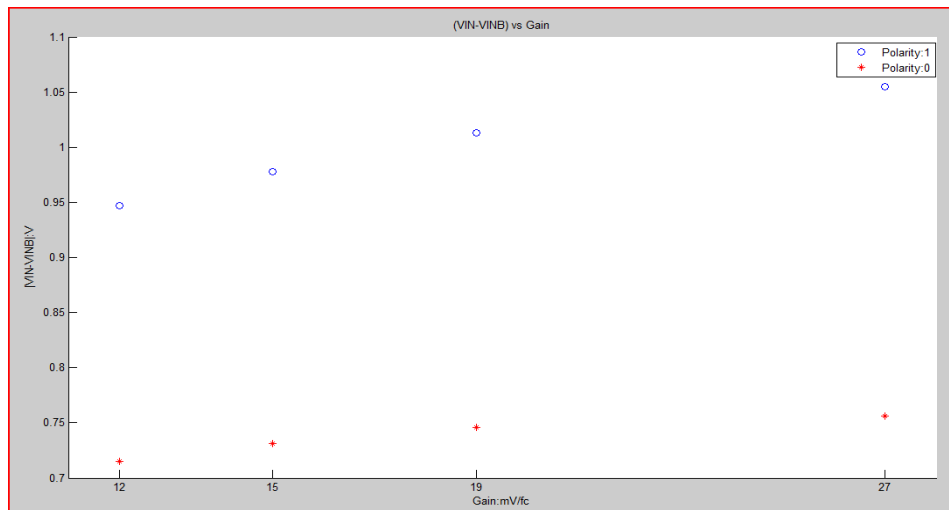
Figure 6.11 DC level difference versus Gain, preamp is disabled
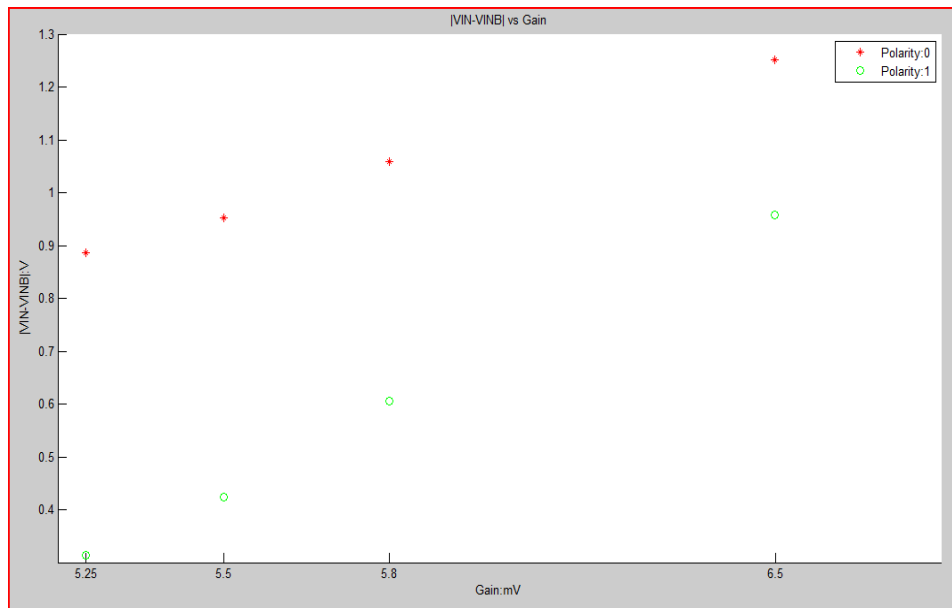
- 54 -

Figure 6.12 DC level difference versus Gain, preamp output is enabled

Based on the figures 6.11 and 6.12, one may notice that a small nonlinearity exists; such nonlinearity can be from both the nonlinearity of the system and the deviation from gain nominal values. The effect of changing decay time on the differential DC level is shown in figure 6.13.
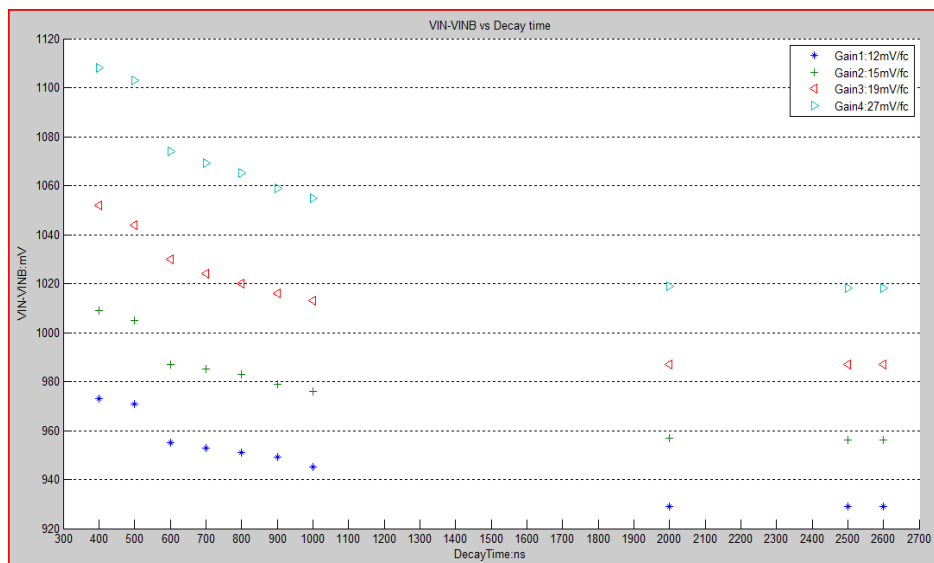

Figure 6.13 DC level difference versus preamp decay time with different gains
(Other configurations: Polarity 1, preamp disabled, peaking time 120 ns)

As the decay time increases, the VINB increases accordingly and the VIN level decreases. Due to this reason it shows the pattern in figure 6.13 as the decay time increases. The figures shown above are based on one channel study.

The dependence of the differential DC levels on the chosen parameters of the PCA16 is a drawback of the flexibility of the amplifier. Ideally the levels should be the same. The solution which partly solves the problem is to adjust the analog range of the ADC scale to accommodate all zero levels. The best solution would be to have the analog endpoints (REFN and REFP) of the ADC scale settable from a DAC, once the amplifier setting has been

chosen. The scale would be optimally chosen for all settings. One can however not avoid that analog saturation will appear at different input charge for different settings. This is of course quite natural for different gain settings but not for the variation of other parameters.

From now on, the configuration of the PCA16 is fixed as polarity 1 (negative input signal as for GEMs), preamp disabled, peaking time 120ns and gain 12mV/fC unless other stated.

6.2.2   Measurements on the ALTRO chip

The purpose of this section is to study the ADC response only. The input to the ADC is visualized with a digital oscilloscope and two values, vin and vinb for the peak amplitudes are determined. Based on equations 6.1-6.3, the expected result after AD conversion is calculated, hereafter called the "calculated value" although it is the high resolution average amplitude measured with the oscilloscope before the ADC in the ALTRO. The oscilloscope measurements are done, taking the average of 200 identical pulses, generated by the pulse generator by sending a step voltage which couples to the amplifier input with a small coupling capacitor. The value of this capacitor is not important until the actual gain is to be determined in the following section. Measurements are done at different gains in order to study the effect of different signal to noise ratios (SNR). The input amplitude averages are determined with an accuracy of 0.3mV i.e. about 0.128 ADC counts.

In figure 6.14, it is shown that the calculated ADC values and the measured values at different gains follow each other well up to a point where either the amplifier output saturates or the ADC scale is exceeded. The calculation does not include the limitation in ADC scale. That is why saturation appears as a difference between the two. Note that this may happen at different ADC values since the pedestals are different for different gain settings.
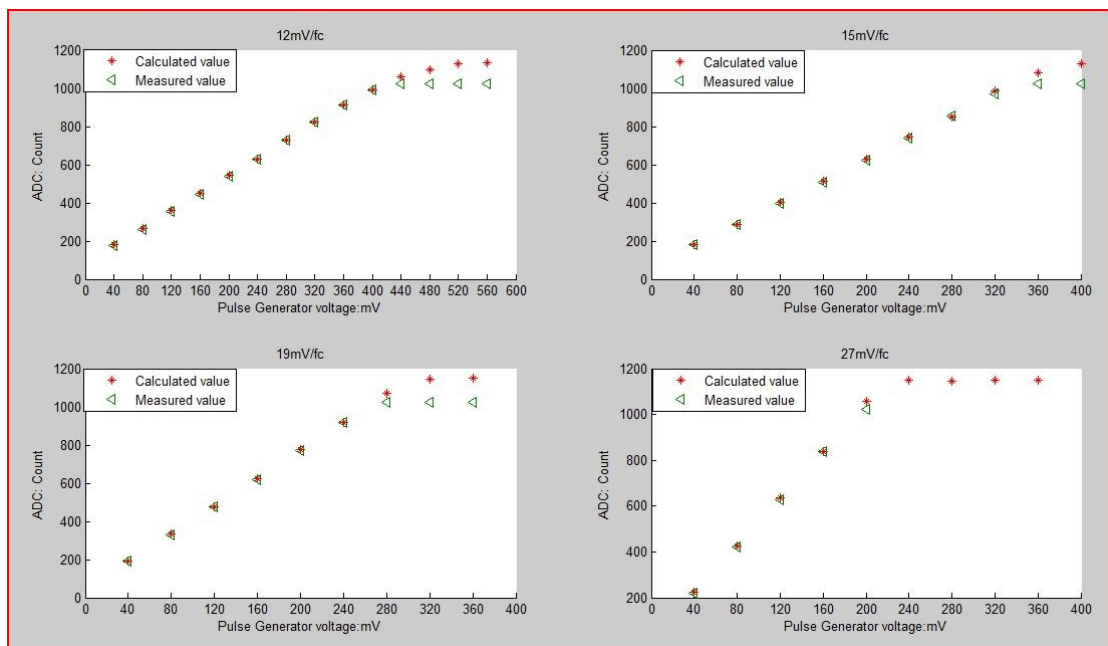

Figure 6.14 Calculated ADC values and measured values versus input step voltage

The input value is generally higher than the measured value, which can be observed from figure 6.14. It is likely because our statistical interpretation of the maximum sampled value distribution has a bias. As we have discussed in chapter 5, the maximum ADC counts distribution can be influenced by the signal to noise ratio (SNR). When the signal amplitude is low, the SNR is low since the noise is constant. Figure 6.15 and 6.16 show two extreme cases: figure 6.15 corresponds to the situation that "SNR" is high where the peak distribution approaches the ideal case. In such case, usage of the most probable value based on the discussion in chapter 5 should show less bias; figure 6.16 shows the opposite case: the input signal pulse amplitude is low corresponding to low SNR. The most probable value of this distribution is influenced by the noise distribution. Figures 6.15 and 6.16 also justify our simulation model, where the noise candidate was set as additive white Gaussian noise.
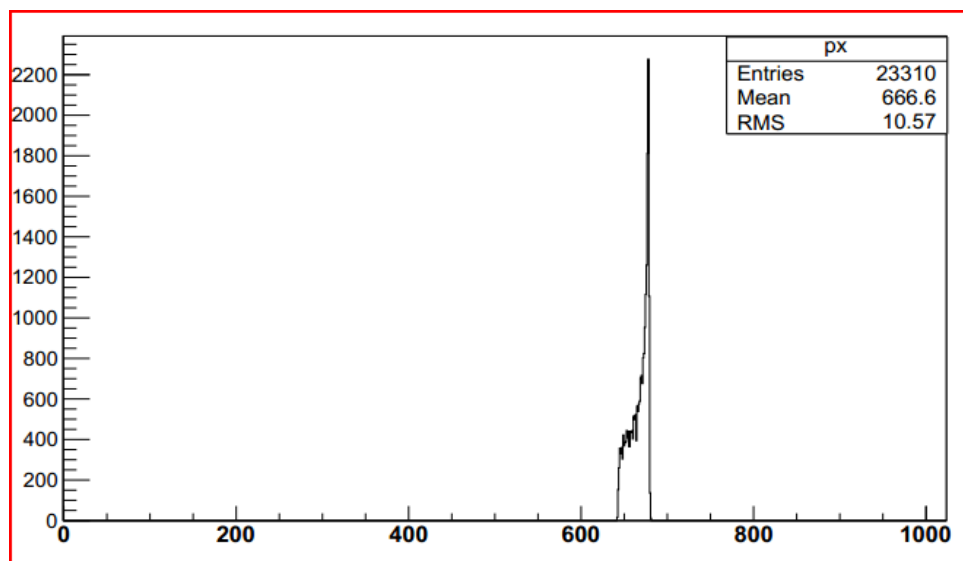
Figure 6.15 maximum sampled value distribution when signal amplitude is high ("high SNR")
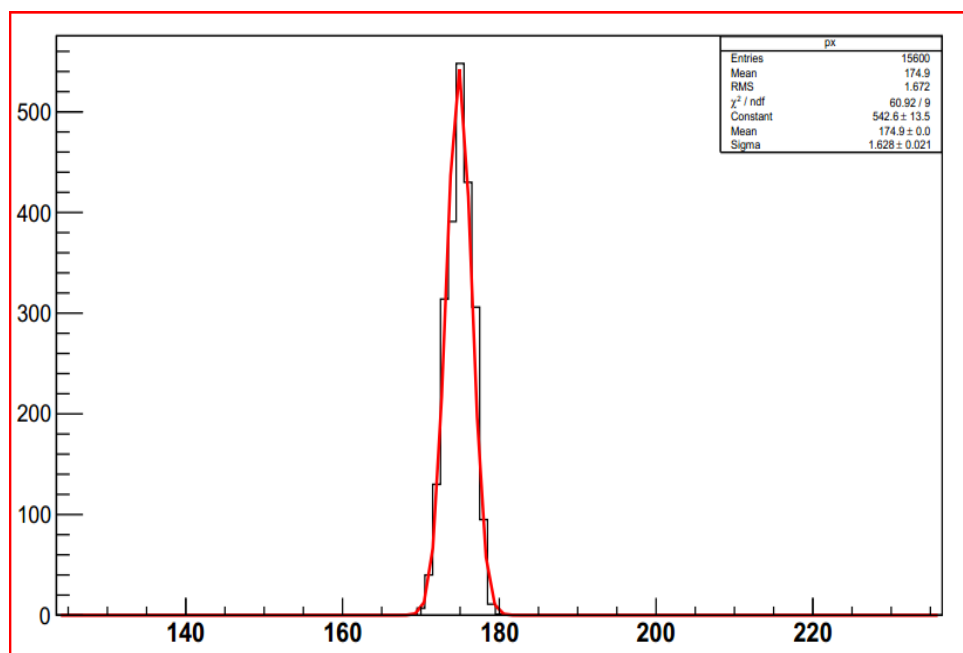

Figure 6.16 maximum sampled value distribution when signal amplitude is small ("Low SNR")

The input capacitance also introduces noise [6], as was extensively investigated in Chapter

3. In figure 6.17, it shows the ADC error versus capacitance when input voltage (200mV from pulse generator) is constant.
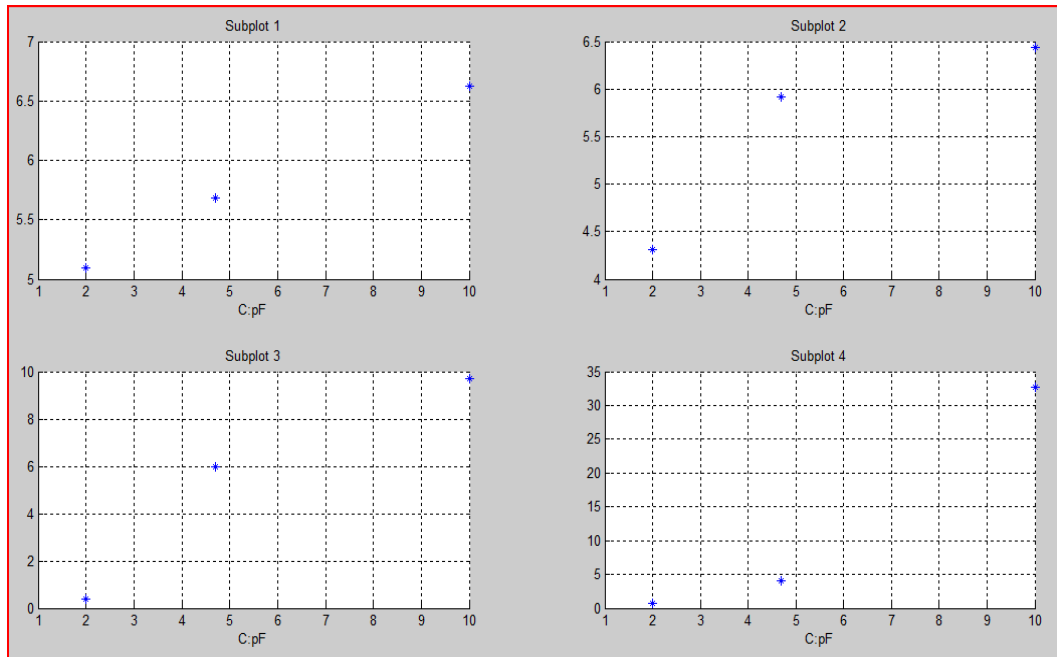

Figure 6.17 ADC error of various gains versus additional input capacitance (i.e. in addition to the amplifier input capacitance)

In figure 6.17, from subplot1 to subplot4, the gain of PCA16 corresponds to 12mV/fC, 15mV/fC, 19mV/fC, and 27mV/fC. It is clearly shown that the pattern in all four subplots is similar. Since the total capacitance influences the system noise level greatly, the difference between theory value and measurement increases as the capacitance value increases. In subplot 4, the 10 pF point shows extreme mismatch with the theory value. However, it is because at this point the ADC already gets saturated.

In conclusion, the difference between the calculated ADC value and the measured value can be explained by the effect of the noise on the method we used to compensate for the random phase of the sampling clock relative to the pulse to be measured. For real data, where the amplitude is not known, this is an unavoidable complication. The effect can be minimized by increased sampling rate (which has severe hardware consequences). In a TPC application, taking the average of many energy loss measurements, (in the ILC TPC about 400 per track) allows a good estimate of the average. In the next section, measurements regarding the FEC77 card are presented.

6.2.3   Measurements on the FEC77

For an absolute calibration of the measurement system, i.e. how much input charge gives a certain ADC value, one can inject a known amount of charge in the amplifier input by a step voltage over a coupling capacitor. The relevant amount of charge (in the fC range) is small and thus small capacitors need to be used. It is then important to know the capacitance values and methods to determine these are discussed in appendix 1. Two methods were studied and both methods depend on the knowledge of a "reference assumption". In the Schmitt trigger circuit, the reference is the linear relation between capacitance and time

constant (which is theoretically justified) but in the UTI method, the reference is a known capacitor. Thus this calibration cannot be said to be absolute but relative. The calibration work was based on the UTI method, and the uncertainty of the reference capacitance is thus more important. We used a high quality capacitor with good rating as reference (The accuracy of the capacitance value provided by the manufacturer is 0.4%. At the same time, the relative comparison of different gain settings has high accuracy since the capacitance uncertainty is eliminated by using the same capacitor for all measurements. If we plot the measured ADC value versus input voltage from the pulse generator, such points are fitted with a linear function. In these plots, only data, safely inside the linear response of the amplifier are used.
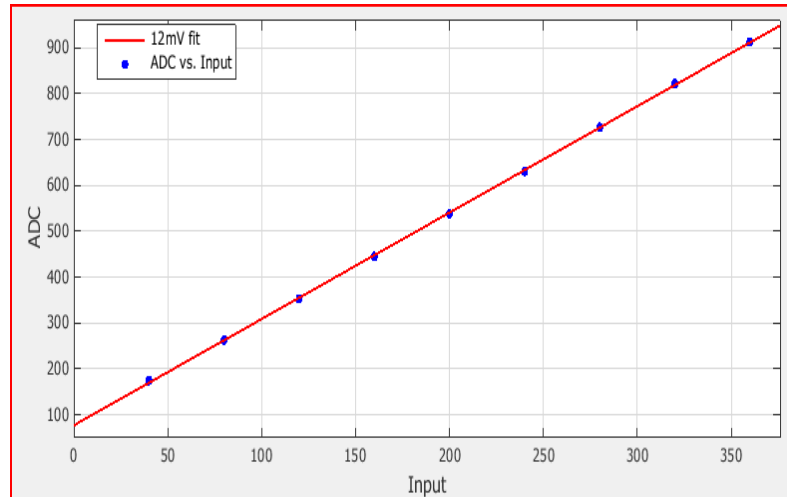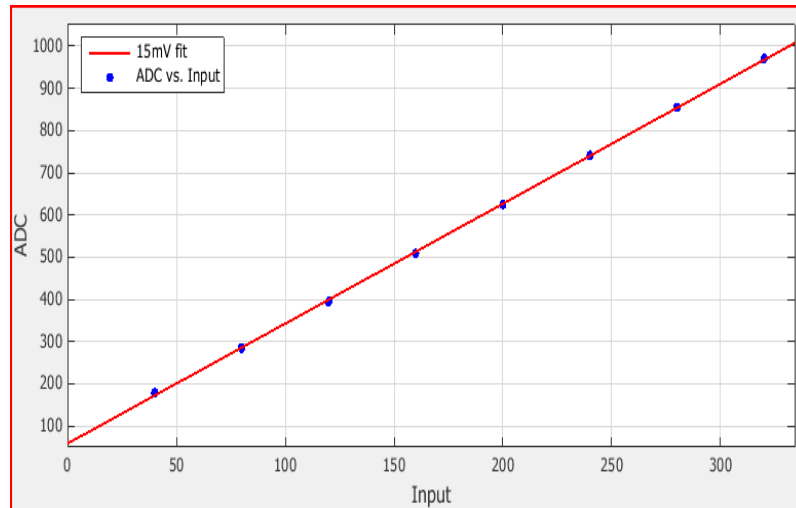

Figure 6.18 fitted with *y = 2.318x+77.19*

Figure 6.19 fitted with *y = 2.842x+58.5*
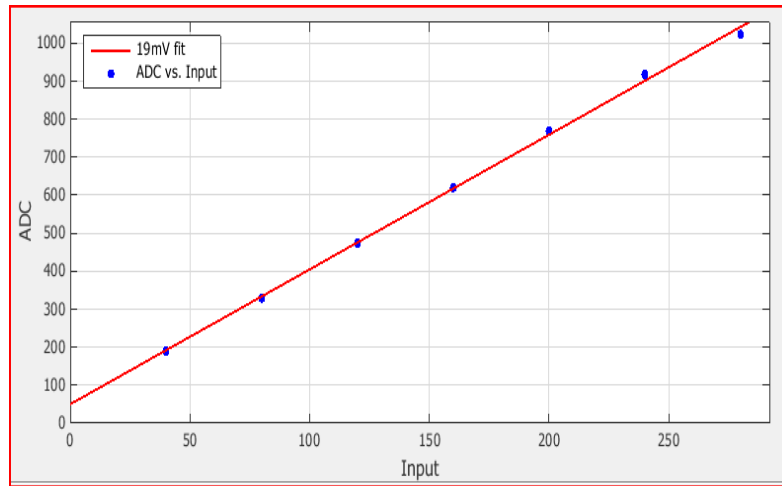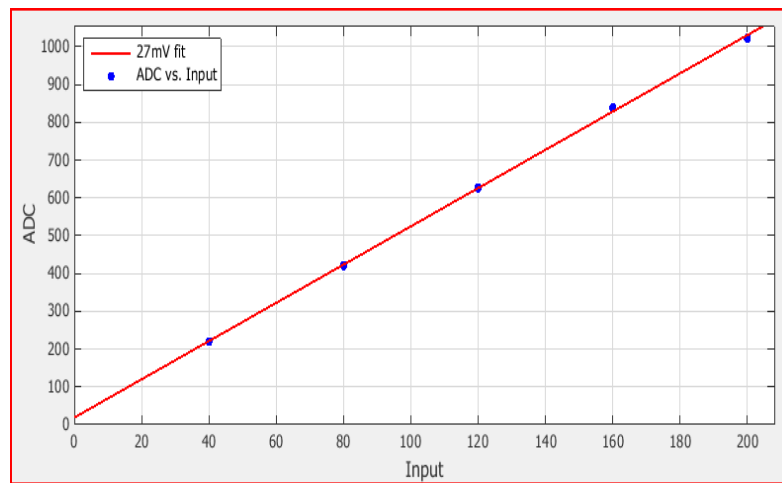
Figure 6.20 fitted with *y = 3.546x+50.14*

Figure 6.21 fitted with *y = 5.06x+18.8*

In the fitted linear equation, 95% confidence level was chosen. The gain information is contained in the slope of the different linear equations. So we plot the nominal gain value versus the slope in figure 6.22.
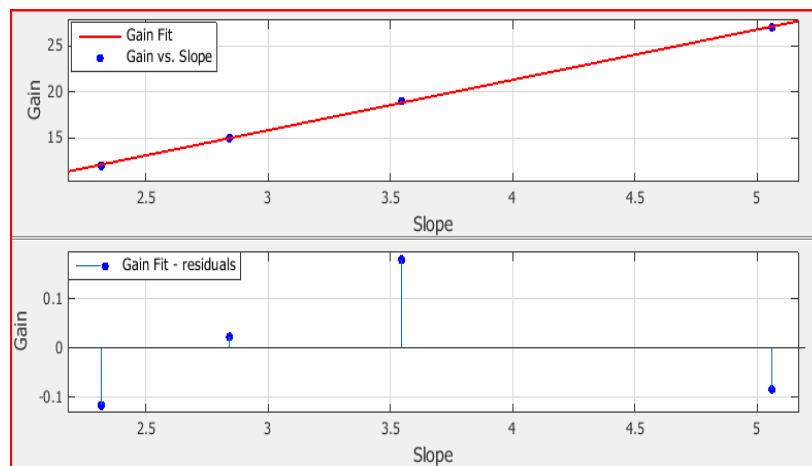

Figure 6.22 Fitted gains versus nominal gain. Fitted with *y = 5.459x - 0.5357*.

From the residual plot above, we can obtain the relative deviation among different nominal gains. The nominal gain 12mV/fC and 19mV/fC deviate more than other two nominal gains.

It is however not evident that the relation should be linear.

Based on the capacitors measurement described in appendix, the calibrated gain versus nominal gain is plotted.
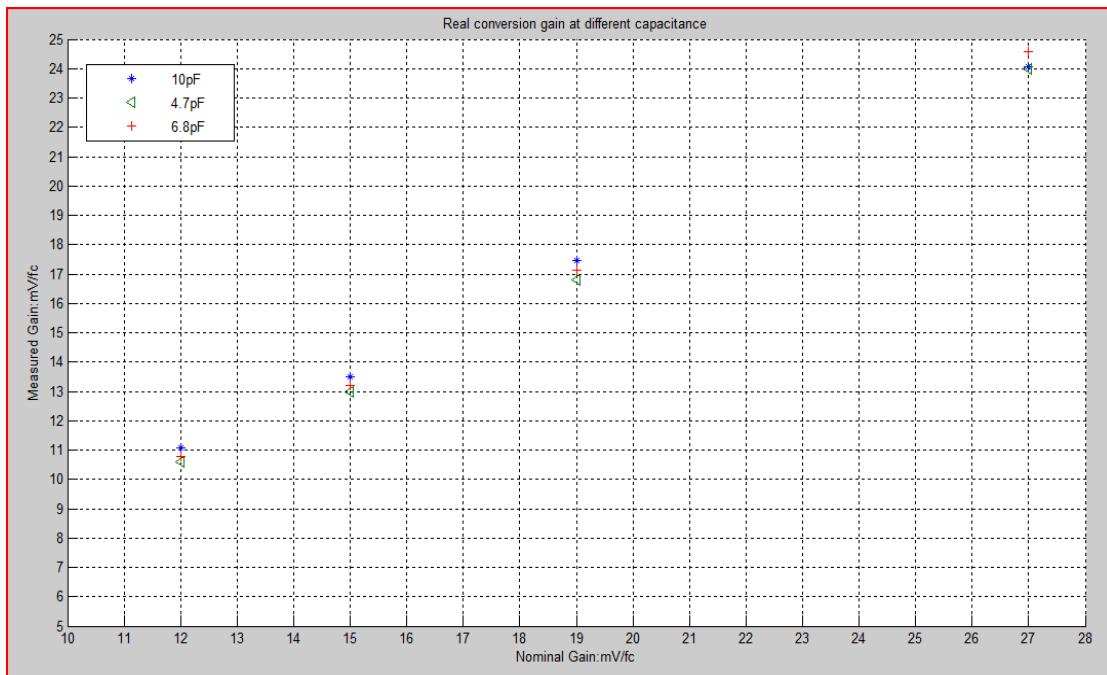

Figure 6.23 real gain versus nominal gain

As we can see from fig 6.23, the measured gain has a linear dependence on the nominal gain. It has dependence on the coupling capacitance. The higher coupling capacitance connected the higher gain value we get. At the same nominal gain (12 mV/fC) setting, the obtained gains at 4.345pF, 6.020pF, 8.964pF are 10.81mV/fC, 10.92mV/fC and 11.32mV/fC respectively.

One feature PCA16 is the programmability of different configurations which makes it suitable for general purpose readout electronics. The peaking time also influences the pulse output amplitude if the rise time of the input signal is comparable to or longer than the peaking time. Ideally the peaking time should be such that the actual time duration of the input signal is integrated in an optimal way, thus maximizing the SNR. The rise time of the input signal to the capacitor was chosen as 75 ns in order to meet the condition mentioned. As it shows in fig 6.24, the output amplitude goes up as the peaking time increases. As for the peaking time itself, if the rise time of the input pulse is smaller than the peaking time, the real peaking time is dominated by the electronics. Also the peak amplitude will be reduced as less charge has been integrated by the shaping amplifier if the rise time of the amplifier is short compared to the duration of the input charge.
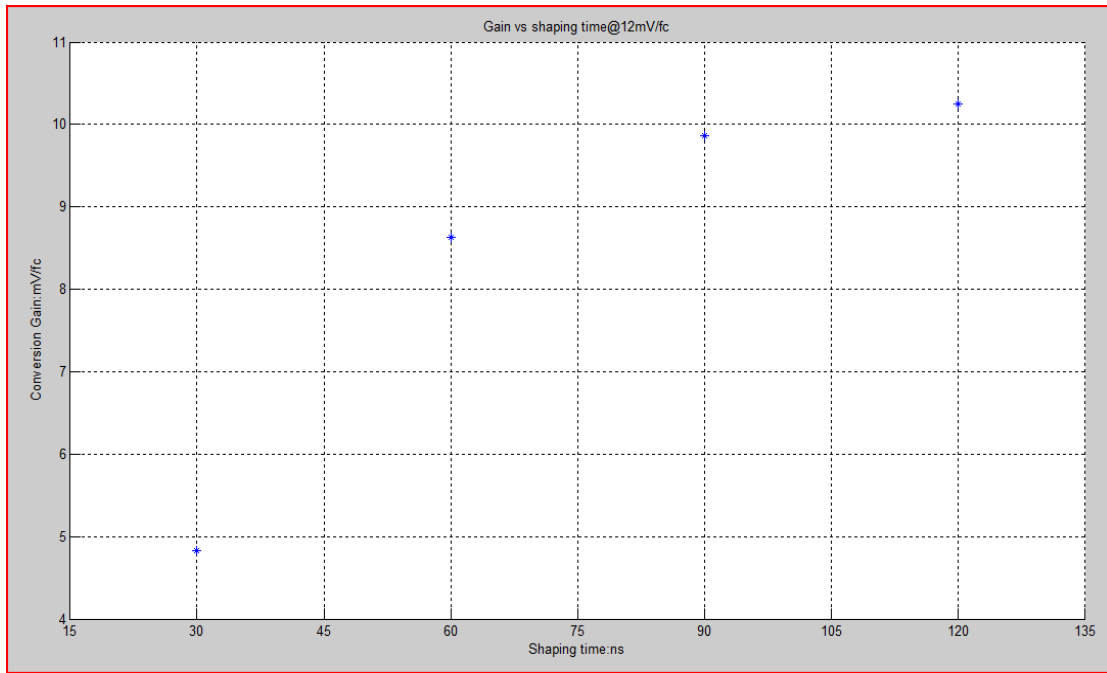
Figure 6.24 conversion gain versus peaking time (Here conversion gain is defined as the output/input ratio of the PCA16)

These effects are illustrated in fig 6.24 where the output amplitude is less than a factor two lower at 30ns shaping than at 120ns. There is nothing strange with a frequency dependent amplitude response of an amplifier system. For radiation detector readout, the matching of the peaking time to the actual input signal is thus essential so that it is used where the conversion gain changes only little with the temporal characteristics of input signal from the detector.
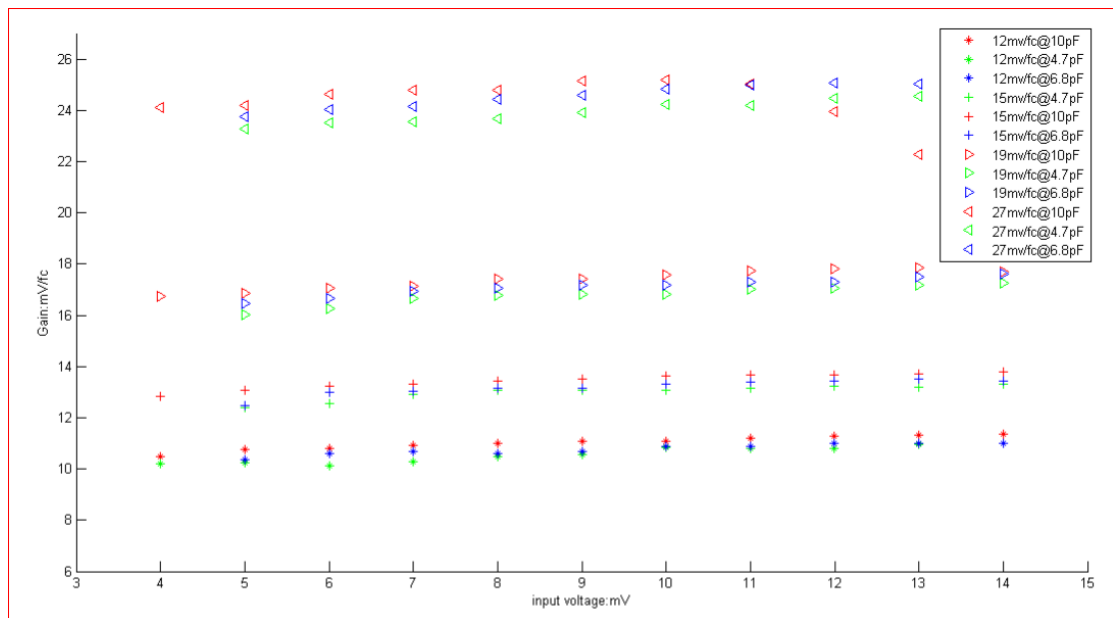

Figure 6.25 measured gain versus input voltage at the coupling capacitance

From fig 6.25 it is clear that the deduced conversion gain increases slightly as the coupling capacitance increases as we discussed above. The conversion gain also depends on the input voltage weakly. The main contribution for this is due to the working limit of signal generator. When we send the step voltage, it is not an ideal step voltage in the sense that

the rise time has to be taken into consideration. For the fixed limit rise time 5ns in our case, the frequency content of the same signal at different amplitude varies.

6.3 Conclusion

The ALTRO chip+PCA16 shows high linearity, low noise (below 600 electrons), and high stability. The carrier board FEC77 fulfills all the tasks in the signal processing chain: amplification, shaping, digitization, baseline correction, digital processing and storage etc. It provides 50 µs recording time at 20 MHz sampling rate, low power consumption, variable gain, peaking time, and polarity, which makes it suitable for general readout tasks. However, the requirement of a long Kapton cable to the TPC contributes to around 40% of the system noise in our test environment. Based on the advanced CMOS technology, the merging of PCA16 and ALTRO into a single chip named S-ALTRO16 reduces the chip size by a factor of 2 to meet the future LC requirements. Detailed discussion of this chip is given chapter 7.

References

[1] "ALICE TPC Readout Chip User Manual". CERN, June 2002 DRAFT 0.2

[2] "The ALICE TPC, a large 3-dimensional tracking device with fast readout for ultra-high multiplicity events" by J.Alme, etc: Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment. Volume 622, Issue 1, October 2010, page 316-367.

[3] "ALICE TPC PASA: technical specifications" ALICE TPC Collaboration

[4] "Description of the Saltro-16 chip for gas detector readout", CERN, Switzerland, LCD-Note-2011-024.

[5] TSA1001 data sheet.

[6] "The pre Amplifier shaper for the ALICE TPC detector" by H.K. Soltveit etc. Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment. Volume 676, 1 June 2012, pages 106-119.

[7] "techniques for nuclear and particle physics experiment: A How-To Approach", by William R.Leo, Springer, 1994

[8] "Design of analog CMOS integrated circuit" by Behzad Razavi, first edition, ISBN-10:0072380322

Chapter 7   The S-ALTRO16 chip and future readout system

In the first part of this chapter, test results from the super ALTRO (S-ALTRO16) are presented. In section 7.2 the design plans for a readout system based on the S-ALTRO16 chip is given. This solution would compact the construction by about a factor 40 compared to the FECs used in the previous sections. This will be approximately compatible with the size constraints of a final TPC at the ILC.

7.1   The first measurements on the S-ALTRO16 ASIC

The S-ALTRO16 chip is the successor of ALTRO system, which was designed for the TPC detector in ALICE. The technological breakthrough is that the preamp/shaper function previously placed in the PCA16 chip is now integrated into the same silicon die with the ALTRO digital functions. The chip is 5.75mm by 8.56mm manufactured in 190µm CMOS technology. Basically, S-ALTRO16 was designed with the same functionalities as the PCA16+ALTRO chips together but to mix a highly sensitive analog frontend together with digital circuitry in the same silicon is a challenge from noise point of view. Another new key feature of the S-ALTRO16 is the concept of power pulsing in order to switch off the power supply to the chip and thus limit the heat generated when the system is inactive. Tests of the S-ALTRO16 in PGA package from CERN showed its full ability of the design with little degradation of analog performance [3]. In terms of RMS noise, it showed around 0.7 ADC count (LSB) with lowest gain and longest peaking time i.e. slightly worse than the performance of the separated PCA16+ ALTRO studied in previous chapters. PGA package is however not ideal from noise point of view and the chip in QFP package is tested in our bench tests.

The test board used is shown in fig 7.1. Since the S-ALTRO16 chip is signal compatible with the PCA16-ALTRO combination, the communication with the test board is roughly identical to what was needed for the FEC77 used in the previous chapters. The test board is equipped with two test positions, one for chips in PGA package and the other with a socket for QFP package. One of the purposes with the tests on the FEC77 in chapters 2-6 was to develop the test procedures so that the first S-ALTRO16 prototype chips could be tested and compared to the previous version. As we discussed, the total capacitance and resistance determines the system noise. The same arguments hold here as well. Capacitors with various capacitances (0pF, 10pF, 33pF, 100pF) were connected to the inputs of the S-ALTRO16 with 62 ohm series resistors on the amplifier inputs built into the chip for input protection. Noise from all 16 channels is shown in fig 7.2. It is clearly seen that the noise level is influenced by the capacitance connected. The noise level at different gain setting is shown in fig 7.3.
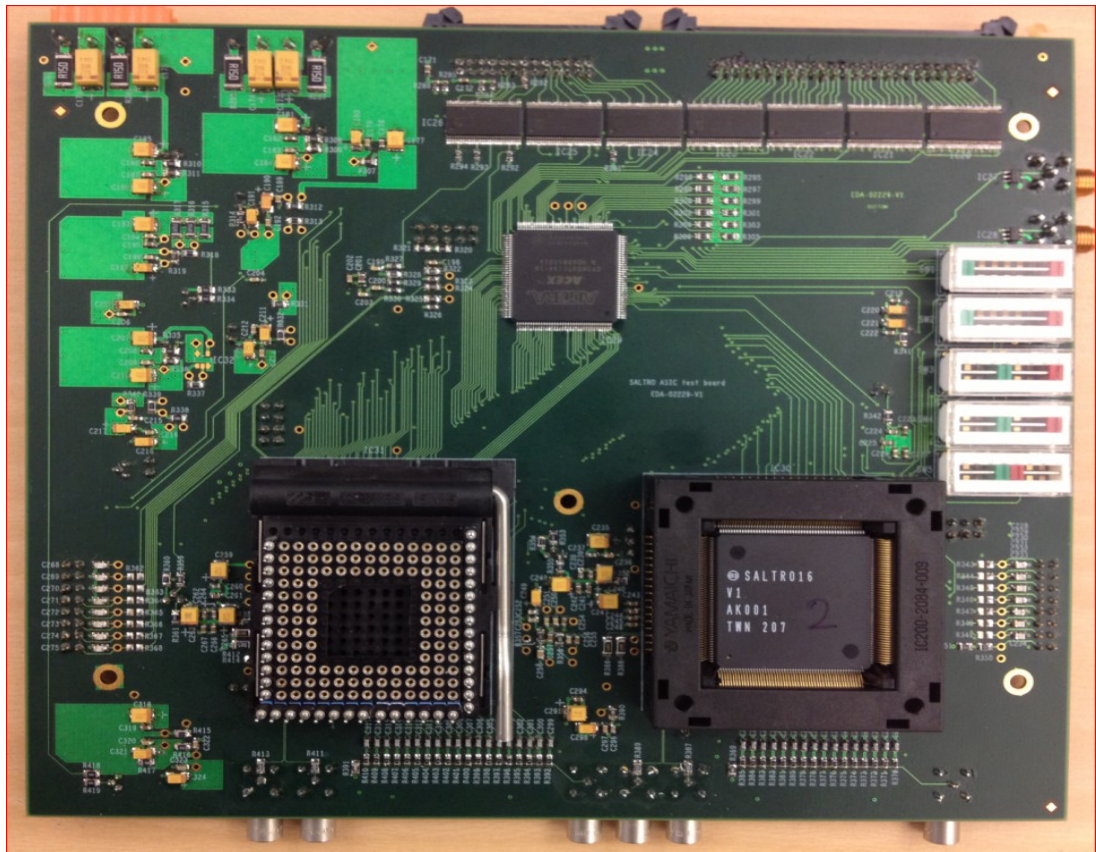
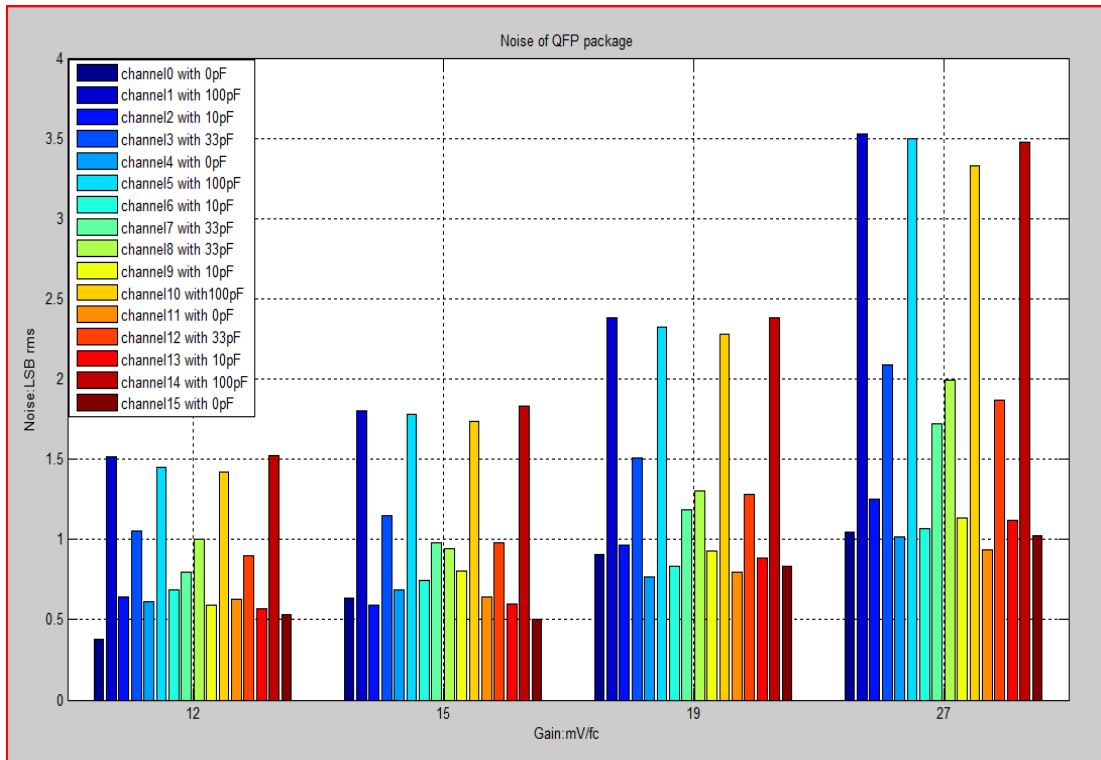Figure 7.1 test board for the S-ALTRO16 chip

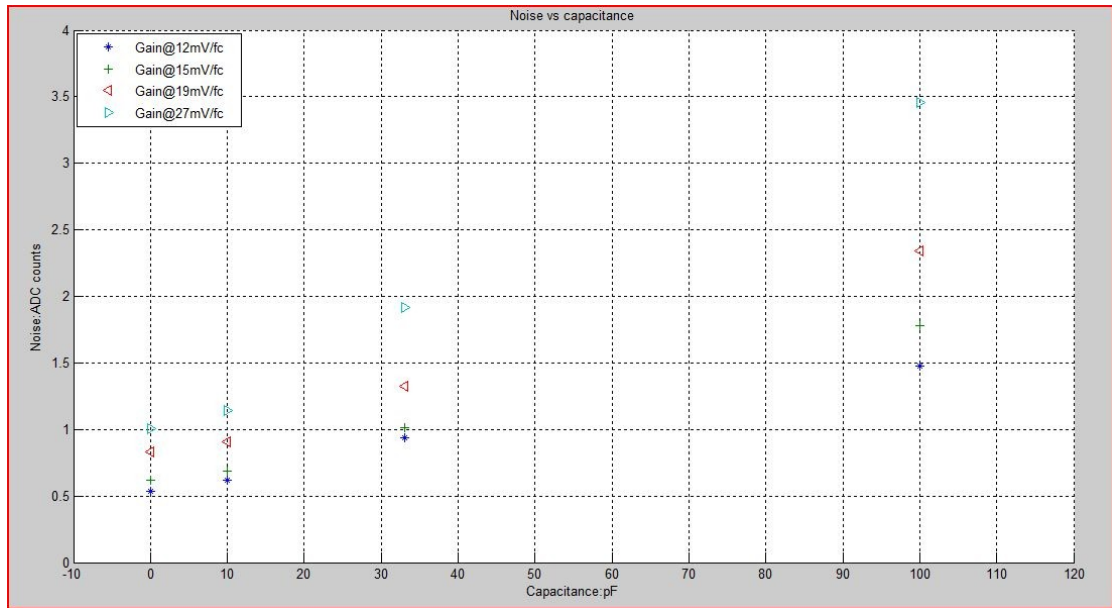Figure 7.2 RMS system noise versus channel@various gains

Figure 7.3 the system noise versus various capacitances to inputs of S-ALTRO16 chip

In fig 7.3, it is clearly indicated that the system noise goes almost linearly with the capacitance connected. At the same capacitance, the noise increases with the chosen gain value when measured in ADC units. It is reasonable since the noise gets amplified along with signal pulse. The system noise in equivalent noise charge is shown in fig 7.4. Note should be paid that the normalized noise electrons is based on the nominal gain value, which explains why there is discrepancy among different gains.
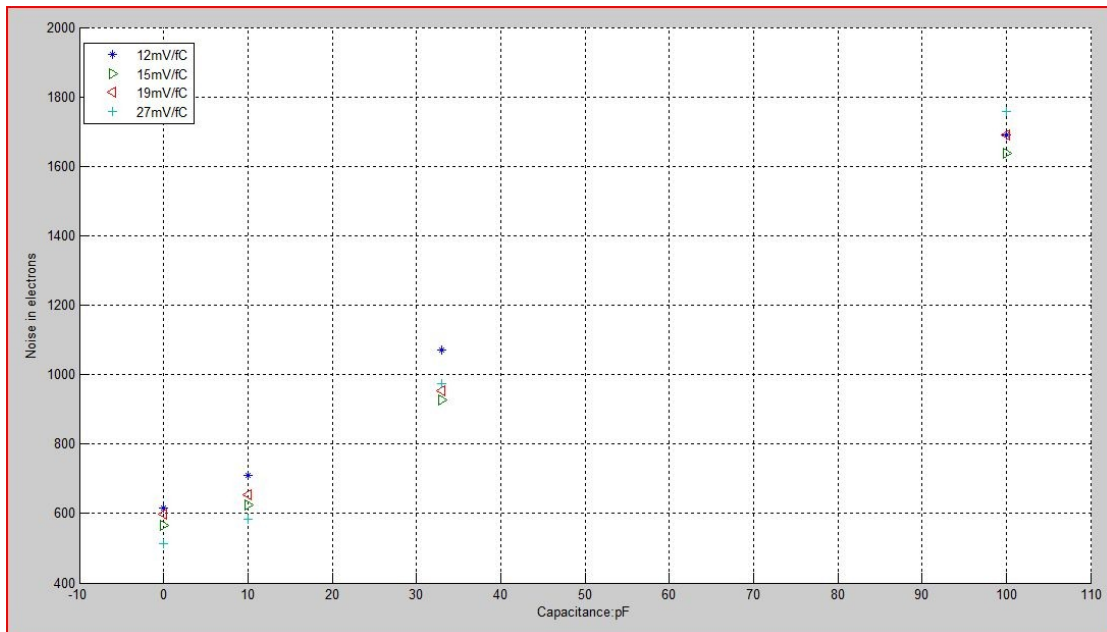

Figure 7.4 the system noise in equivalent noise charge

Here as we can perceive based on fig 7.4, 3.6-2 and 3.7-2, the noise in ENC is around 600 electrons for both chips (S-ALTRO16 and ALTRO system).

7.2   TPC readout system for LC-TPC

The physics goals presented in chapter 1 require that the TPC at LC project needs high performance in terms of spatial, momentum and dE/dx resolution. The most important one being the momentum resolution implies strong B-field which results in small lateral diffusion i.e. the electron cloud is small when arriving at the readout plane. This influences directly the optimization of the pad size to 1 by 5-6 mm^2. The available space for the front end electronics and the way to connect is determined by the pad size to a large extent since in a final system with multimillion number of pads per end cap, makes it necessary to fit the electronics belonging to a channel behind the actual pad. From the previous chapter, we also observed that the Kapton cables needed to connect between readout pads and FECs in the present version of the electronics add to the total noise of the system. Therefore, it is desirable to remove the cable connection with an innovative solution. This can also be done if the electronics for a pad fits behind it.

In order to meet the size constraints one cannot package the chips in QFP or similar package. The mounting of the naked silicon die on the PC board is necessary which however has drawbacks in terms of reparability.
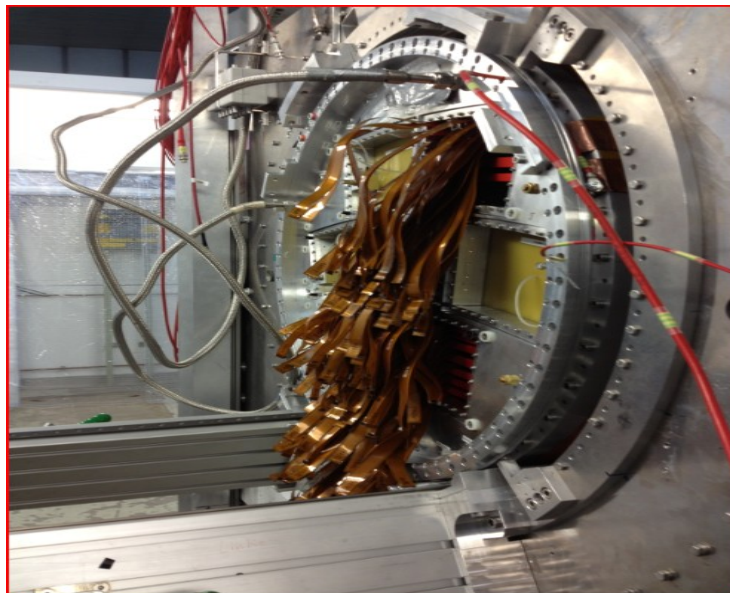

Figure 7.5 the complexity of Kapton cable connecting to the prototype TPC

The S-ALTRO16 dies are delivered untested and up to 10% of the chips can be expected to be non functional. Silicon die, wire bonded directly to the circuit board cannot be replaced and thus one cannot place 8 untested die on a fabrication unit. The yield will be too low. A transition solution is to employ a smaller carrier board (marginally larger than the die) to host the S-ALTRO16 chip which provides the necessary modularity for the manufacturing and reparability. The size of the carrier board is 12.0mm by 8.9 mm (whereas the SALTRO16 8.7mm by 6.2mm). Eight of these carrier boards are mounted on a Multi Chip Modules (MCM) with a so called ball grid array (BGA) that fits all connections underneath the carrier card. The MCM connects the TPC readout pads. The pulse signals are brought to S-ALTRO16 input via 4 multi-pin micro-connectors.
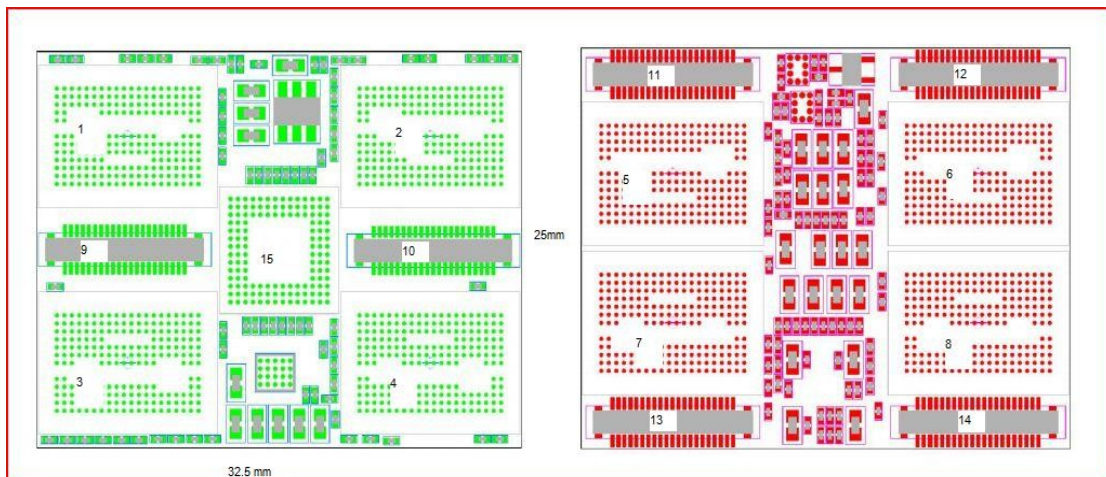
Figure 7.6 the MCM top (left) and bottom (right) side: 1-8 carrier board of SALTRO16; 9-10 HDMI connectors and LV connectors; 11-14 multi-pin micro connectors; 15 CPLD.[1]

The MCM serves the same role as FEC in ALTRO system. The MCM has the dimension of 25mm by 32.5 mm compared with 170 mm by 185 mm for FEC under test. With this achievable size, the MCM can be mounted to TPC pads directly without cable. Although the removal of Kapton cables could reduce the system noise, the scaling down of the system size and narrow separation of digital and analogue part may also contribute to system noise.

In the ALTRO system, data transfer between FECs and RCU is done with 40 bit wide parallel, bidirectional data bus through the back plane. In the S-ALTRO16 based system, a CPLD translates the data on the ALTRO bus to a serial protocol communicating data on one HDMI cable per MCM module. Basically, there are four types of communication between DAQ pc and individual S-ALTRO16 chip channel: 1. Send a command; 2. Write data to a register; 3. Read data from a register; 4. Read the data of an event. The SALTRO-16 expects these actions as parallel 40 bit data. The translation from serial data between DAQ and MCM to parallel data requested by the SALTRO16 is done by a CPLD on the MCM.

Several concepts have been considered for the readout and communication between DAQ PC and MCM. One promising candidate is the high speed serial (several Gbit per second) readout now offered by many chips. Parallel to serial conversion can be implemented inside the central CPLD. A general solution to serial data readout can be achieved through the so called Scalable Readout System which can handle 10 k channels which is suitable, at least in the prototyping stage. It contains a core FPGA and timing and trigger system for distribution of clocks and triggers. One SRU is able to cope with 40 MCMs. The communication between MCM and SRU can be accomplished by Data Trigger Control link (DTC). Slow control should be coded into high speed data and interpreted on the MCM. The schematic view of a serial readout system is shown in the fig 7.7.
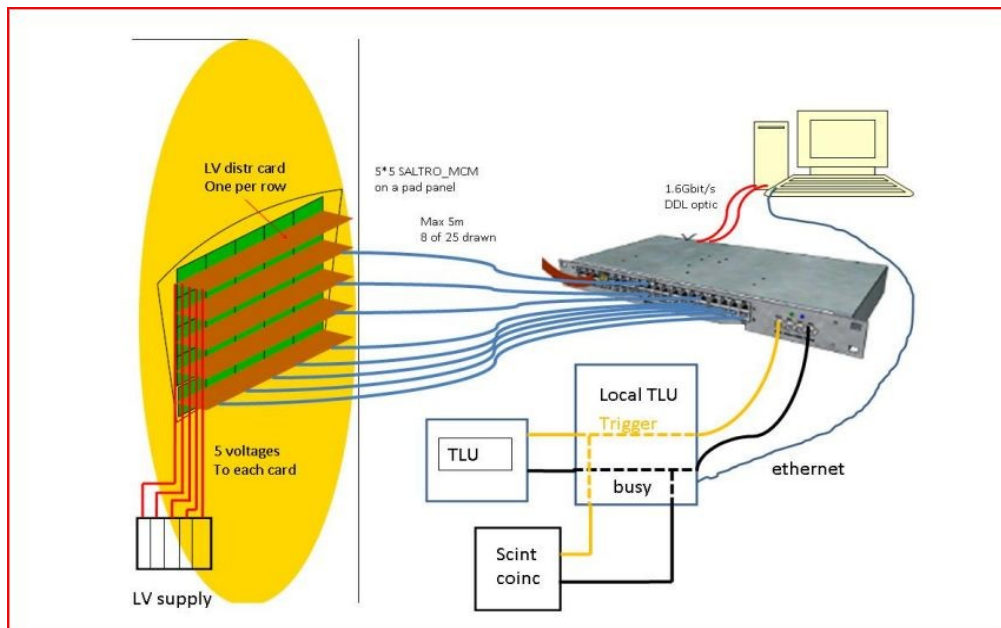
Figure 7.7 schematic view of a serial readout system [1]

The electronics connection is not only influenced by the available connectors but also the space for mechanical construction such as high voltage cables and cooling system which are key to the stability of the whole system.

From our test results and tests from other collaborations, the S-ALTRO16 shows good noise performance and stability. Power consumption is acceptable for the million channel scale system. Preliminary results for S-ALTRO16 show its good noise performance, power consumption, and stability of the chip functions. For a less critical which is needed for production of a full size system construction, the design needs to be another factor 2 more compact. This can be achieved by integrating more channels in the same silicon die. Either 32 or 64 channels per chip is likely the final choice.

In summary, the S-ALTRO16 shows satisfactory results in terms of noise. The functionalities are comparable to its predecessor the PCA16+ALTRO chips. New DSP within the chip was implemented to further reduce the power. Measurement results from other collaborators show that it has acceptable cross talk and linearity [9]. The successful integration at this stage makes the integration of higher density be desirable (32 or 64 channels per chip).

References

[1] "Development of the readout system for a TPC at the future linear collider", by V.Hedberg etc, LC-DET-2012-080.

[2] "Super-Altro 16: a Front-End system on the chip for DSP based readout of gaseous detectors" P.Aspell, M.De Gaspari, H.Franca etc, Draft for publication on IEEE Trans Nucl Sci. Submission number: TNS-00459-2012.

[3] The 16 - channel Super -ALTRO Demonstrator 2012 Nov from CERN.

[4] "Micropattern Gas Detectors", by Jochen Kaminski, 17th International Workshop on Vertex Detectors July 28-August 1, 2008.

[5] www-flc.desy.de/tpc/basicstpc.php

[6] "techniques for nuclear and particle physics experiment: A How-To Approach", by William R.Leo, Springer, 1994

[7] "The ALICE TPC, a large 3-dimensional tracking device with fast readout for ultra-high multiplicity events" by J.Alme, etc. Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment. Volume 622, Issue 1, October 2010, page 316-367.

[8] "the international large detector: letter of intent", by the ILD concept group Feb, 2010. ArXiv: 1006.3396.

[9]"Novel Front-end electronics for Time Projection Chamber Detectors", Eduardo José García García, Ph.D thesis, June 2012, Universidad Politécnica de Valencia

Appendix 1

In the previous discussion all results were given in the uncalibrated unit ADC channels except the calibration part. A nominal calibration can be obtained from the datasheet based on the target amplification from the chip design. For the 12mV/fC gain setting, one would then expect one input electron to give amplitude of the differential amplifier output of 1.92×10^{-3}mV. The ADC scale has 0.428 ADC counts per mV and thus one input electron should give 0.0080 ADC counts in PCA16+ALTRO system.

Due to process uncertainties one cannot expect the actual gain to be the same as planned and it needs to be calibrated. This can be accomplished by sending a step voltage over a capacitor to the input and the actually injected charge would be: *Q = step voltage/capacitance*. This is however a highly nontrivial task since the sensitivity is so large that, in order to obtain small enough charge, only capacitors in the low Pico farad range can be used. Then the question arises: what is the accuracy of the capacitance values of such components.

This calibration task initiated an evaluation of different methods of capacitance measurements.

The Schmitt trigger method

Figure 1 shows a circuit description of Schmitt trigger RC oscillator. The typical square wave output is shown on the right side. On top of it, the charging and discharging curve for the test capacitor is shown. By combining positive and negative feedback to the operational amplifier, an astable multivibrator is formed. Since the amplifier only works in the saturation region (positive feedback), the output from the operational amplifier can only take +Sat or -Sat which depends on the relation between inverting and non-inverting inputs of the amplifier. So the point T serves as the trigger point for transition. If the output is in +Sat, the C1 begins to charge until it reaches UTP (upper trigger point) which is defined by the voltage divider R3 and R2. Beyond this point, the output switches to -Sat. The same mechanism applies for the circuit flipping back to +Sat state. In real cases, there is a transition region between the states. However, the width of such states depends on the open loop gain of the operation amplifier, which is negative for the amplifier we used.

From the analysis above, we can draw the conclusion that the period of the output square wave depends on the value of Sat, trigger point, and the RC time constant of the charging path. In general the period can be calculated from the equation:

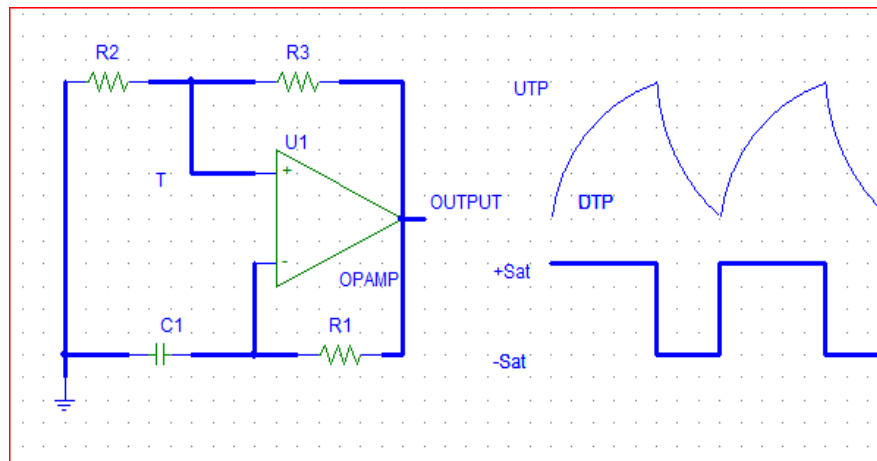$$T = 2R_1C_1 \ln(1 + 2\frac{R_2}{R_3}) \quad (1)$$

Figure 1 Schmitt trigger circuit and sample output

In Eq1, the period can be measured readily with oscilloscope. The simple linear relation makes it suitable for fitting and calculations. In figure 2, it shows the measured data which was fitted linearly with 4 valid digits. The fitted equation serves as the ideal equation as Eq.1 in this case. The real value was extracted and the relative error is shown for individual nominal data points. It is noticeable that the fitted equation has intercept which is not indicated in the euq1. The appearance of intercept is due to the parasitic capacitance from the implemented circuit which corresponds to around 10pF. The real implemented circuit is shown in figure 3.
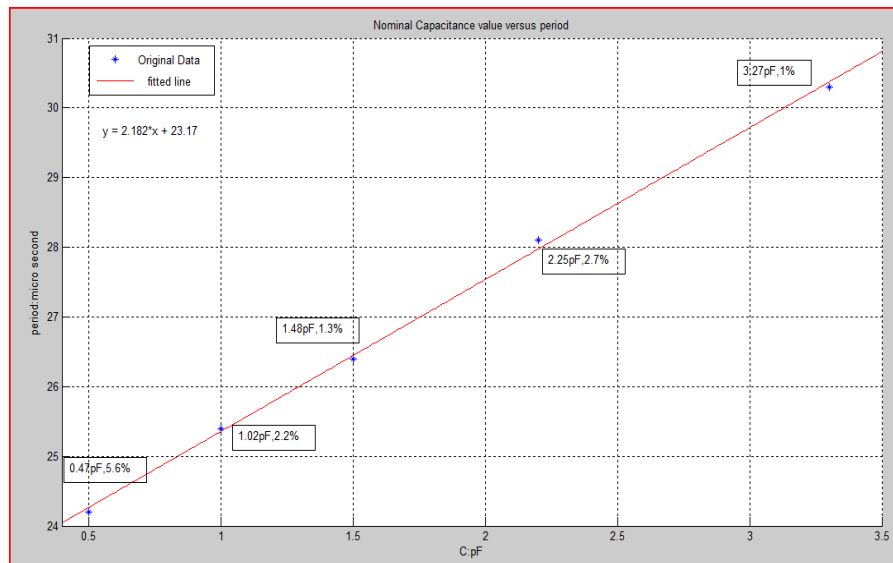

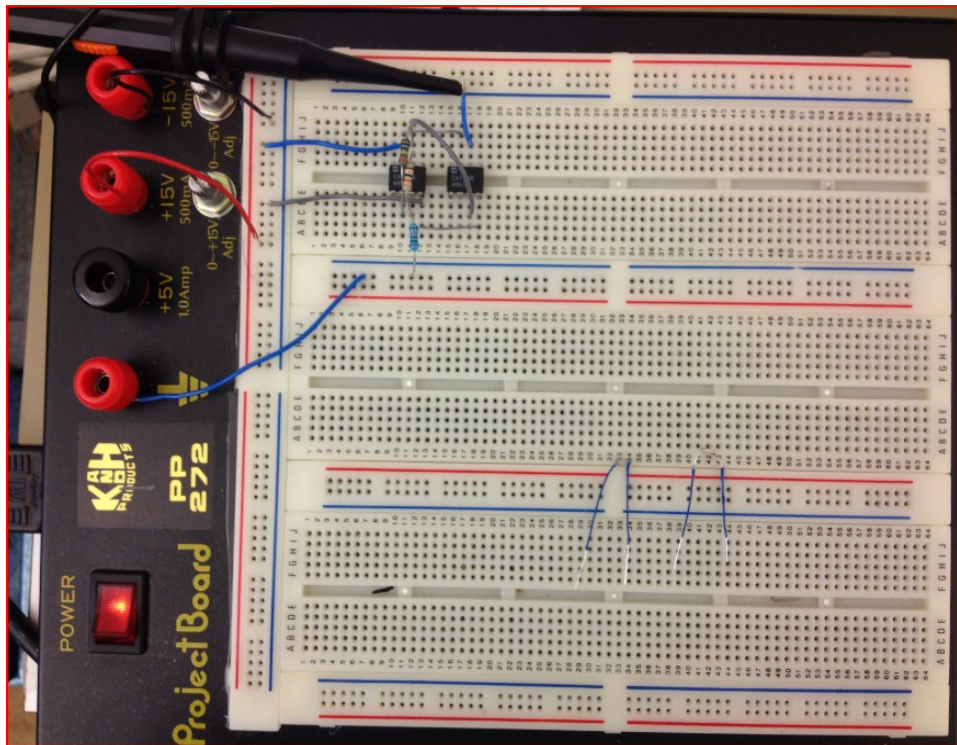Figure 2 Capacitance versus measured period and relative errors are also plotted

Figure 3 Schmitt trigger circuit.

It is shown that such parasitic capacitance also contributes to the slope of the line which accounts for part of the deviation from fitted line from calculated one.

Capacitance measurement with UTI

The UTI interface is a complete front end for capacitive sensors and widely used in temperature, displacement, humidity measurements. It features high resolution, long distance and continuous auto-calibration of gain and offset etc. The whole interface is developed by Delft University. At distances up to a meter for measurements, it shows 14 bits resolution. The UTI was designed by combining two principles [1]:

✓ Four wire measurement (to suppress the parasitic capacitance).
✓ Three signal technique (to accomplish auto-calibration).

In figure 4, is shown how the UTI works conceptually. Both C_{p1} and C_{p2} are parasitic capacitances which become short-circuited by the chip. The C_x under measurement is excited by the voltage signal from chip output, and the charge signal or current is collected on the right side input in fig 4. The induced charge on the input controls the excitation period to which the C_x is proportional. Below, the three signal technique is briefly introduced. A detailed description can be found in [1].
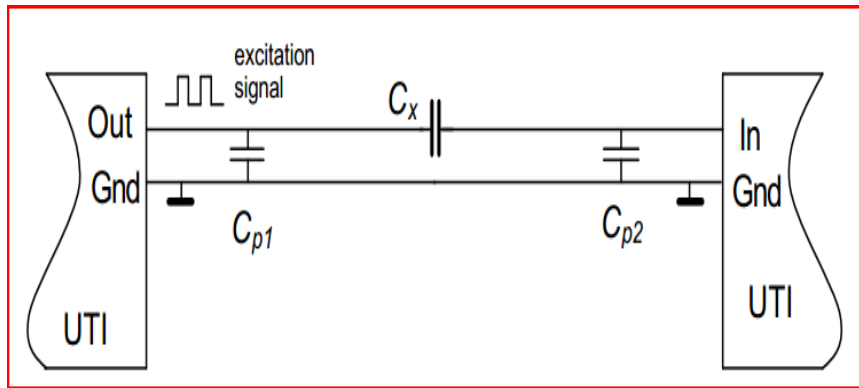
Figure 4 two-port UTI approach [1]

- The three signal technique

The three signal technique is supposed to eliminate the effects caused by unknown offset and unknown gain in a linear system. If we assume that the linear transfer function of a system is $M_x = A \cdot C_x + M_{off}$, where M_x is the measured period, A the unknown gain, C_x is the unknown capacitance, and M_{off} is the offset due to various reasons. Three periods (M_{off}, M_{ref}, M_x) are measured in order to extract the unknown capacitance. The ratio of this linear system is calculated to eliminate the offset and gain effects.

$$M = \frac{M_X - M_{off}}{M_{ref} - M_{off}} = \frac{C_x}{C_{ref}} \quad (2)$$

Such measurements and calculation is performed in a micro controller. The conceptual setup and real circuit are shown in figure 5 and figure 7 respectively.
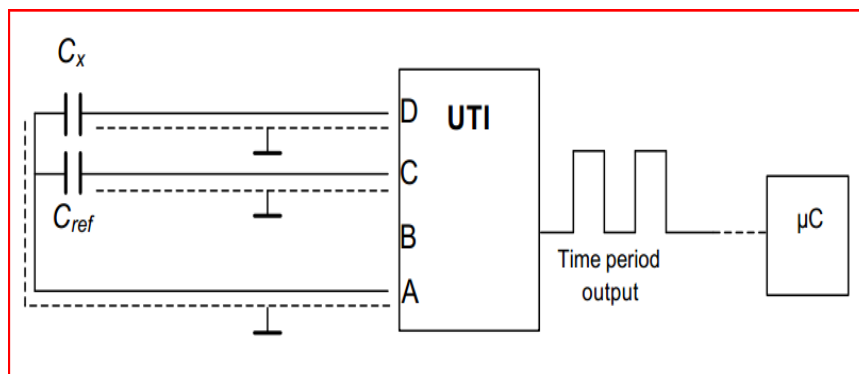

Figure 5 block diagram of UTI system [1]

The user interface between chip and PC is shown in figure 6. Slow mode was chosen which gives the best precision. The measured value is given on the average of 100 measurements and the standard deviation was well controlled below 0.00004.
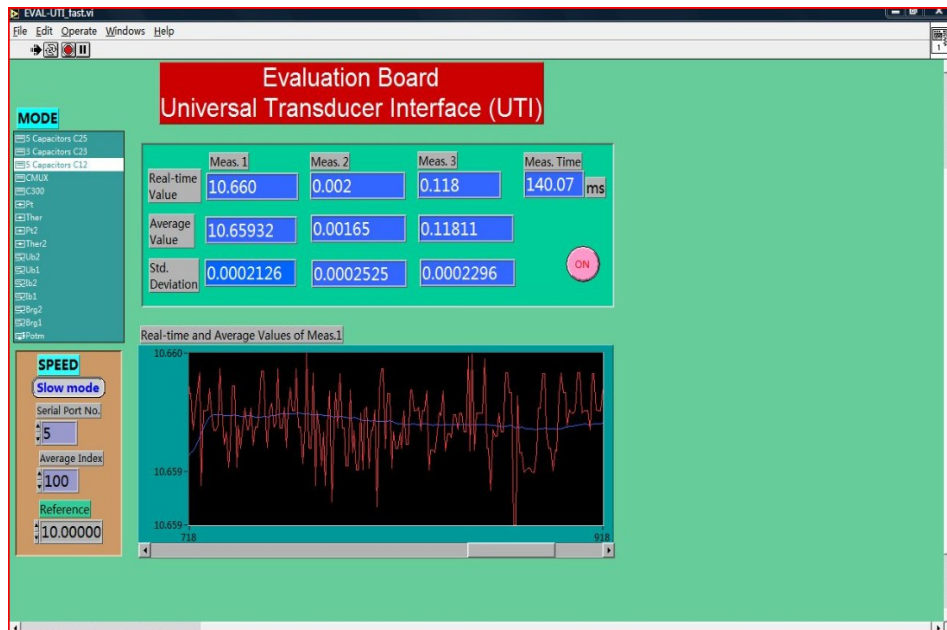
Figure 6 UTI user interface

The resolution of such measurement is dominated by two noise sources: thermal noise and quantization noise. It gives around 15 bit resolution as documented in the mode we selected. However, the measurement depends heavily on how precisely we know the reference capacitance value (Eq.1). Such reference capacitor was carefully chosen from high quality capacitors. Measured results were used to do calibration of the PCA16 + ALTRO readout chain and to understand the parasitic capacitance resides in various components such as connectors, cables, protection card etc.
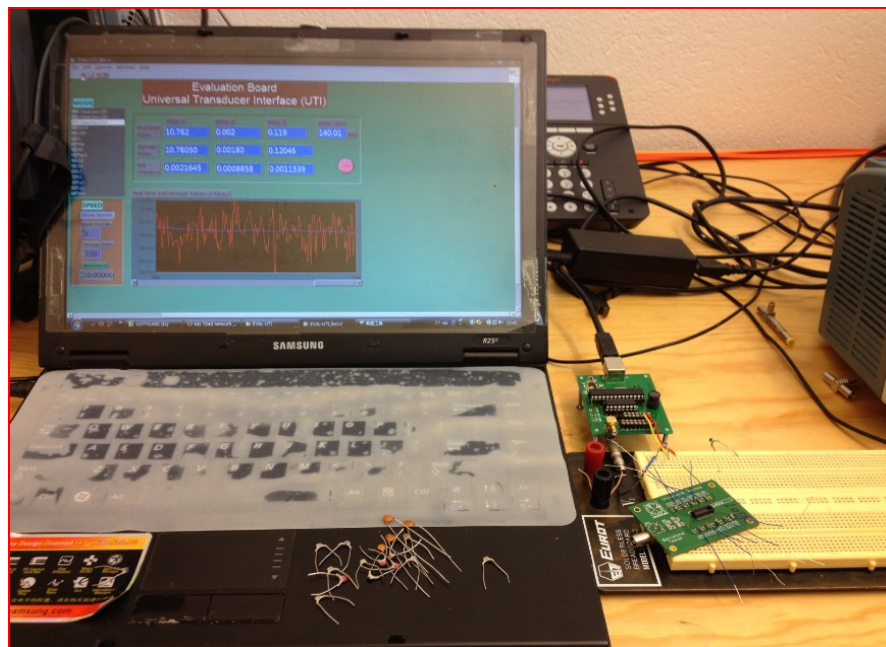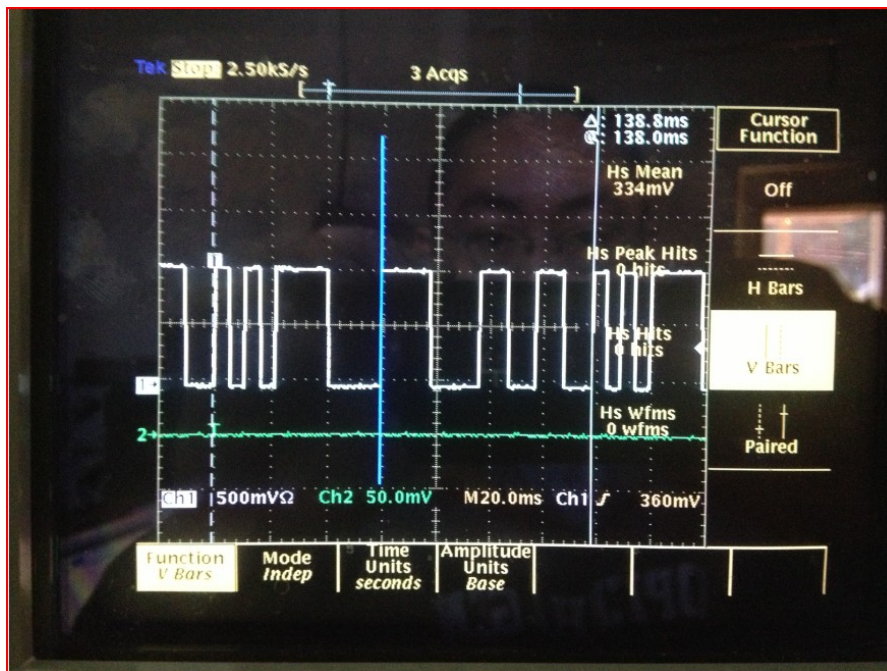

Figure 7 real setup

Figure 8 sample output directly from UTI chip

The measured capacitance based on UTI method is given in table below.

Nominal value	4.7pF	6.8pF	10pF
Measured value	4.346pF	6.020pF	8.964pF

Reference

[1] "Measuring accurately small-capacitive (and other)-sensor signal via long wires with a micro-controller", www.smartec.nl/pdf/apputi06.pdf