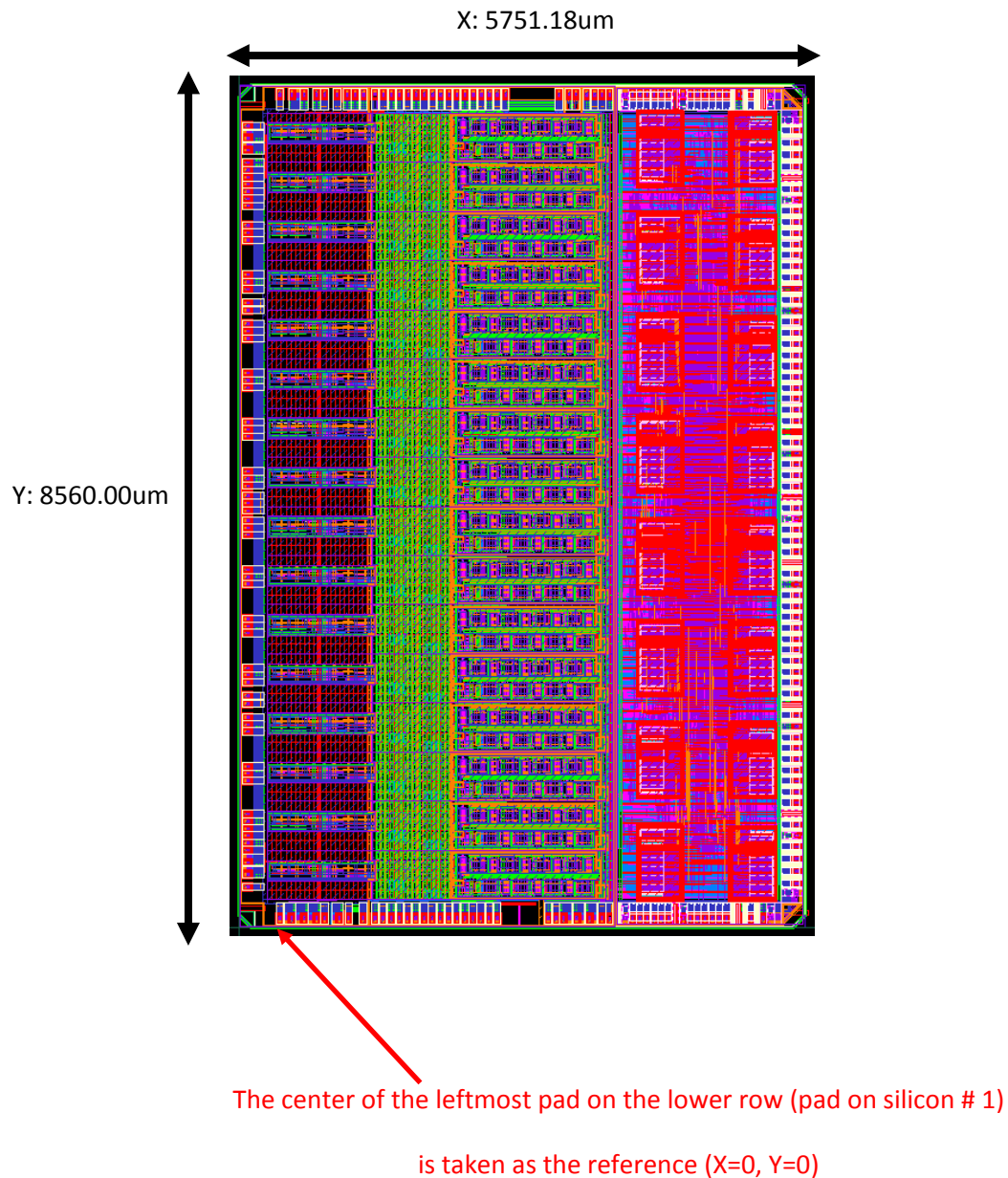


SALTRO16 Bonding Information

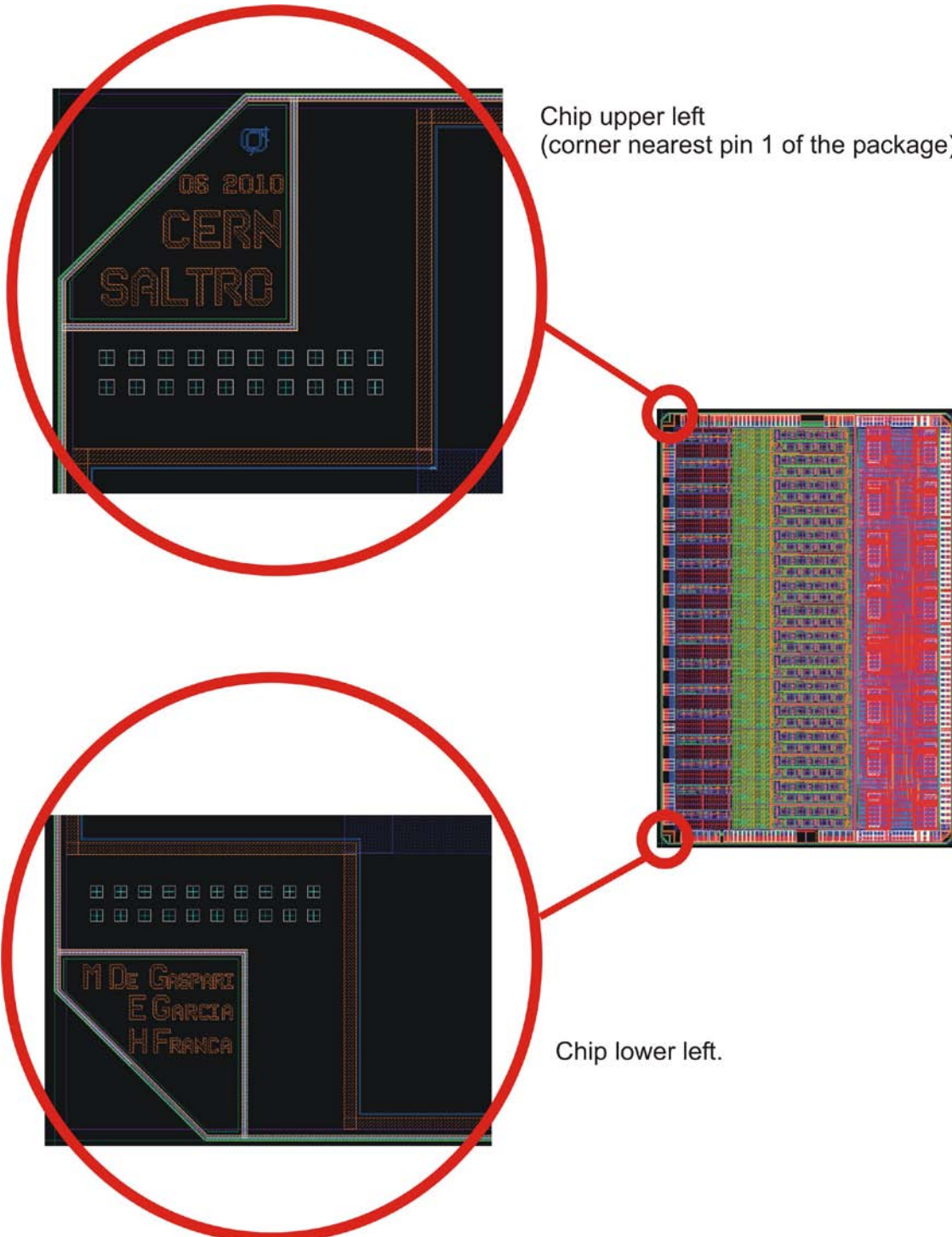
Chip Layout:



The indicated sizes refer to the sizes of the CHIPEDGE layer.

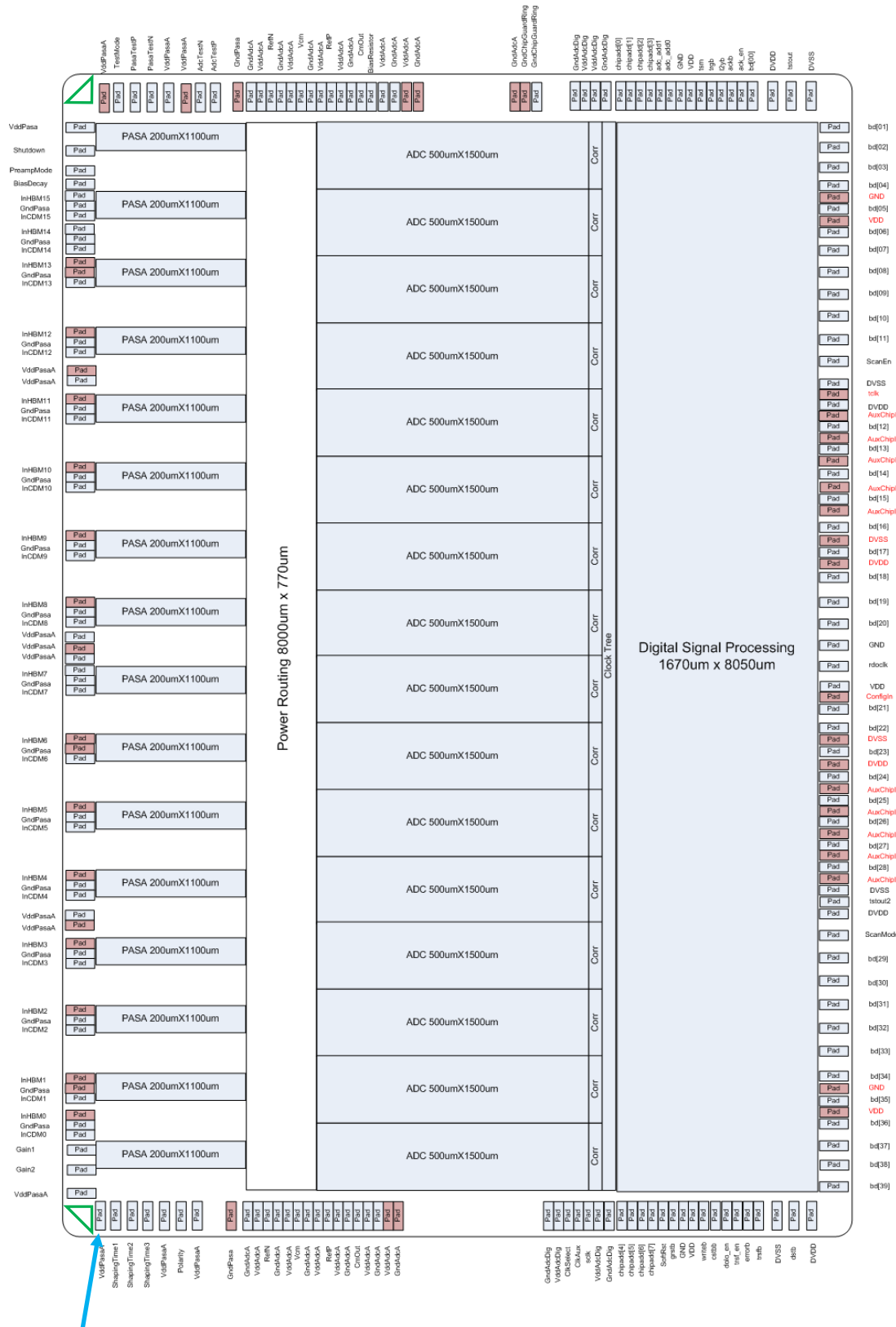
The Logo positions.

The chip has two logos. Both logos are located on the left side of the chip as shown below. The upper left logo is to be located nearest pin 1 of the package.



Pad names and location:

Pads in **brown** are left unbound (NC).



Pad on silicon #1

A total of 229 pads are located on the die; only 180 are bonded.

The table below shows the bonding connections required between the Pads on the silicon and the pins on the package. The origin for the coordinates is the center of the leftmost pad in the lower row of pads, units are um.

Pin # on Package	Pin # on Silicon	Pin Name	CenterX	CenterY
NC	167	VddPasaA	0.00	8398.09
1	168	VddPasaA	-329.55	8068.55
2	169	Shutdown	-329.55	7943.55
3	170	PreampMode	-329.55	7818.55
4	171	BiasDecay	-329.55	7693.55
5	172	InHBM15	-329.55	7620.55
6	173	GndPasaA	-329.55	7547.55
7	174	InCDM15	-329.55	7474.55
8	175	InHBM14	-329.55	7401.55
9	176	GndPasaA	-329.55	7328.55
10	177	InCDM14	-329.55	7255.55
NC	178	InHBM13	-329.55	7055.10
NC	179	GndPasaA	-329.55	6982.10
11	180	InCDM13	-329.55	6909.10
NC	181	InHBM12	-329.55	6555.10
12	182	GndPasaA	-329.55	6482.10
13	183	InCDM12	-329.55	6409.10
NC	184	VddPasaA	-329.55	6271.60
14	185	VddPasaA	-329.55	6192.60
NC	186	InHBM11	-329.55	6055.10
15	187	GndPasaA	-329.55	5982.10
16	188	InCDM11	-329.55	5909.10
NC	189	InHBM10	-329.55	5555.10
17	190	GndPasaA	-329.55	5482.10
18	191	InCDM10	-329.55	5409.10
NC	192	InHBM9	-329.55	5055.10
19	193	GndPasaA	-329.55	4982.10
20	194	InCDM9	-329.55	4909.10
NC	195	InHBM8	-329.55	4555.10
21	196	GndPasaA	-329.55	4482.10
22	197	InCDM8	-329.55	4409.10
23	198	VddPasaA	-329.55	4308.10
NC	199	VddPasaA	-329.55	4232.10
24	200	VddPasaA	-329.55	4156.10
25	201	InHBM7	-329.55	4055.10

26	202	GndPasaA	-329.55	3982.10
27	203	InCDM7	-329.55	3909.10
NC	204	InHBM6	-329.55	3555.10
NC	205	GndPasaA	-329.55	3482.10
28	206	InCDM6	-329.55	3409.10
NC	207	InHBM5	-329.55	3055.10
29	208	GndPasaA	-329.55	2982.10
30	209	InCDM5	-329.55	2909.10
NC	210	InHBM4	-329.55	2555.10
31	211	GndPasaA	-329.55	2482.10
32	212	InCDM4	-329.55	2409.10
33	213	VddPasaA	-329.55	2271.60
NC	214	VddPasaA	-329.55	2192.60
NC	215	InHBM3	-329.55	2055.10
34	216	GndPasaA	-329.55	1982.10
35	217	InCDM3	-329.55	1909.10
NC	218	InHBM2	-329.55	1555.10
36	219	GndPasaA	-329.55	1482.10
37	220	InCDM2	-329.55	1409.10
NC	221	InHBM1	-329.55	1069.55
NC	222	GndPasaA	-329.55	996.55
38	223	InCDM1	-329.55	923.55
NC	224	InHBM0	-329.55	850.55
39	225	GndPasaA	-329.55	777.55
40	226	InCDM0	-329.55	704.55
41	227	Gain1	-329.55	579.55
42	228	Gain2	-329.55	454.55
43	229	VddPasaA	-329.55	329.55
44	1	VddPasaA	0.00	0.00
45	2	ShapingTime1	125.00	0.00
46	3	ShapingTime2	250.00	0.00
47	4	ShapingTime3	375.00	0.00
48	5	VddPasaA	453.90	0.00
49	6	Polarity	607.97	0.00
50	7	VddPasaA	699.34	0.00
NC	8	GndPasaA	846.36	0.00
51	9	GndAdcA	968.89	0.00
52	10	VddAdcA	1049.26	0.00
53	11	RefN	1133.57	0.00
54	12	GndAdcA	1217.89	0.00
55	13	VddAdcA	1298.26	0.00

56	14	Vcm	1382.57	0.00
57	15	GndAdcA	1466.89	0.00
58	16	VddAdcA	1547.26	0.00
59	17	RefP	1631.57	0.00
60	18	VddAdcA	1713.26	0.00
61	19	GndAdcA	1798.89	0.00
62	20	CmOut	1880.57	0.00
63	21	VddAdcA	1962.25	0.00
64	22	GndAdcA	2043.93	0.00
NC	23	VddAdcA	2125.61	0.00
NC	24	GndAdcA	2207.29	0.00
65	25	GndAdcDig	2728.90	0.00
66	26	VddAdcDig	2806.10	0.00
67	27	ClkSelect	2883.30	0.00
68	28	ClkAux	3013.30	0.00
69	29	sclk	3143.30	0.00
70	30	VddAdcDig	3273.30	0.00
71	31	GndAdcDig	3350.73	0.00
72	32	chipadd [4]	3585.32	0.00
73	33	chipadd [5]	3658.32	0.00
74	34	chipadd [6]	3731.32	0.00
75	35	chipadd [7]	3804.32	0.00
76	36	SoftRst	3877.32	0.00
77	37	grstb	3950.32	0.00
78	38	GND	4023.32	0.00
79	39	VDD	4100.32	0.00
80	40	writeb	4173.32	0.00
81	41	cstbb	4246.32	0.00
82	42	dolo_en	4319.32	0.00
83	43	trsf_en	4392.32	0.00
84	44	errorb	4465.32	0.00
85	45	trsfb	4538.32	0.00
86	46	DVSS	4663.32	0.00
87	47	dstb	4788.32	0.00
88	48	DVDD	4913.32	0.00
89	49	bd[39]	5259.72	365.50
90	50	bd[38]	5259.72	490.50
91	51	bd[37]	5259.72	615.50
92	52	bd[36]	5259.72	740.50
NC	53	VDD	5259.72	852.60
93	54	bd[35]	5259.72	963.60

NC	55	GND	5259.72	1074.60
94	56	bd[34]	5259.72	1185.60
95	57	bd[33]	5259.72	1296.60
96	58	bd[32]	5259.72	1407.60
97	59	bd[31]	5259.72	1518.60
98	60	bd[30]	5259.72	1629.60
99	61	bd[29]	5259.72	1740.60
100	62	ScanMode	5259.72	1851.60
101	63	DVDD	5259.72	1962.60
102	64	tstout2	5259.72	2073.60
103	65	DVSS	5259.72	2184.60
NC	66	AuxChipIn[0]	5259.72	2295.60
104	67	bd[28]	5259.72	2406.60
NC	68	AuxChipIn[1]	5259.72	2517.60
105	69	bd[27]	5259.72	2628.60
NC	70	AuxChipIn[2]	5259.72	2739.60
106	71	bd[26]	5259.72	2850.60
NC	72	AuxChipIn[3]	5259.72	2961.60
107	73	bd[25]	5259.72	3072.60
NC	74	AuxChipIn[4]	5259.72	3183.60
108	75	bd[24]	5259.72	3294.60
NC	76	DVDD	5259.72	3405.60
109	77	bd[23]	5259.72	3516.60
NC	78	DVSS	5259.72	3627.60
110	79	bd[22]	5259.72	3738.60
111	80	bd[21]	5259.72	3849.60
NC	81	ConfigIn	5259.72	3960.60
112	82	VDD	5259.72	4071.60
113	83	rdoclk	5259.72	4182.60
114	84	GND	5259.72	4293.60
115	85	bd[20]	5259.72	4404.60
116	86	bd[19]	5259.72	4515.60
117	87	bd[18]	5259.72	4626.60
NC	88	DVDD	5259.72	4737.60
118	89	bd[17]	5259.72	4848.60
NC	90	DVSS	5259.72	4959.60
119	91	bd[16]	5259.72	5070.60
NC	92	AuxChipIn[5]	5259.72	5181.60
120	93	bd[15]	5259.72	5292.60
NC	94	AuxChipIn[6]	5259.72	5403.60
121	95	bd[14]	5259.72	5514.60

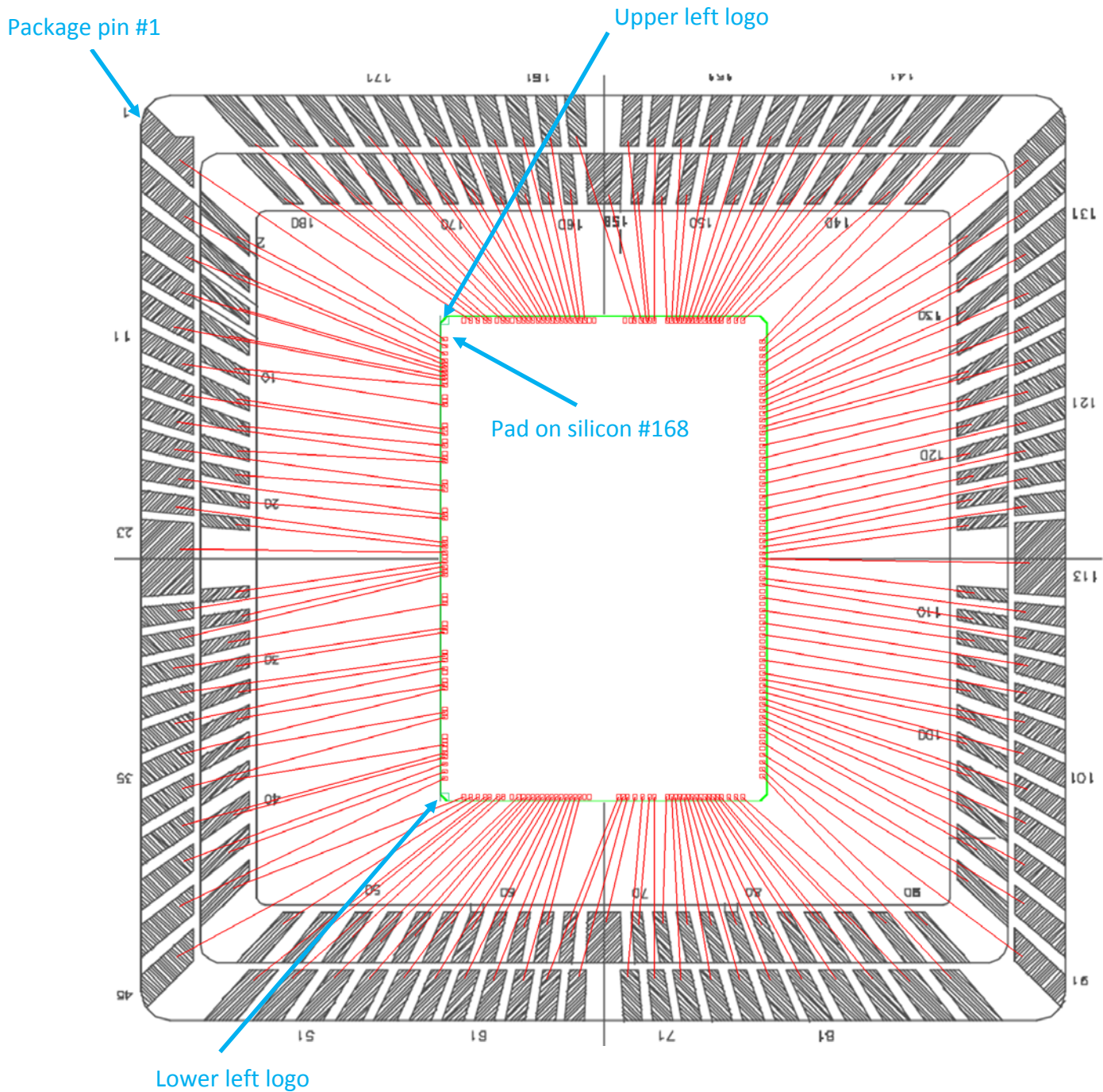
NC	96	AuxChipIn[7]	5259.72	5625.60
122	97	bd[13]	5259.72	5736.60
NC	98	AuxChipIn[8]	5259.72	5849.60
123	99	bd[12]	5259.72	5962.60
NC	100	AuxChipIn[9]	5259.72	6075.60
124	101	DVDD	5259.72	6188.60
NC	102	tclk	5259.72	6301.60
125	103	DVSS	5259.72	6414.60
126	104	ScanEn	5259.72	6527.60
127	105	bd[11]	5259.72	6640.60
128	106	bd[10]	5259.72	6753.60
129	107	bd[09]	5259.72	6866.60
130	108	bd[08]	5259.72	6979.60
131	109	bd[07]	5259.72	7092.60
132	110	bd[06]	5259.72	7203.90
NC	111	VDD	5259.72	7315.20
133	112	bd[05]	5259.72	7426.50
NC	113	GND	5259.72	7537.70
134	114	bd[04]	5259.72	7650.70
135	115	bd[03]	5259.72	7775.70
136	116	bd[02]	5259.72	7900.70
137	117	bd[01]	5259.72	8025.70
138	118	DVSS	4913.32	8398.09
139	119	tstout	4788.32	8398.09
140	120	DVDD	4663.32	8398.09
141	121	bd[00]	4538.32	8398.09
142	122	ack_en	4465.32	8398.09
143	123	ackb	4392.32	8398.09
144	124	l2yb	4319.32	8398.09
145	125	trgb	4246.32	8398.09
146	126	tsm	4173.32	8398.09
147	127	VDD	4096.32	8398.09
148	128	GND	4023.32	8398.09
149	129	adc_add0	3950.32	8398.09
150	130	adc_add1	3877.32	8398.09
151	131	chipadd [3]	3804.32	8398.09
152	132	chipadd [2]	3731.32	8398.09
153	133	chipadd [1]	3658.32	8398.09
154	134	chipadd [0]	3585.32	8398.09
155	135	GndAdcDig	3350.38	8398.09
156	136	VddAdcDig	3273.30	8398.09

157	137	VddAdcDig	3196.22	8398.09
158	138	GndAdcDig	3119.14	8398.09
159	139	GndChipGuardRing	3010.58	8398.09
NC	140	GndChipGuardRing	2937.58	8398.09
NC	141	GndAdcA	2837.41	8398.09
NC	142	GndAdcA	2292.92	8398.09
NC	143	VddAdcA	2211.24	8398.09
160	144	GndAdcA	2129.56	8398.09
161	145	VddAdcA	2047.88	8398.09
162	146	BiasGate	1966.20	8398.09
163	147	CmOut	1883.20	8398.09
164	148	GndAdcA	1798.89	8398.09
165	149	VddAdcA	1718.52	8398.09
166	150	RefP	1634.20	8398.09
167	151	VddAdcA	1552.52	8398.09
168	152	GndAdcA	1466.89	8398.09
169	153	Vcm	1385.20	8398.09
170	154	VddAdcA	1303.52	8398.09
171	155	GndAdcA	1217.89	8398.09
172	156	RefN	1136.20	8398.09
173	157	VddAdcA	1054.52	8398.09
174	158	GndAdcA	968.89	8398.09
NC	159	GndPasaA	852.30	8398.09
175	160	AdcTestP	766.67	8398.09
176	161	AdcTestN	683.67	8398.09
NC	162	VddPasaA	582.66	8398.09
177	163	VddPasaA	453.90	8398.09
178	164	PasaTestN	375.00	8398.09
179	165	PasaTestP	250.00	8398.09
180	166	TestMode	125.00	8398.09

The size of the opening of each pad is 95.03um x 62.00um.
The minimum pad pitch is 73um.

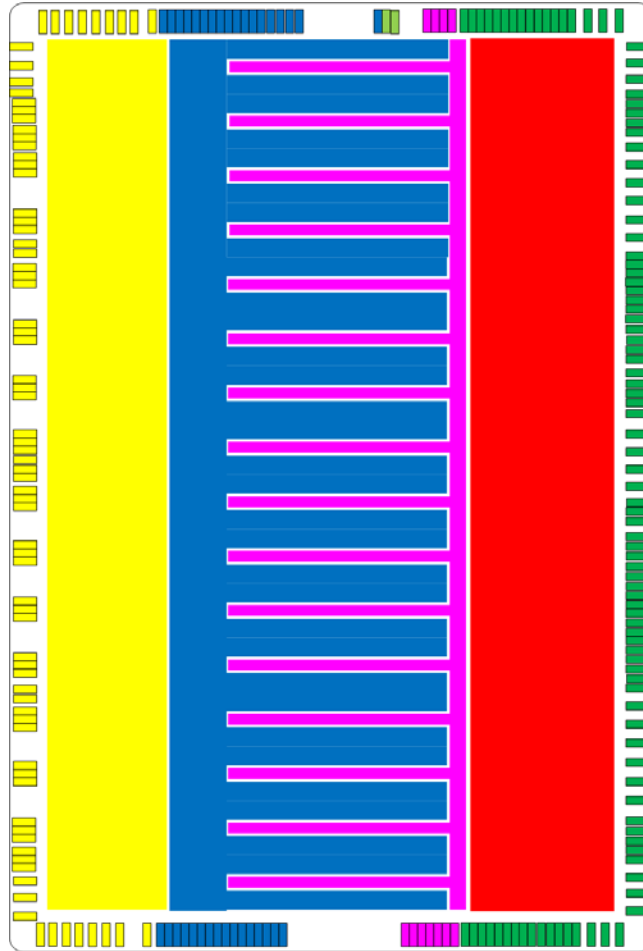
Total # signal IOs: 115.
Total # power pins: 65.

Bonding diagram in package PGA180:



Orientation of the silicon die: package pin #1 corresponds to pad on silicon #168.

Power domains:



Yellow: power domain of GndPasaA / VddPasaA; 135mW @ 1.5V.
Blue: power domain of GndAdcA / VddAdcA; 600mW @ 1.5V.
Purple: power domain of GndAdcDig / VddAdcDig; 150mW @ 1.5V.
Red: power domain of GND / VDD; 150mW @ 1.5V.
Green: power domain of DVSS / DVDD; 150mW @ 2.5V.
Light green: connection to the chip guard ring.

Next page:

Connections of the signals on the pins of the package. The colors correspond to the power domains. The grey rectangles are meant to identify the analog inputs of each channel and the PasaTest and AdcTest IOs of the test channel.

