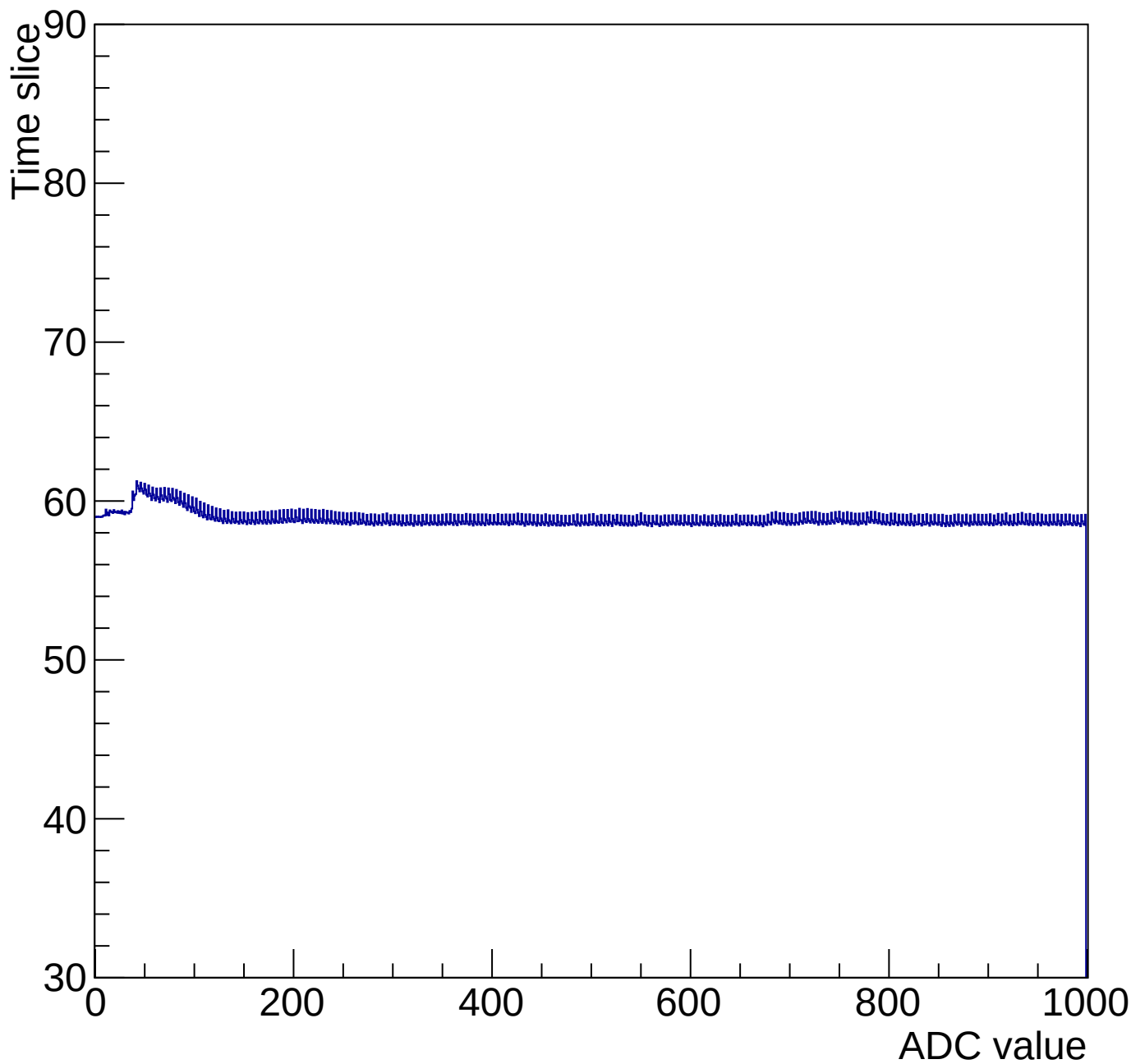
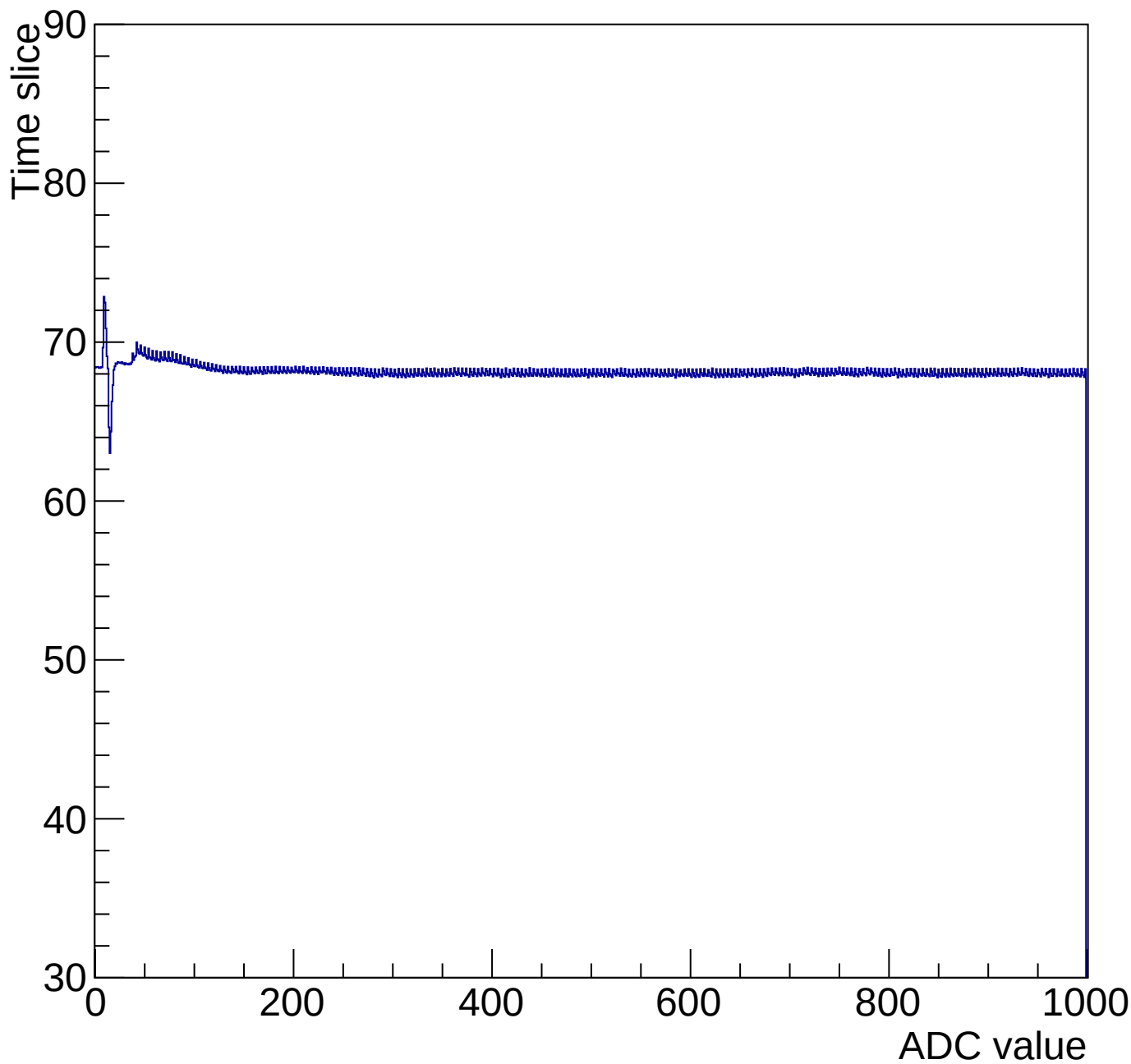


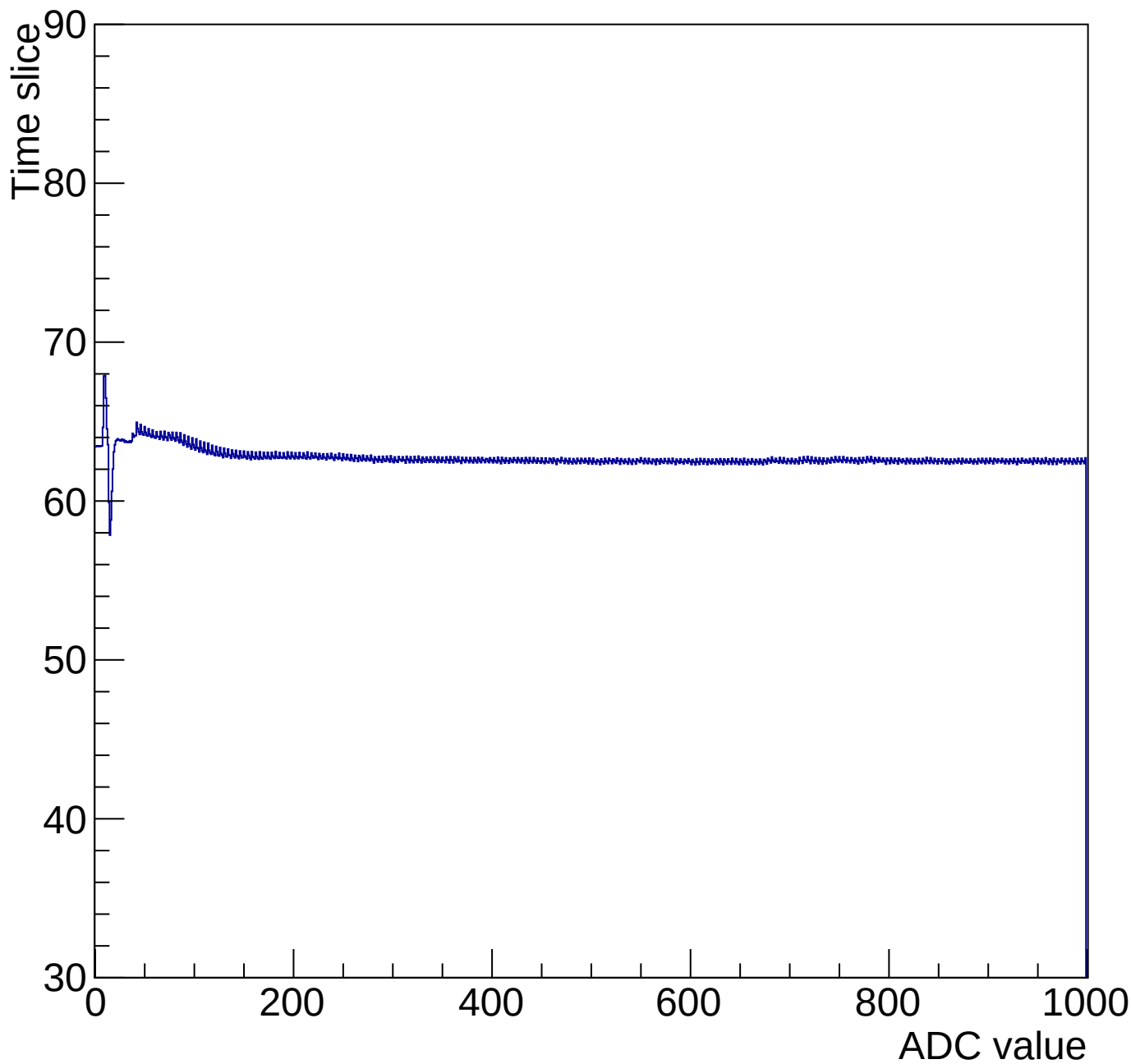
Time mcm 2000 chip 0 chan 0 1000-gain0-shaper0



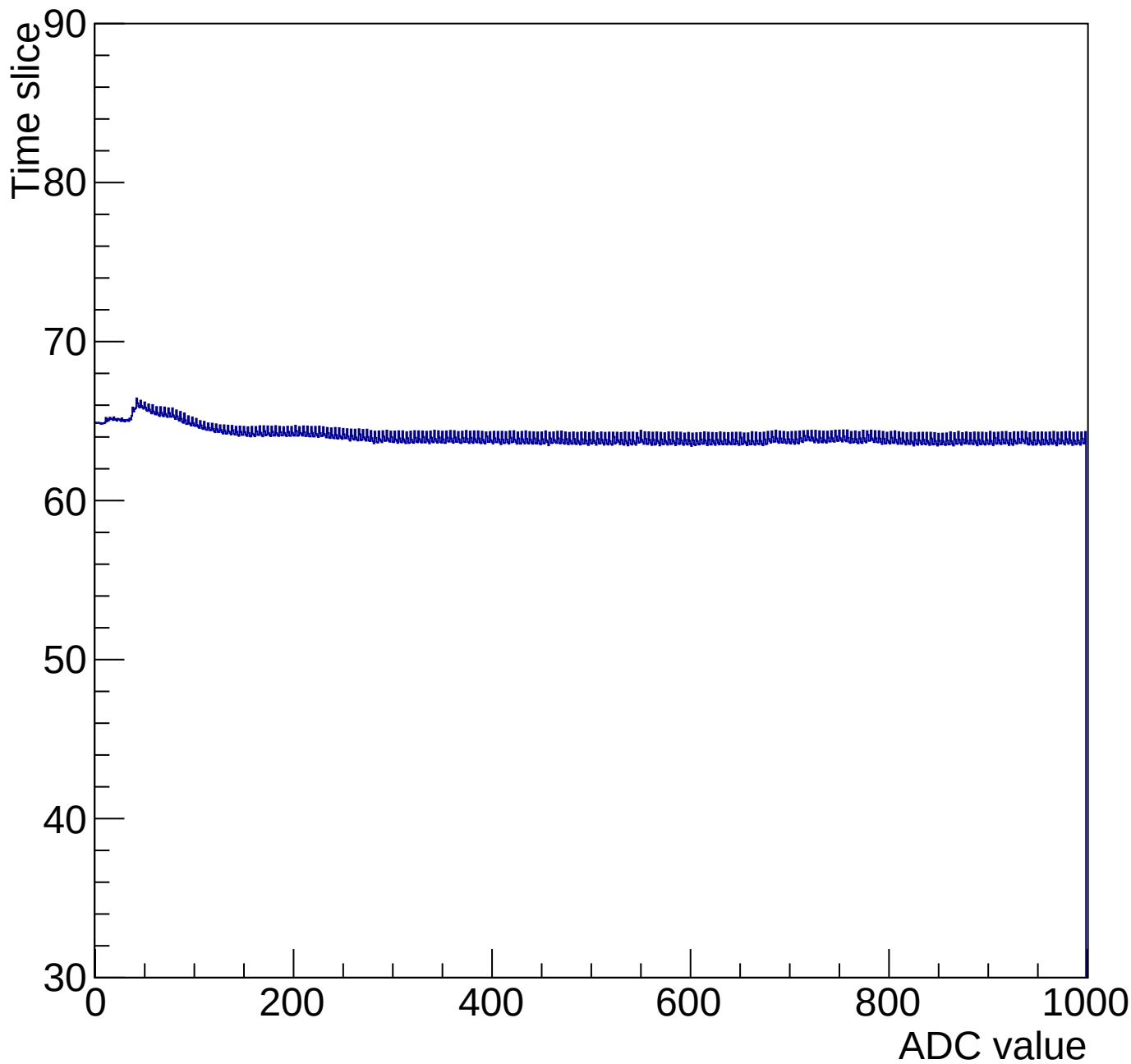
Time mcm 2000 chip 0 chan 1 1000-gain0-shaper0



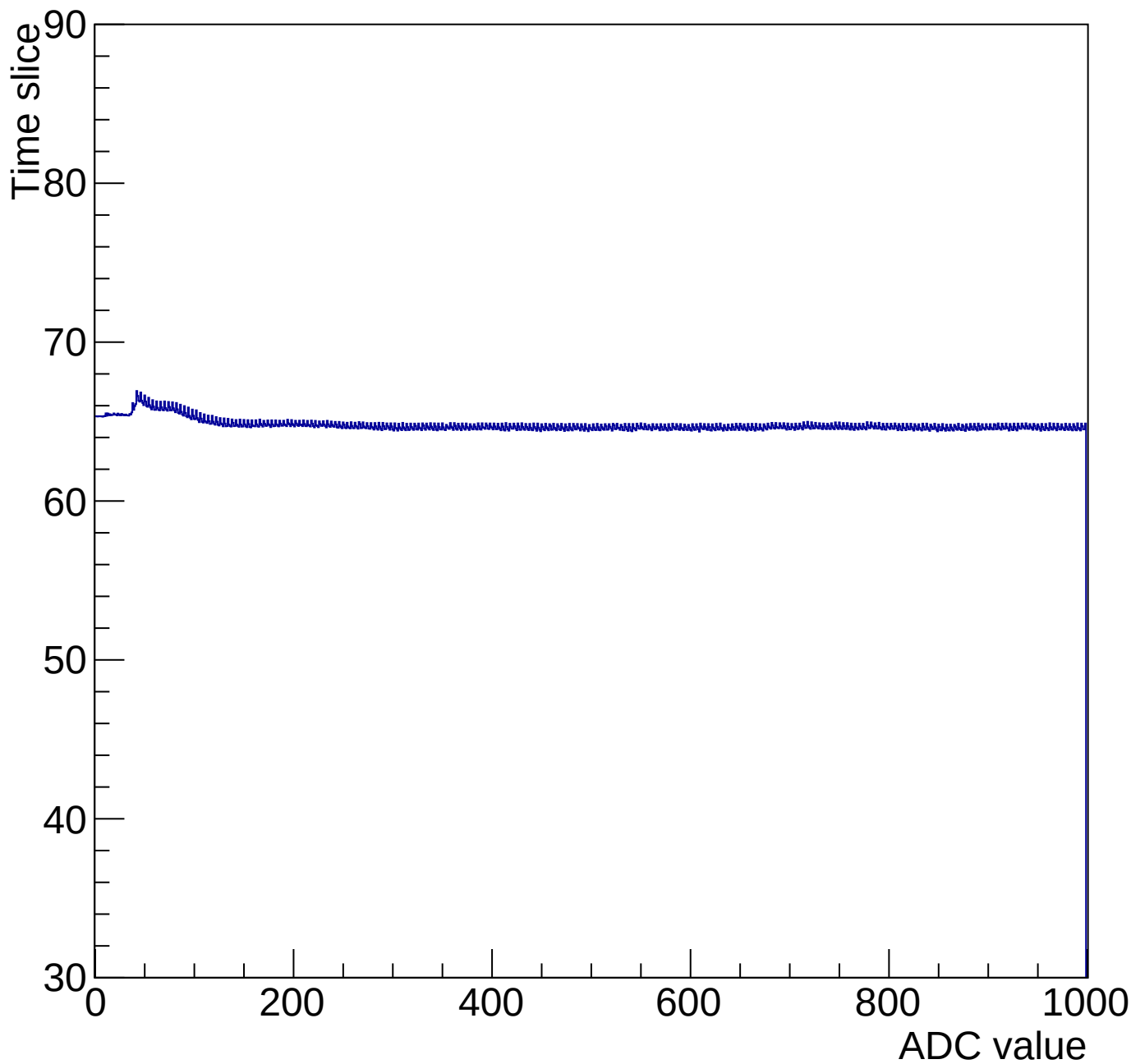
Time mcm 2000 chip 0 chan 2 1000-gain0-shaper0



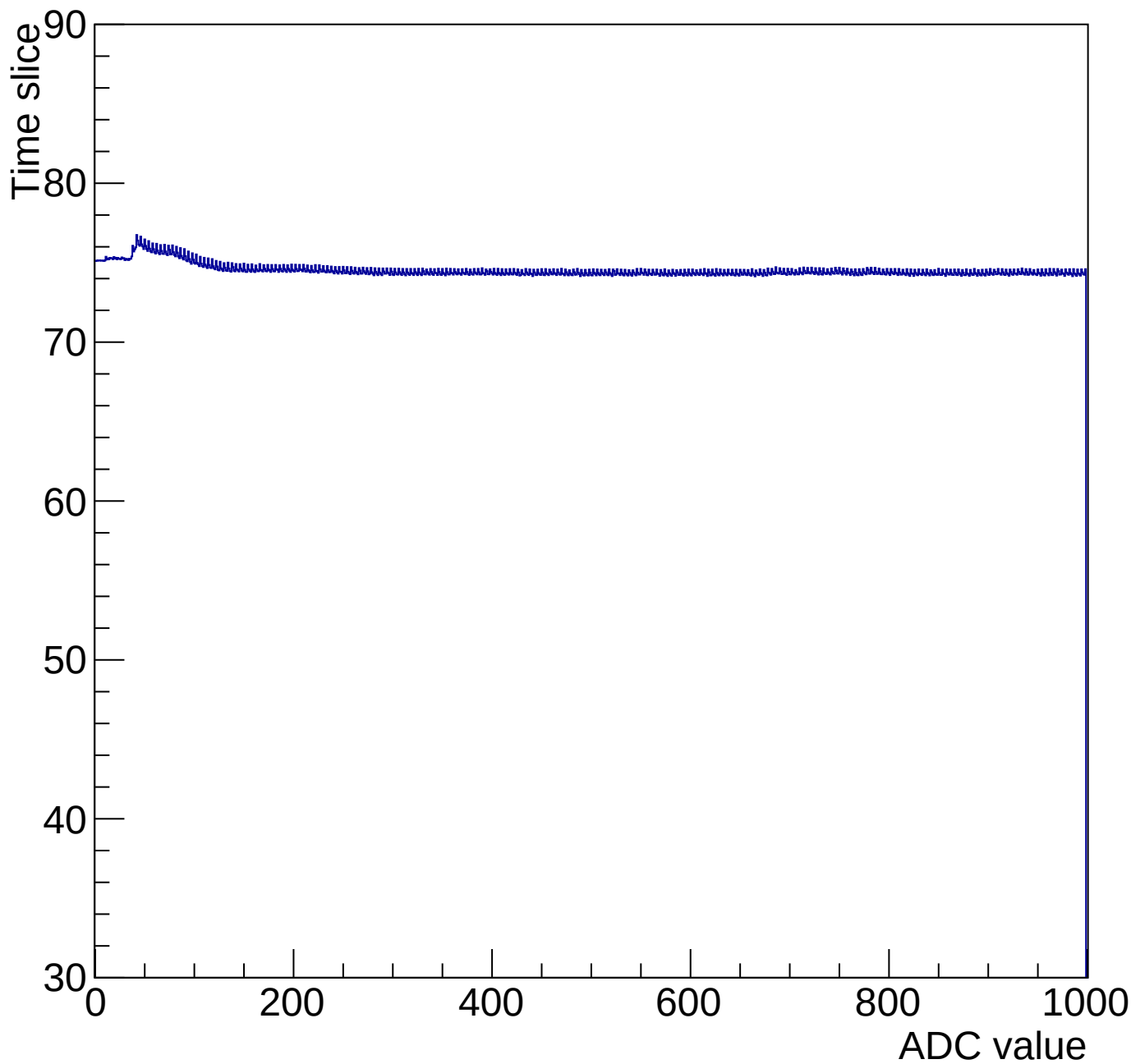
Time mcm 2000 chip 0 chan 3 1000-gain0-shaper0



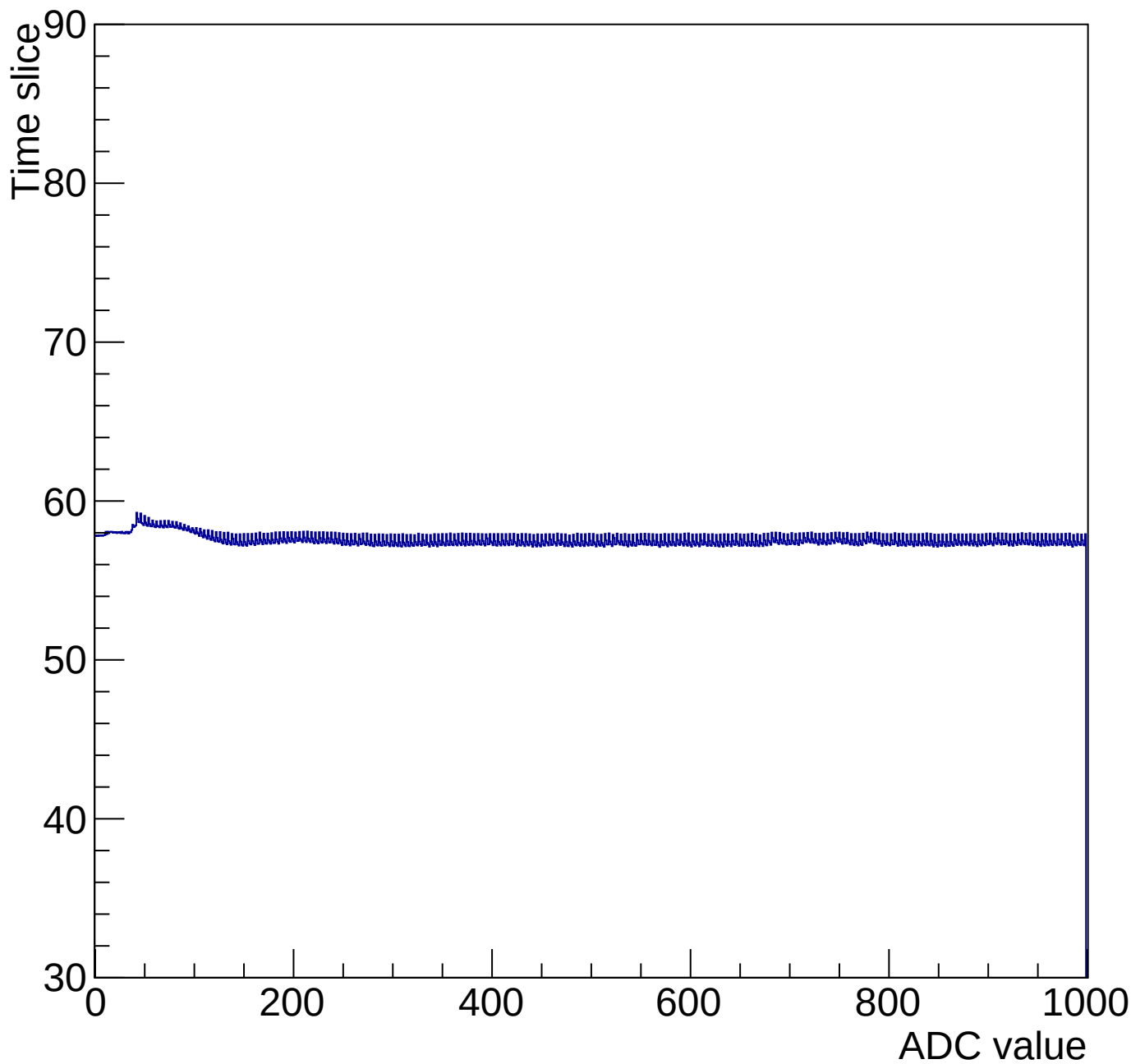
Time mcm 2000 chip 0 chan 4 1000-gain0-shaper0



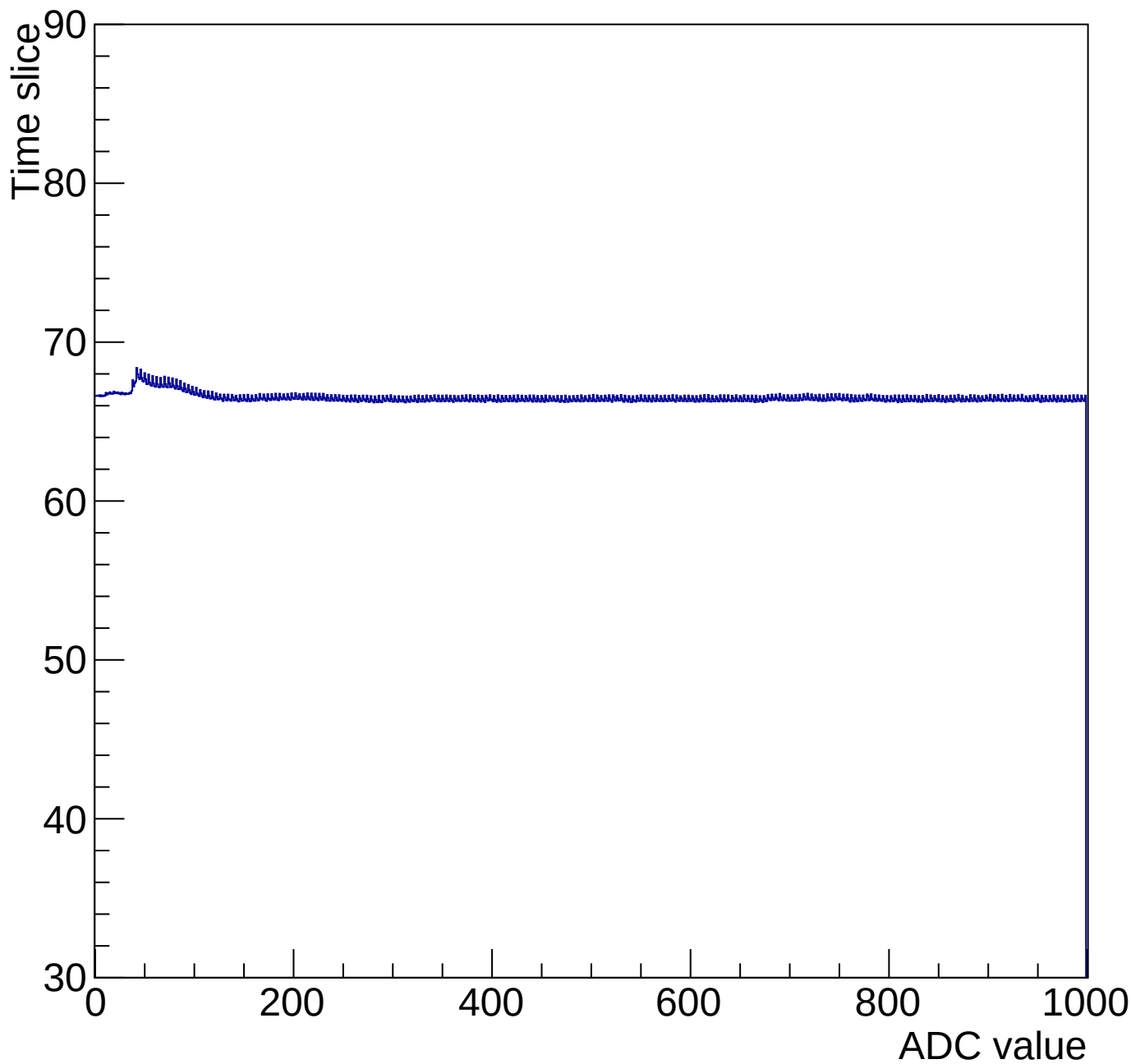
Time mcm 2000 chip 0 chan 5 1000-gain0-shaper0



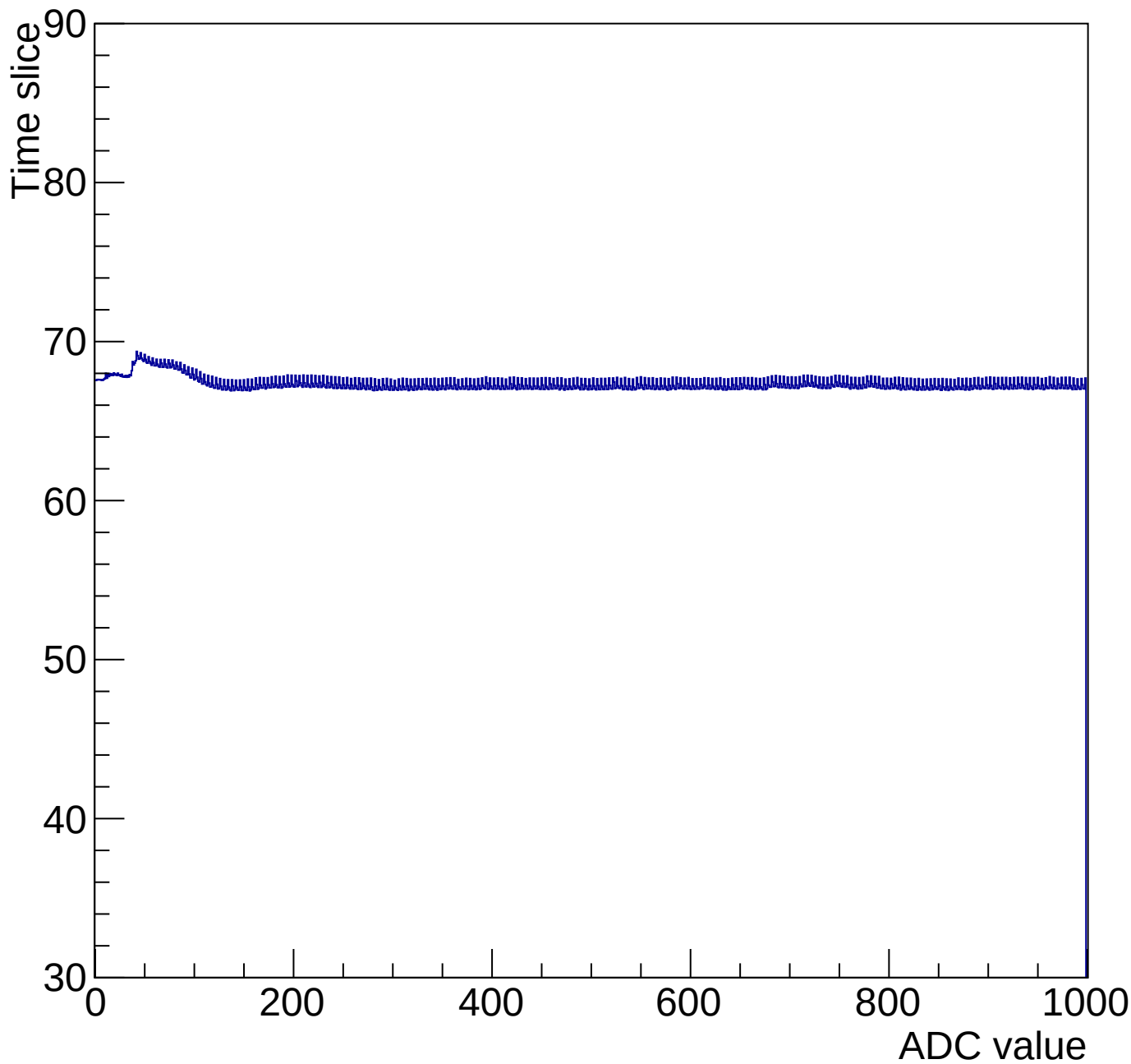
Time mcm 2000 chip 0 chan 6 1000-gain0-shaper0



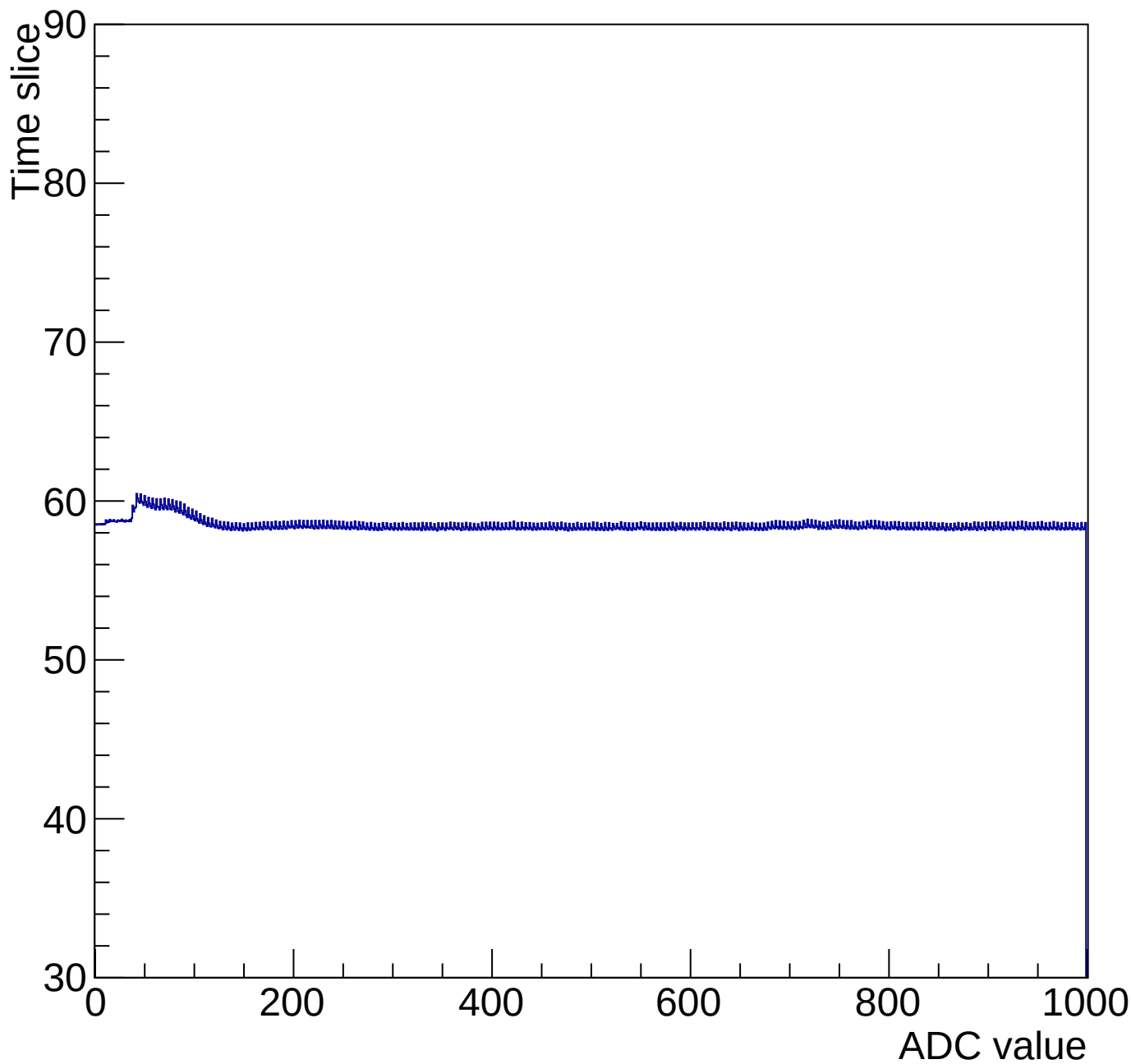
Time mcm 2000 chip 0 chan 7 1000-gain0-shaper0



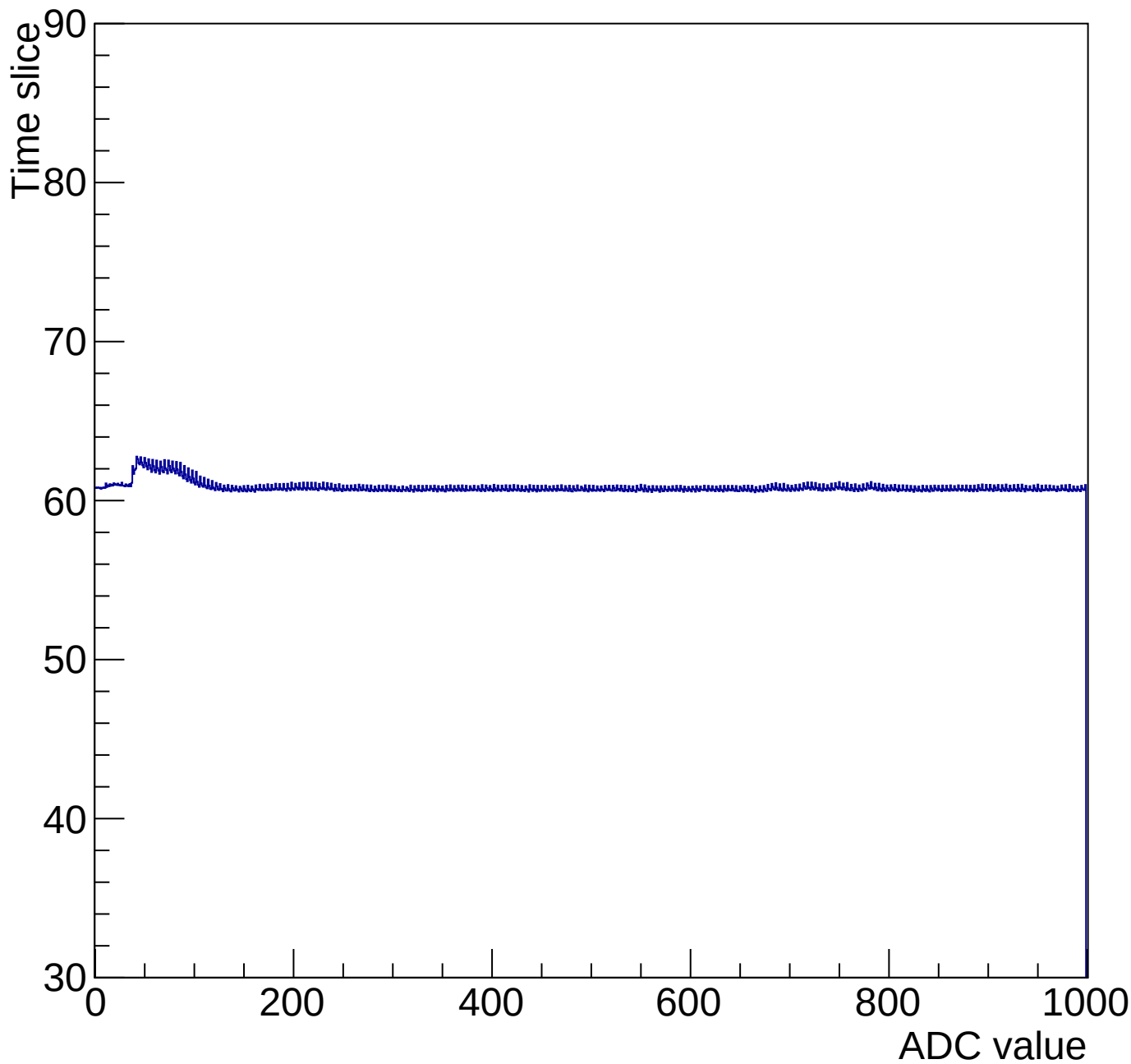
Time mcm 2000 chip 0 chan 8 1000-gain0-shaper0



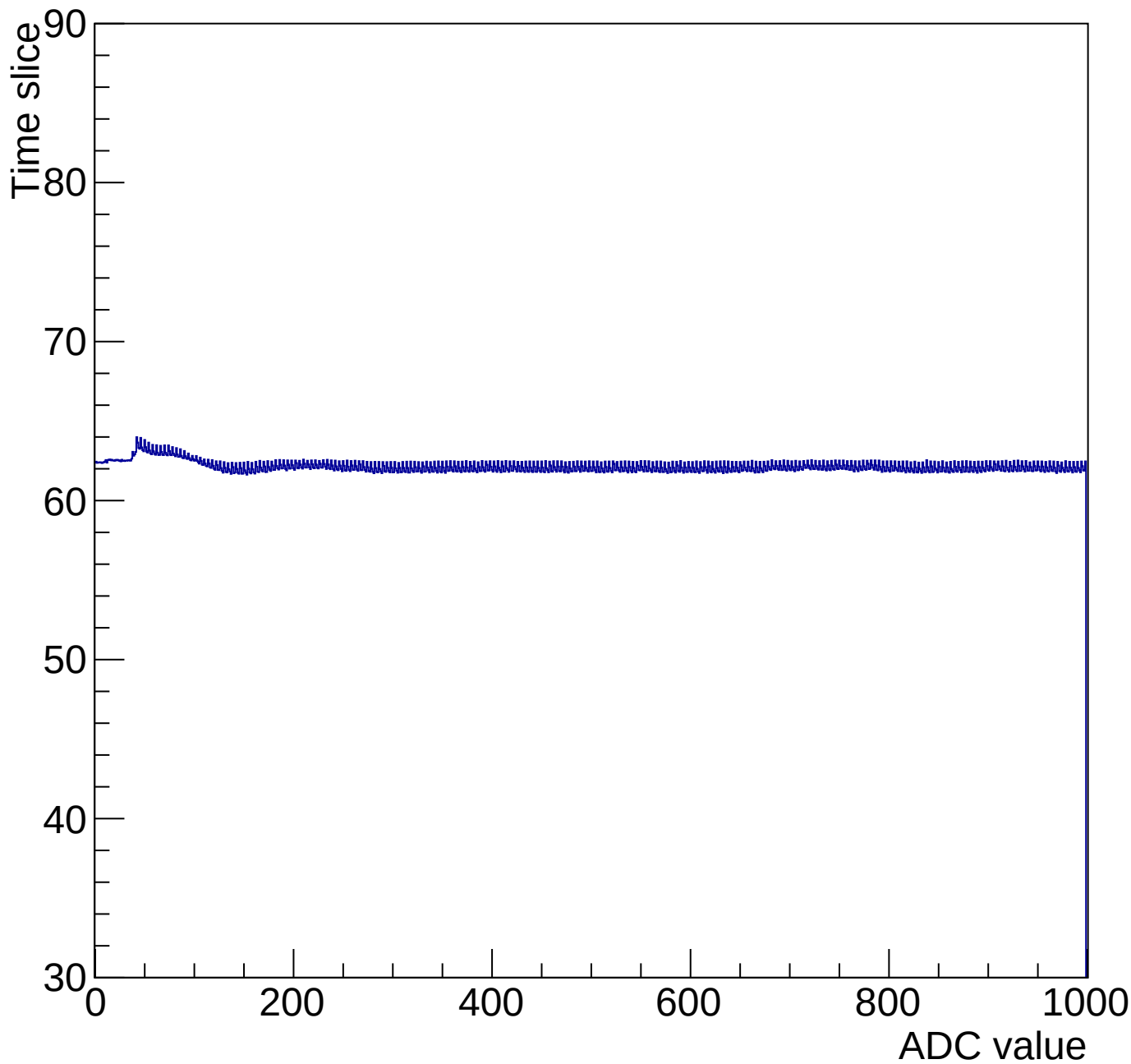
Time mcm 2000 chip 0 chan 9 1000-gain0-shaper0



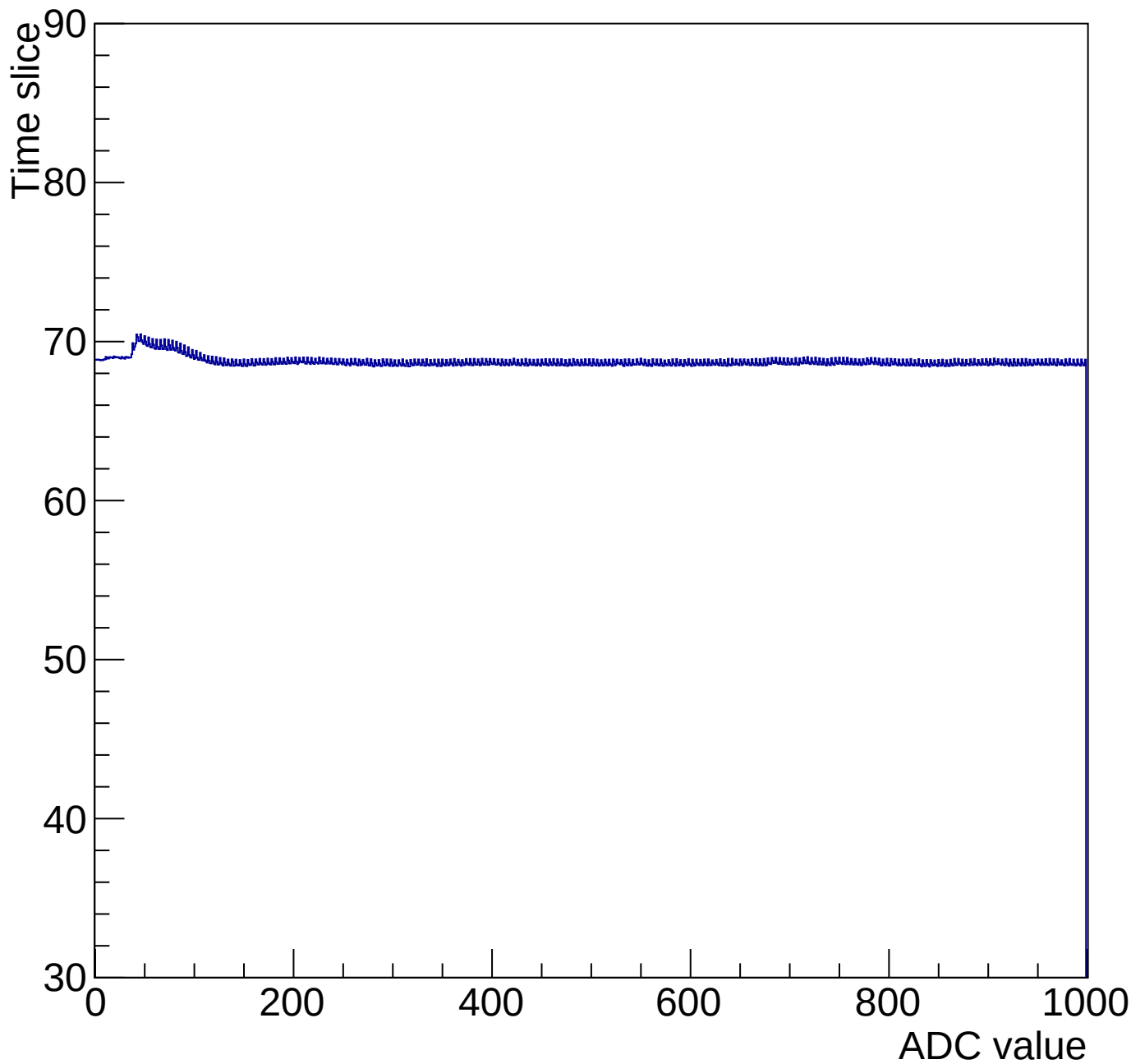
Time mcm 2000 chip 0 chan 10 1000-gain0-shaper0



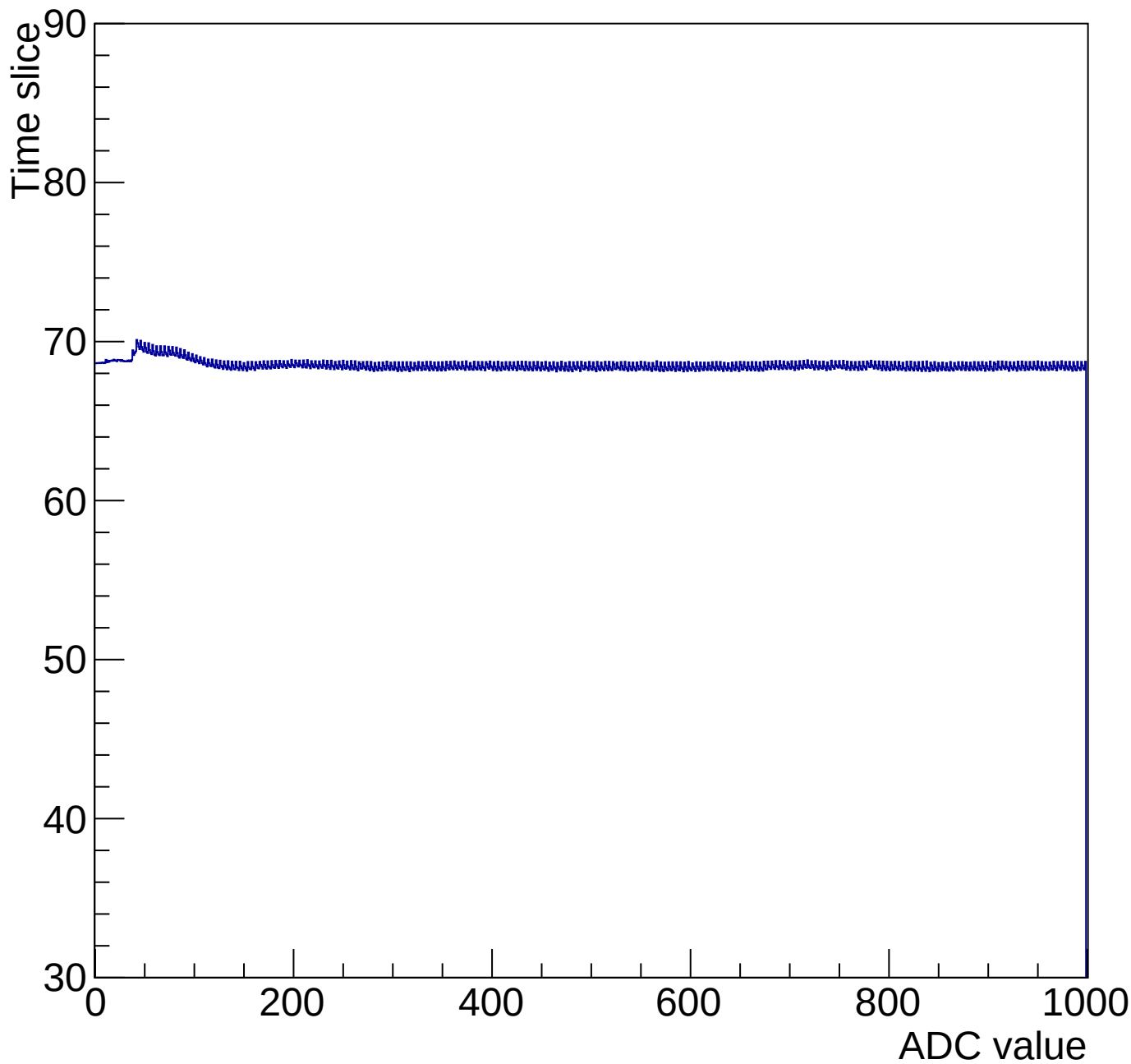
Time mcm 2000 chip 0 chan 11 1000-gain0-shaper0



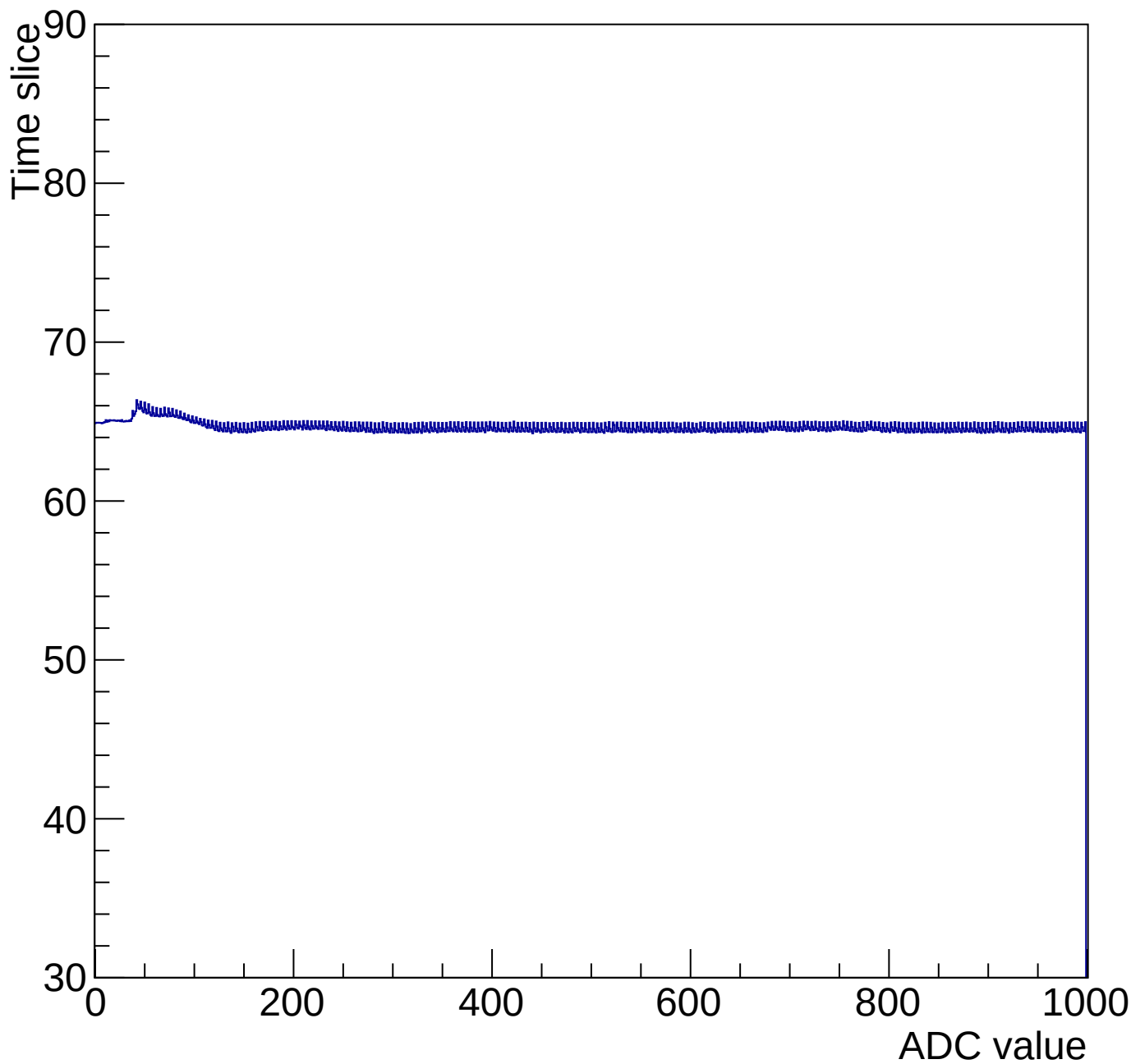
Time mcm 2000 chip 0 chan 12 1000-gain0-shaper0



Time mcm 2000 chip 0 chan 13 1000-gain0-shaper0



Time mcm 2000 chip 0 chan 14 1000-gain0-shaper0



Time mcm 2000 chip 0 chan 15 1000-gain0-shaper0

