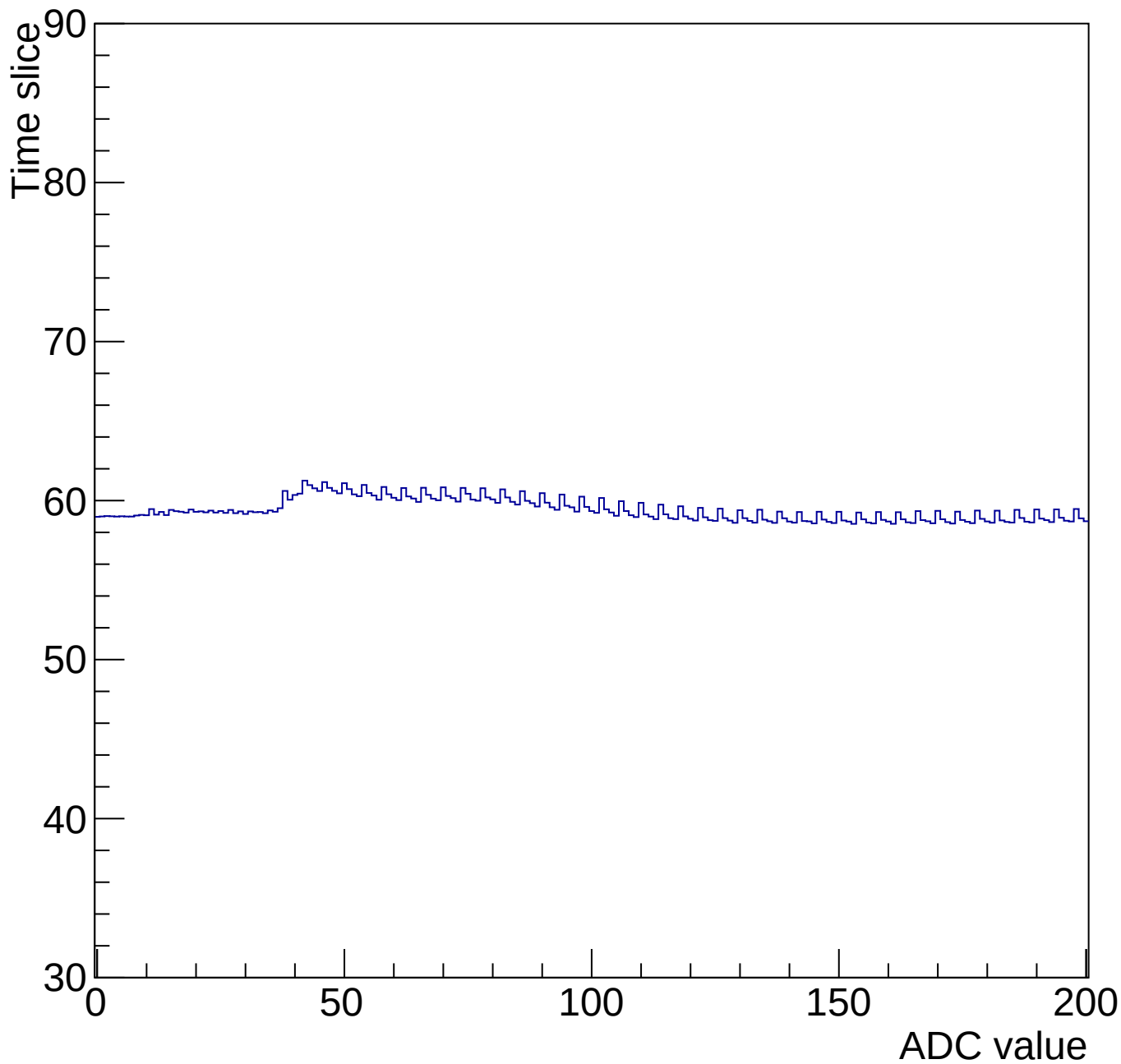
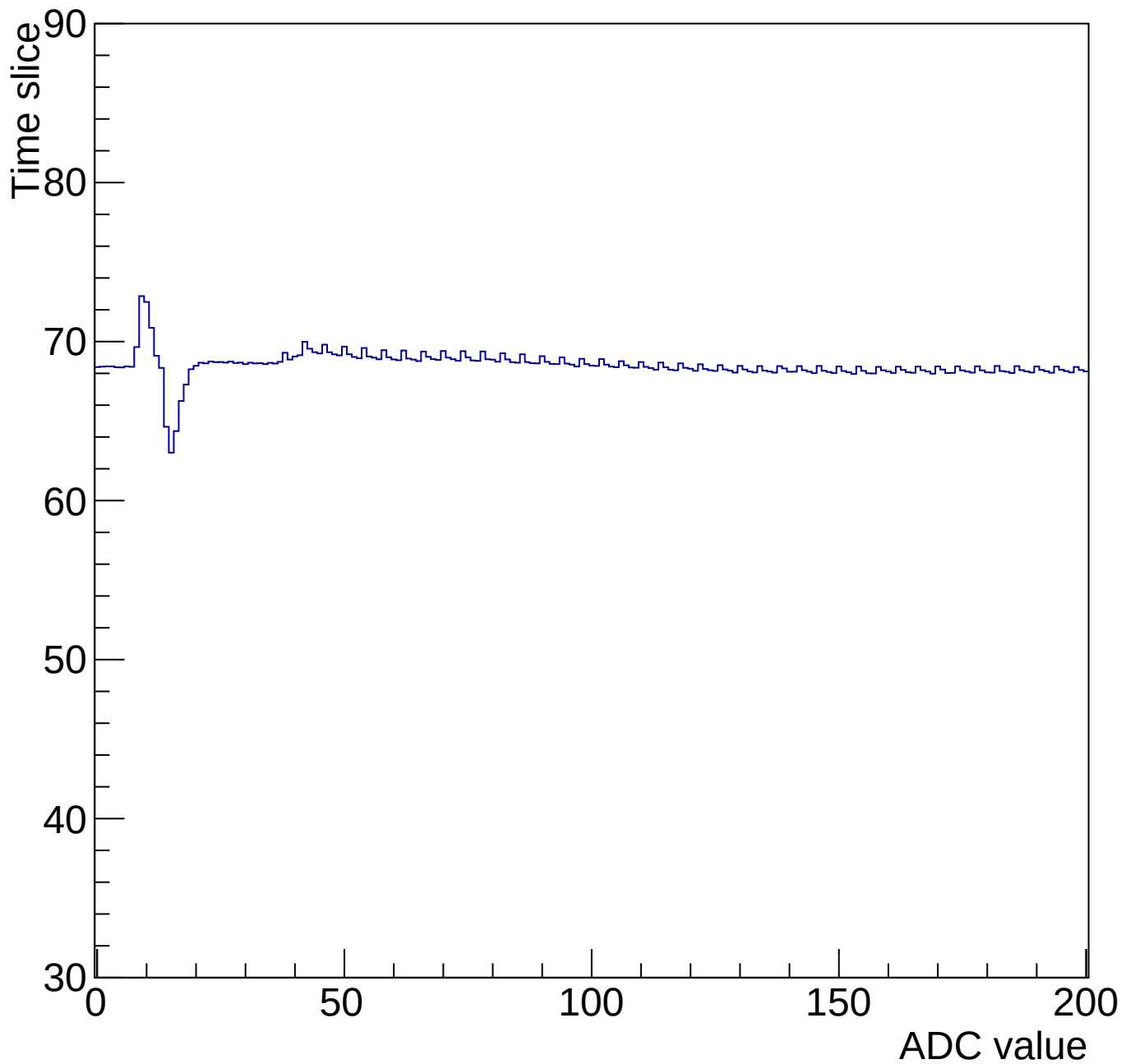


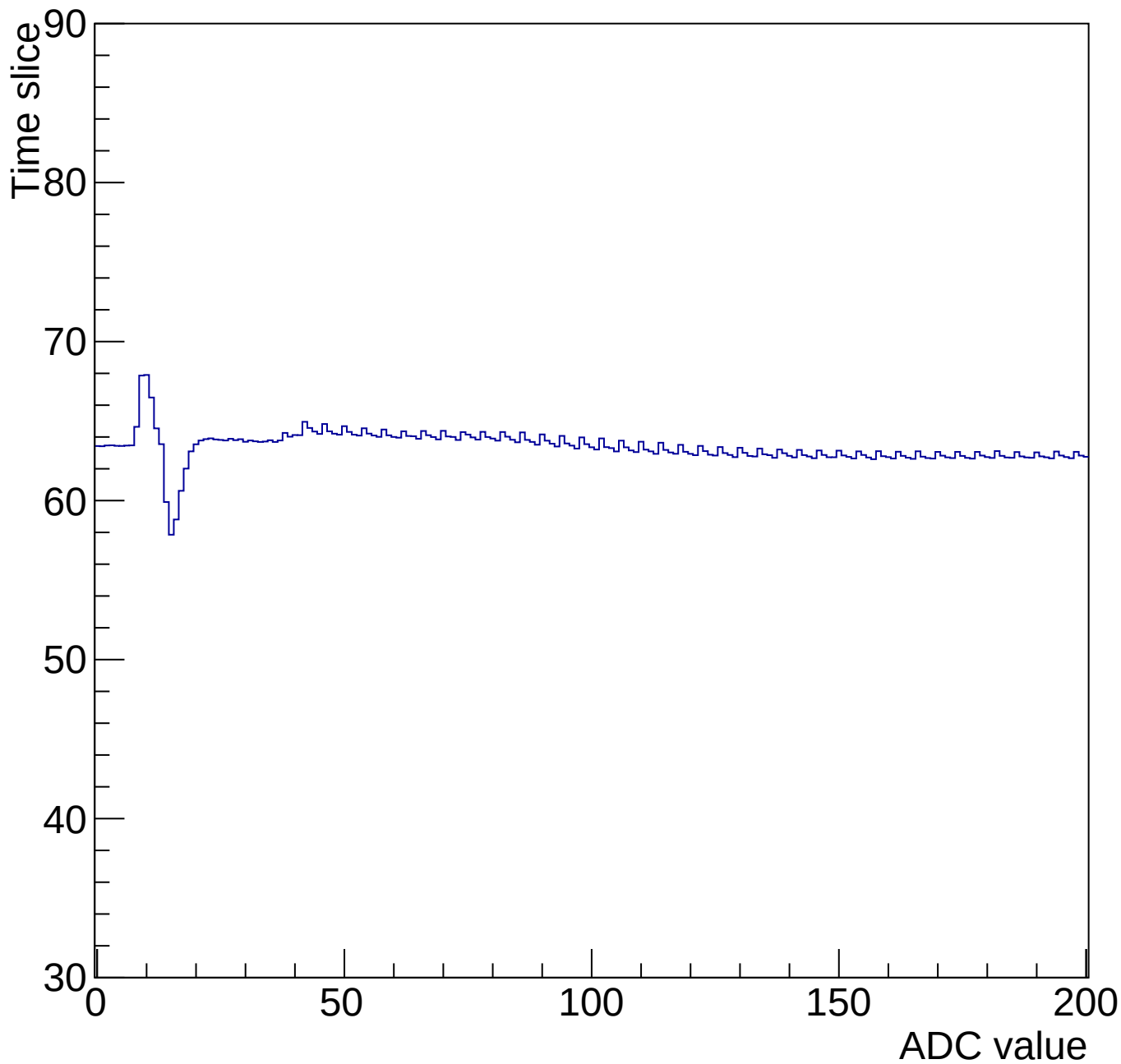
Time mcm 2000 chip 0 chan 0 200-gain0-shaper0



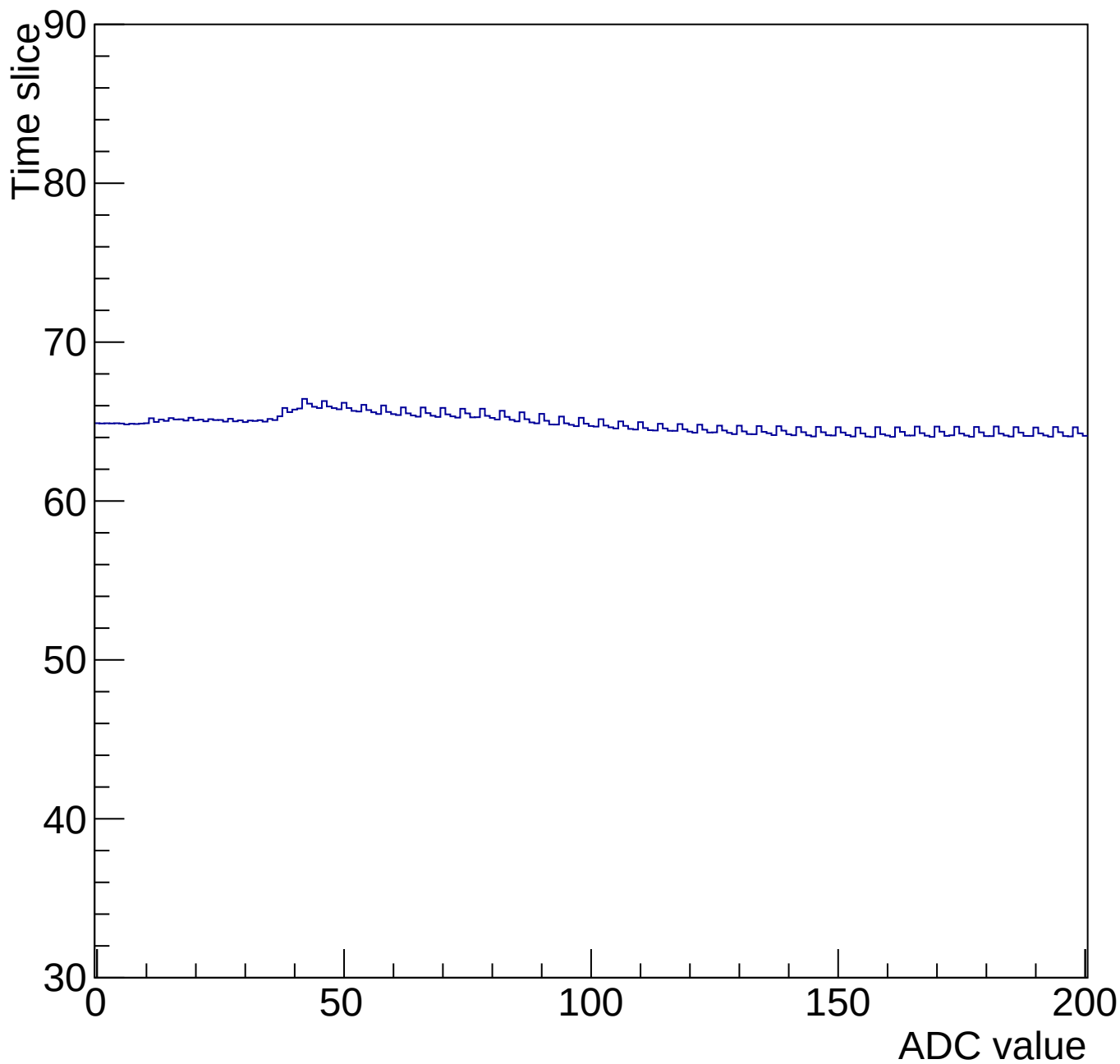
Time mcm 2000 chip 0 chan 1 200-gain0-shaper0



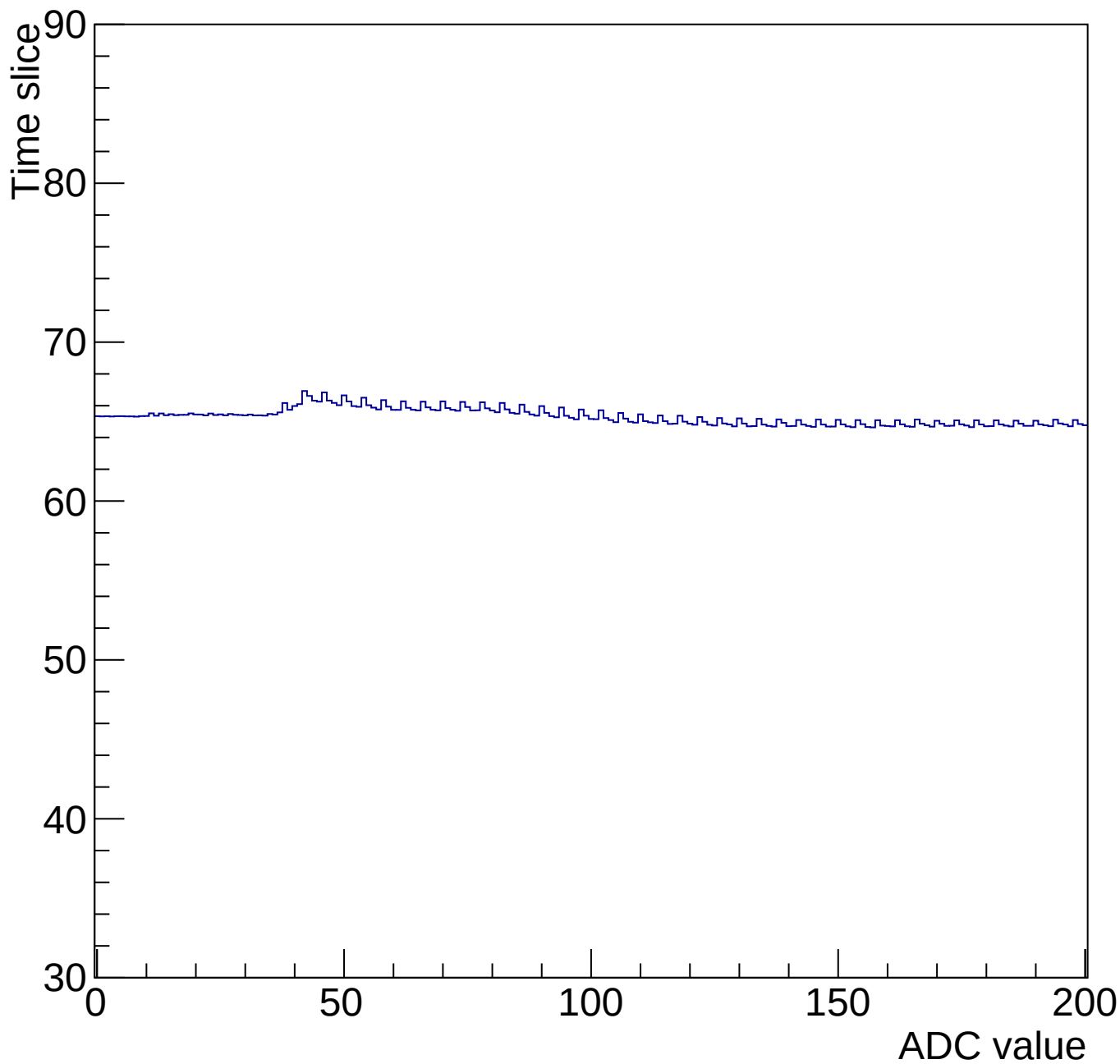
Time mcm 2000 chip 0 chan 2 200-gain0-shaper0



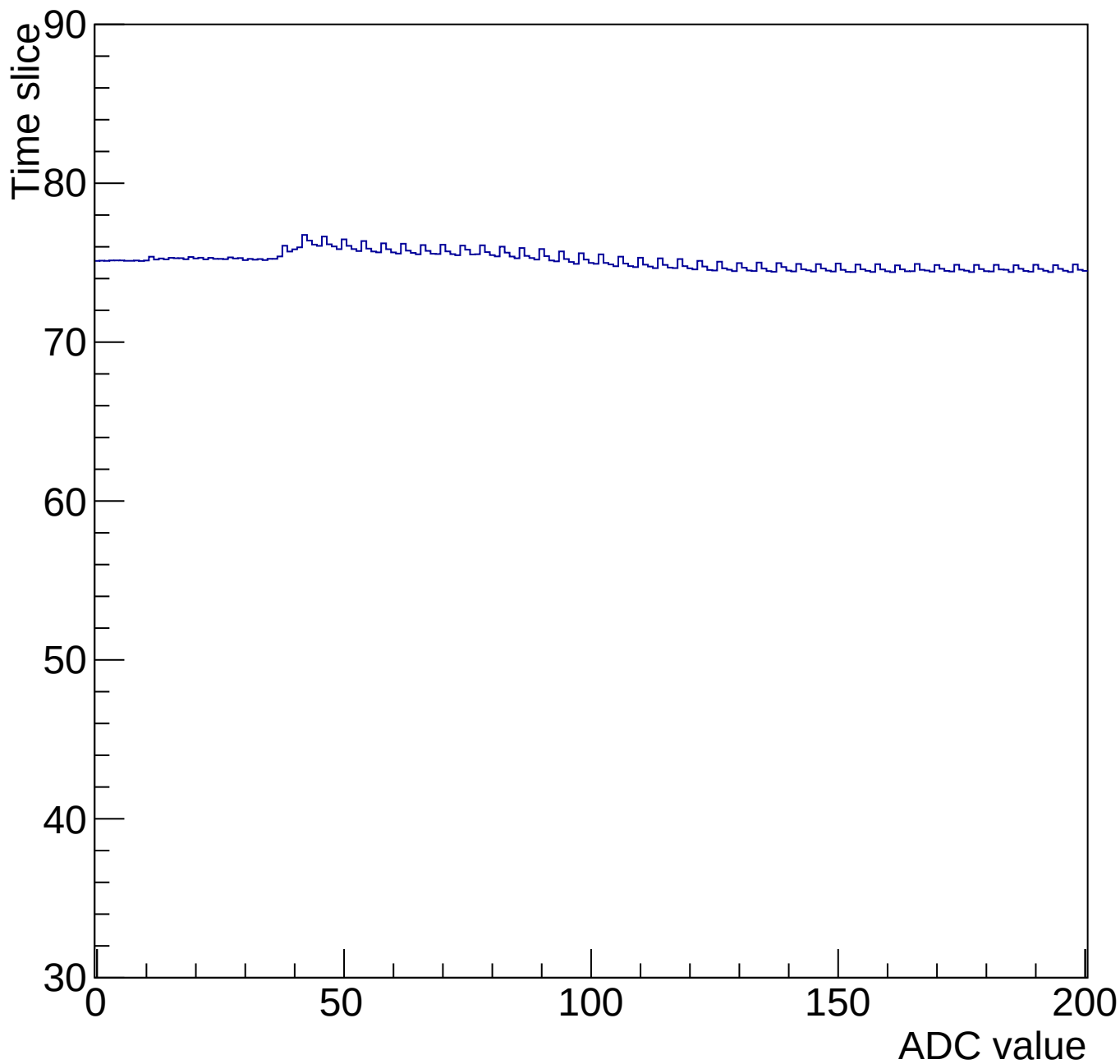
Time mcm 2000 chip 0 chan 3 200-gain0-shaper0



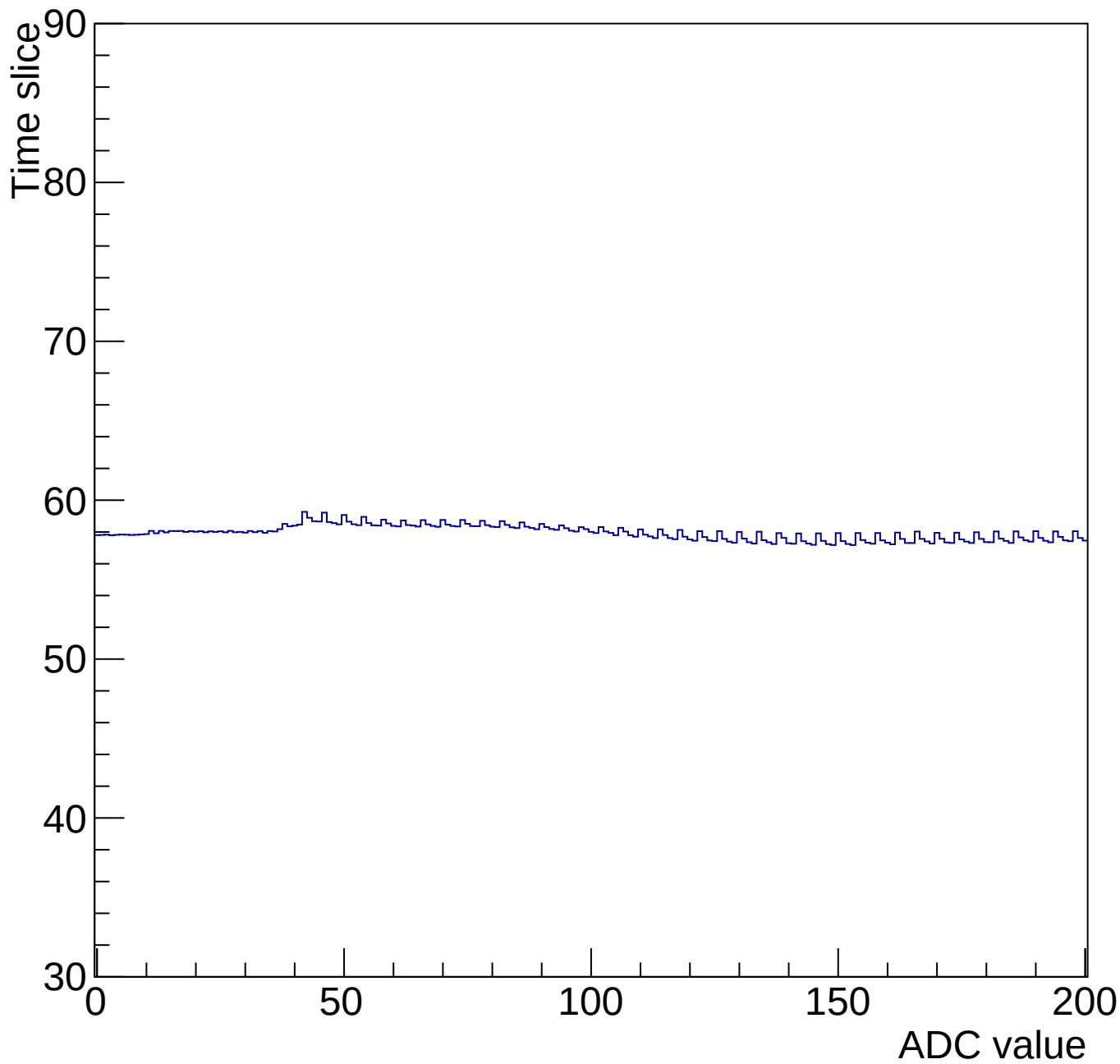
Time mcm 2000 chip 0 chan 4 200-gain0-shaper0



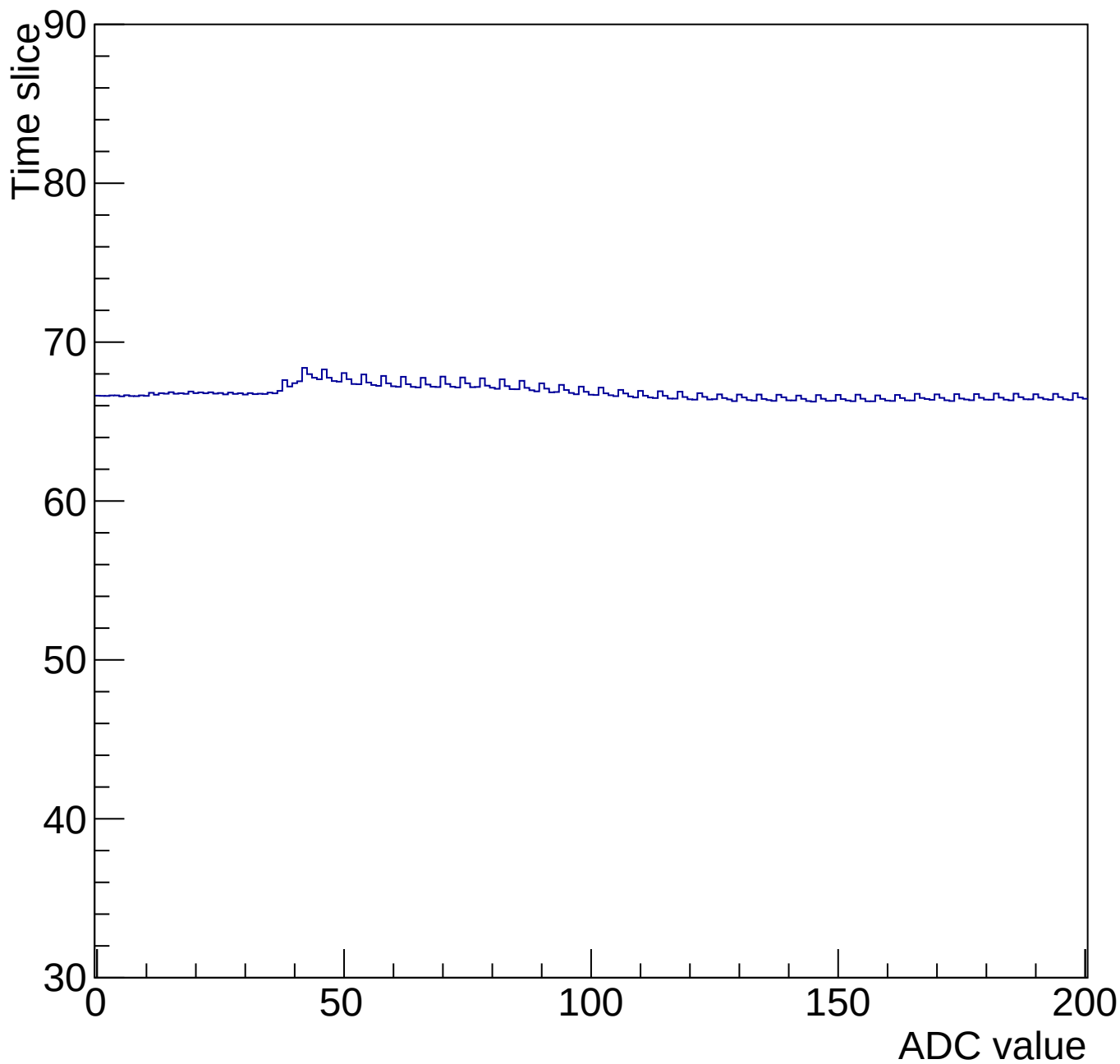
Time mcm 2000 chip 0 chan 5 200-gain0-shaper0



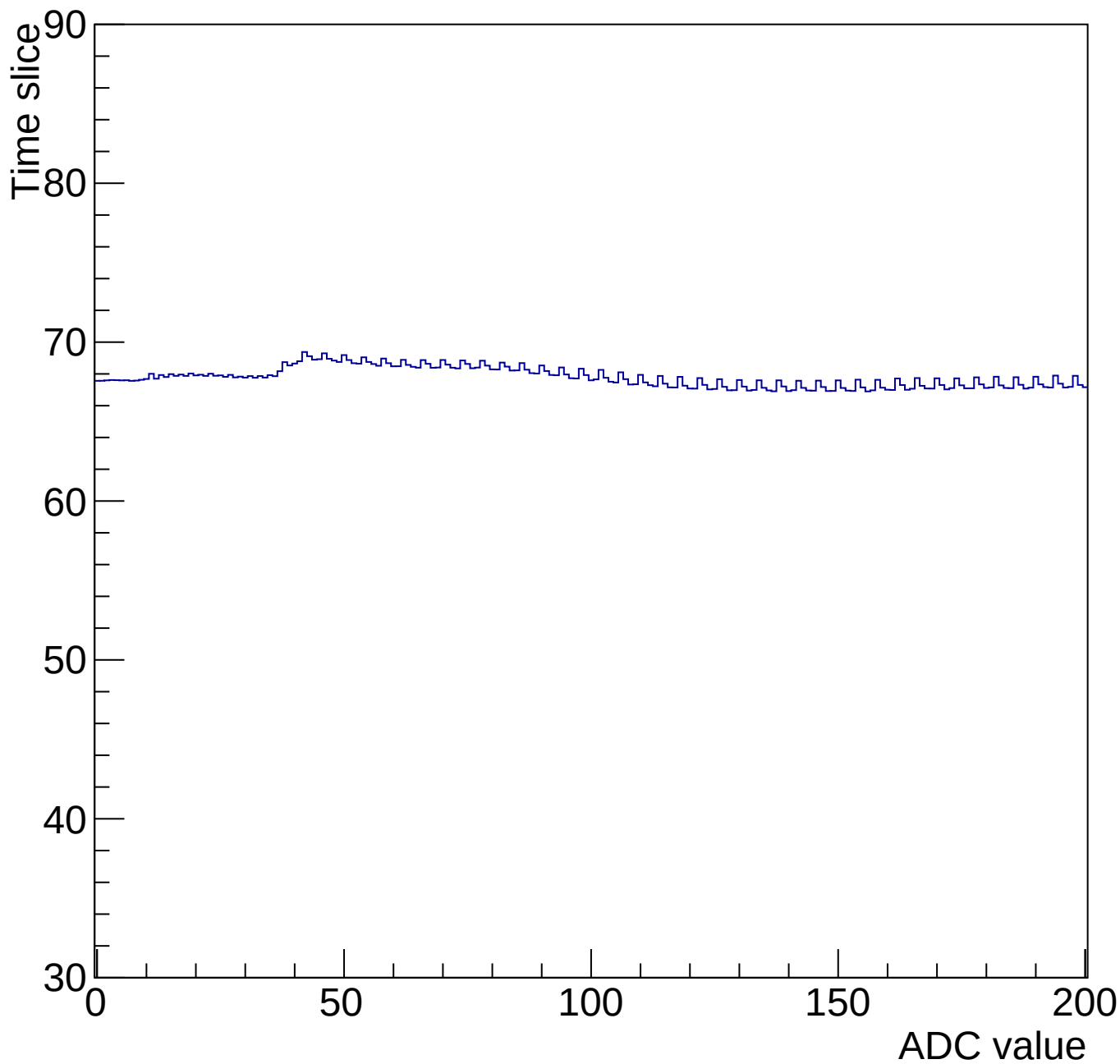
Time mcm 2000 chip 0 chan 6 200-gain0-shaper0



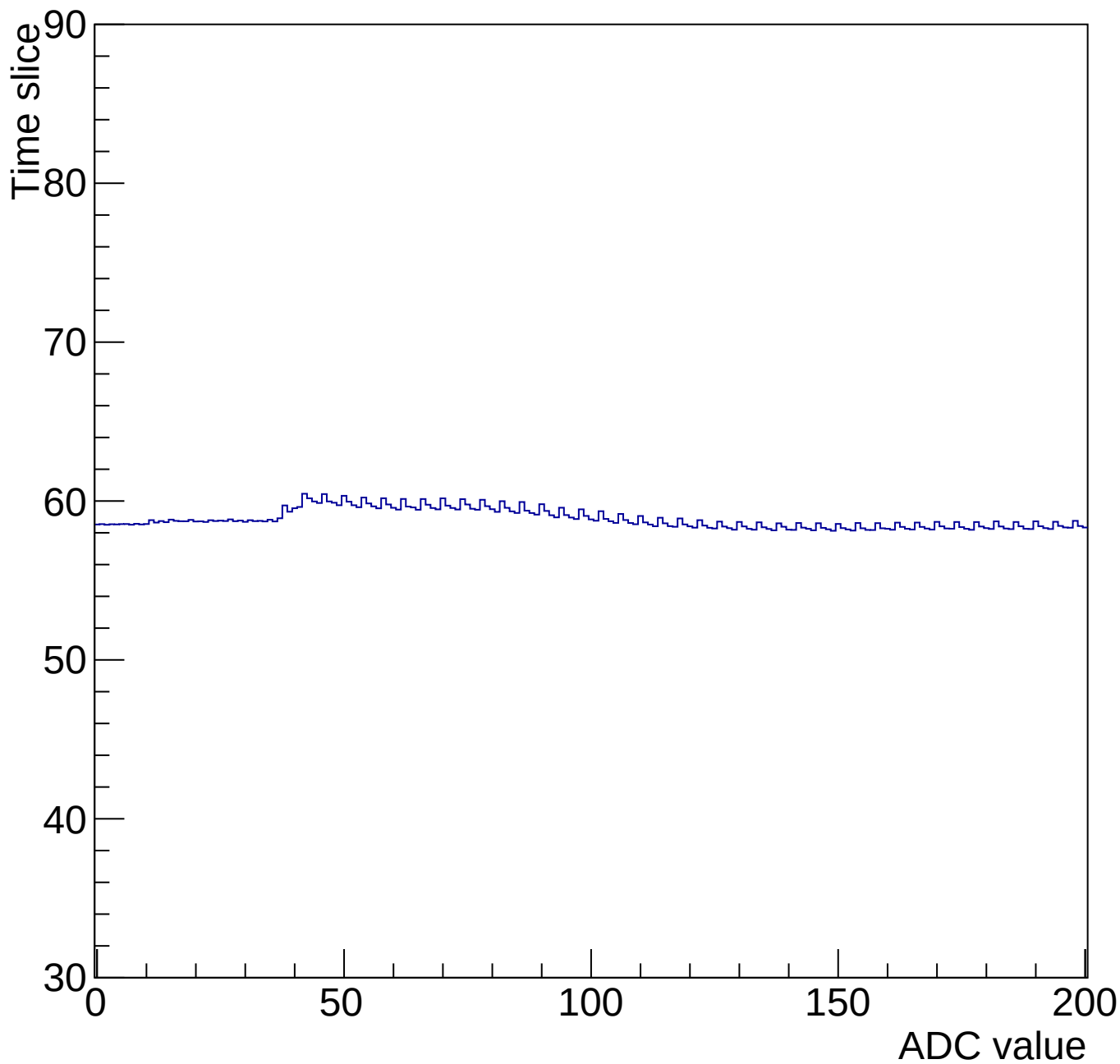
Time mcm 2000 chip 0 chan 7 200-gain0-shaper0



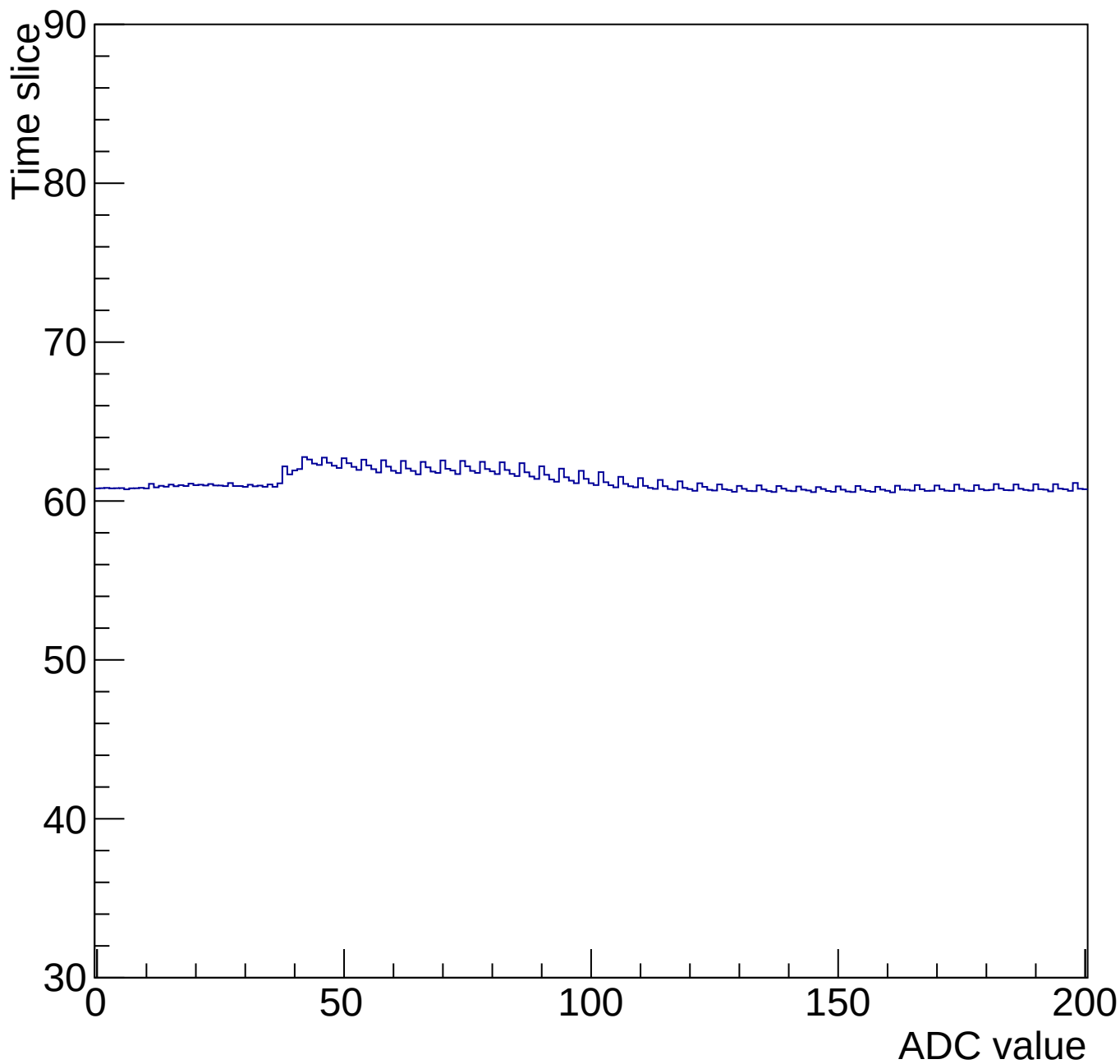
Time mcm 2000 chip 0 chan 8 200-gain0-shaper0



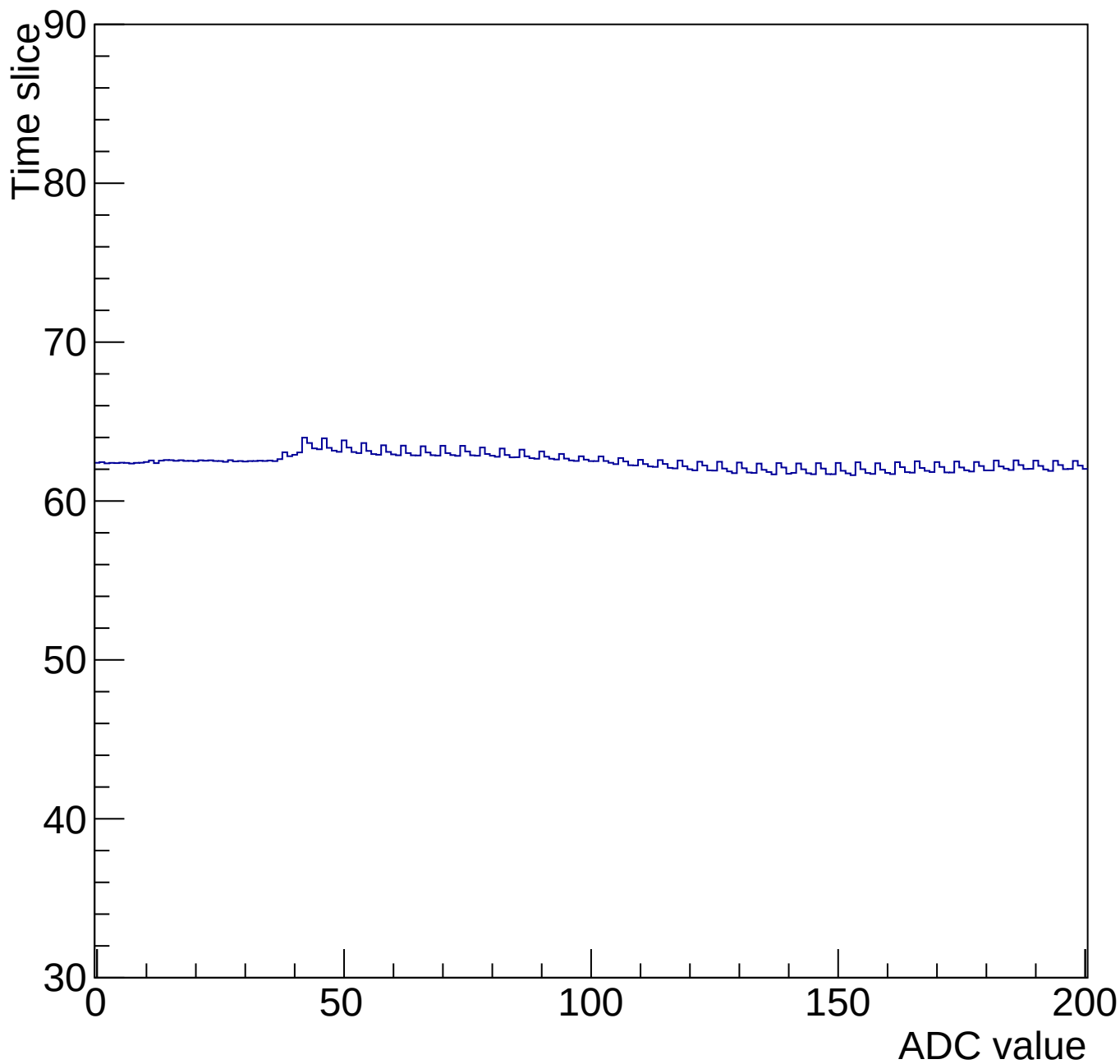
Time mcm 2000 chip 0 chan 9 200-gain0-shaper0



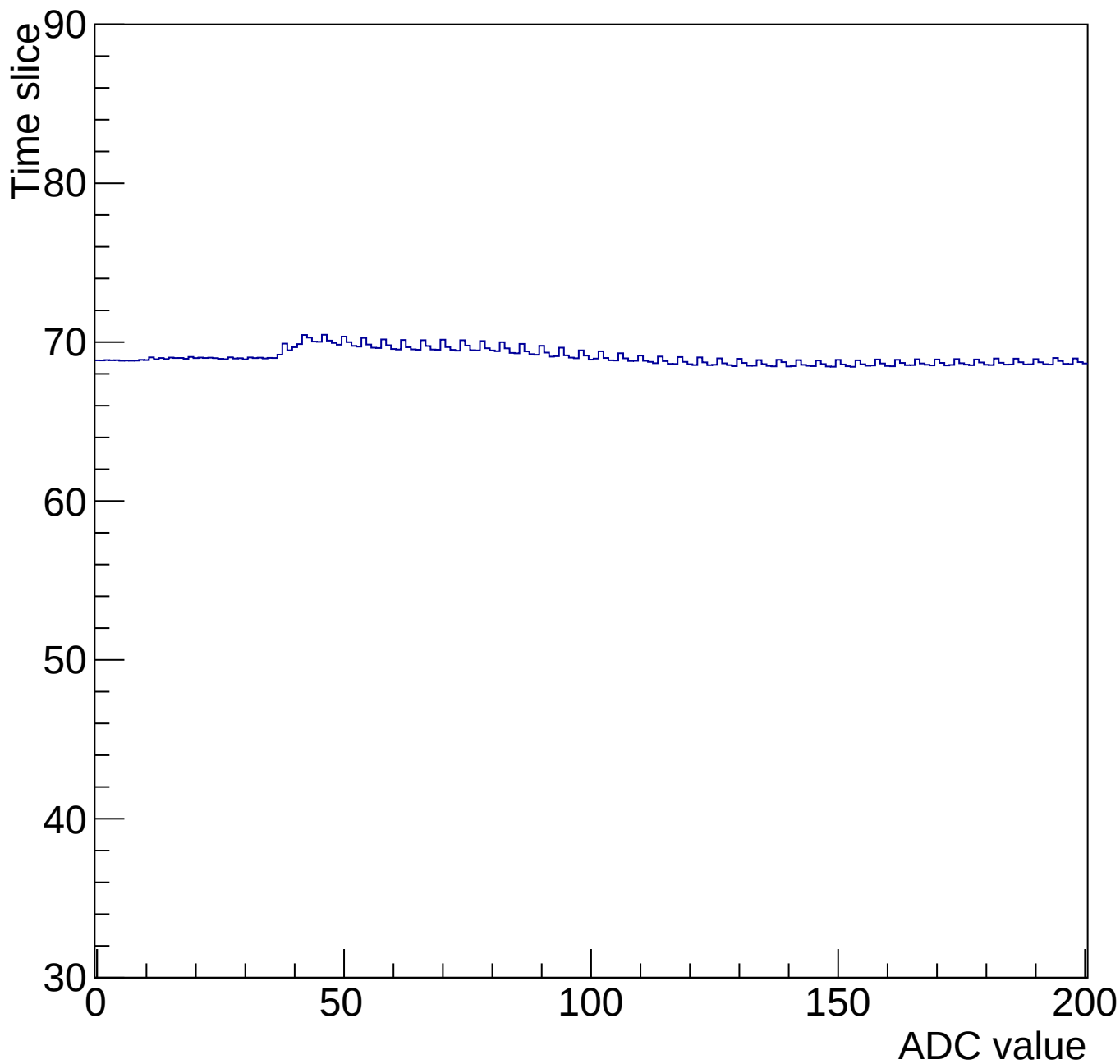
Time mcm 2000 chip 0 chan 10 200-gain0-shaper0



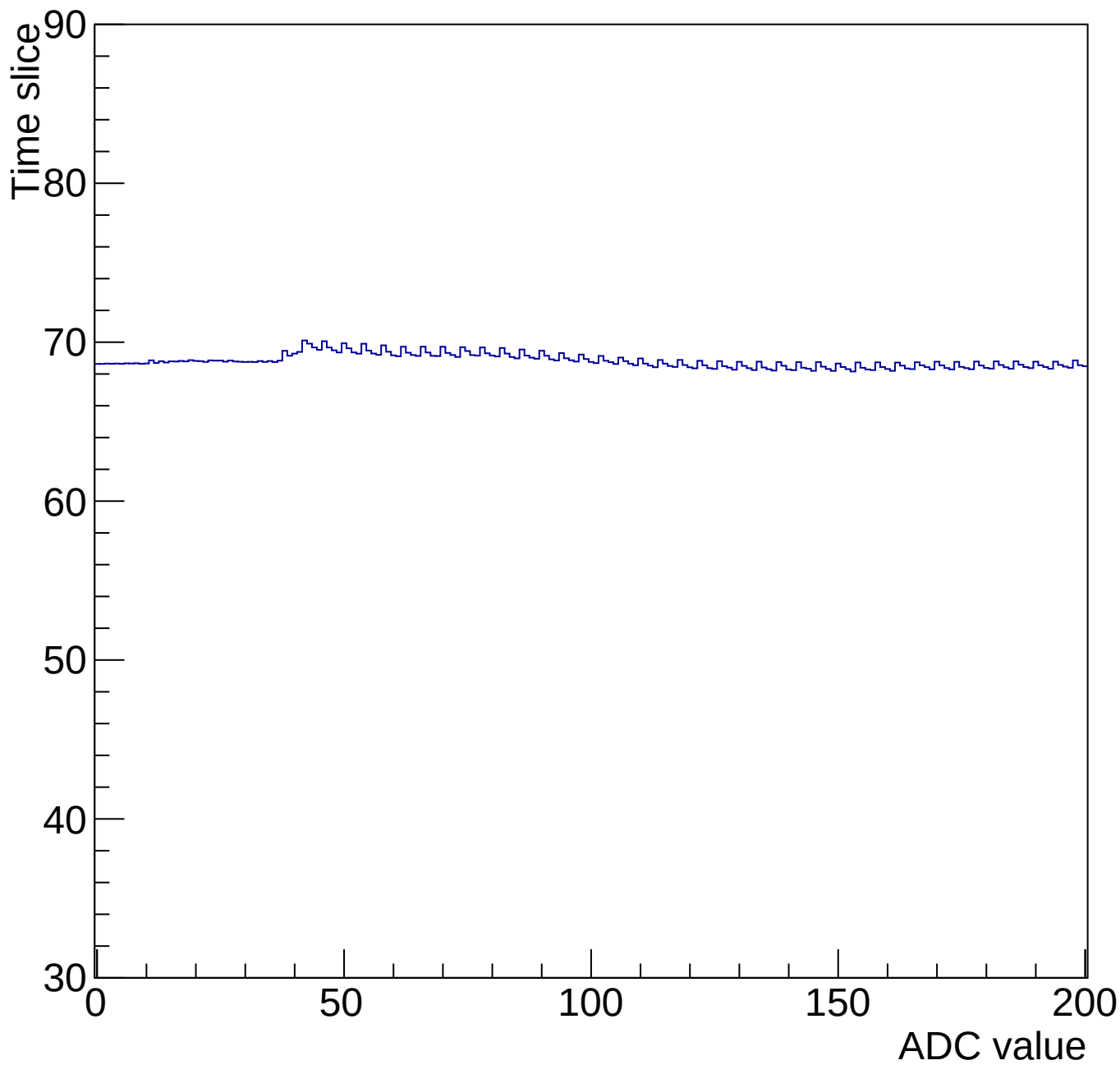
Time mcm 2000 chip 0 chan 11 200-gain0-shaper0



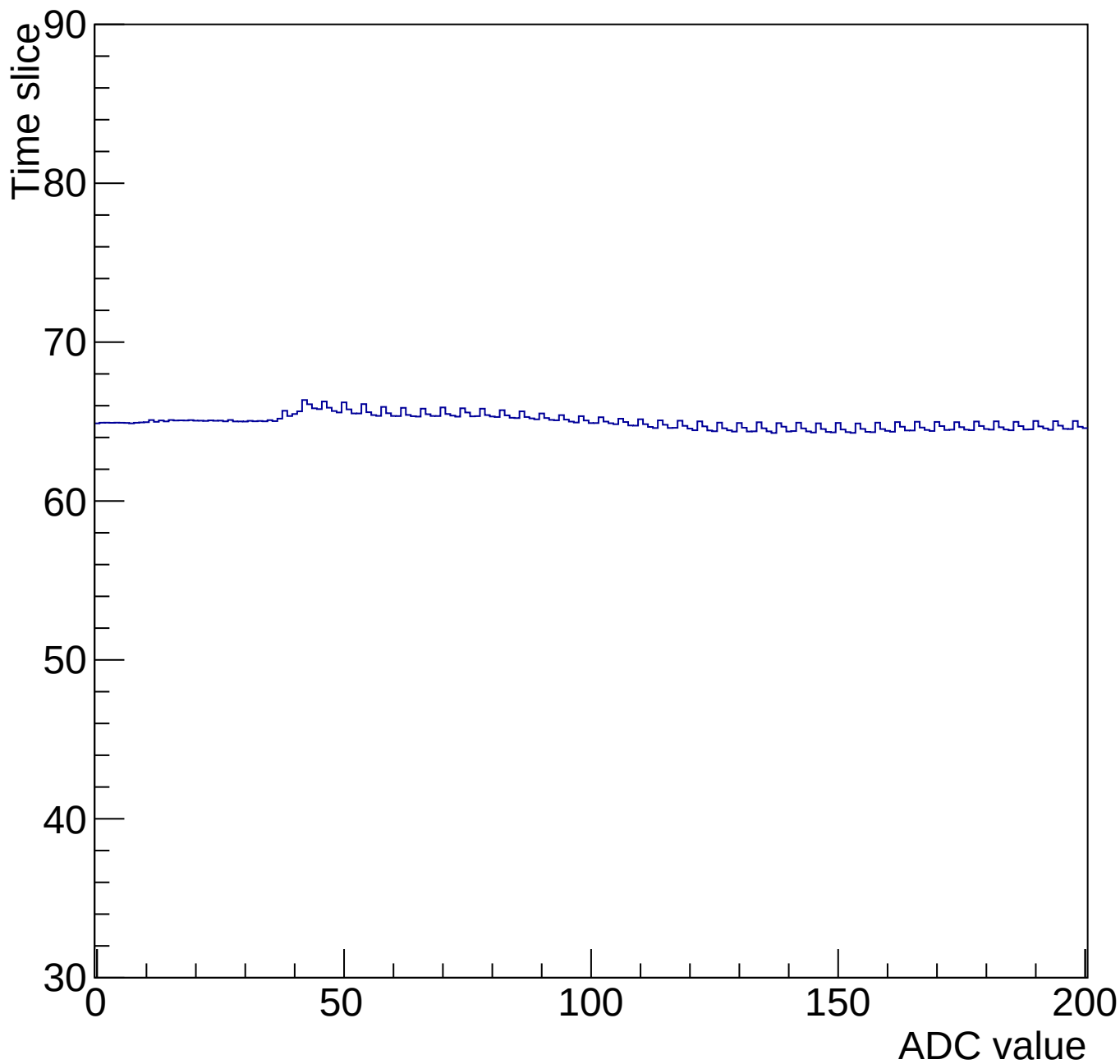
Time mcm 2000 chip 0 chan 12 200-gain0-shaper0



Time mcm 2000 chip 0 chan 13 200-gain0-shaper0



Time mcm 2000 chip 0 chan 14 200-gain0-shaper0



Time mcm 2000 chip 0 chan 15 200-gain0-shaper0

