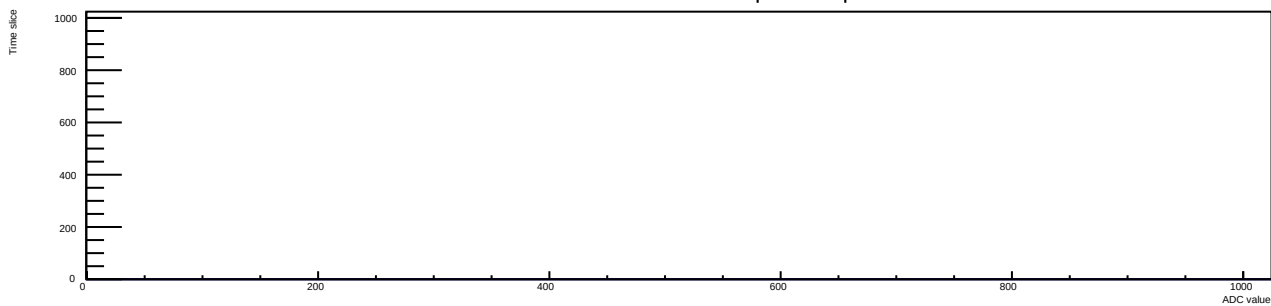
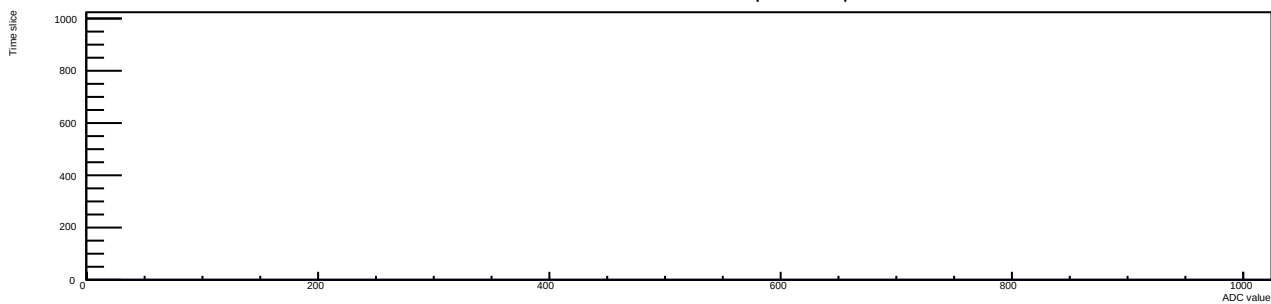


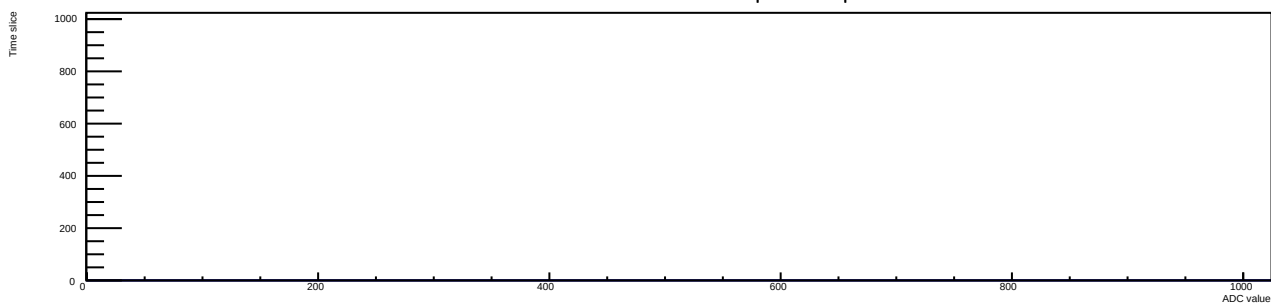
Run 36523 Evt 1000 Time mcm 2 chip 0 chan 0 pulses



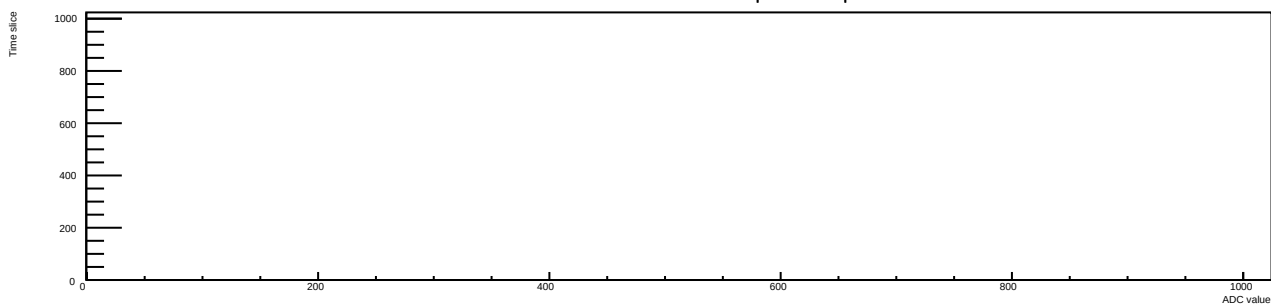
Run 36523 Evt 1000 Time mcm 2 chip 0 chan 1 pulses



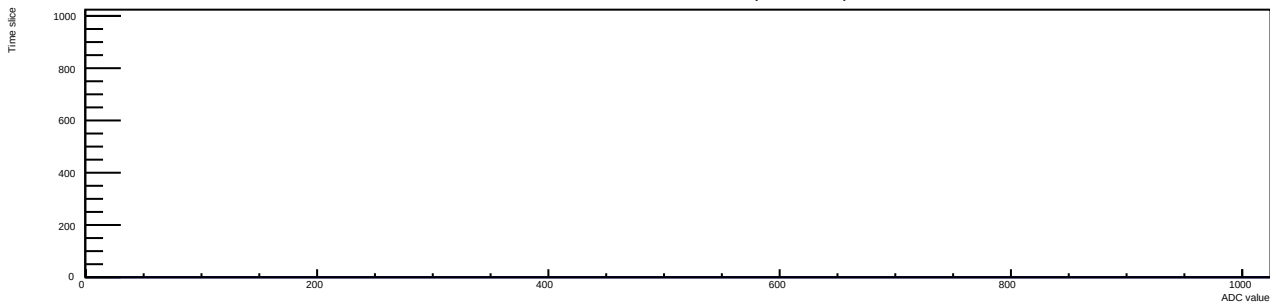
Run 36523 Evt 1000 Time mcm 2 chip 0 chan 2 pulses



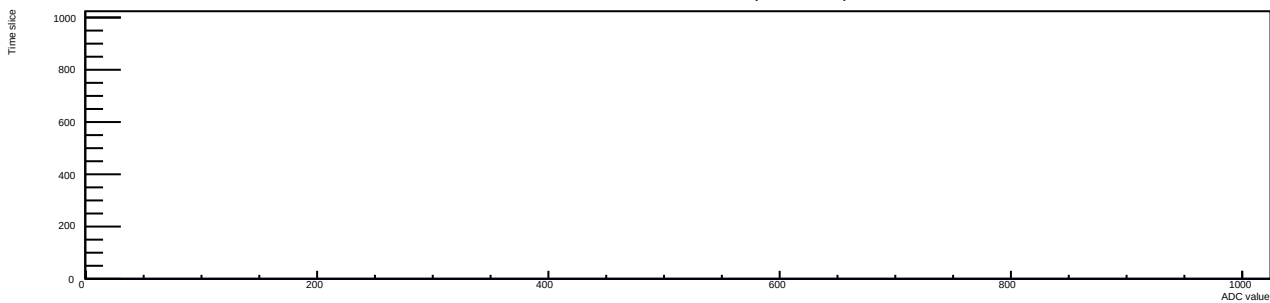
Run 36523 Evt 1000 Time mcm 2 chip 0 chan 3 pulses



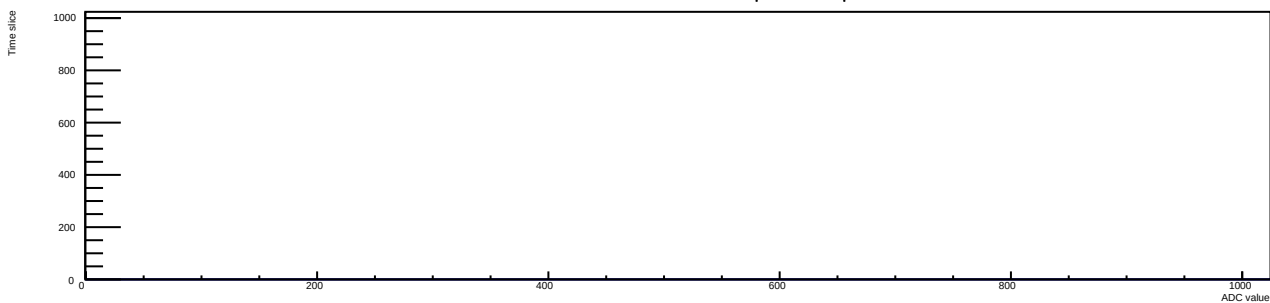
Run 36523 Evt 1000 Time mcm 2 chip 0 chan 4 pulses



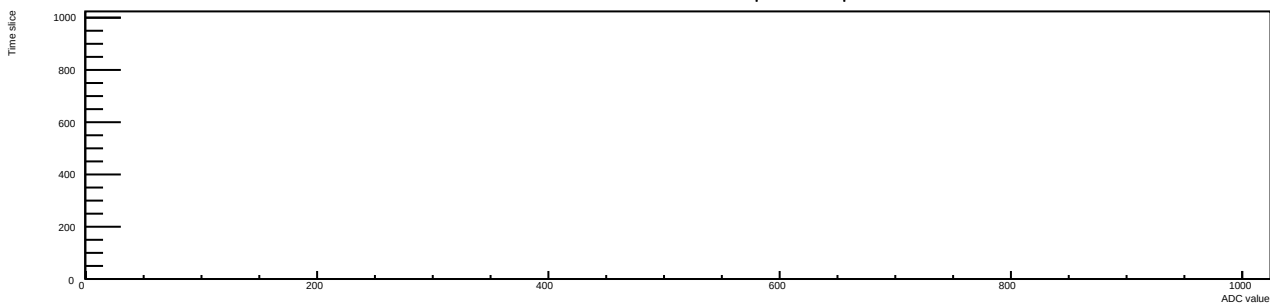
Run 36523 Evt 1000 Time mcm 2 chip 0 chan 5 pulses



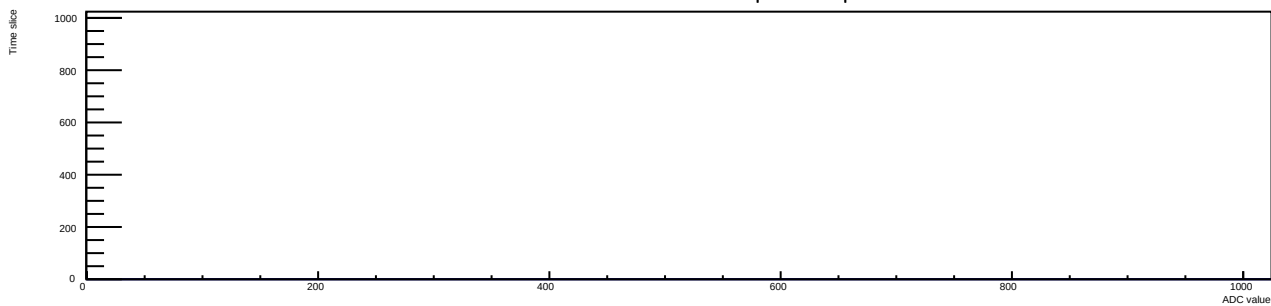
Run 36523 Evt 1000 Time mcm 2 chip 0 chan 6 pulses



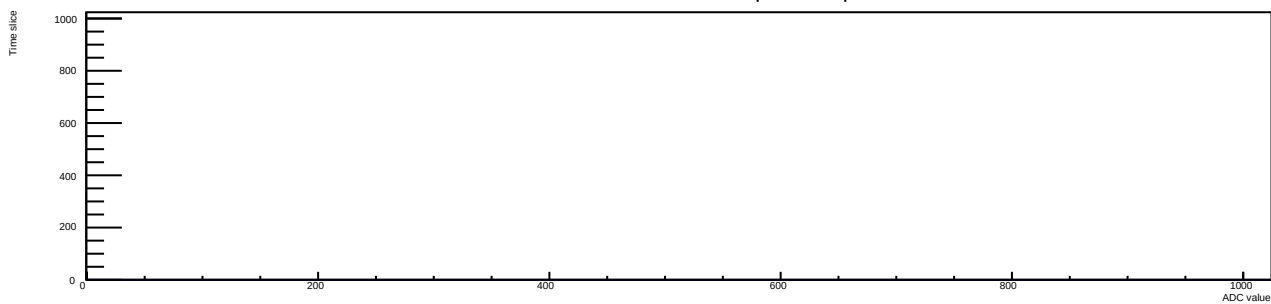
Run 36523 Evt 1000 Time mcm 2 chip 0 chan 7 pulses



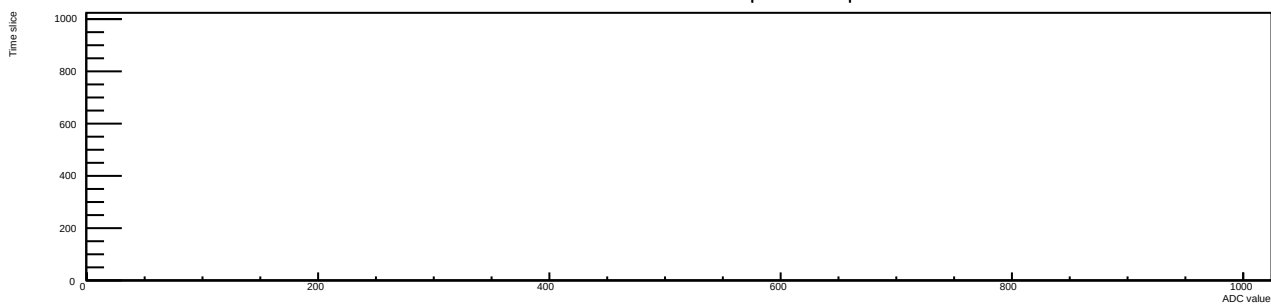
Run 36523 Evt 1000 Time mcm 2 chip 0 chan 8 pulses



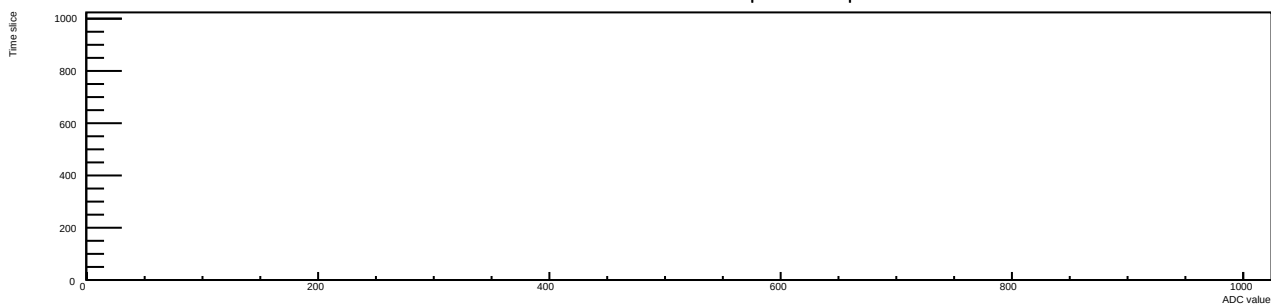
Run 36523 Evt 1000 Time mcm 2 chip 0 chan 9 pulses



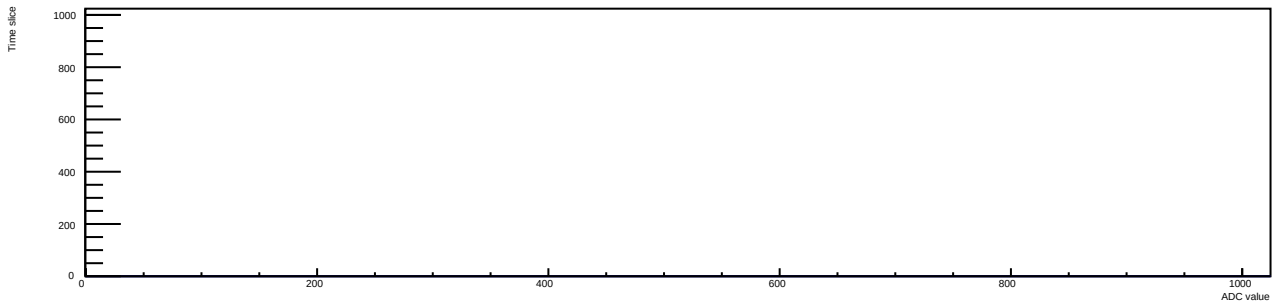
Run 36523 Evt 1000 Time mcm 2 chip 0 chan 10 pulses



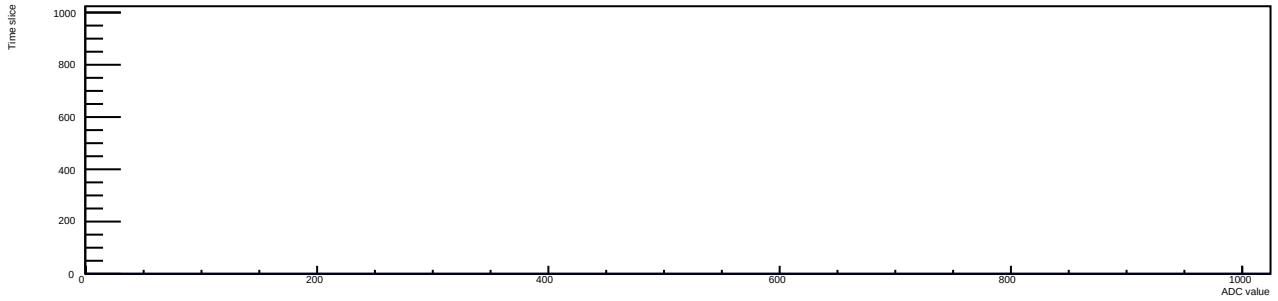
Run 36523 Evt 1000 Time mcm 2 chip 0 chan 11 pulses



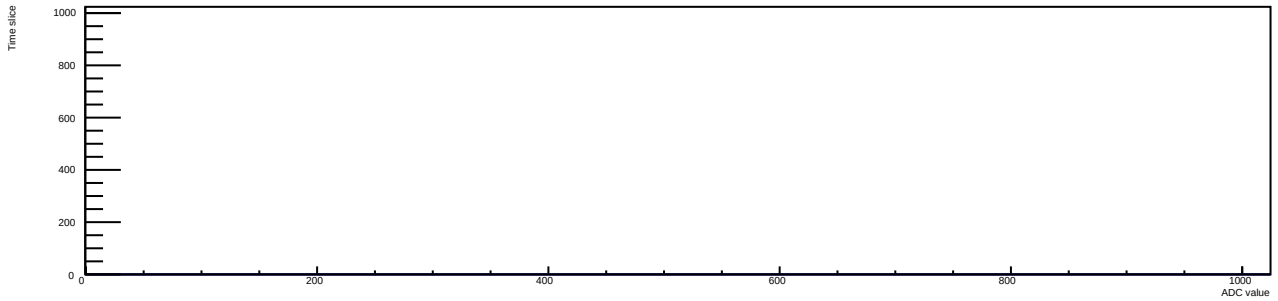
Run 36523 Evt 1000 Time mcm 2 chip 0 chan 12 pulses



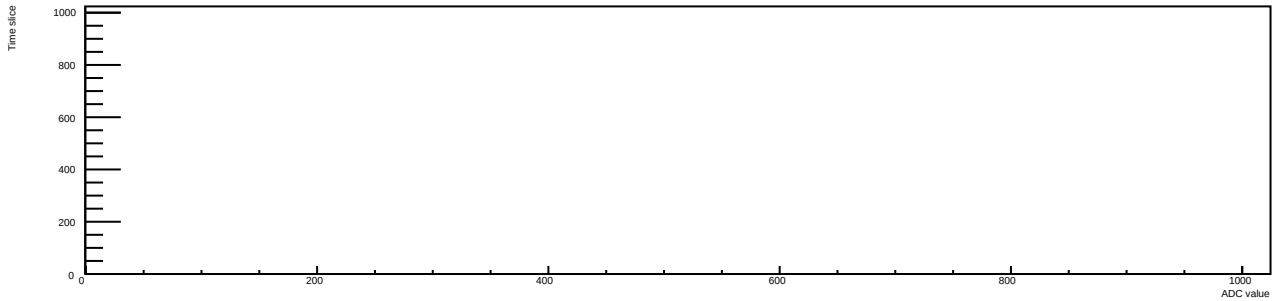
Run 36523 Evt 1000 Time mcm 2 chip 0 chan 13 pulses



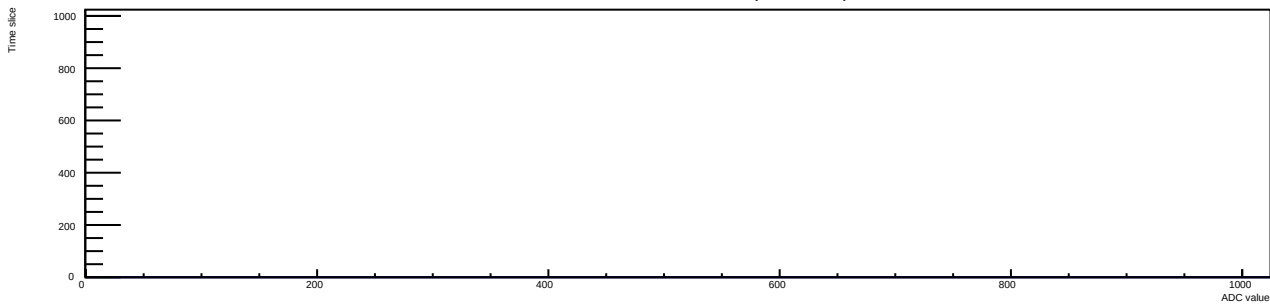
Run 36523 Evt 1000 Time mcm 2 chip 0 chan 14 pulses



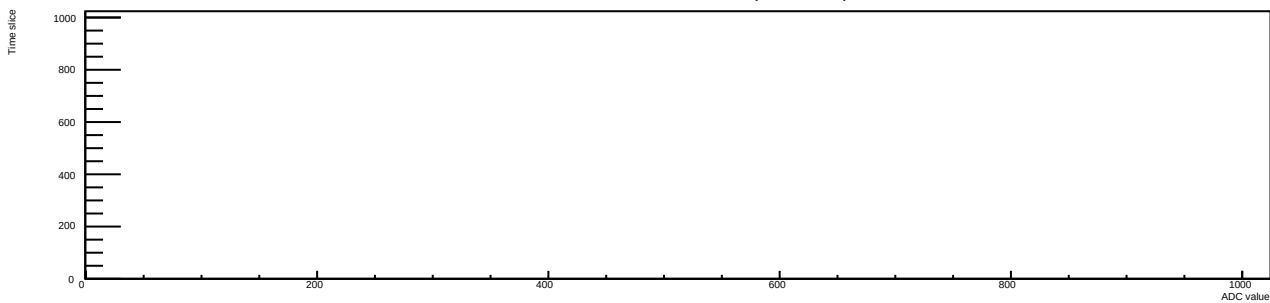
Run 36523 Evt 1000 Time mcm 2 chip 0 chan 15 pulses



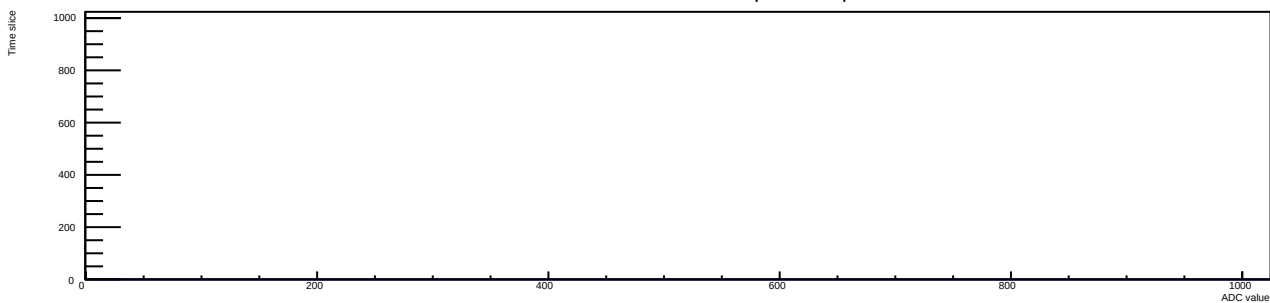
Run 36523 Evt 1000 Time mcm 2 chip 1 chan 0 pulses



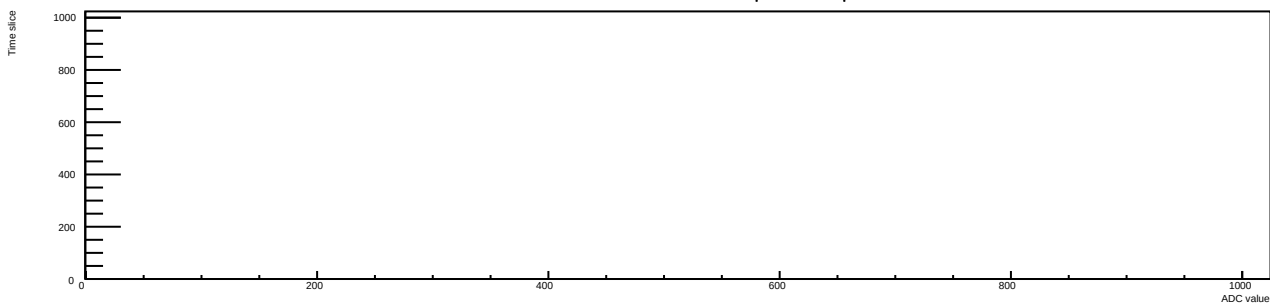
Run 36523 Evt 1000 Time mcm 2 chip 1 chan 1 pulses



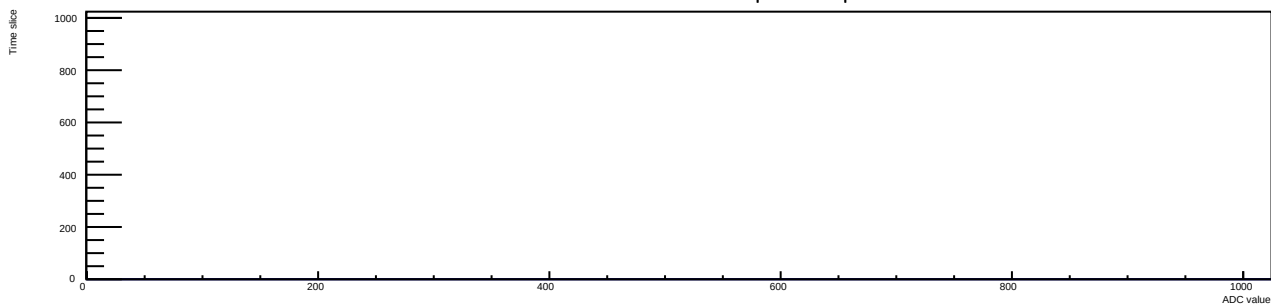
Run 36523 Evt 1000 Time mcm 2 chip 1 chan 2 pulses



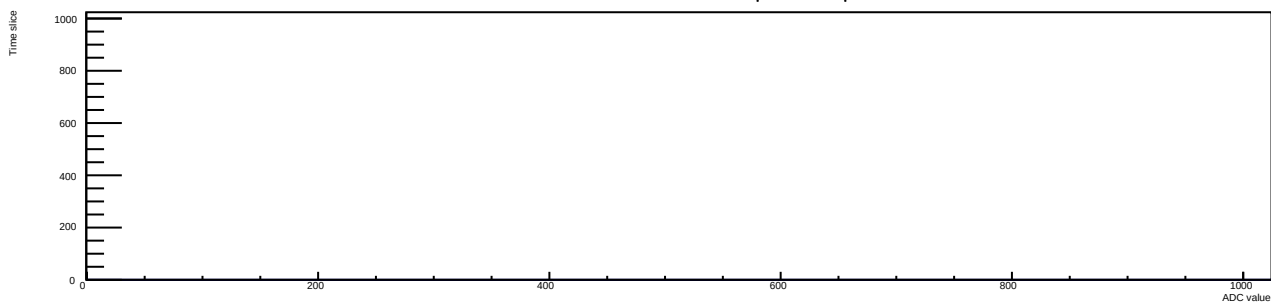
Run 36523 Evt 1000 Time mcm 2 chip 1 chan 3 pulses



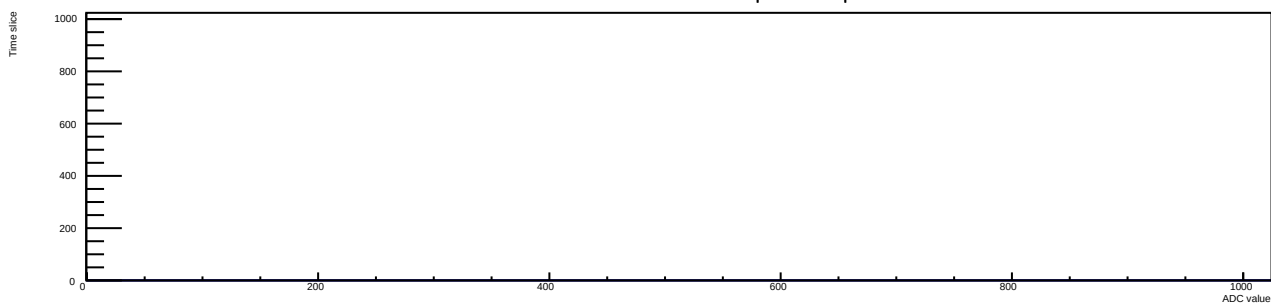
Run 36523 Evt 1000 Time mcm 2 chip 1 chan 4 pulses



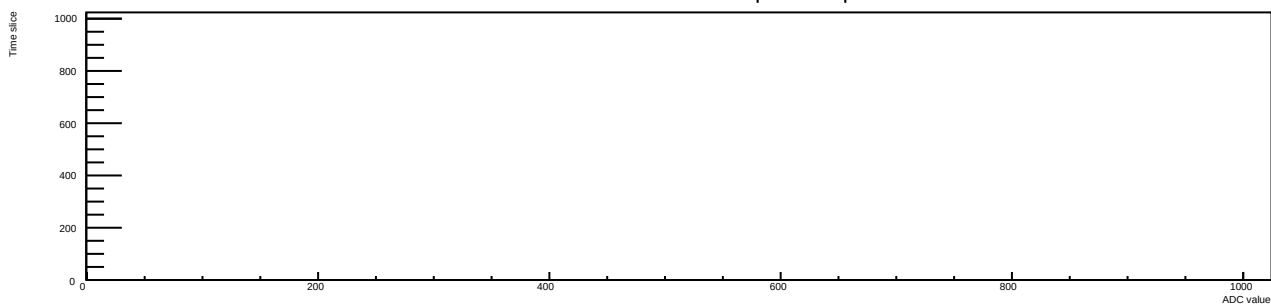
Run 36523 Evt 1000 Time mcm 2 chip 1 chan 5 pulses



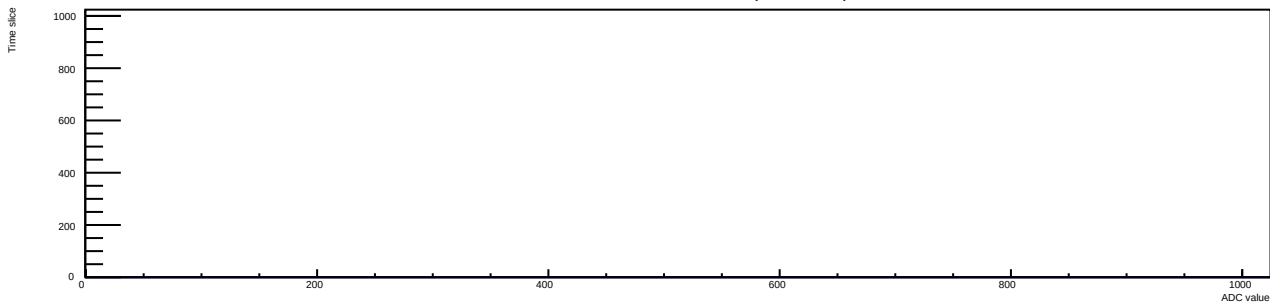
Run 36523 Evt 1000 Time mcm 2 chip 1 chan 6 pulses



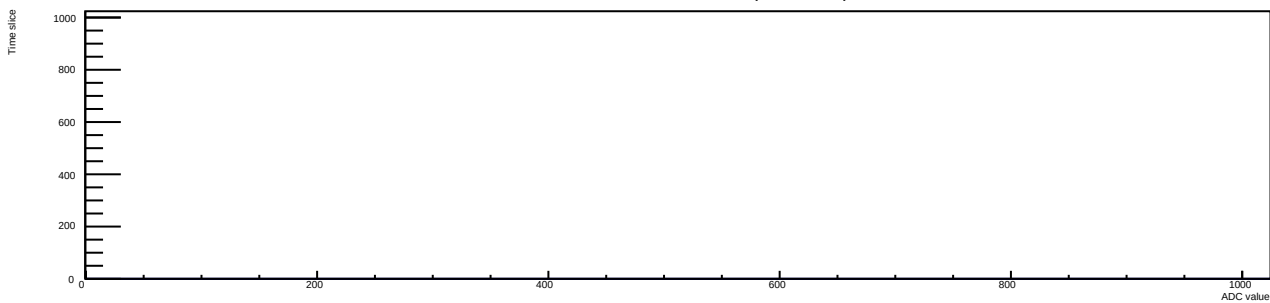
Run 36523 Evt 1000 Time mcm 2 chip 1 chan 7 pulses



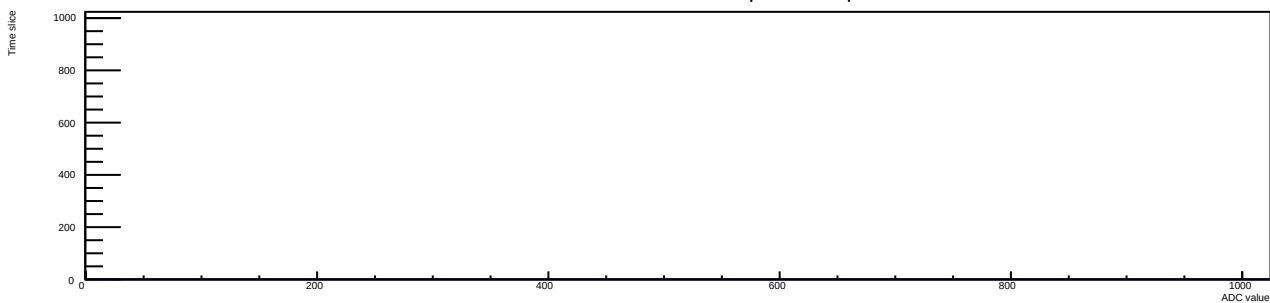
Run 36523 Evt 1000 Time mcm 2 chip 1 chan 8 pulses



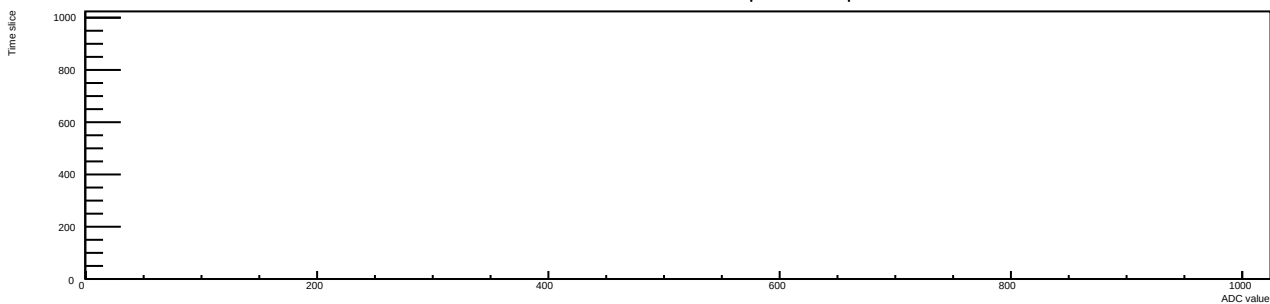
Run 36523 Evt 1000 Time mcm 2 chip 1 chan 9 pulses



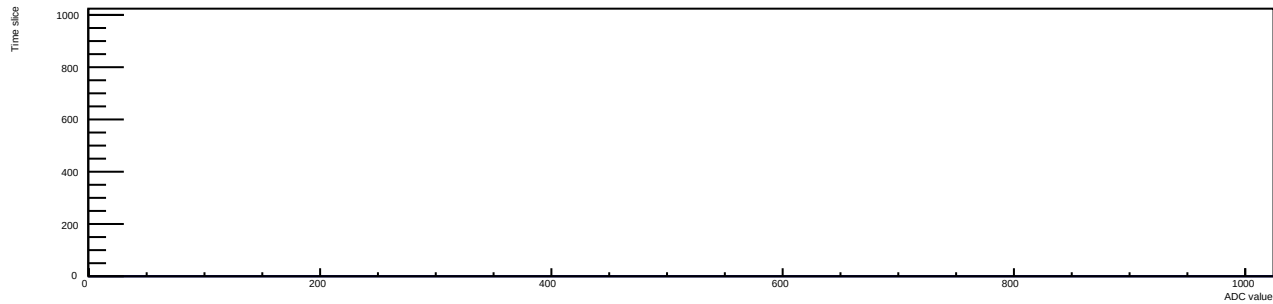
Run 36523 Evt 1000 Time mcm 2 chip 1 chan 10 pulses



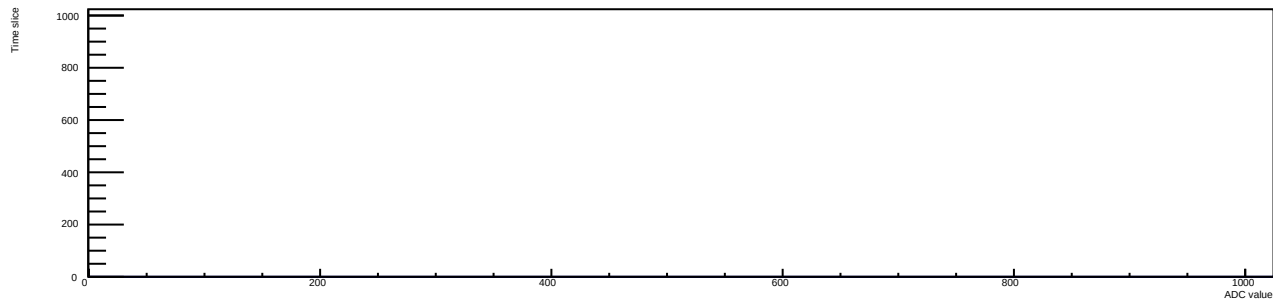
Run 36523 Evt 1000 Time mcm 2 chip 1 chan 11 pulses



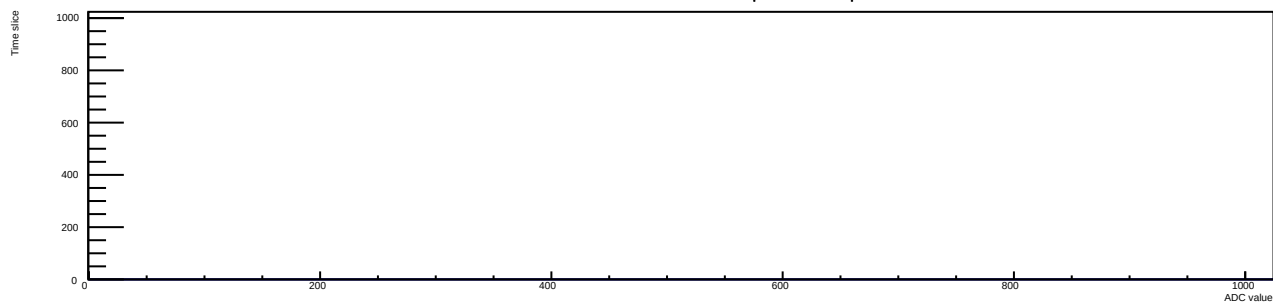
Run 36523 Evt 1000 Time mcm 2 chip 1 chan 12 pulses



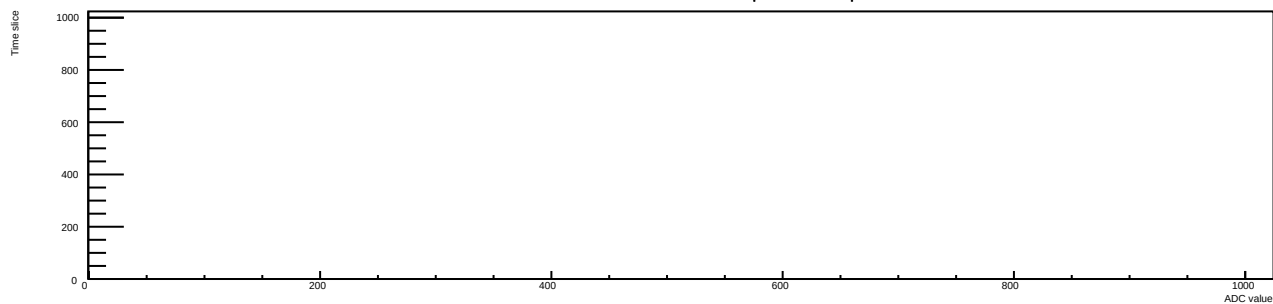
Run 36523 Evt 1000 Time mcm 2 chip 1 chan 13 pulses



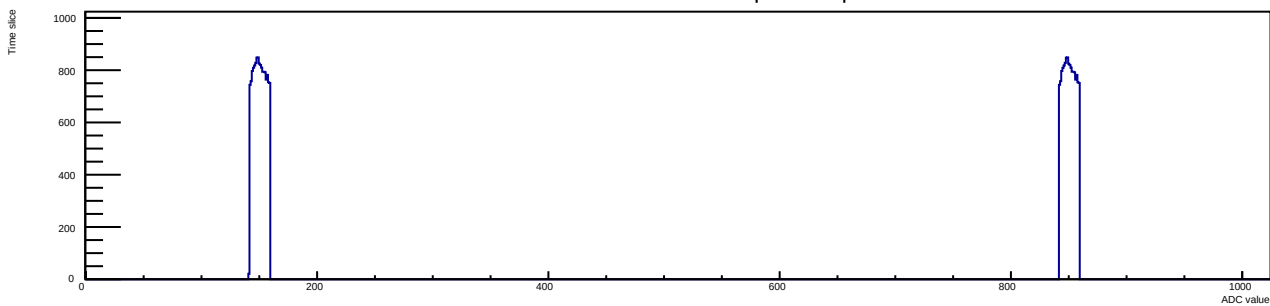
Run 36523 Evt 1000 Time mcm 2 chip 1 chan 14 pulses



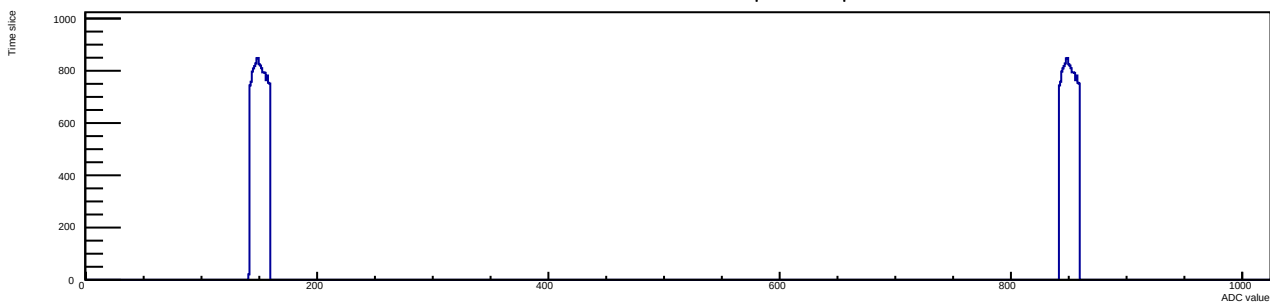
Run 36523 Evt 1000 Time mcm 2 chip 1 chan 15 pulses



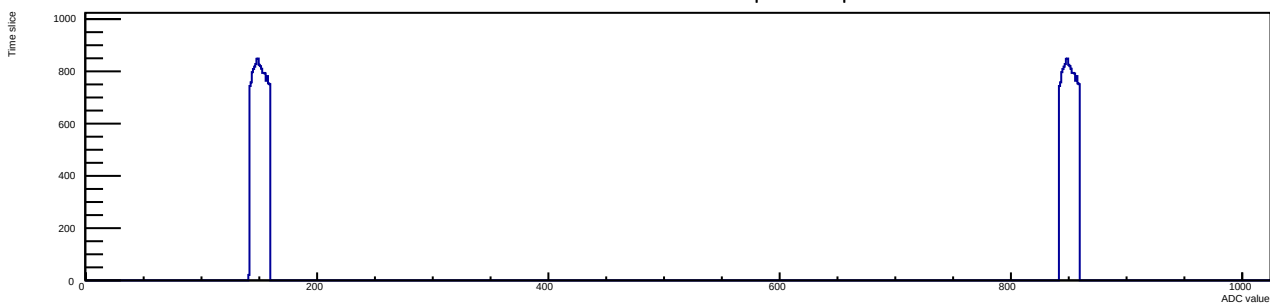
Run 36523 Evt 1000 Time mcm 2 chip 2 chan 0 pulses



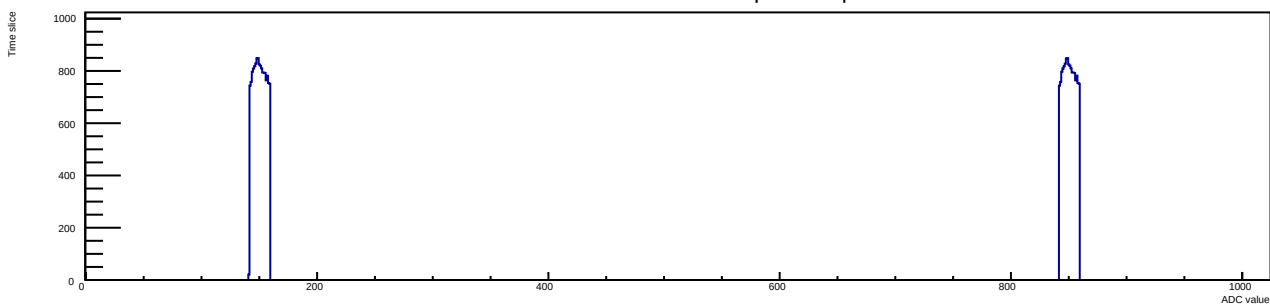
Run 36523 Evt 1000 Time mcm 2 chip 2 chan 1 pulses



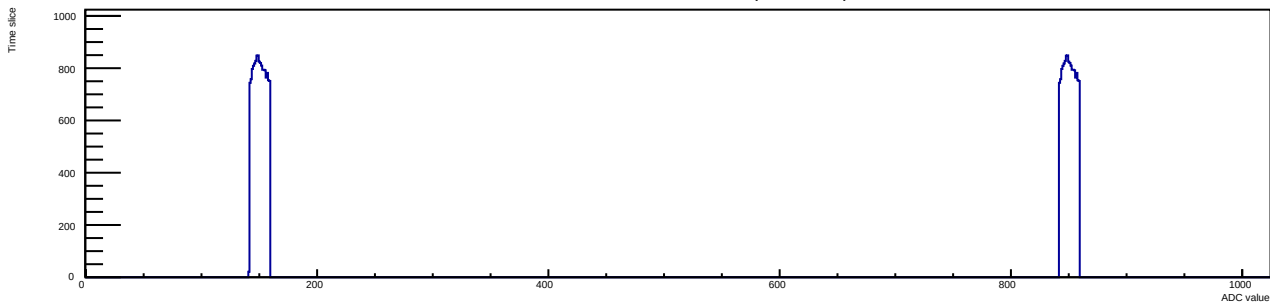
Run 36523 Evt 1000 Time mcm 2 chip 2 chan 2 pulses



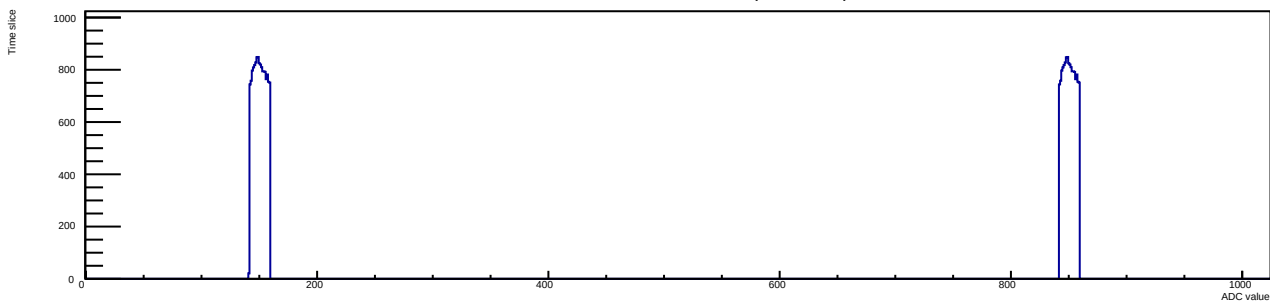
Run 36523 Evt 1000 Time mcm 2 chip 2 chan 3 pulses



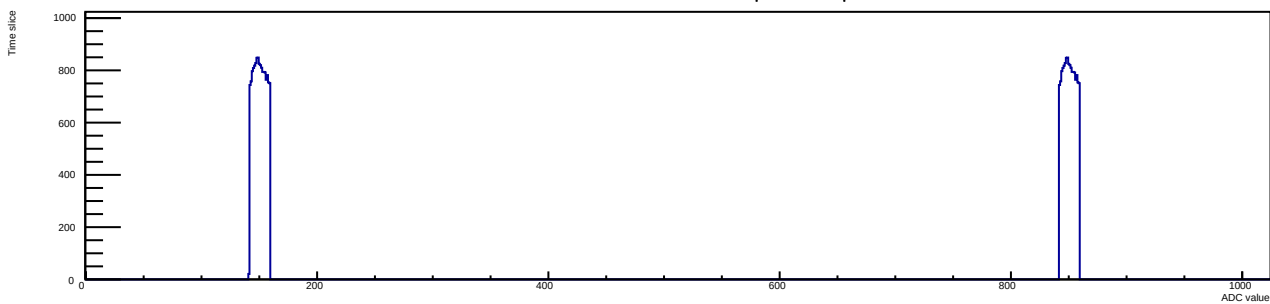
Run 36523 Evt 1000 Time mcm 2 chip 2 chan 4 pulses



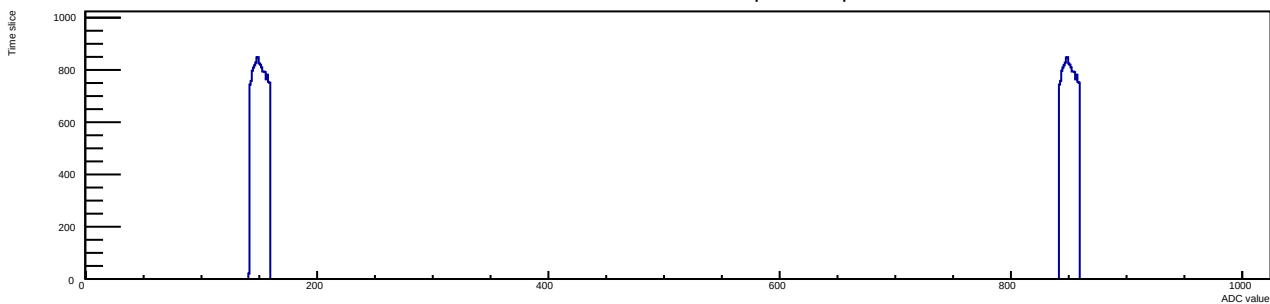
Run 36523 Evt 1000 Time mcm 2 chip 2 chan 5 pulses



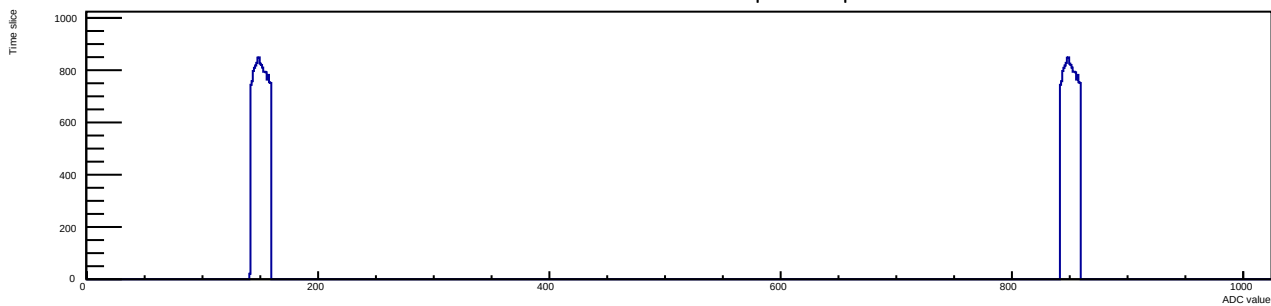
Run 36523 Evt 1000 Time mcm 2 chip 2 chan 6 pulses



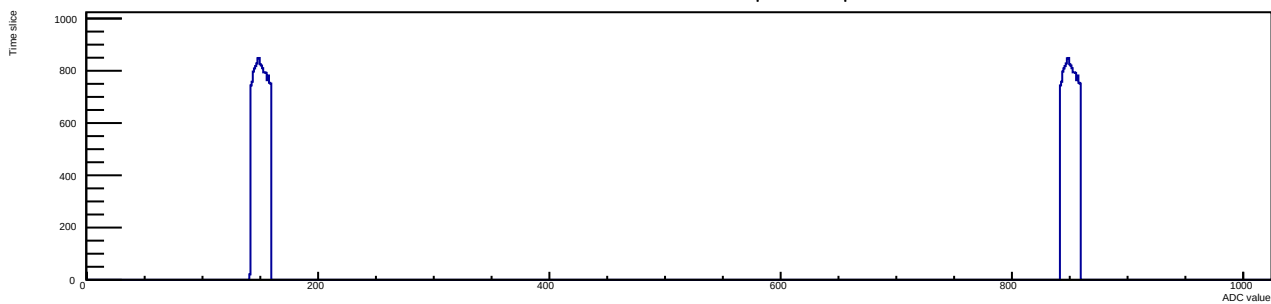
Run 36523 Evt 1000 Time mcm 2 chip 2 chan 7 pulses



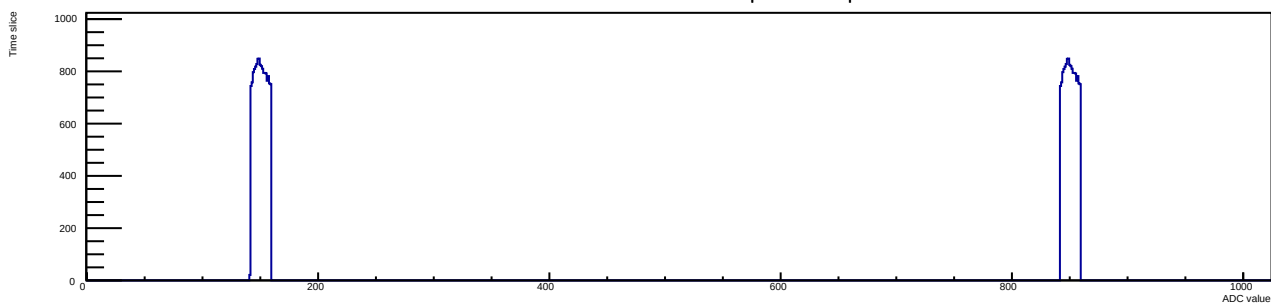
Run 36523 Evt 1000 Time mcm 2 chip 2 chan 8 pulses



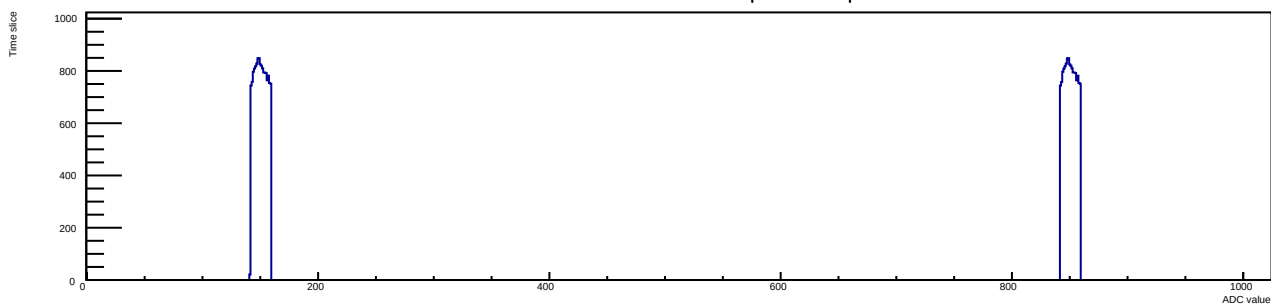
Run 36523 Evt 1000 Time mcm 2 chip 2 chan 9 pulses



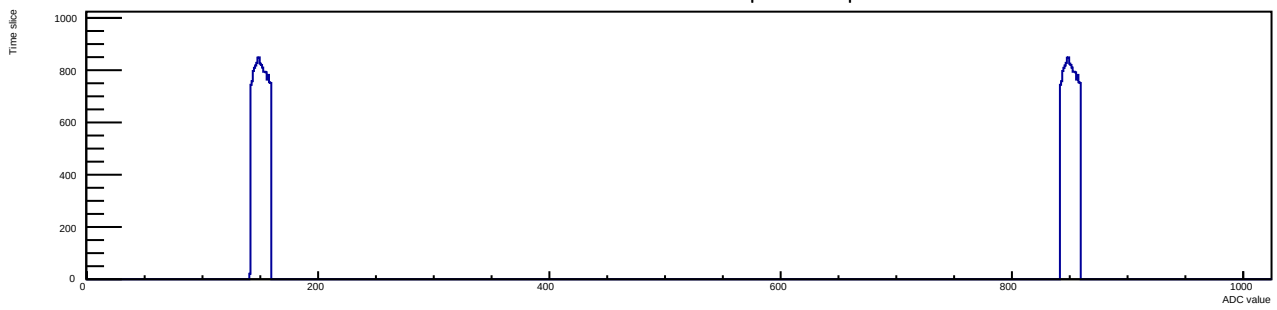
Run 36523 Evt 1000 Time mcm 2 chip 2 chan 10 pulses



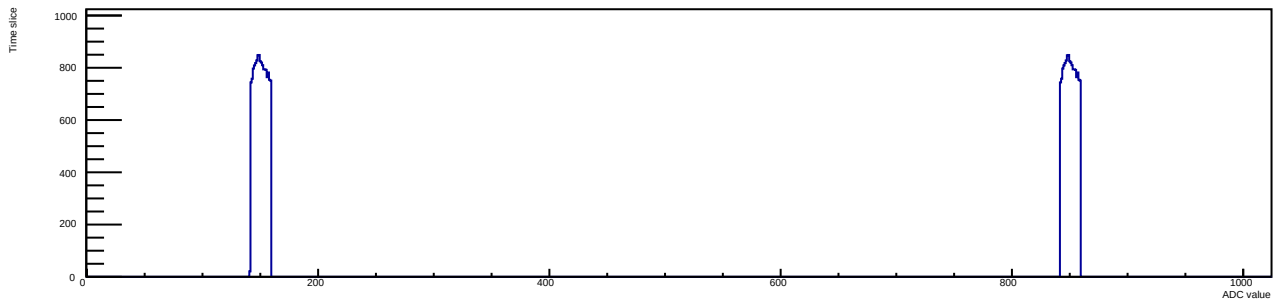
Run 36523 Evt 1000 Time mcm 2 chip 2 chan 11 pulses



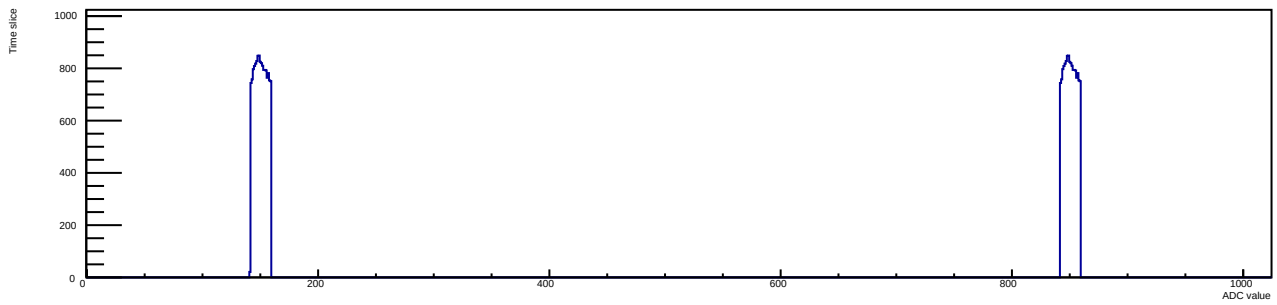
Run 36523 Evt 1000 Time mcm 2 chip 2 chan 12 pulses



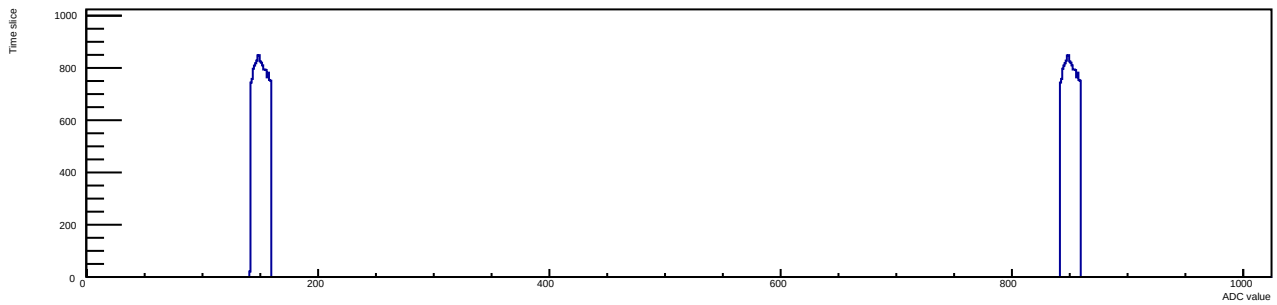
Run 36523 Evt 1000 Time mcm 2 chip 2 chan 13 pulses



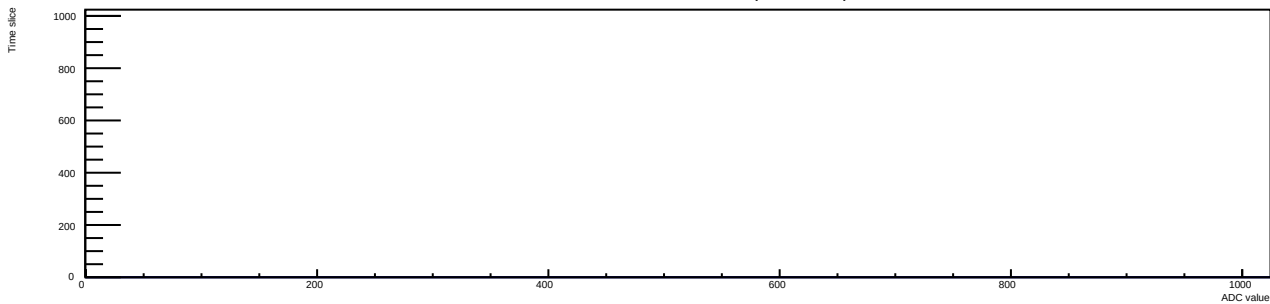
Run 36523 Evt 1000 Time mcm 2 chip 2 chan 14 pulses



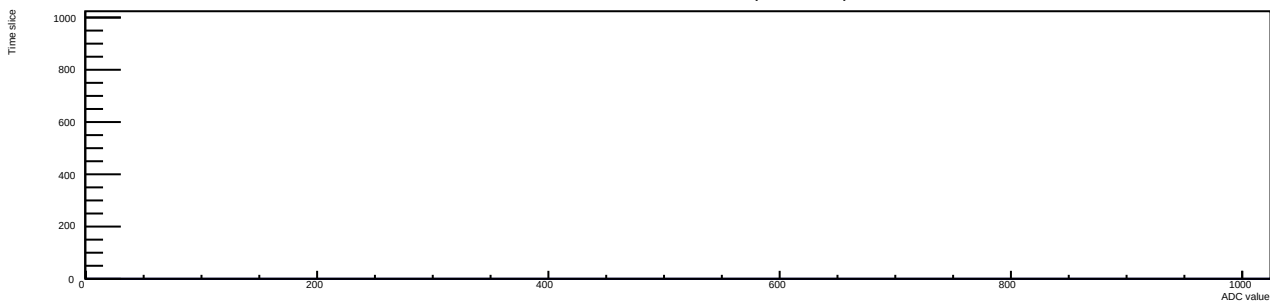
Run 36523 Evt 1000 Time mcm 2 chip 2 chan 15 pulses



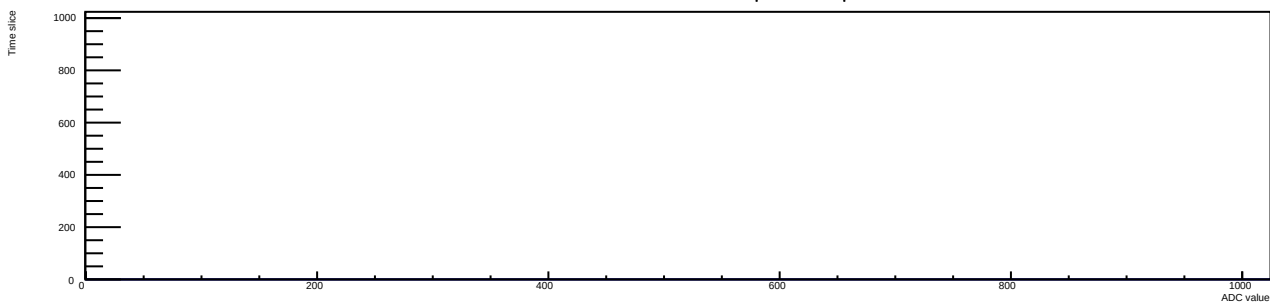
Run 36523 Evt 1000 Time mcm 2 chip 3 chan 0 pulses



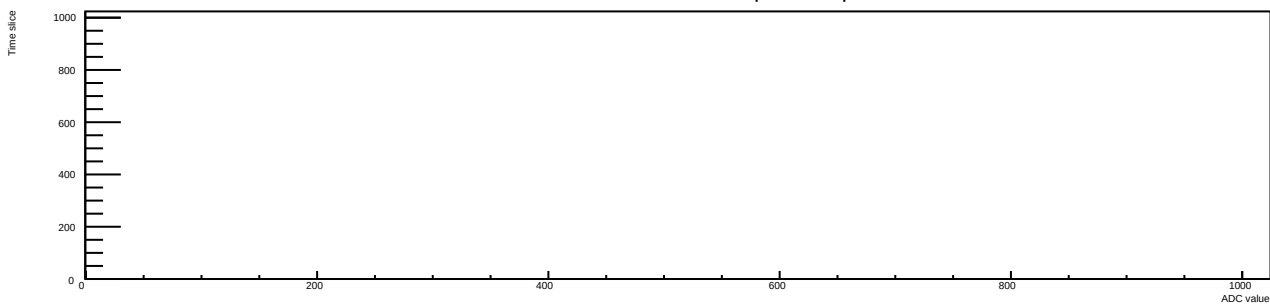
Run 36523 Evt 1000 Time mcm 2 chip 3 chan 1 pulses



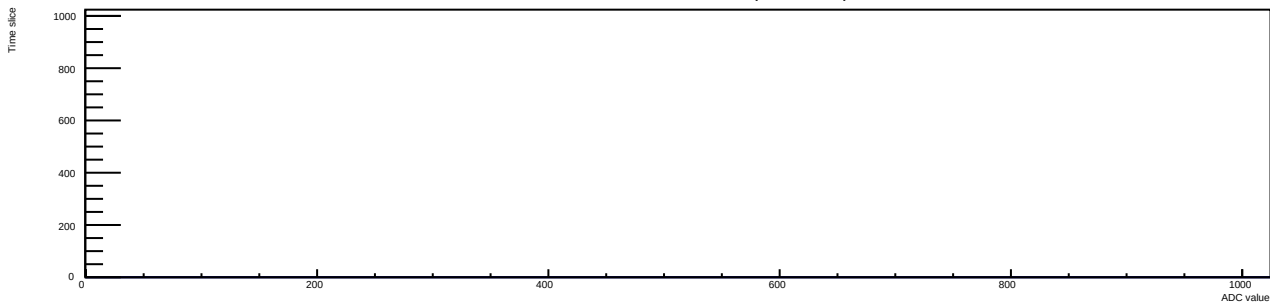
Run 36523 Evt 1000 Time mcm 2 chip 3 chan 2 pulses



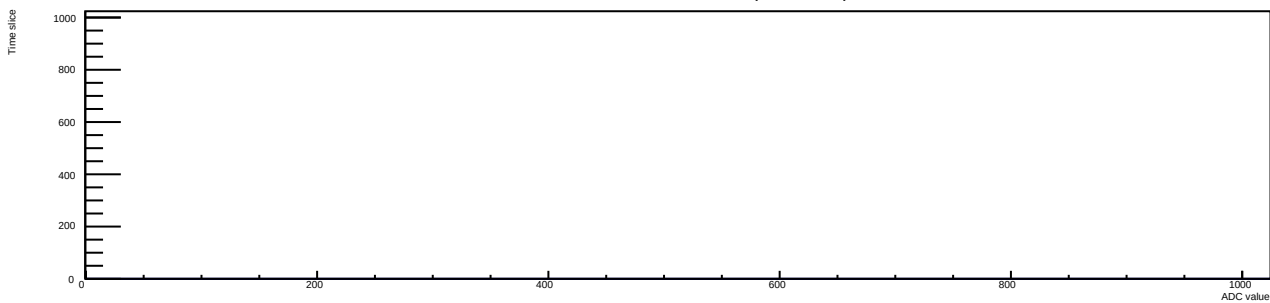
Run 36523 Evt 1000 Time mcm 2 chip 3 chan 3 pulses



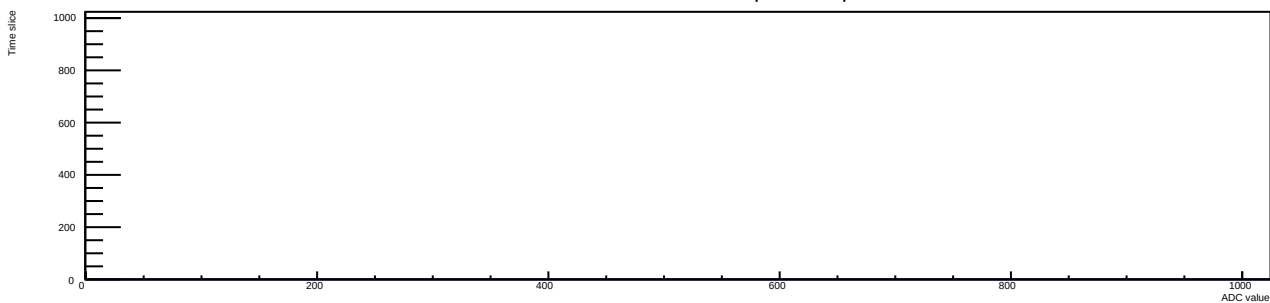
Run 36523 Evt 1000 Time mcm 2 chip 3 chan 4 pulses



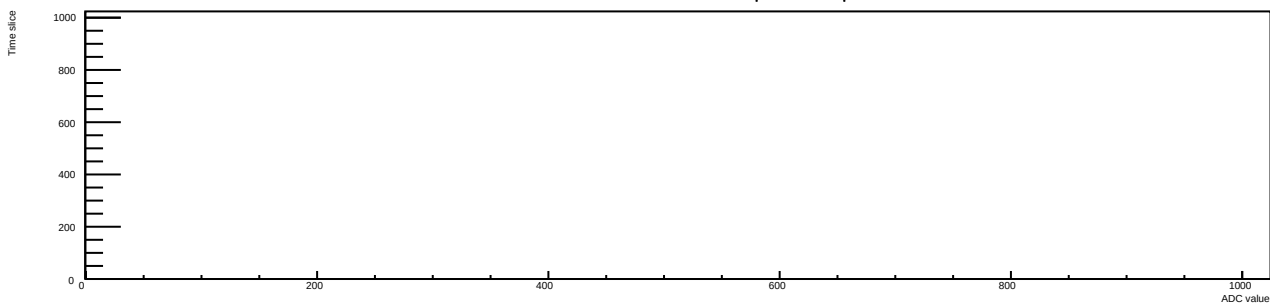
Run 36523 Evt 1000 Time mcm 2 chip 3 chan 5 pulses



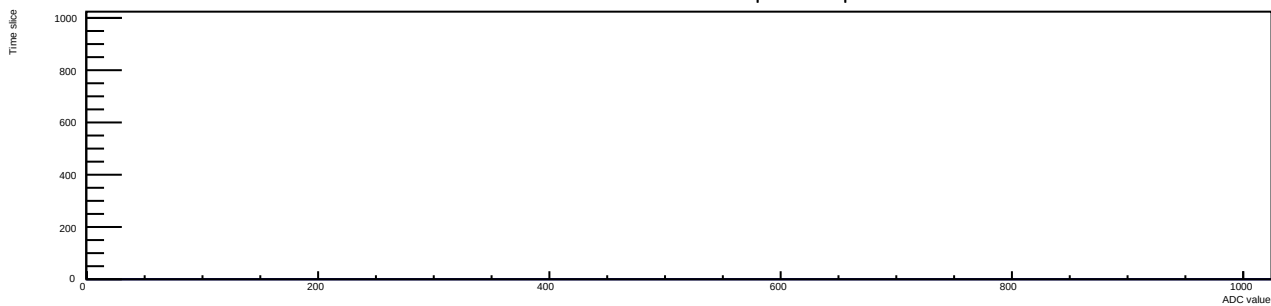
Run 36523 Evt 1000 Time mcm 2 chip 3 chan 6 pulses



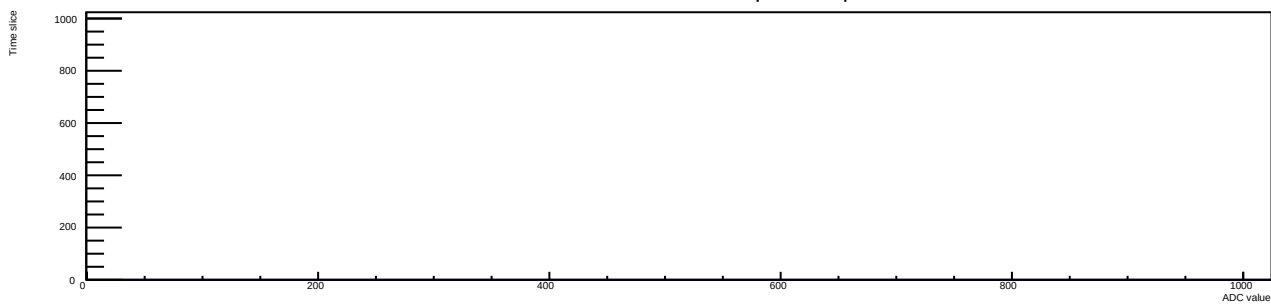
Run 36523 Evt 1000 Time mcm 2 chip 3 chan 7 pulses



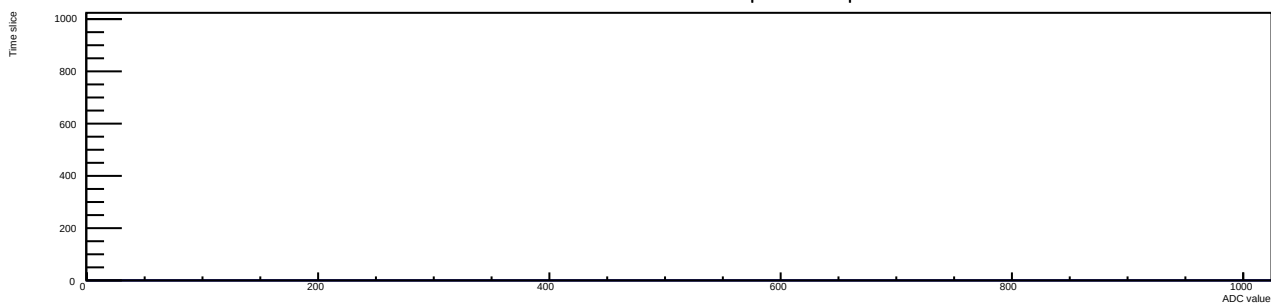
Run 36523 Evt 1000 Time mcm 2 chip 3 chan 8 pulses



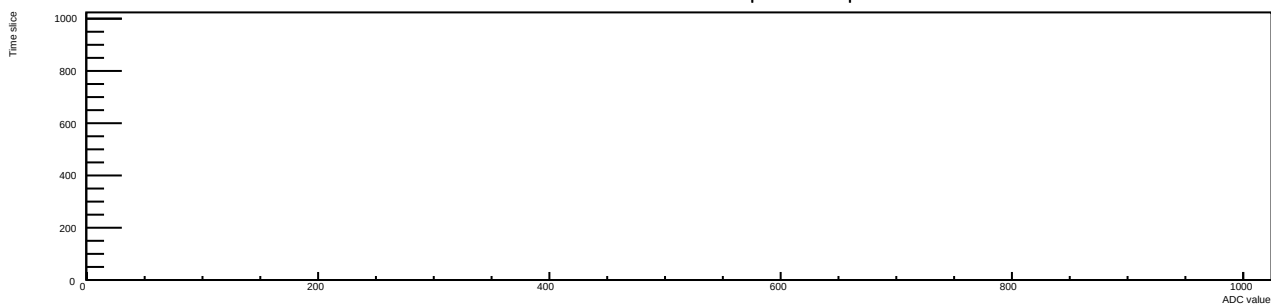
Run 36523 Evt 1000 Time mcm 2 chip 3 chan 9 pulses



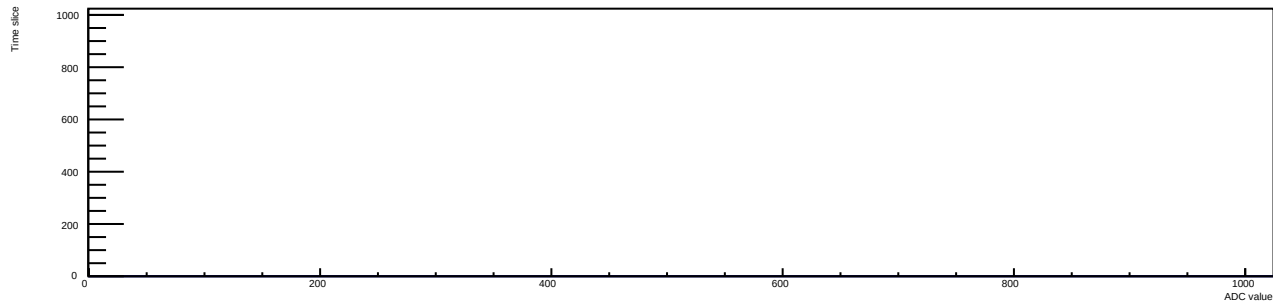
Run 36523 Evt 1000 Time mcm 2 chip 3 chan 10 pulses



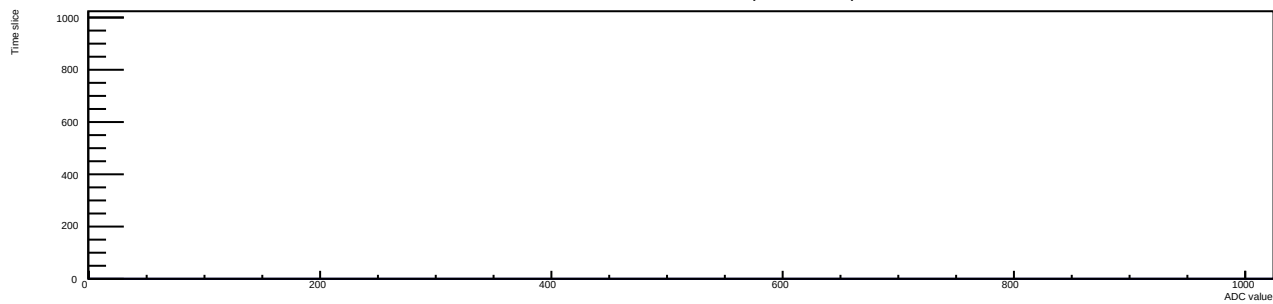
Run 36523 Evt 1000 Time mcm 2 chip 3 chan 11 pulses



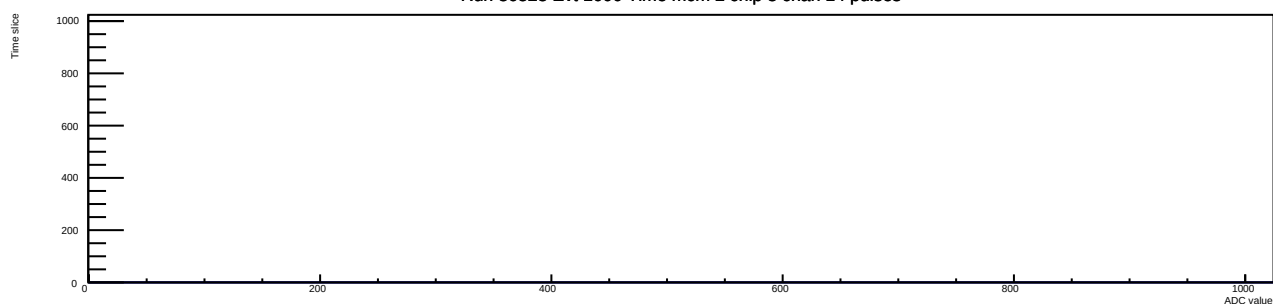
Run 36523 Evt 1000 Time mcm 2 chip 3 chan 12 pulses



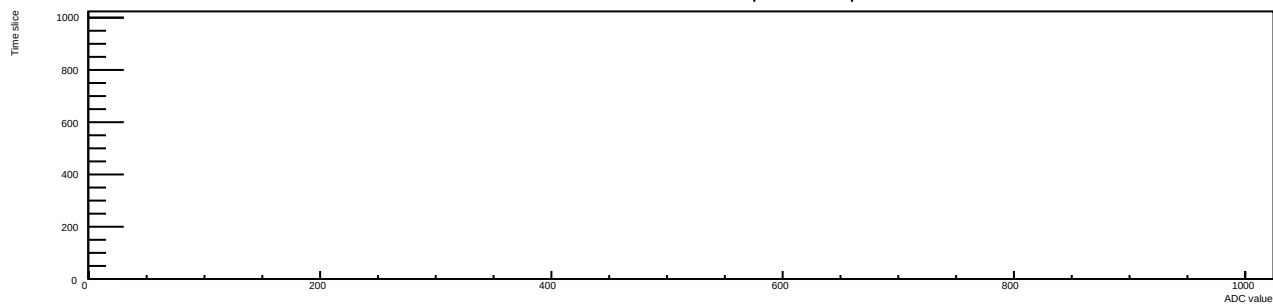
Run 36523 Evt 1000 Time mcm 2 chip 3 chan 13 pulses



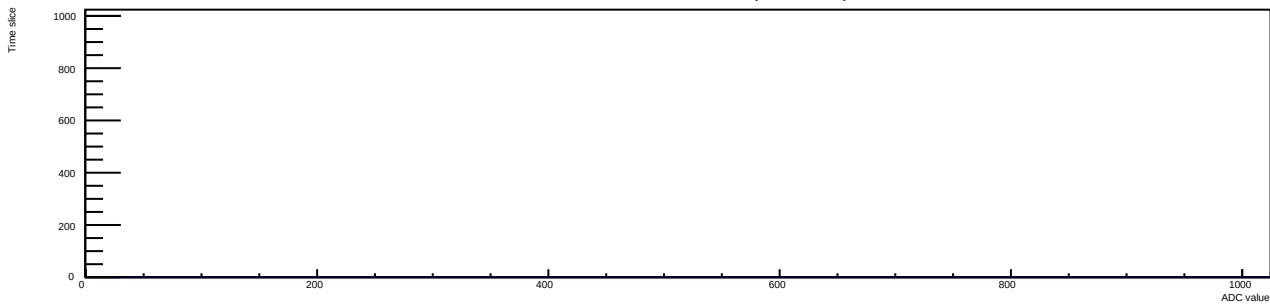
Run 36523 Evt 1000 Time mcm 2 chip 3 chan 14 pulses



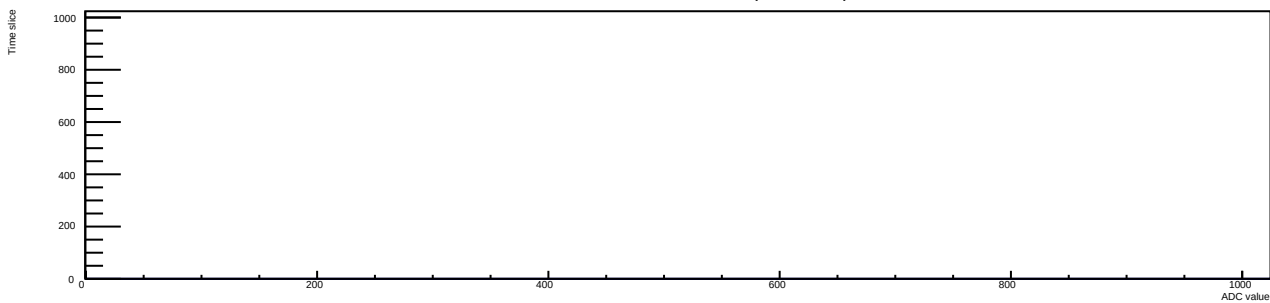
Run 36523 Evt 1000 Time mcm 2 chip 3 chan 15 pulses



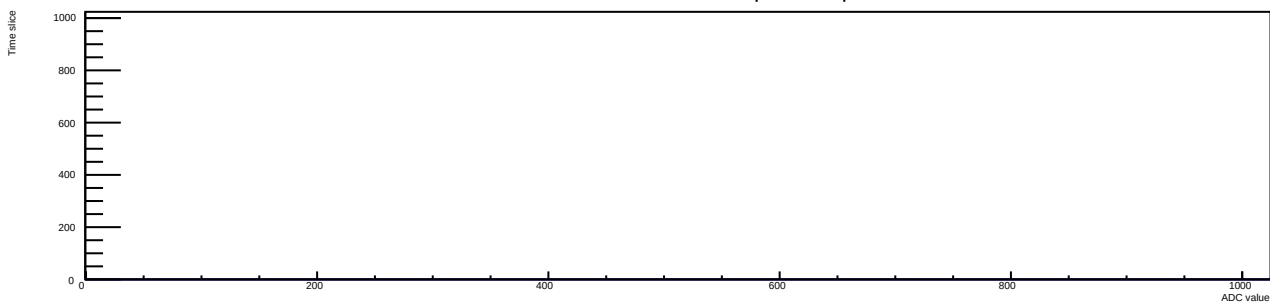
Run 36523 Evt 1000 Time mcm 2 chip 4 chan 0 pulses



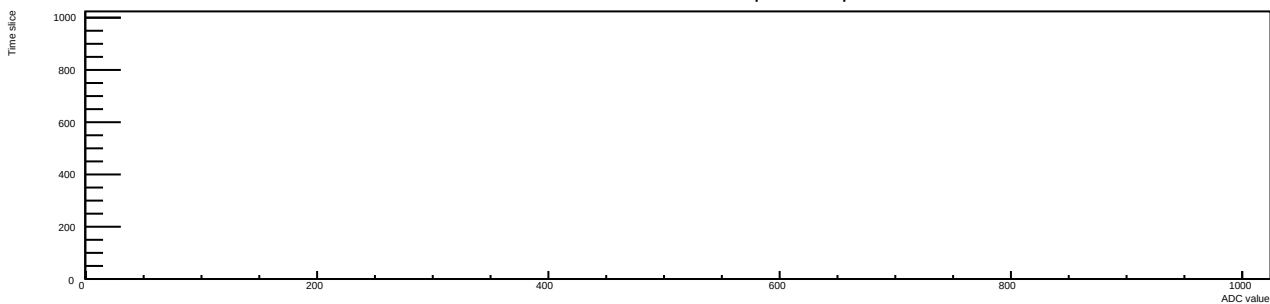
Run 36523 Evt 1000 Time mcm 2 chip 4 chan 1 pulses



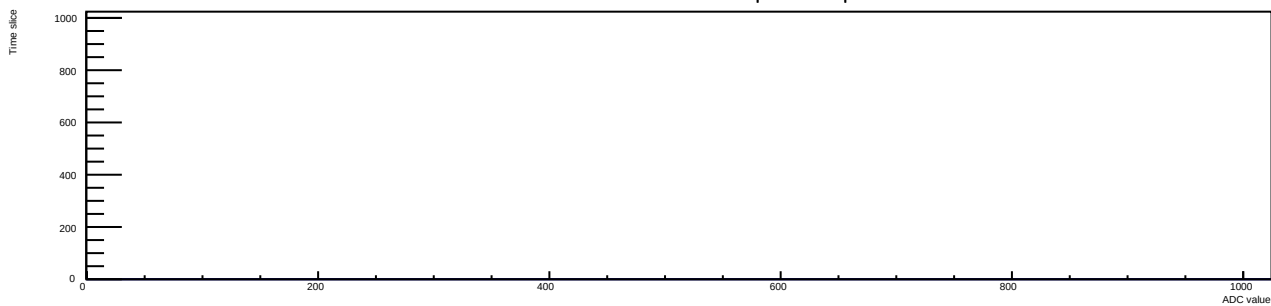
Run 36523 Evt 1000 Time mcm 2 chip 4 chan 2 pulses



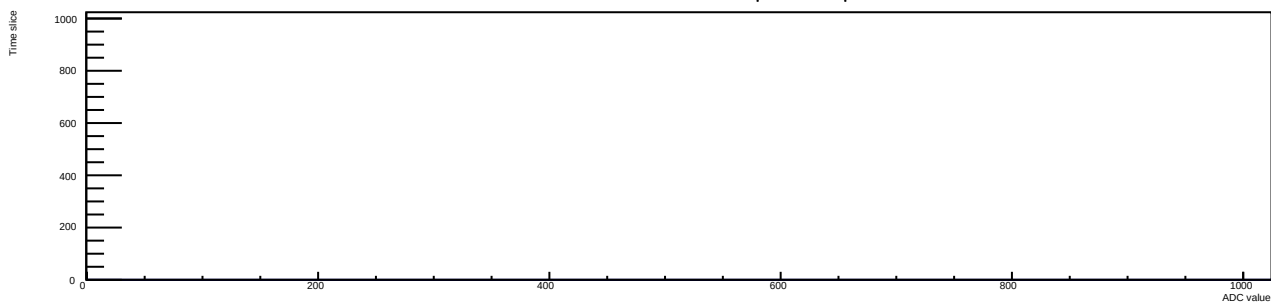
Run 36523 Evt 1000 Time mcm 2 chip 4 chan 3 pulses



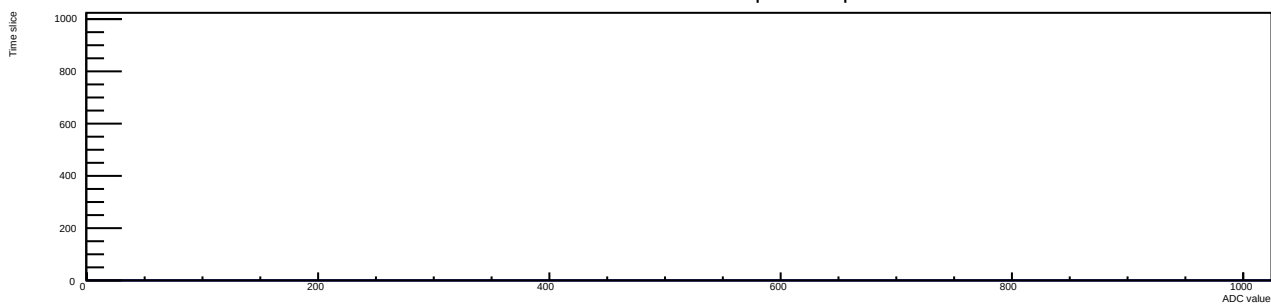
Run 36523 Evt 1000 Time mcm 2 chip 4 chan 4 pulses



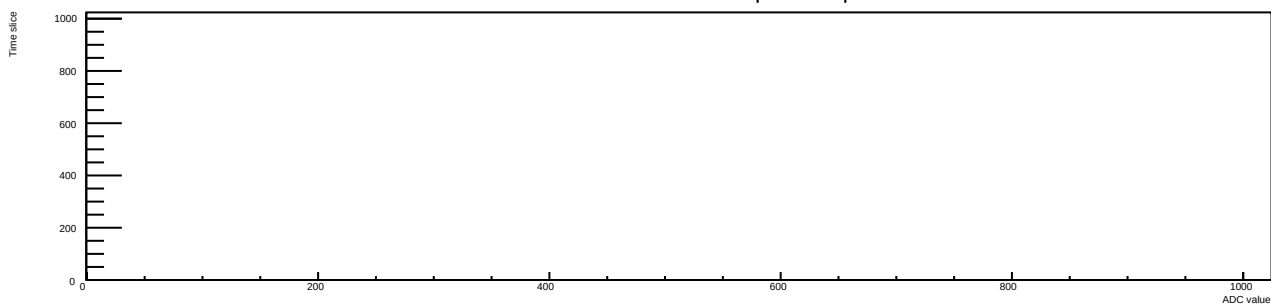
Run 36523 Evt 1000 Time mcm 2 chip 4 chan 5 pulses



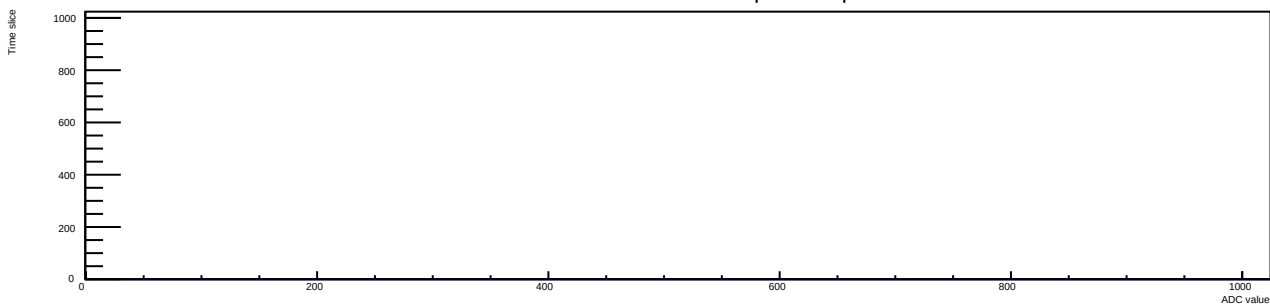
Run 36523 Evt 1000 Time mcm 2 chip 4 chan 6 pulses



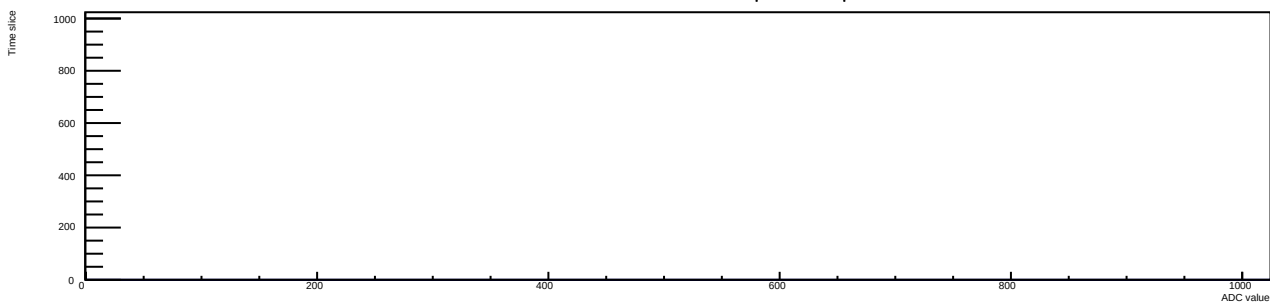
Run 36523 Evt 1000 Time mcm 2 chip 4 chan 7 pulses



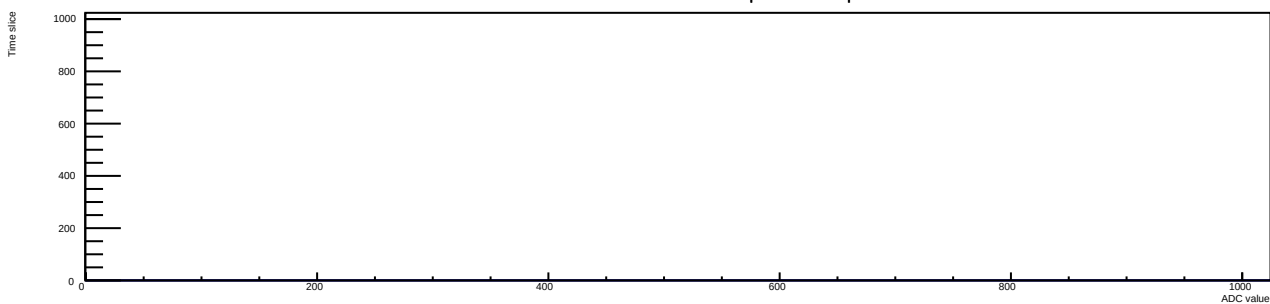
Run 36523 Evt 1000 Time mcm 2 chip 4 chan 8 pulses



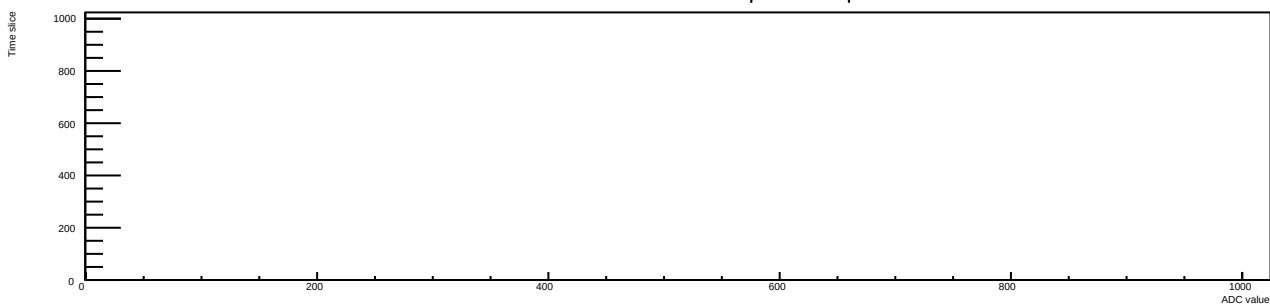
Run 36523 Evt 1000 Time mcm 2 chip 4 chan 9 pulses



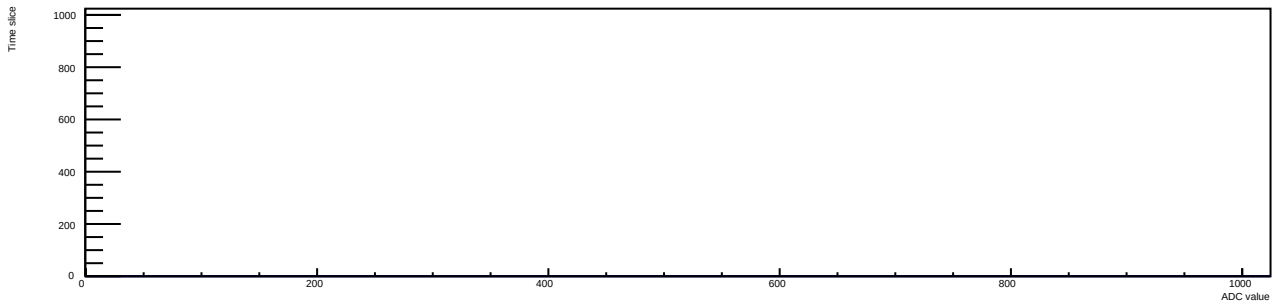
Run 36523 Evt 1000 Time mcm 2 chip 4 chan 10 pulses



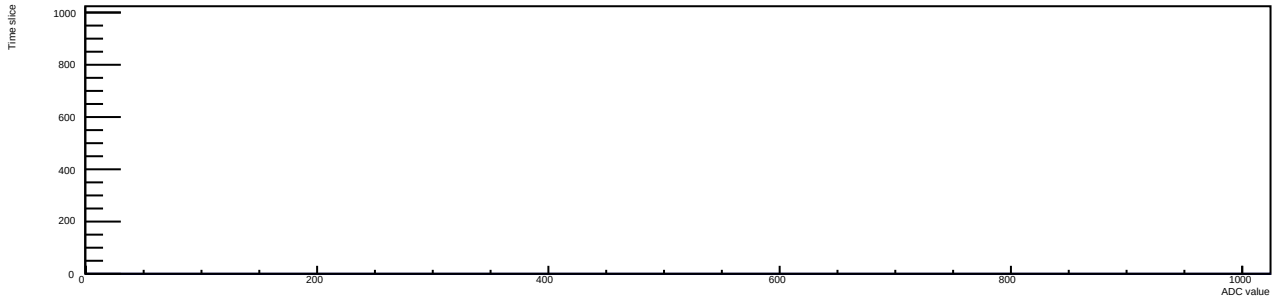
Run 36523 Evt 1000 Time mcm 2 chip 4 chan 11 pulses



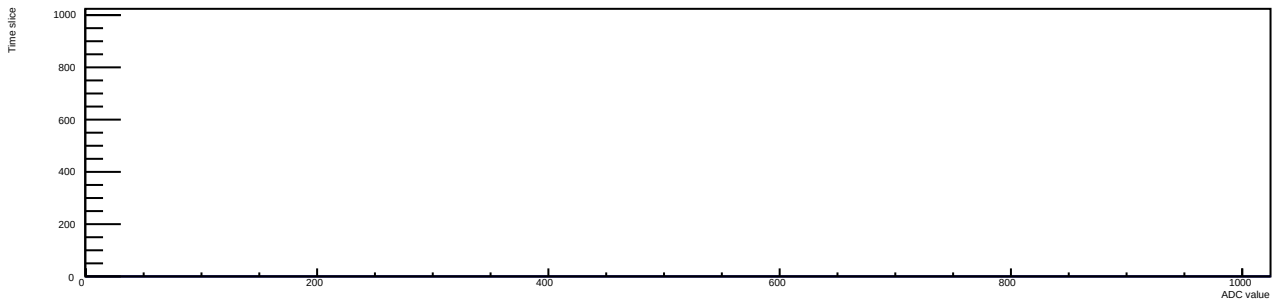
Run 36523 Evt 1000 Time mcm 2 chip 4 chan 12 pulses



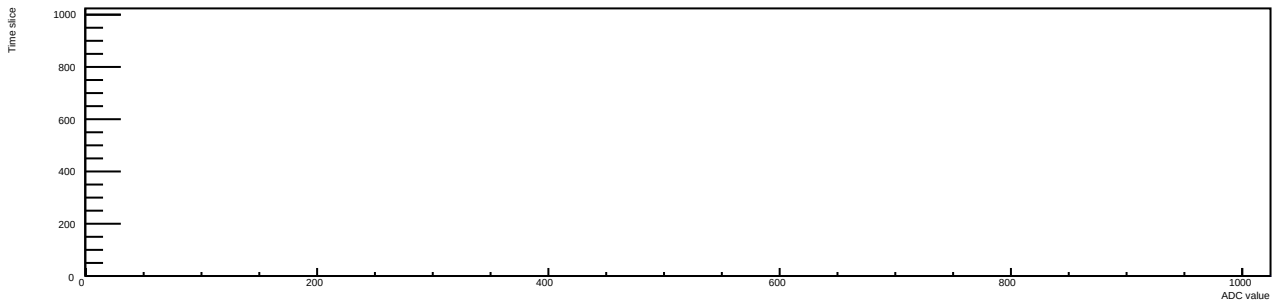
Run 36523 Evt 1000 Time mcm 2 chip 4 chan 13 pulses



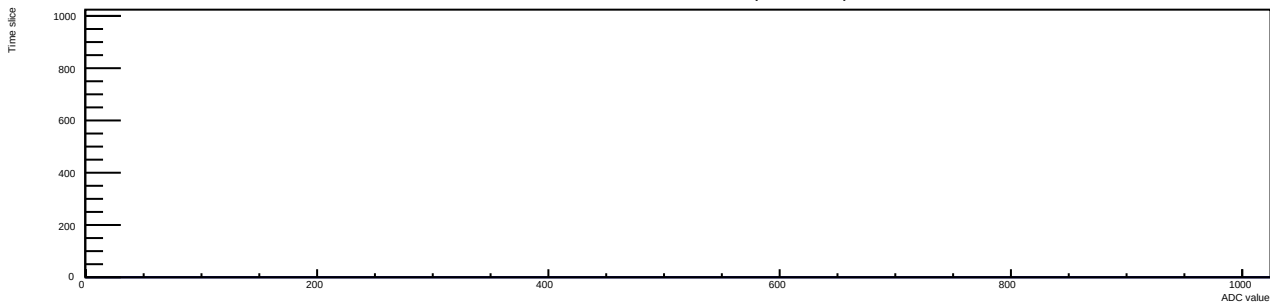
Run 36523 Evt 1000 Time mcm 2 chip 4 chan 14 pulses



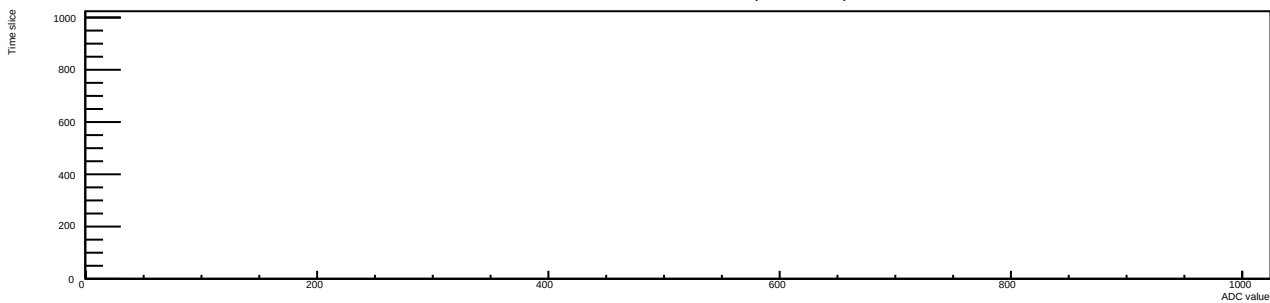
Run 36523 Evt 1000 Time mcm 2 chip 4 chan 15 pulses



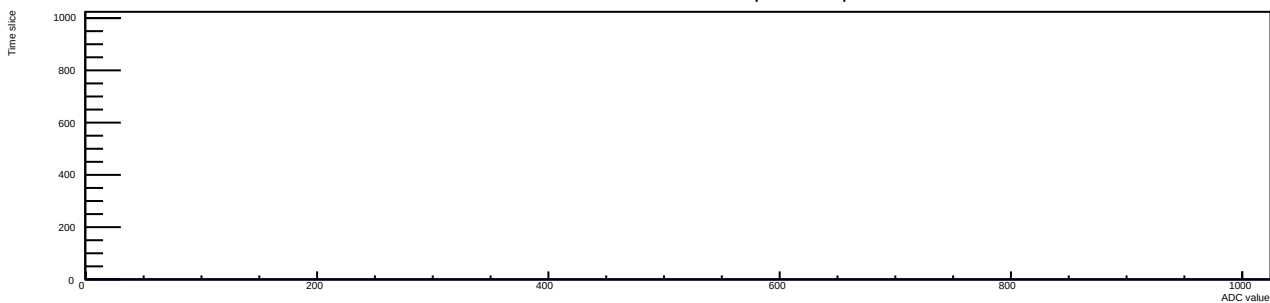
Run 36523 Evt 1000 Time mcm 2 chip 5 chan 0 pulses



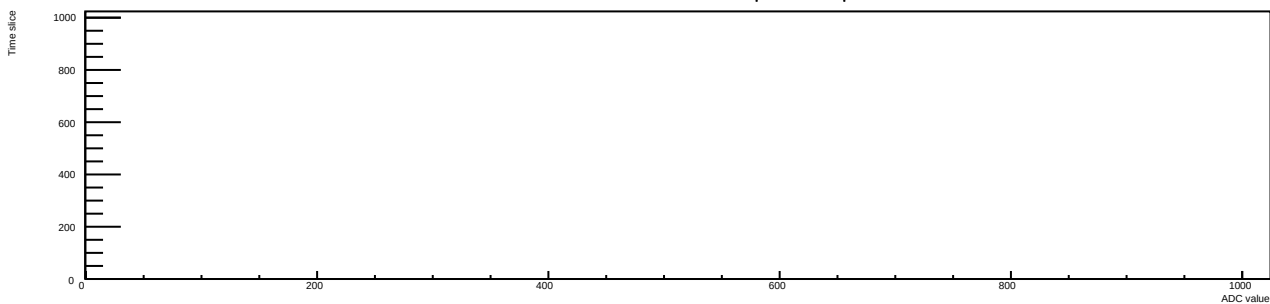
Run 36523 Evt 1000 Time mcm 2 chip 5 chan 1 pulses



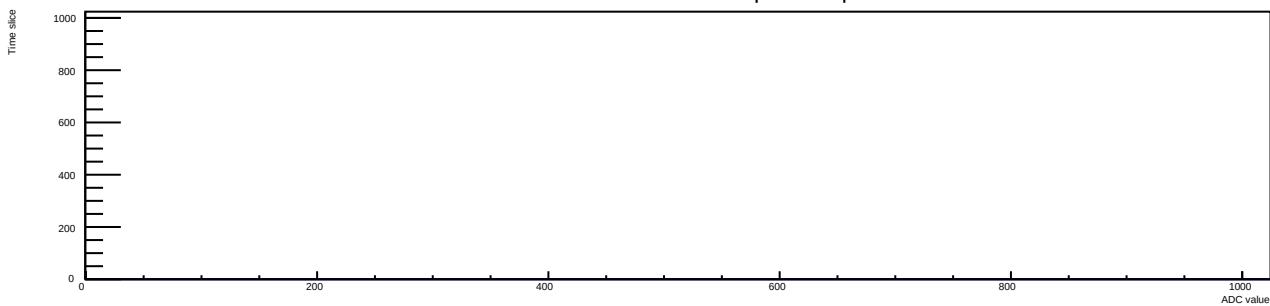
Run 36523 Evt 1000 Time mcm 2 chip 5 chan 2 pulses



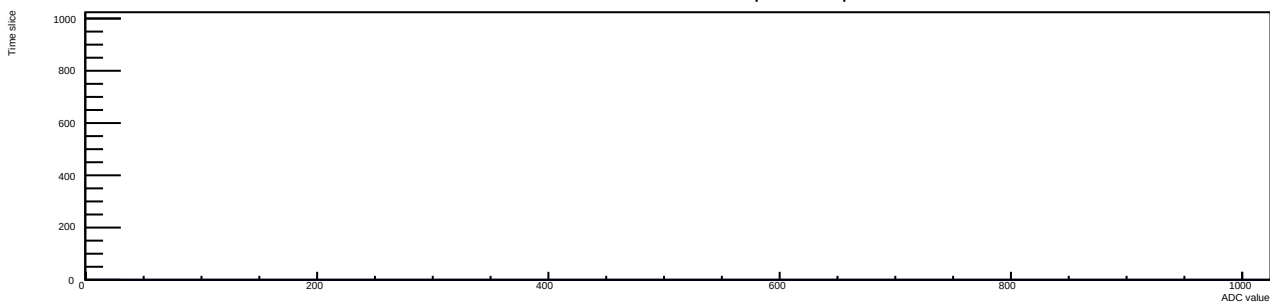
Run 36523 Evt 1000 Time mcm 2 chip 5 chan 3 pulses



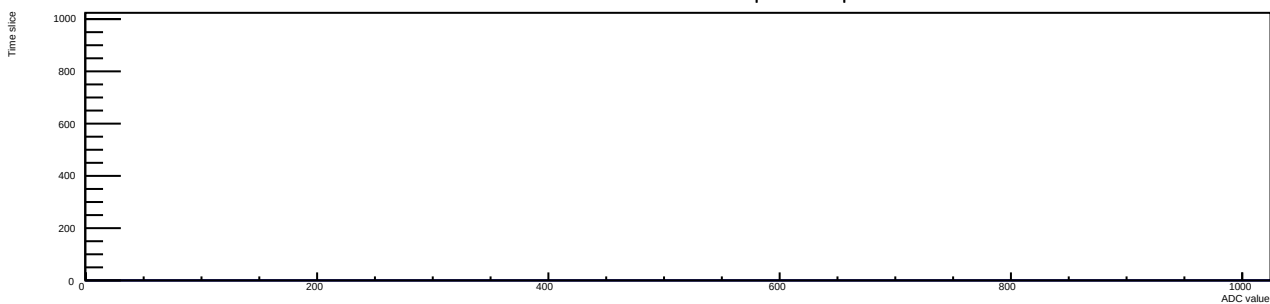
Run 36523 Evt 1000 Time mcm 2 chip 5 chan 4 pulses



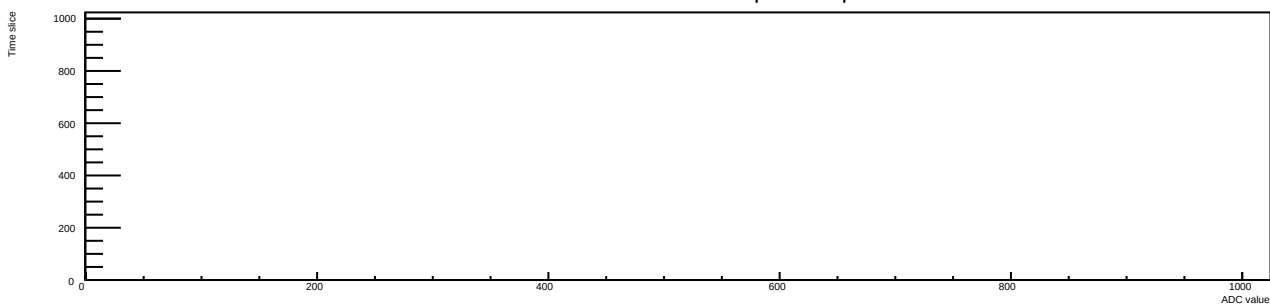
Run 36523 Evt 1000 Time mcm 2 chip 5 chan 5 pulses



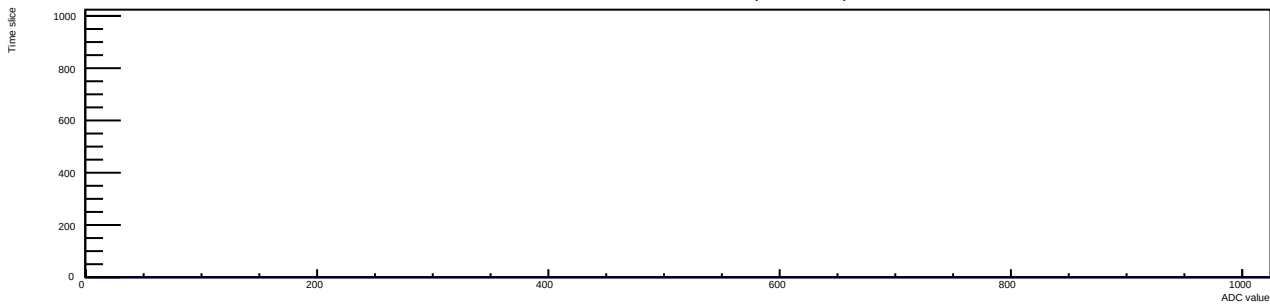
Run 36523 Evt 1000 Time mcm 2 chip 5 chan 6 pulses



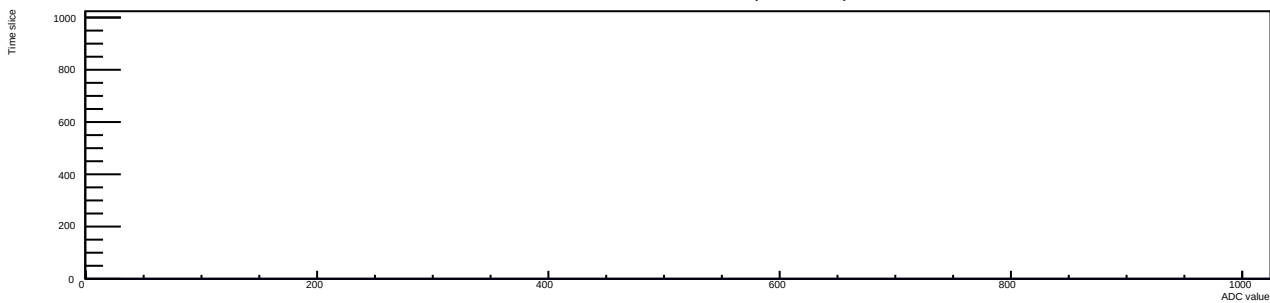
Run 36523 Evt 1000 Time mcm 2 chip 5 chan 7 pulses



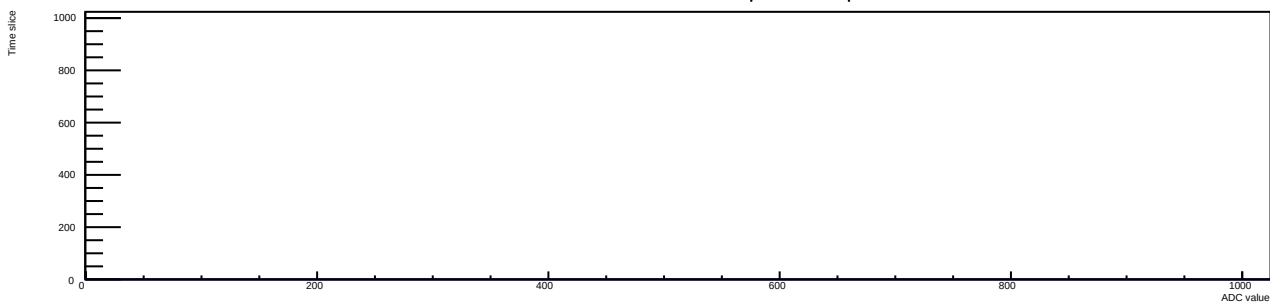
Run 36523 Evt 1000 Time mcm 2 chip 5 chan 8 pulses



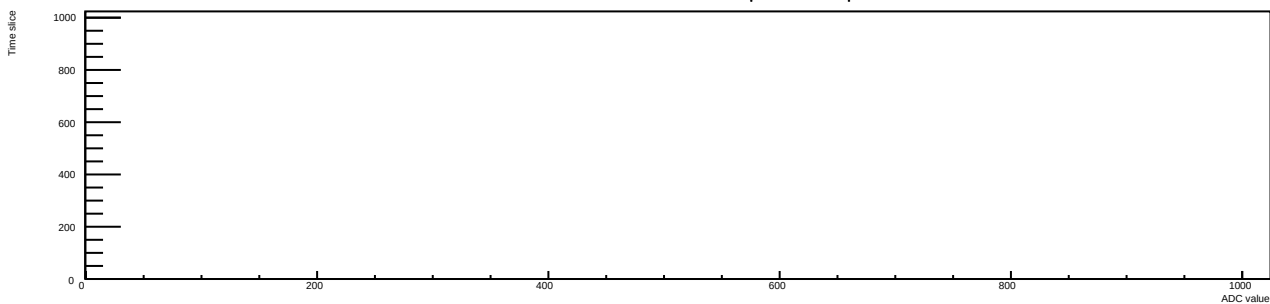
Run 36523 Evt 1000 Time mcm 2 chip 5 chan 9 pulses



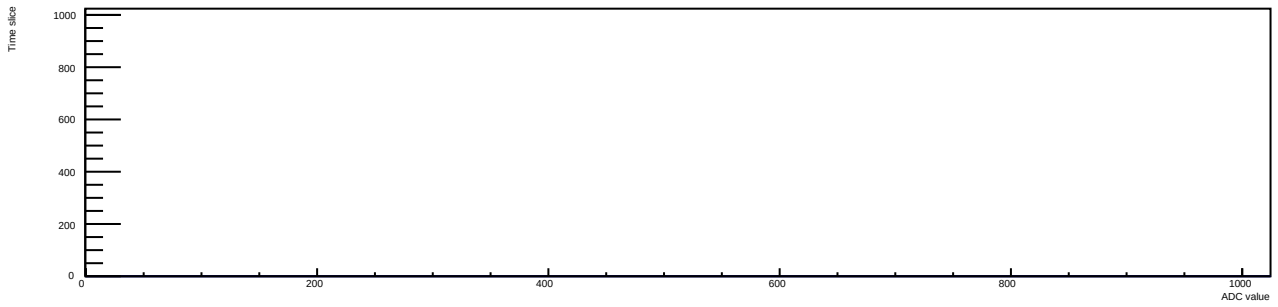
Run 36523 Evt 1000 Time mcm 2 chip 5 chan 10 pulses



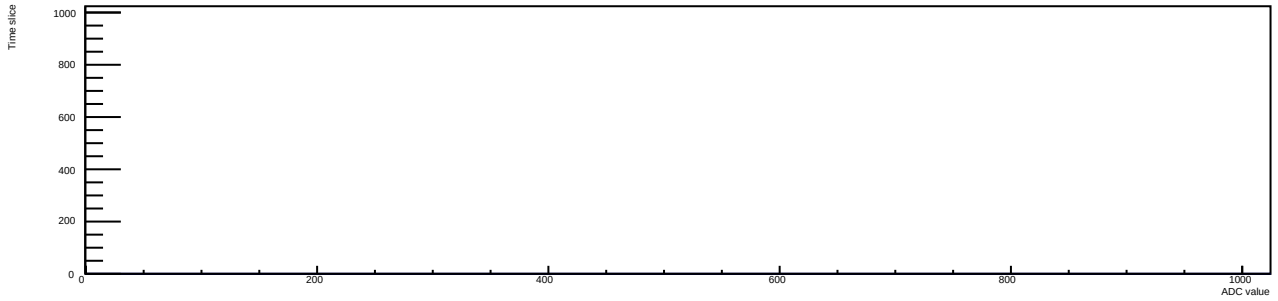
Run 36523 Evt 1000 Time mcm 2 chip 5 chan 11 pulses



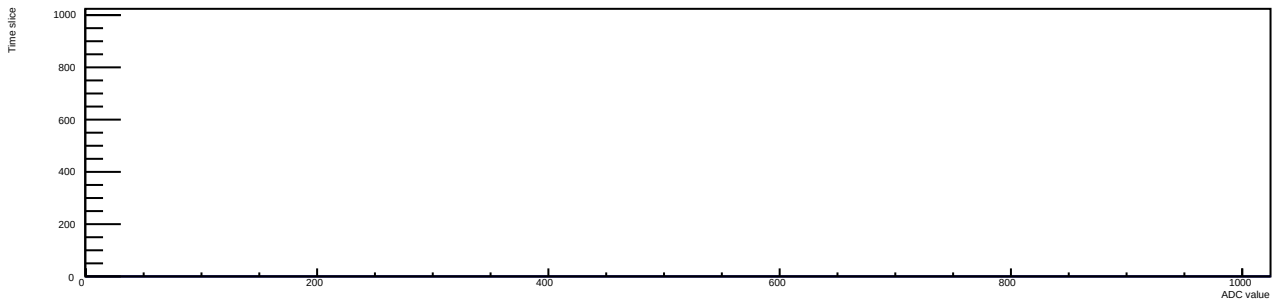
Run 36523 Evt 1000 Time mcm 2 chip 5 chan 12 pulses



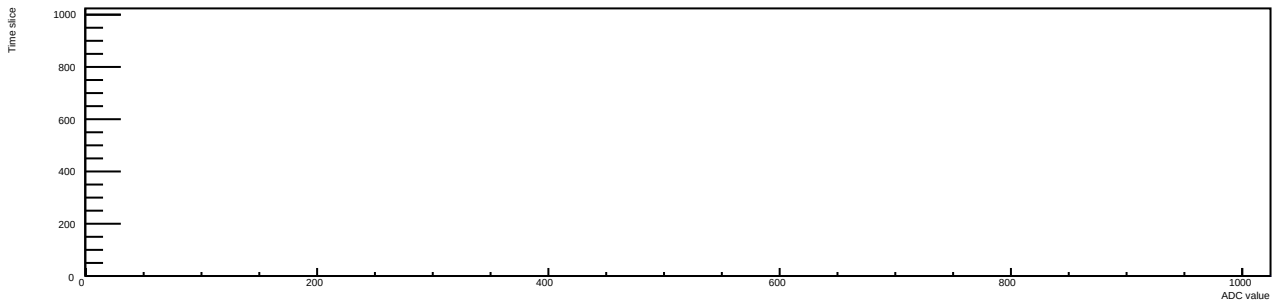
Run 36523 Evt 1000 Time mcm 2 chip 5 chan 13 pulses



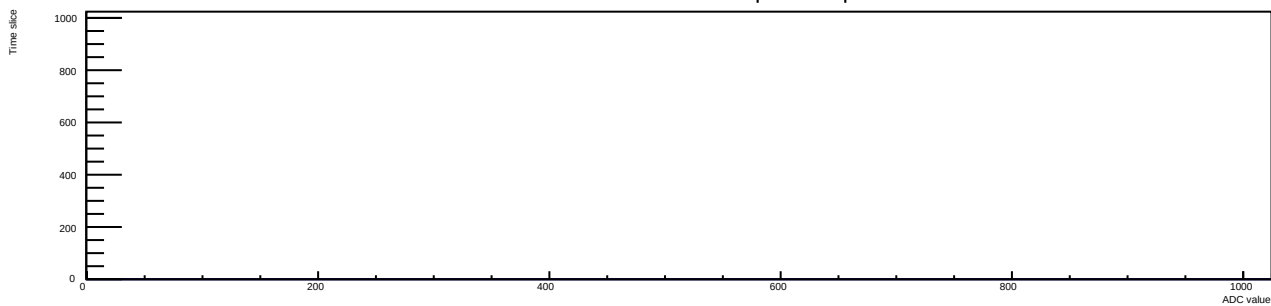
Run 36523 Evt 1000 Time mcm 2 chip 5 chan 14 pulses



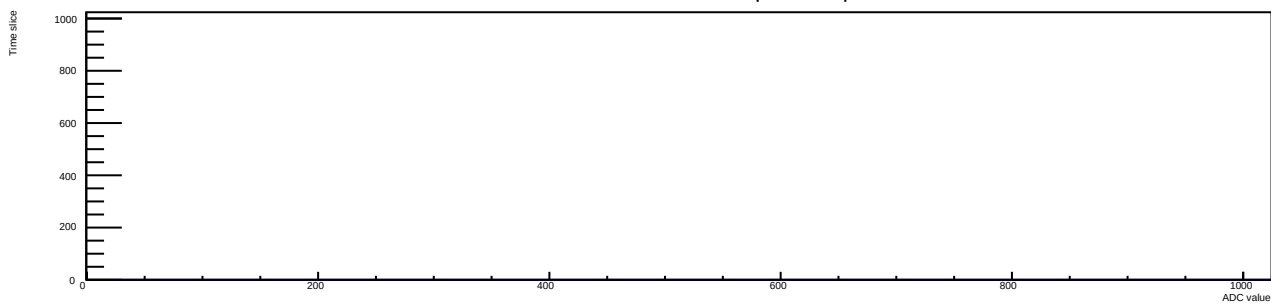
Run 36523 Evt 1000 Time mcm 2 chip 5 chan 15 pulses



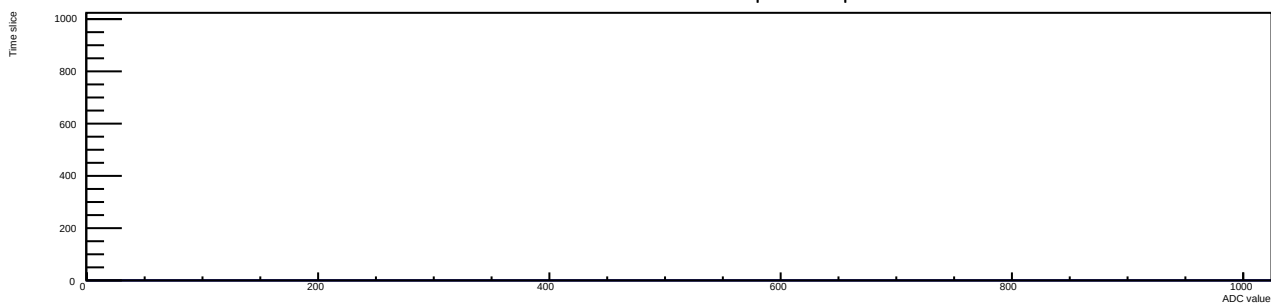
Run 36523 Evt 1000 Time mcm 2 chip 6 chan 0 pulses



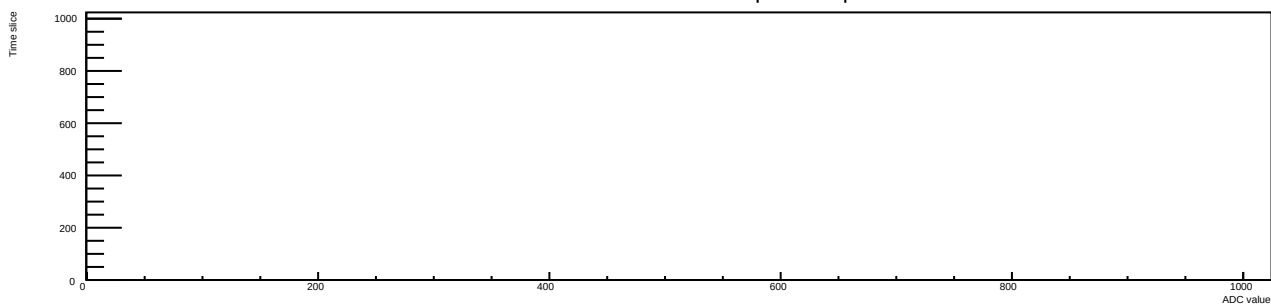
Run 36523 Evt 1000 Time mcm 2 chip 6 chan 1 pulses



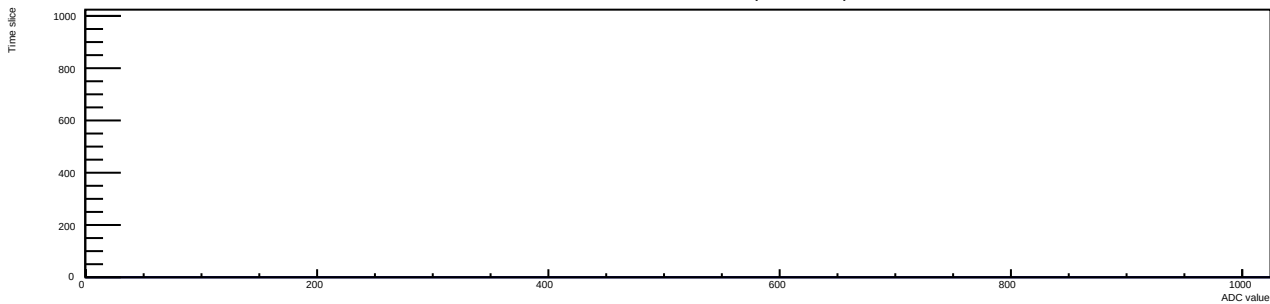
Run 36523 Evt 1000 Time mcm 2 chip 6 chan 2 pulses



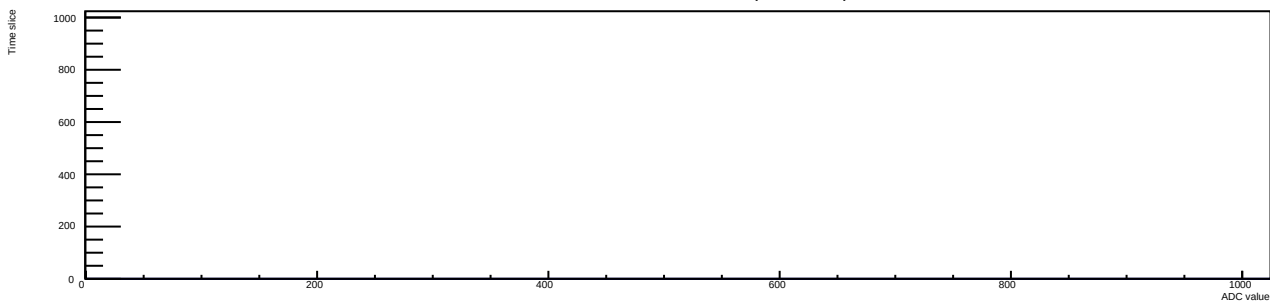
Run 36523 Evt 1000 Time mcm 2 chip 6 chan 3 pulses



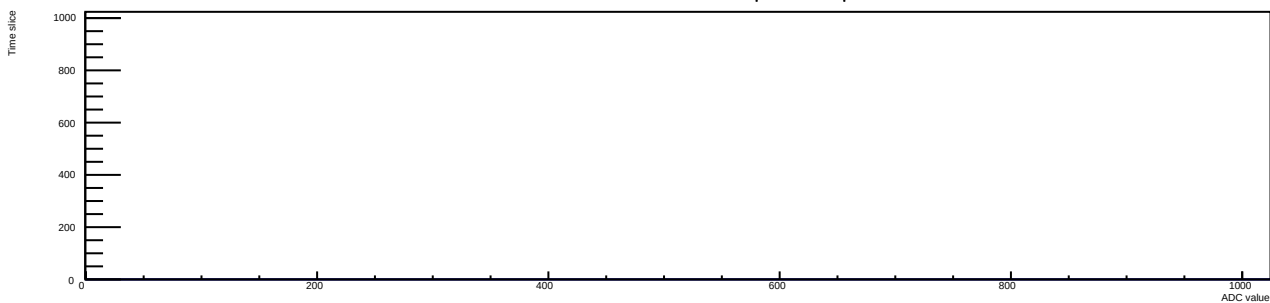
Run 36523 Evt 1000 Time mcm 2 chip 6 chan 4 pulses



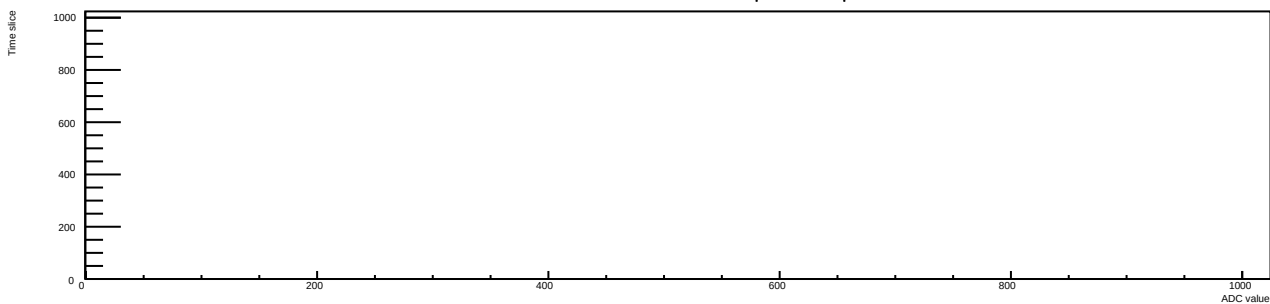
Run 36523 Evt 1000 Time mcm 2 chip 6 chan 5 pulses



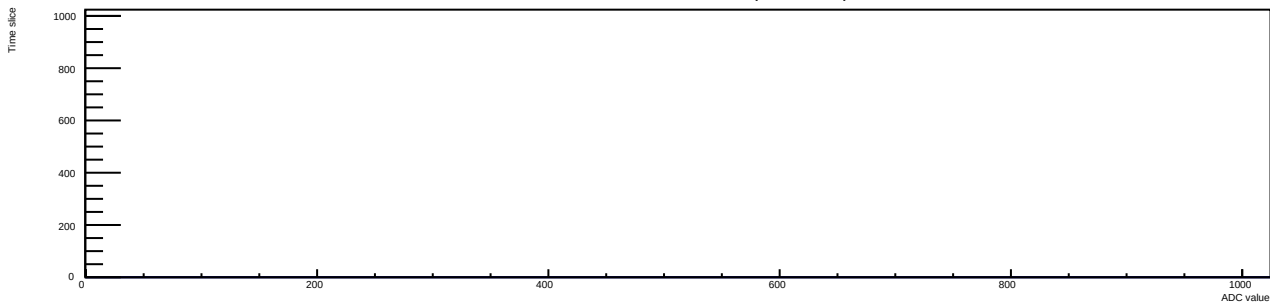
Run 36523 Evt 1000 Time mcm 2 chip 6 chan 6 pulses



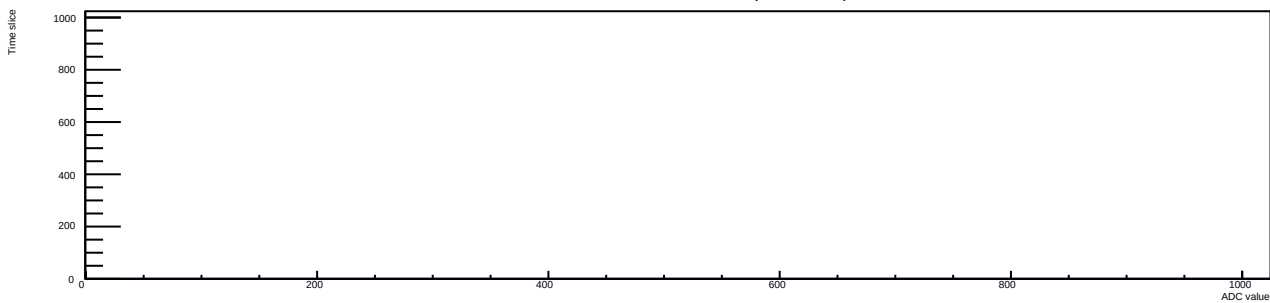
Run 36523 Evt 1000 Time mcm 2 chip 6 chan 7 pulses



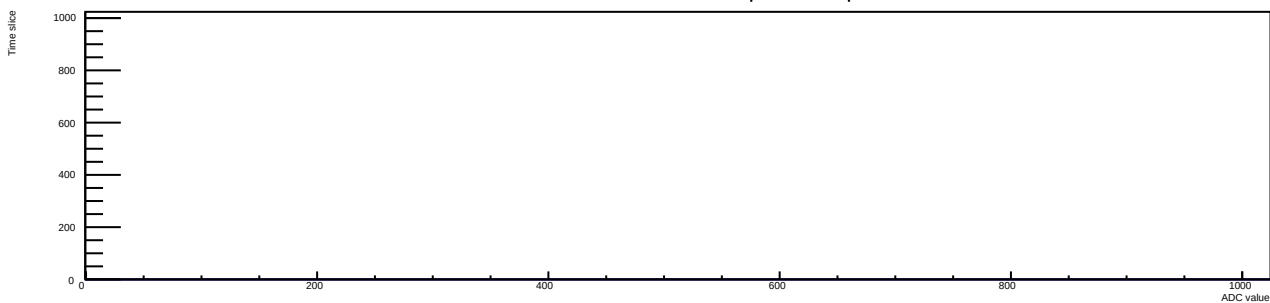
Run 36523 Evt 1000 Time mcm 2 chip 6 chan 8 pulses



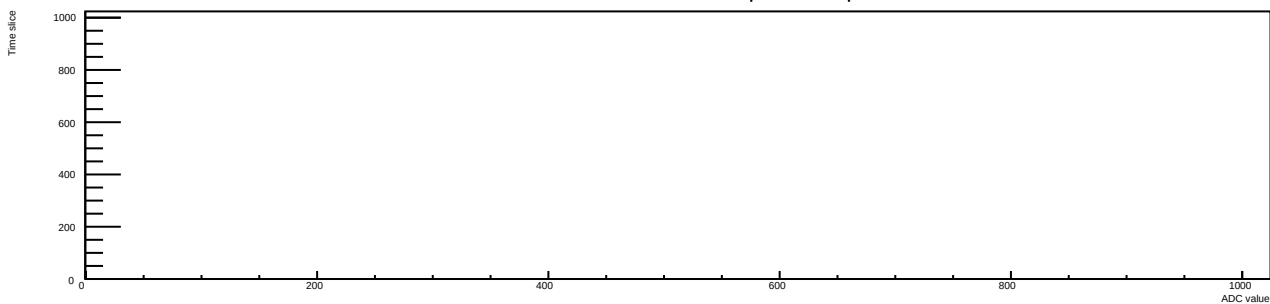
Run 36523 Evt 1000 Time mcm 2 chip 6 chan 9 pulses



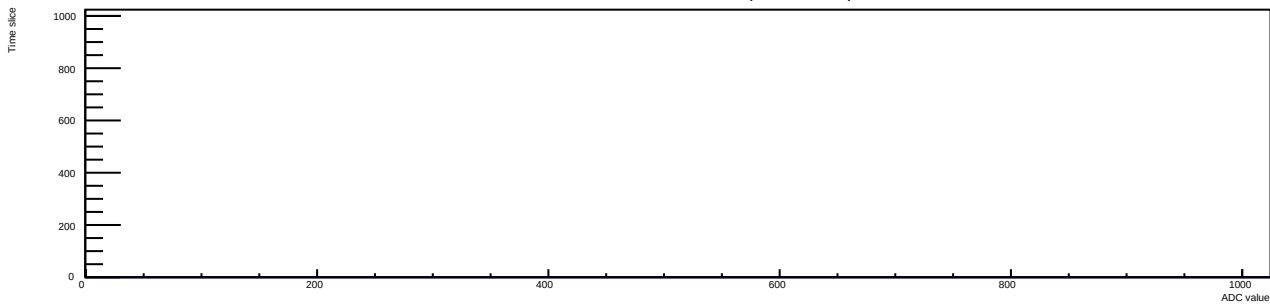
Run 36523 Evt 1000 Time mcm 2 chip 6 chan 10 pulses



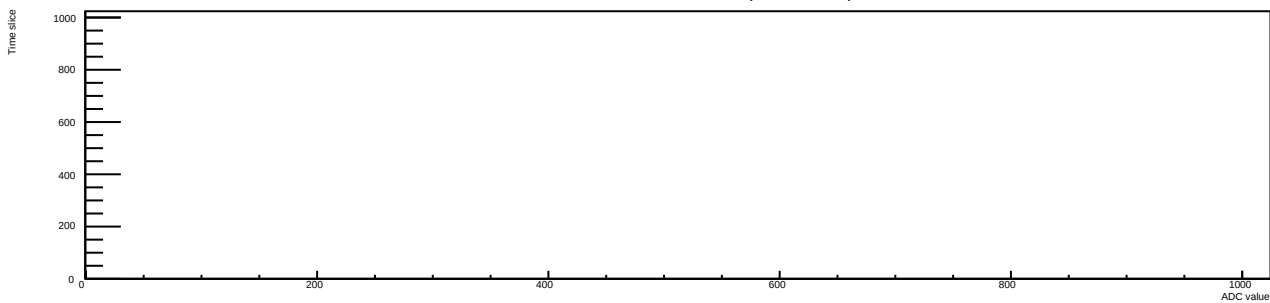
Run 36523 Evt 1000 Time mcm 2 chip 6 chan 11 pulses



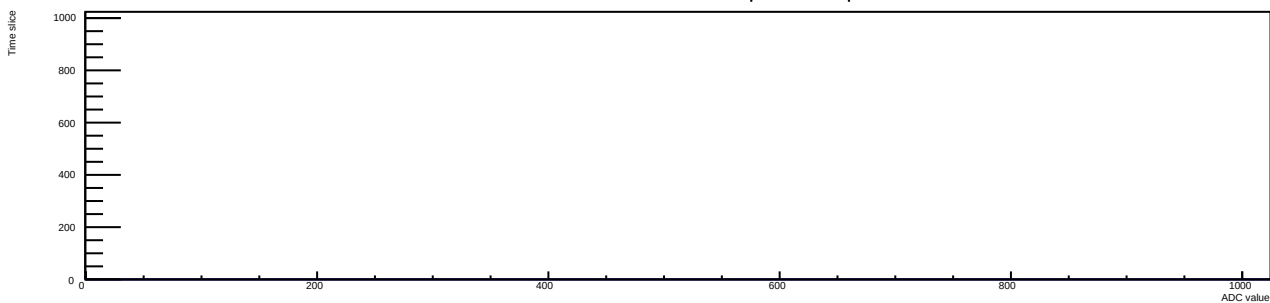
Run 36523 Evt 1000 Time mcm 2 chip 6 chan 12 pulses



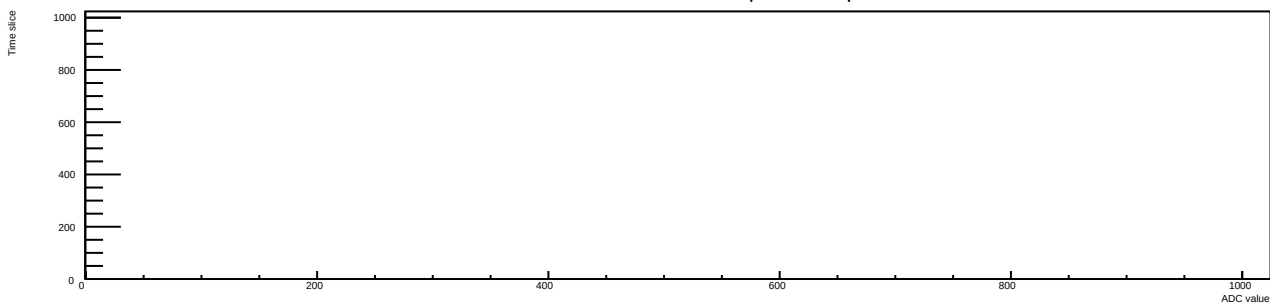
Run 36523 Evt 1000 Time mcm 2 chip 6 chan 13 pulses



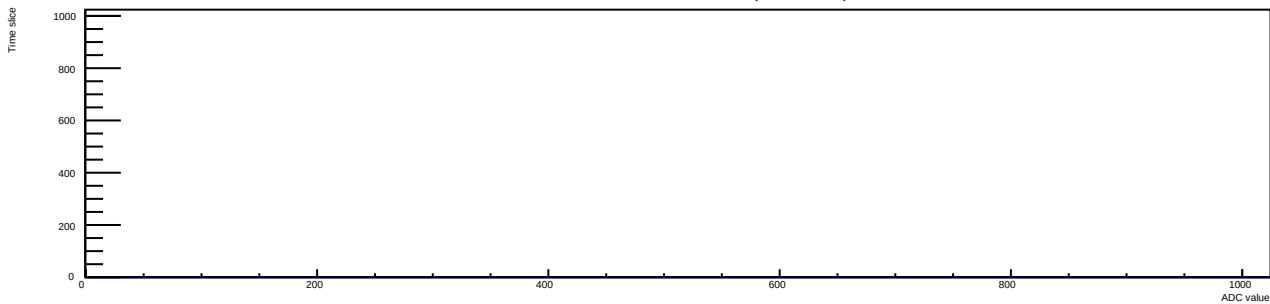
Run 36523 Evt 1000 Time mcm 2 chip 6 chan 14 pulses



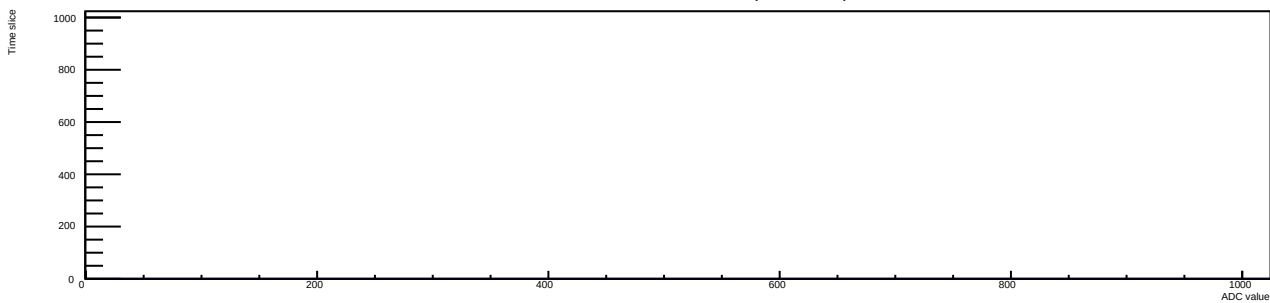
Run 36523 Evt 1000 Time mcm 2 chip 6 chan 15 pulses



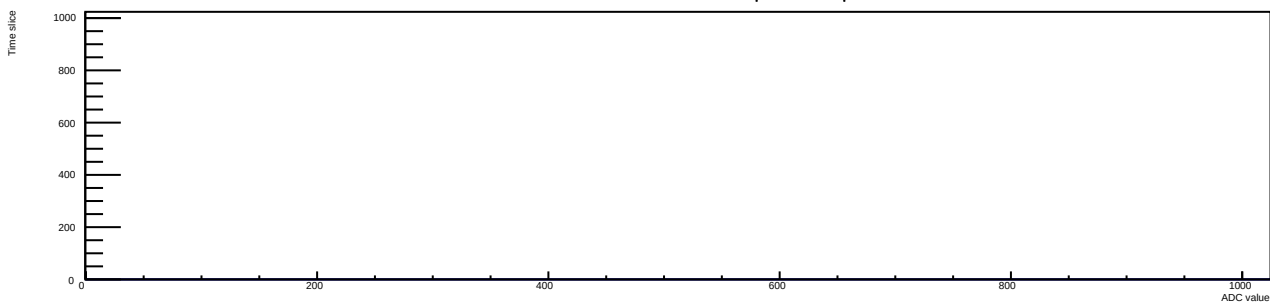
Run 36523 Evt 1000 Time mcm 2 chip 7 chan 0 pulses



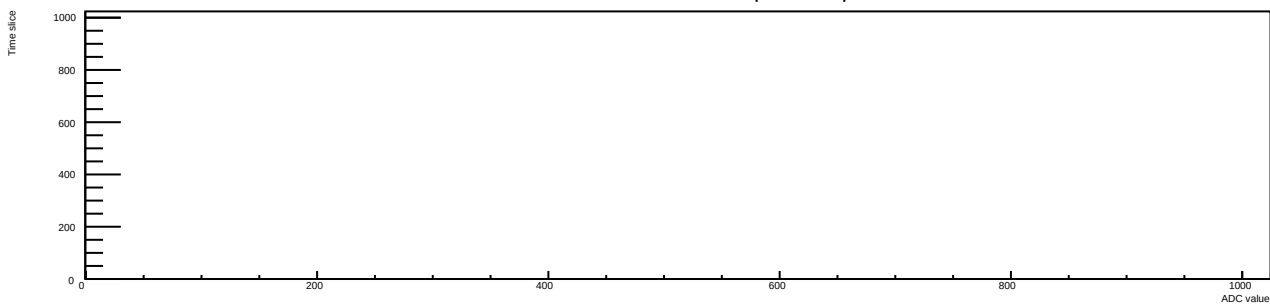
Run 36523 Evt 1000 Time mcm 2 chip 7 chan 1 pulses



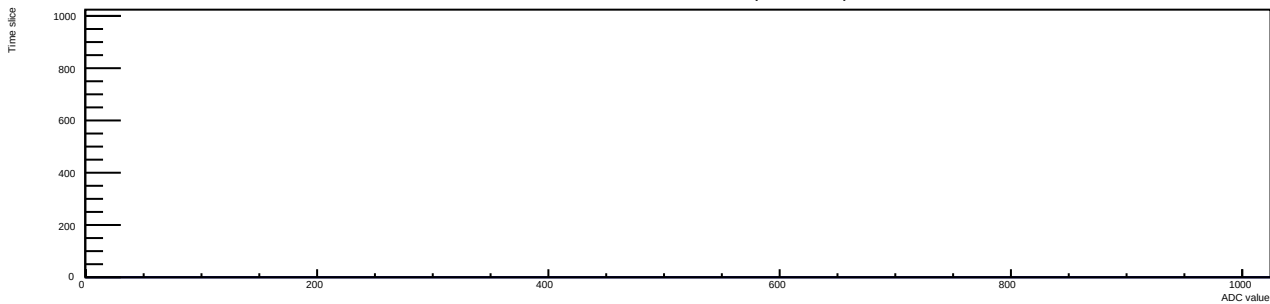
Run 36523 Evt 1000 Time mcm 2 chip 7 chan 2 pulses



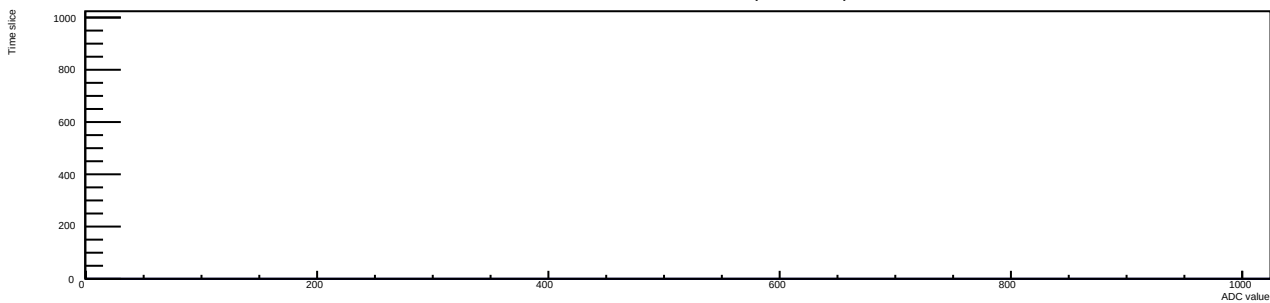
Run 36523 Evt 1000 Time mcm 2 chip 7 chan 3 pulses



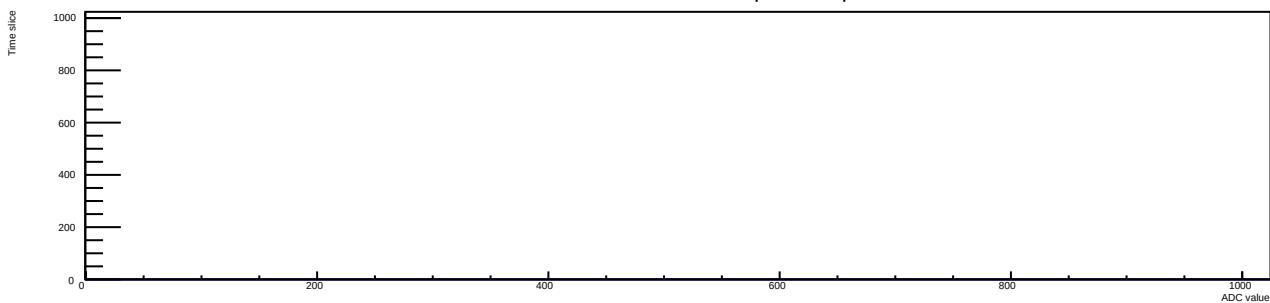
Run 36523 Evt 1000 Time mcm 2 chip 7 chan 4 pulses



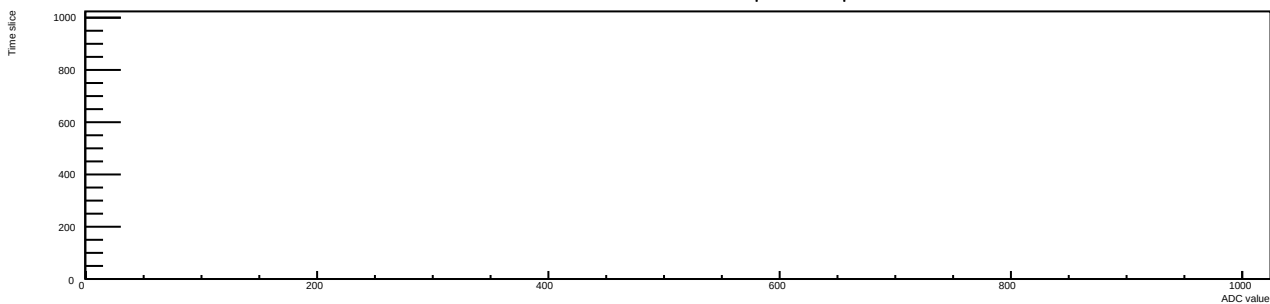
Run 36523 Evt 1000 Time mcm 2 chip 7 chan 5 pulses



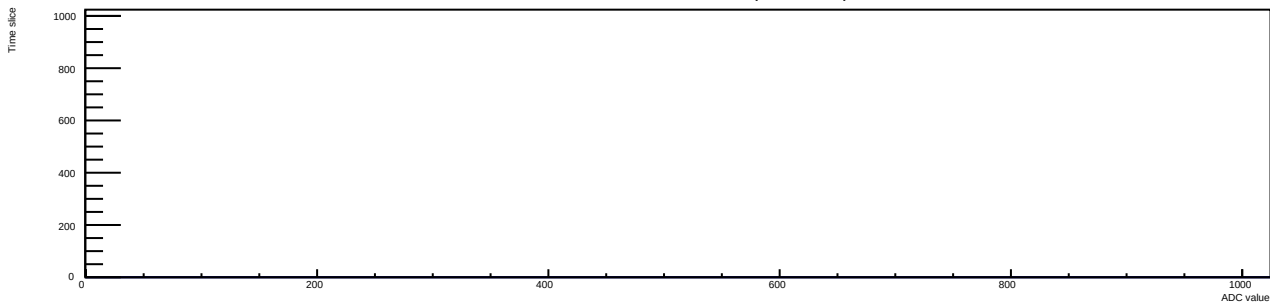
Run 36523 Evt 1000 Time mcm 2 chip 7 chan 6 pulses



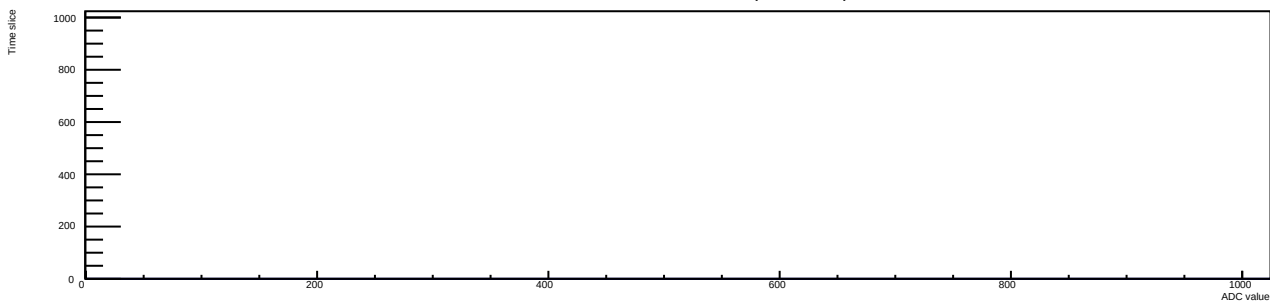
Run 36523 Evt 1000 Time mcm 2 chip 7 chan 7 pulses



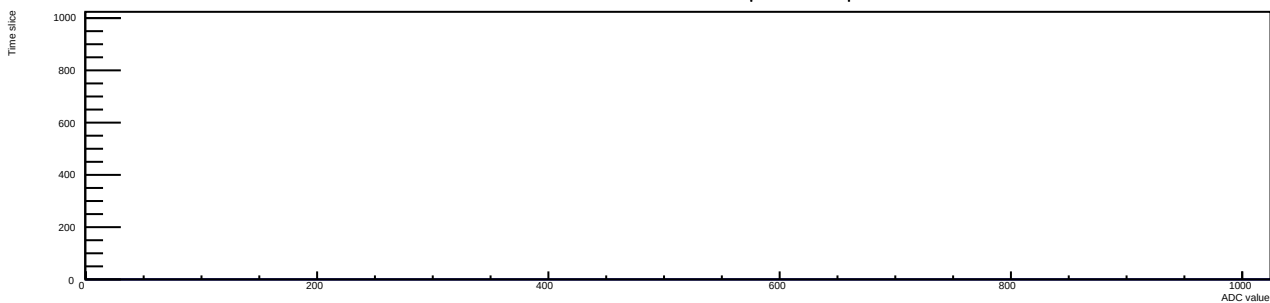
Run 36523 Evt 1000 Time mcm 2 chip 7 chan 8 pulses



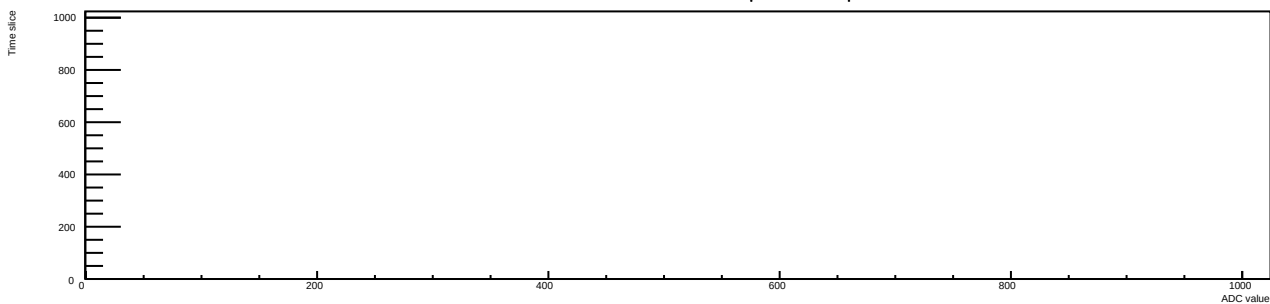
Run 36523 Evt 1000 Time mcm 2 chip 7 chan 9 pulses



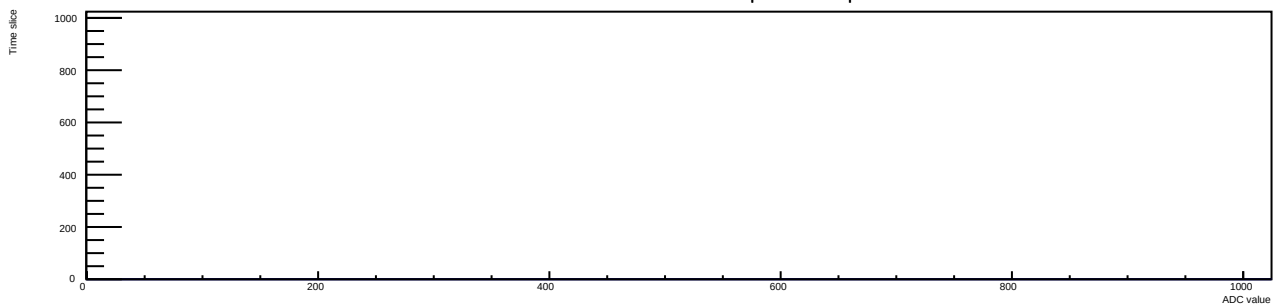
Run 36523 Evt 1000 Time mcm 2 chip 7 chan 10 pulses



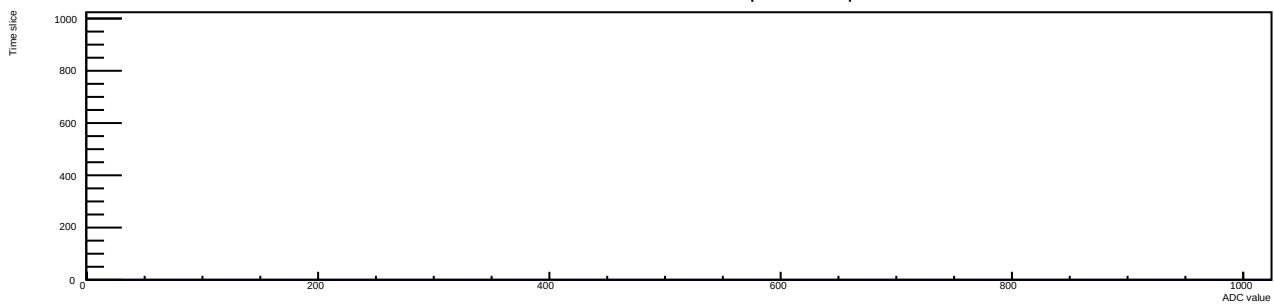
Run 36523 Evt 1000 Time mcm 2 chip 7 chan 11 pulses



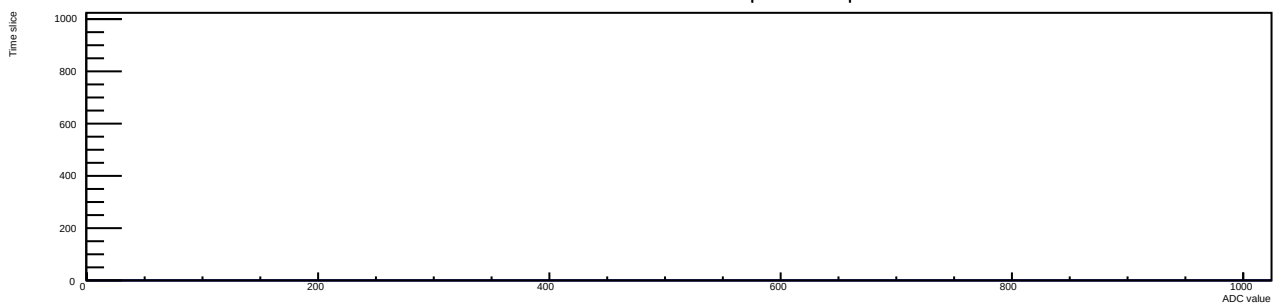
Run 36523 Evt 1000 Time mcm 2 chip 7 chan 12 pulses



Run 36523 Evt 1000 Time mcm 2 chip 7 chan 13 pulses



Run 36523 Evt 1000 Time mcm 2 chip 7 chan 14 pulses



Run 36523 Evt 1000 Time mcm 2 chip 7 chan 15 pulses

