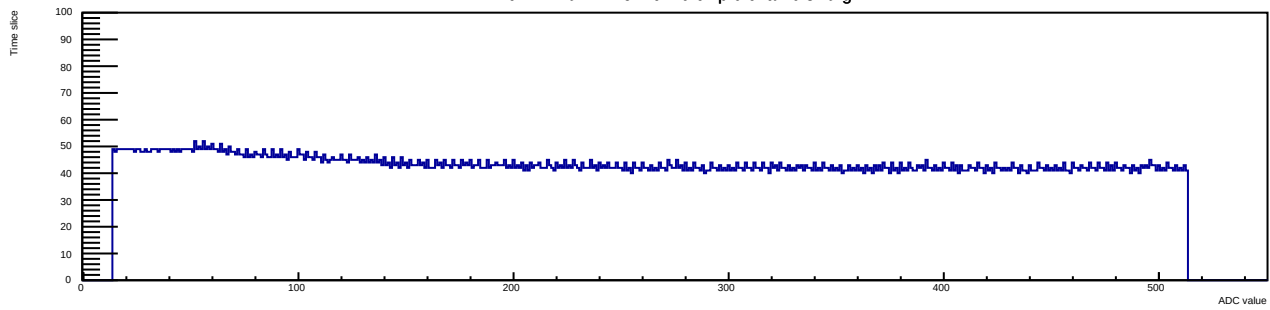
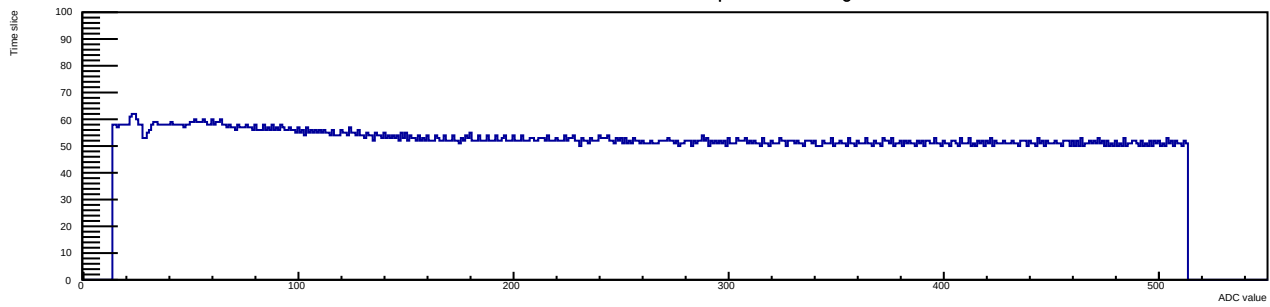


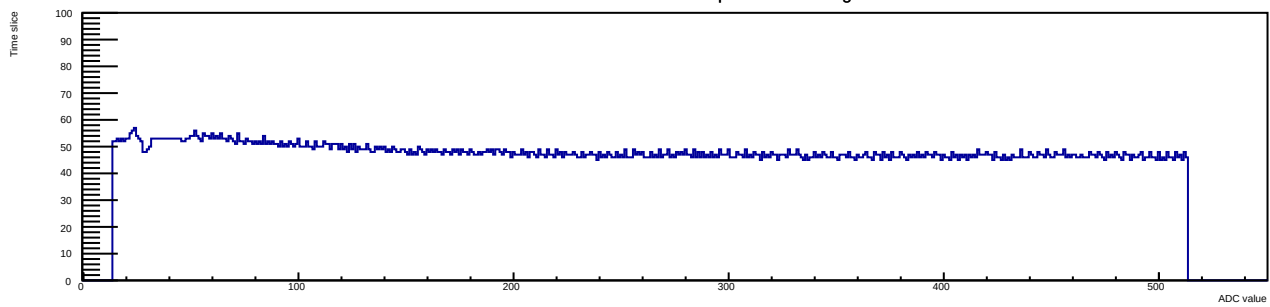
Run 7 Evt 2 Time mcm 0 chip 0 chan 0 swtrig



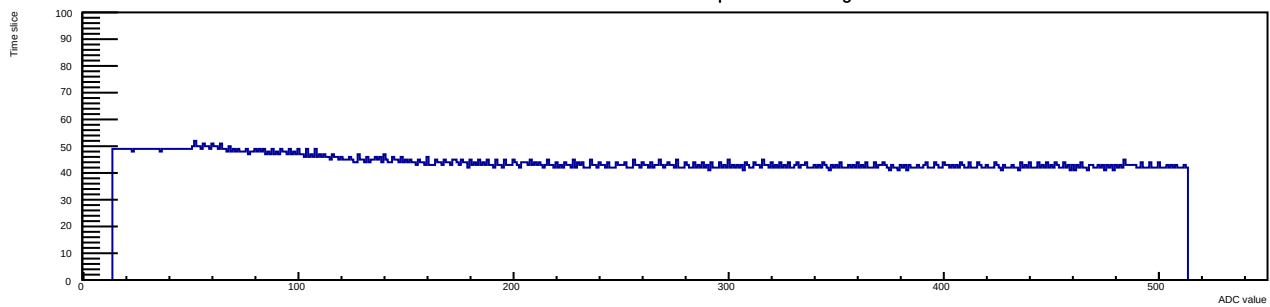
Run 7 Evt 2 Time mcm 0 chip 0 chan 1 swtrig



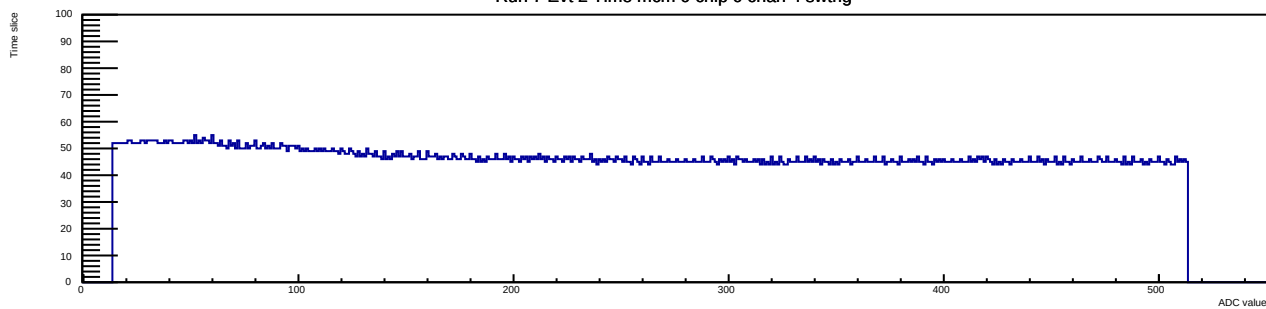
Run 7 Evt 2 Time mcm 0 chip 0 chan 2 swtrig



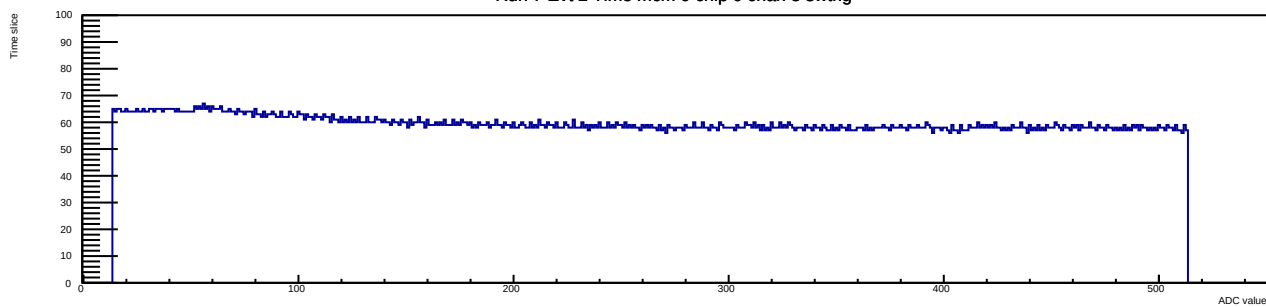
Run 7 Evt 2 Time mcm 0 chip 0 chan 3 swtrig



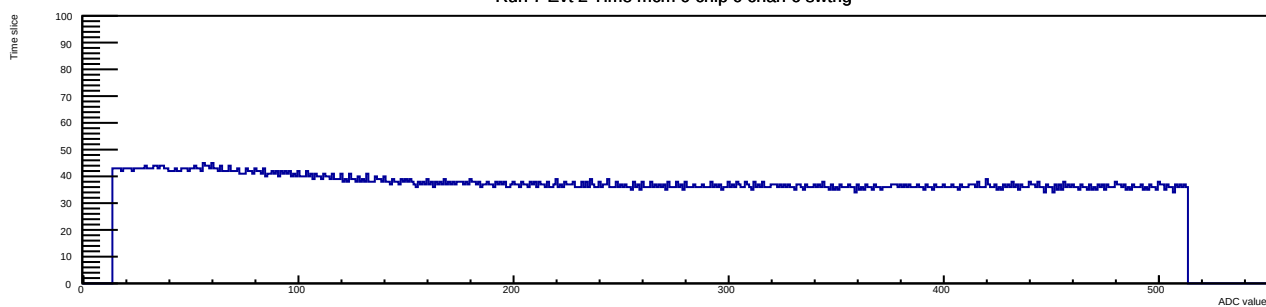
Run 7 Evt 2 Time mcm 0 chip 0 chan 4 swtrig



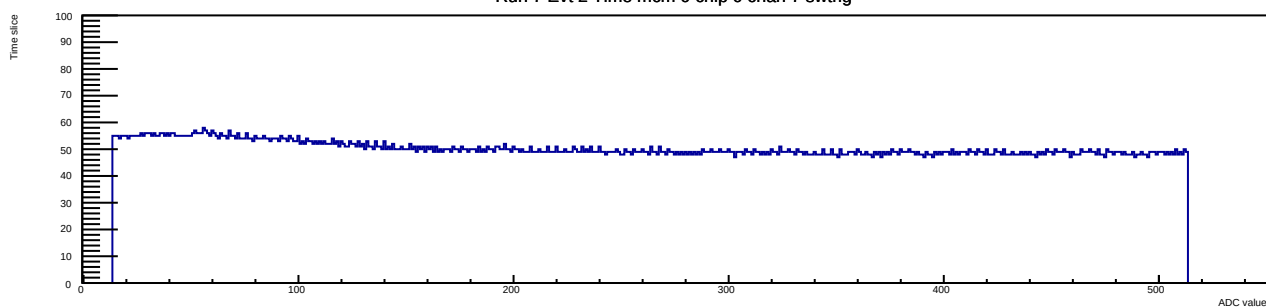
Run 7 Evt 2 Time mcm 0 chip 0 chan 5 swtrig



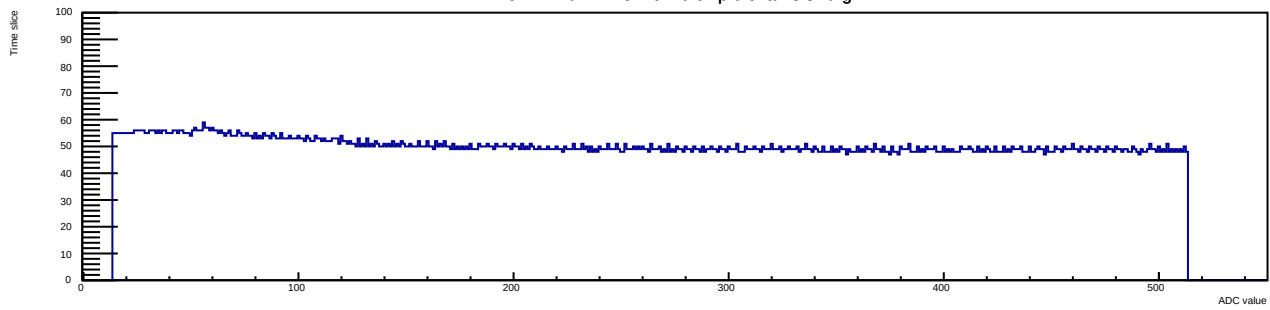
Run 7 Evt 2 Time mcm 0 chip 0 chan 6 swtrig



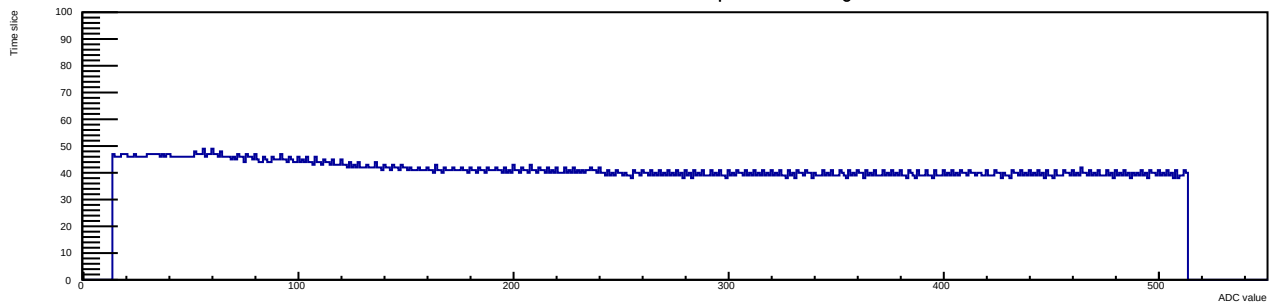
Run 7 Evt 2 Time mcm 0 chip 0 chan 7 swtrig



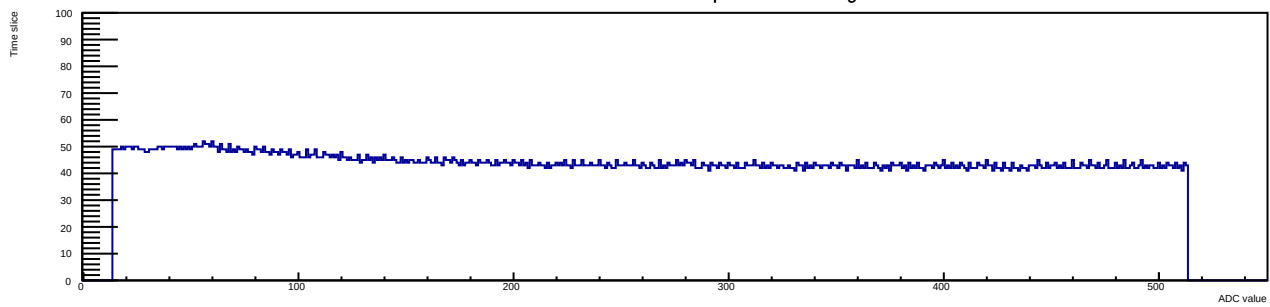
Run 7 Evt 2 Time mcm 0 chip 0 chan 8 swtrig



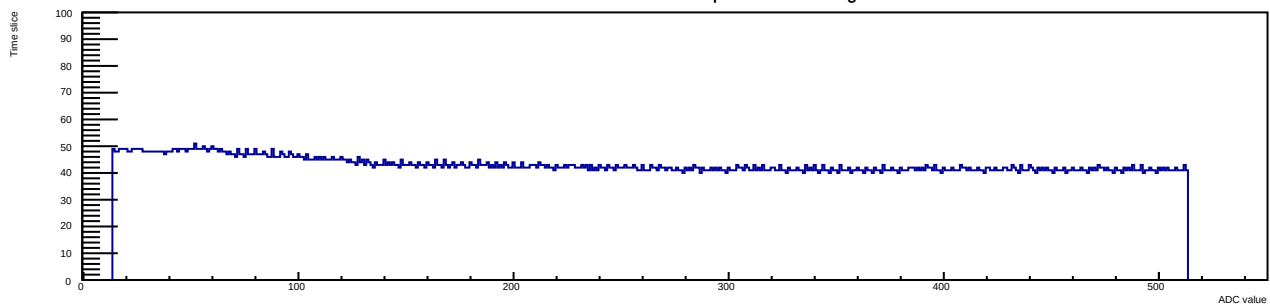
Run 7 Evt 2 Time mcm 0 chip 0 chan 9 swtrig



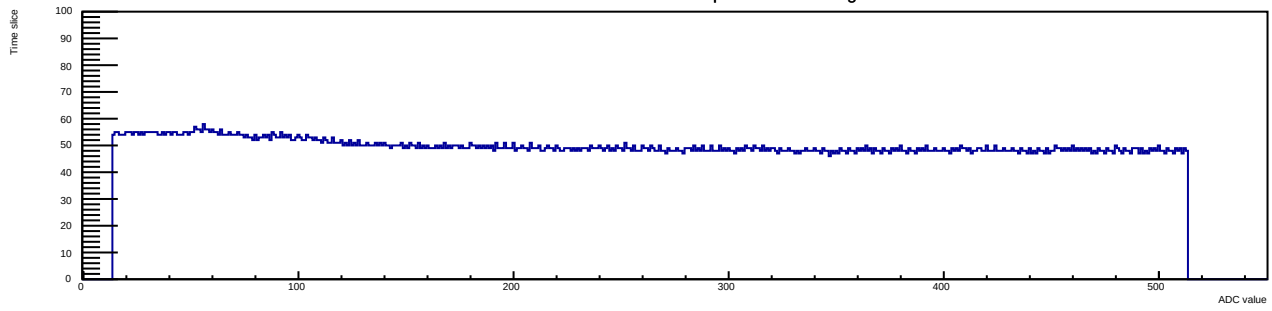
Run 7 Evt 2 Time mcm 0 chip 0 chan 10 swtrig



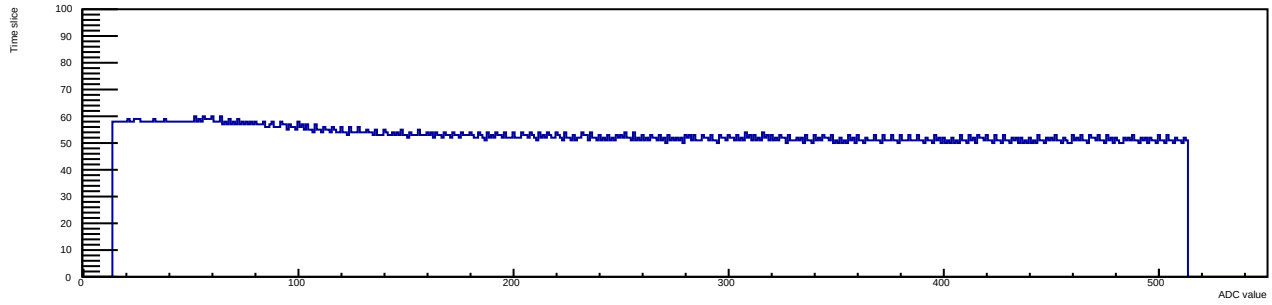
Run 7 Evt 2 Time mcm 0 chip 0 chan 11 swtrig



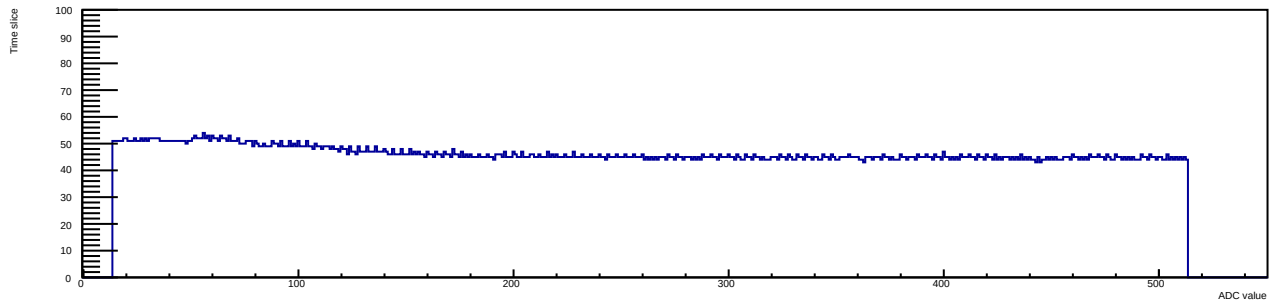
Run 7 Evt 2 Time mcm 0 chip 0 chan 12 swtrig



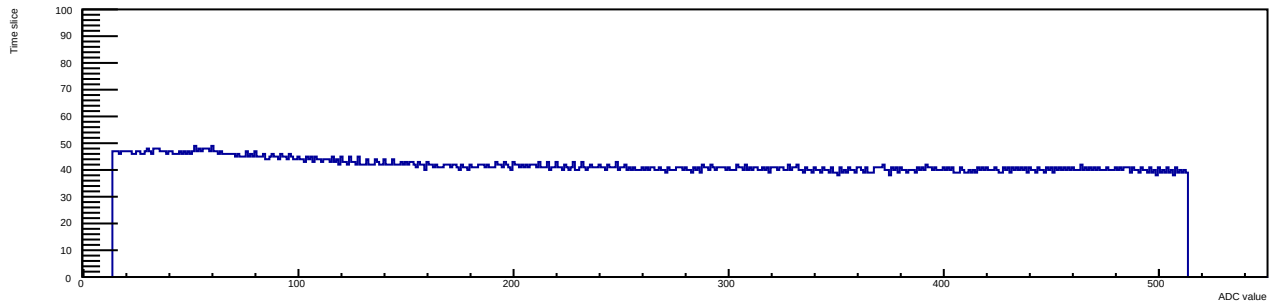
Run 7 Evt 2 Time mcm 0 chip 0 chan 13 swtrig



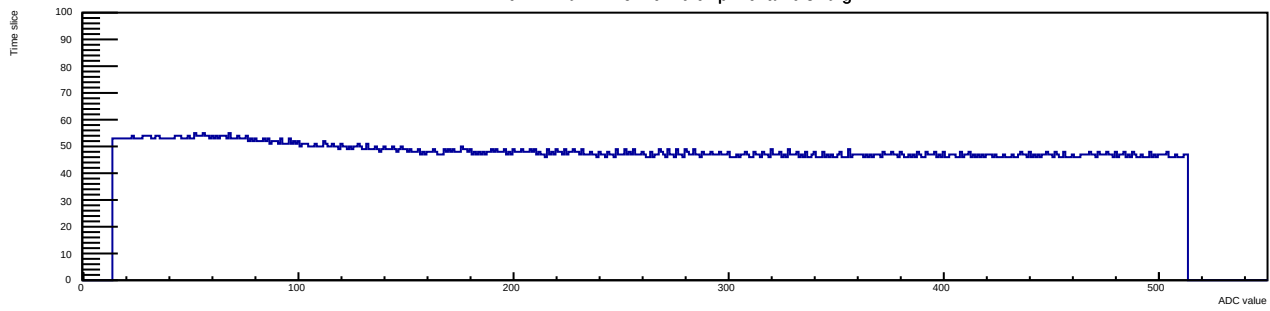
Run 7 Evt 2 Time mcm 0 chip 0 chan 14 swtrig



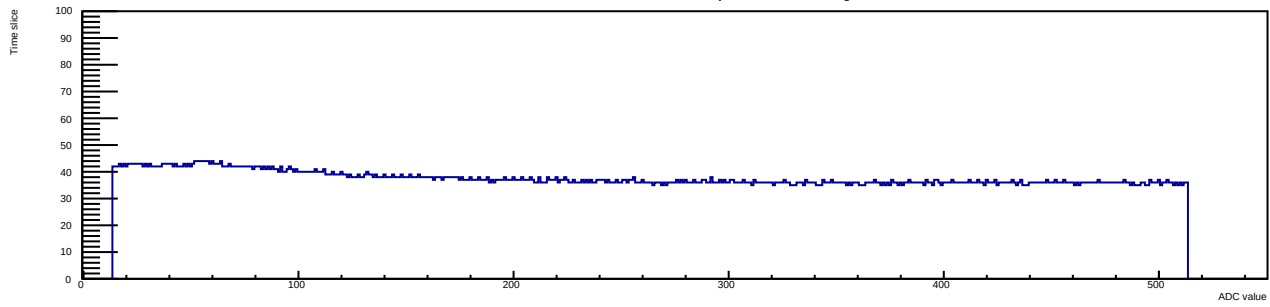
Run 7 Evt 2 Time mcm 0 chip 0 chan 15 swtrig



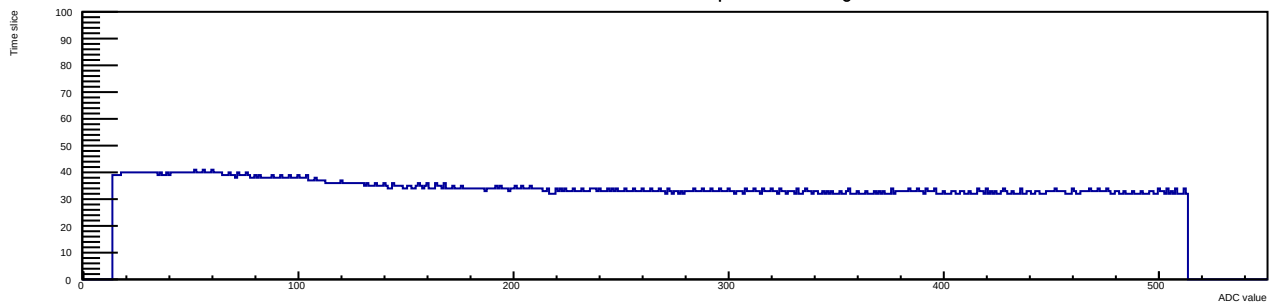
Run 7 Evt 2 Time mcm 0 chip 1 chan 0 swtrig



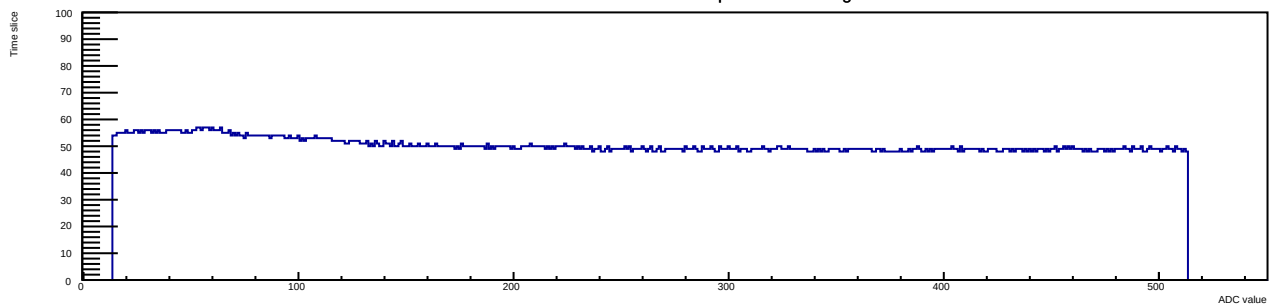
Run 7 Evt 2 Time mcm 0 chip 1 chan 1 swtrig



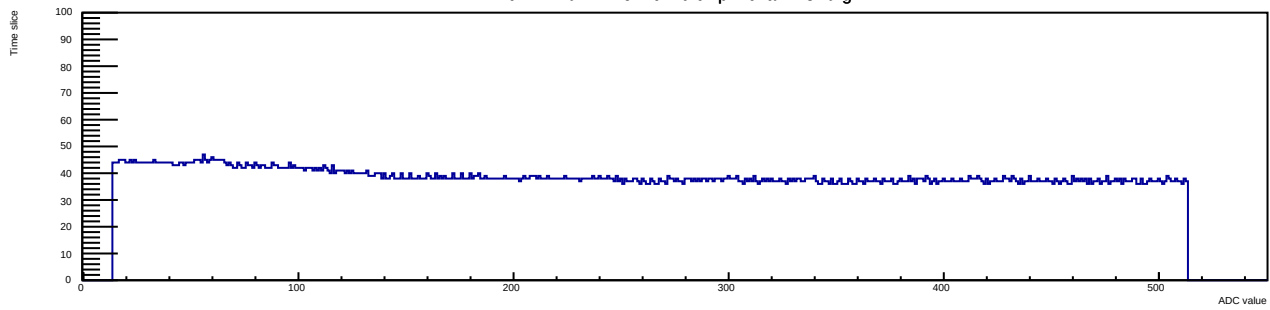
Run 7 Evt 2 Time mcm 0 chip 1 chan 2 swtrig



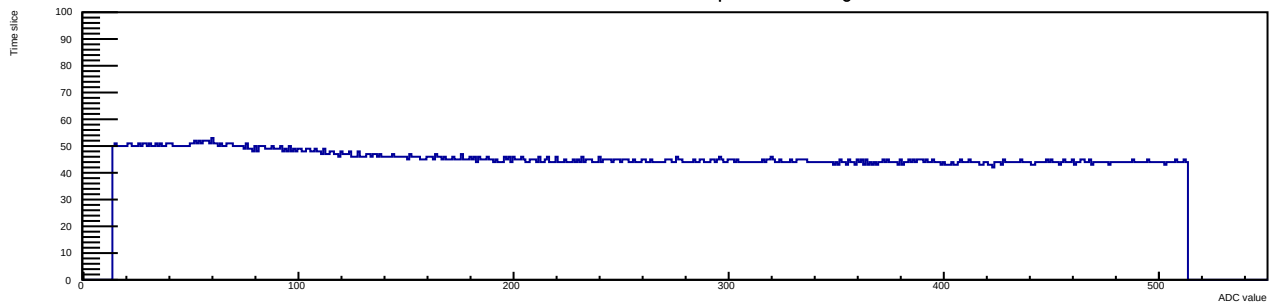
Run 7 Evt 2 Time mcm 0 chip 1 chan 3 swtrig



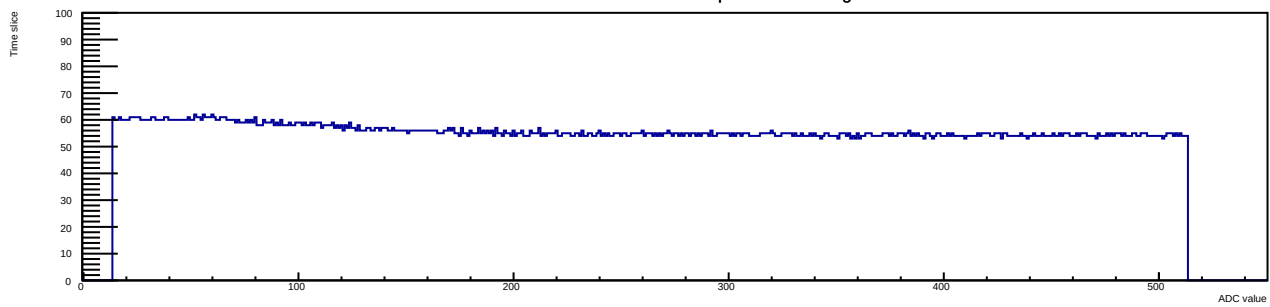
Run 7 Evt 2 Time mcm 0 chip 1 chan 4 swtrig



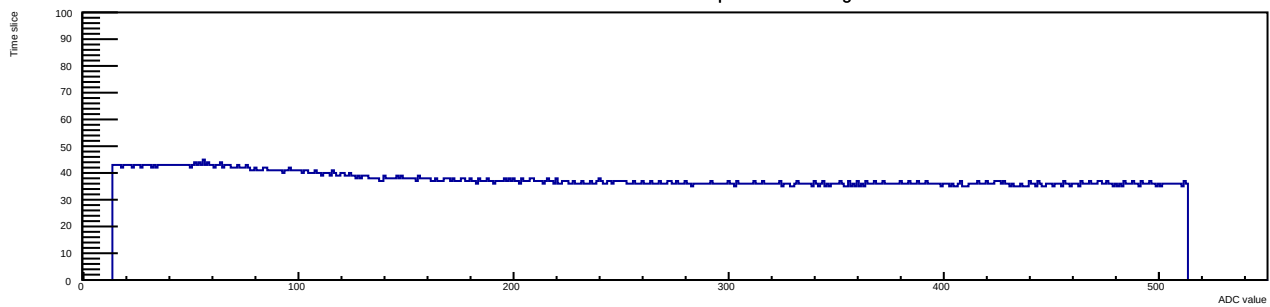
Run 7 Evt 2 Time mcm 0 chip 1 chan 5 swtrig



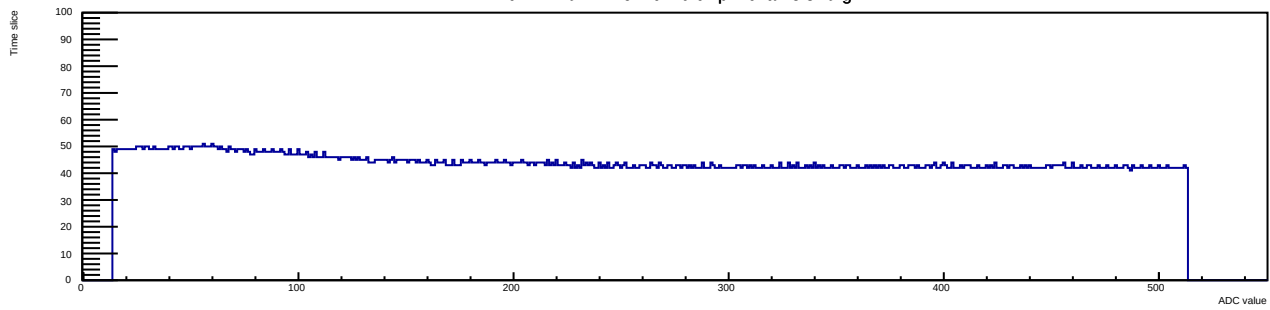
Run 7 Evt 2 Time mcm 0 chip 1 chan 6 swtrig



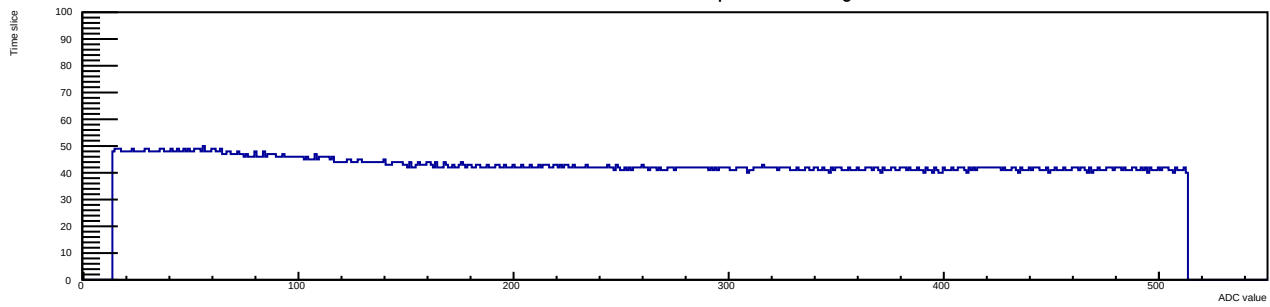
Run 7 Evt 2 Time mcm 0 chip 1 chan 7 swtrig



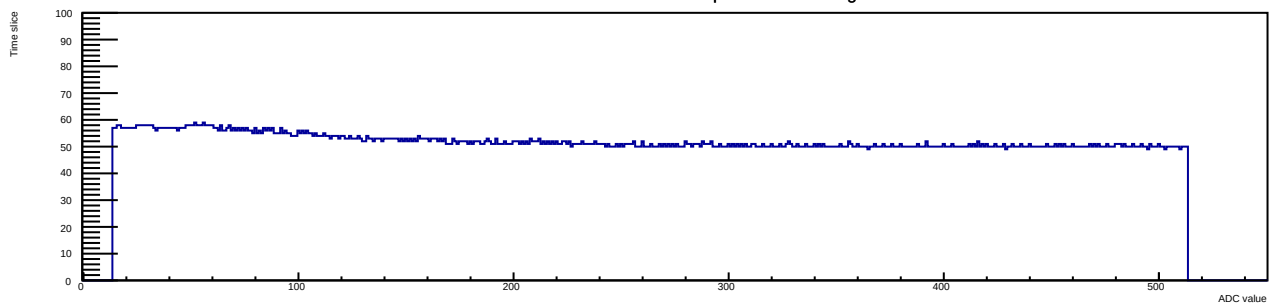
Run 7 Evt 2 Time mcm 0 chip 1 chan 8 swtrig



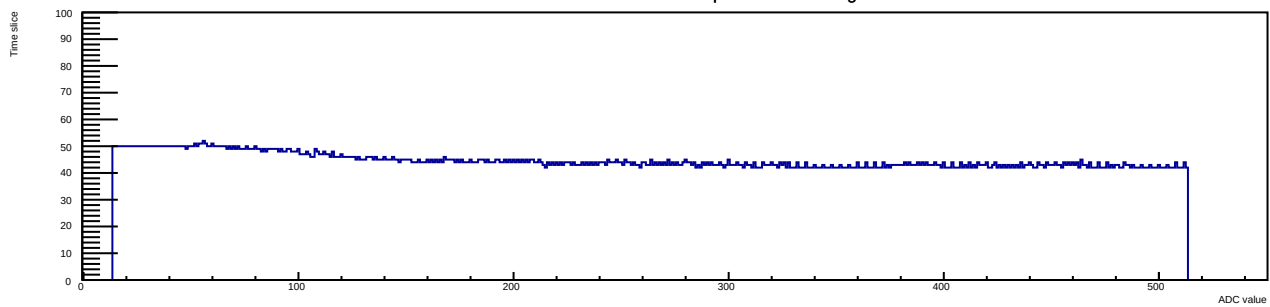
Run 7 Evt 2 Time mcm 0 chip 1 chan 9 swtrig



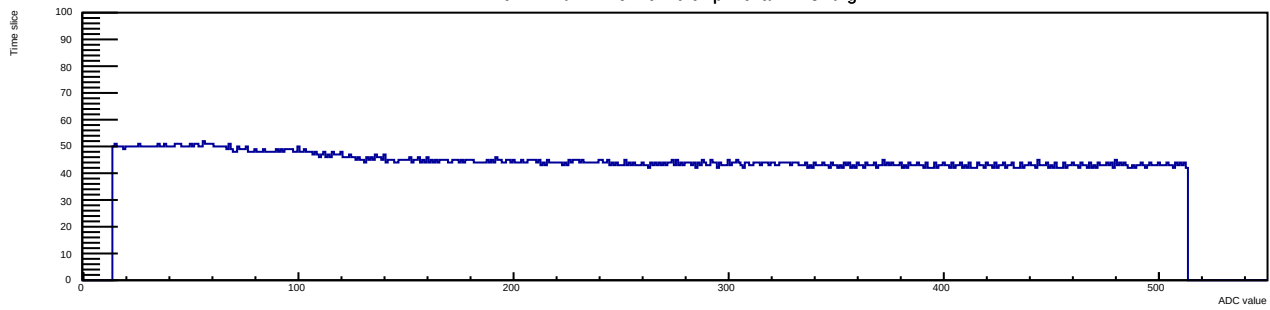
Run 7 Evt 2 Time mcm 0 chip 1 chan 10 swtrig



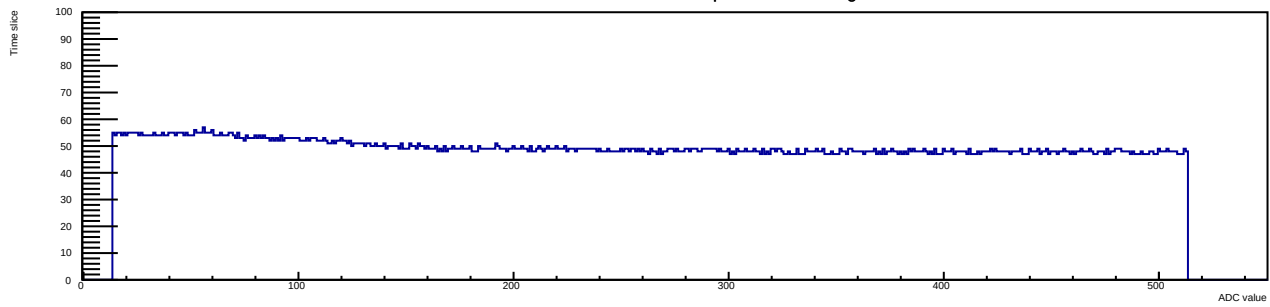
Run 7 Evt 2 Time mcm 0 chip 1 chan 11 swtrig



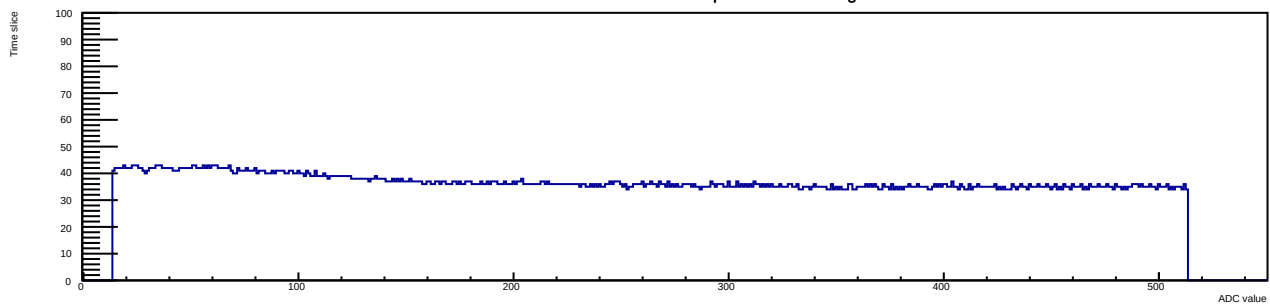
Run 7 Evt 2 Time mcm 0 chip 1 chan 12 swtrig



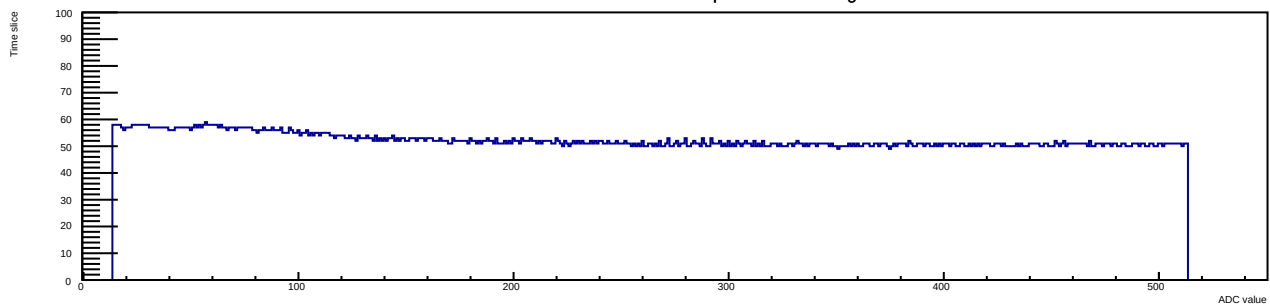
Run 7 Evt 2 Time mcm 0 chip 1 chan 13 swtrig



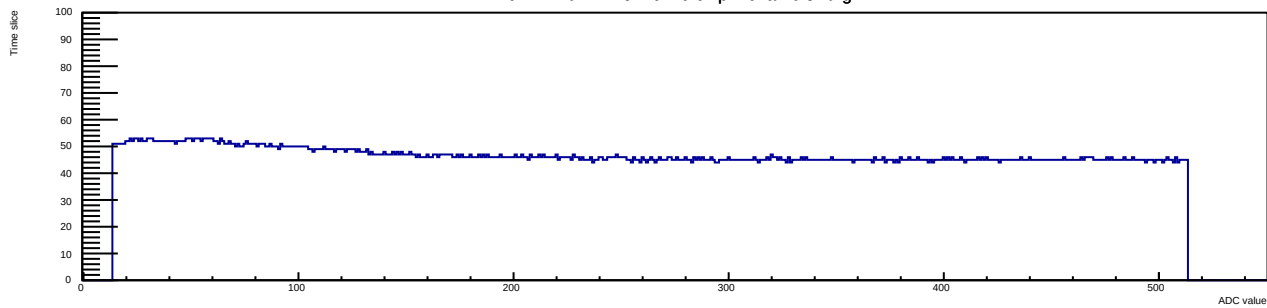
Run 7 Evt 2 Time mcm 0 chip 1 chan 14 swtrig



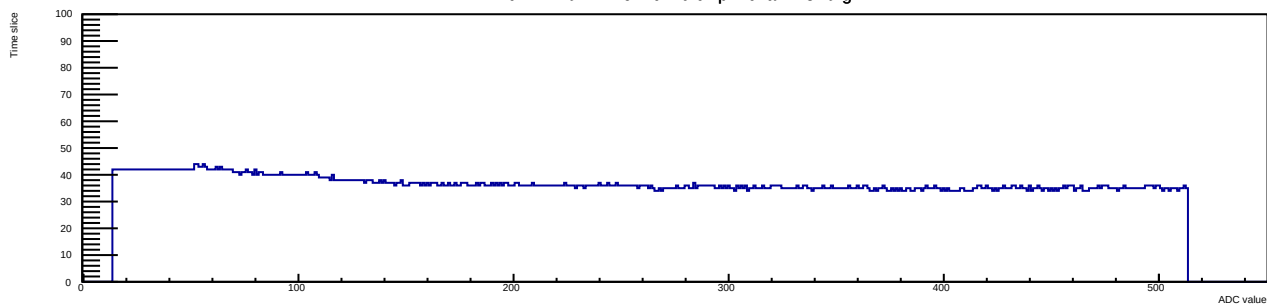
Run 7 Evt 2 Time mcm 0 chip 1 chan 15 swtrig



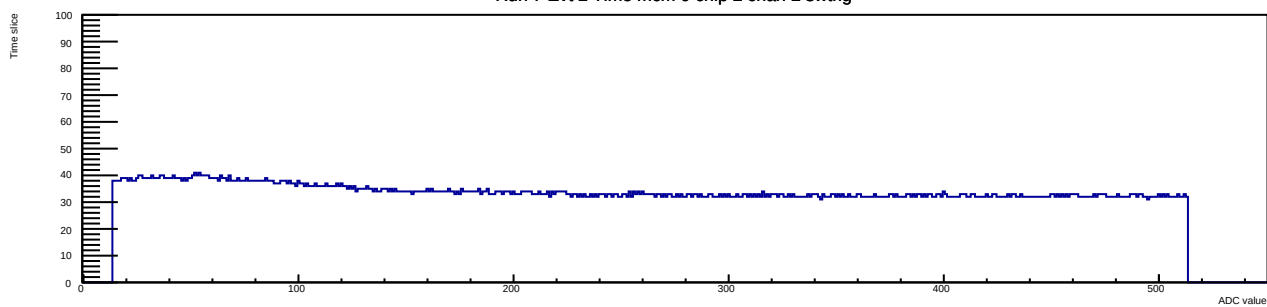
Run 7 Evt 2 Time mcm 0 chip 2 chan 0 swtrig



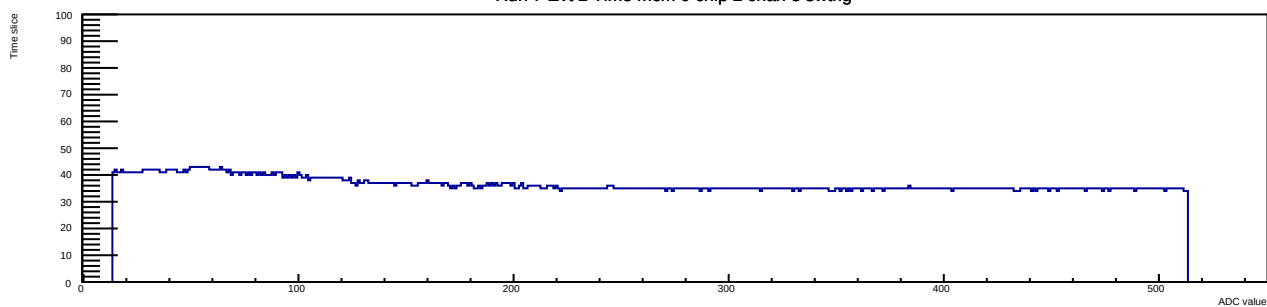
Run 7 Evt 2 Time mcm 0 chip 2 chan 1 swtrig



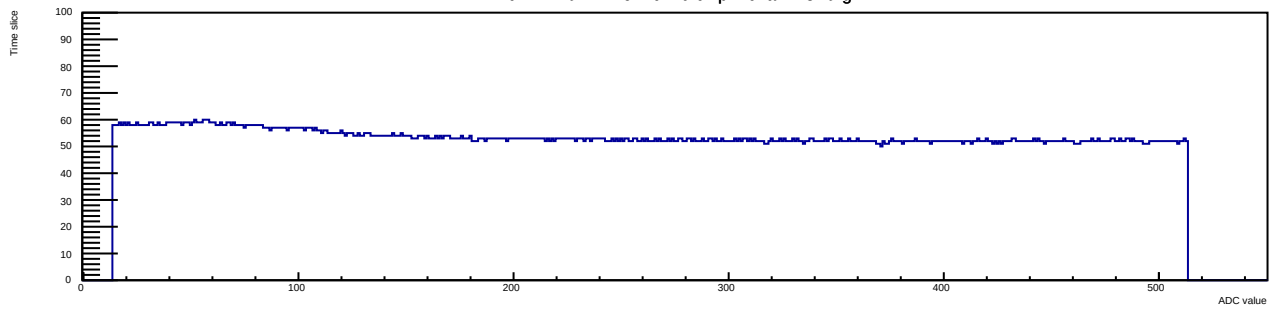
Run 7 Evt 2 Time mcm 0 chip 2 chan 2 swtrig



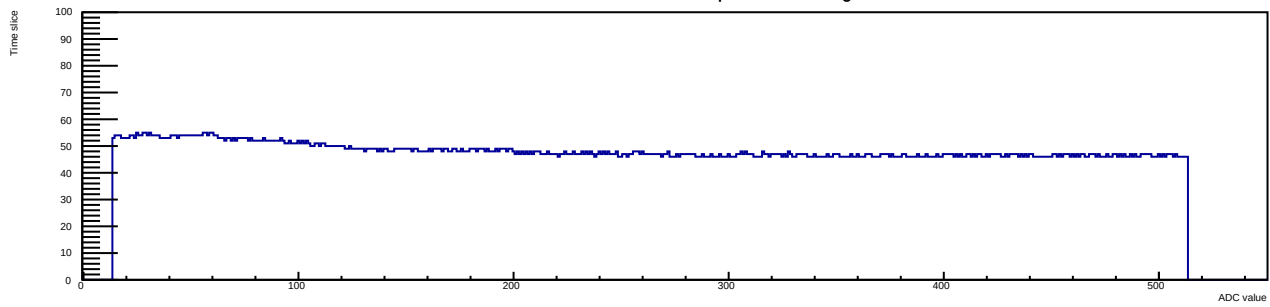
Run 7 Evt 2 Time mcm 0 chip 2 chan 3 swtrig



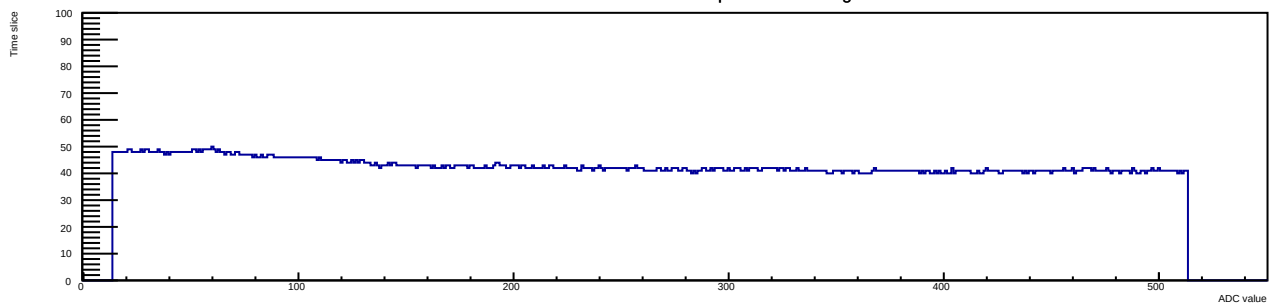
Run 7 Evt 2 Time mcm 0 chip 2 chan 4 swtrig



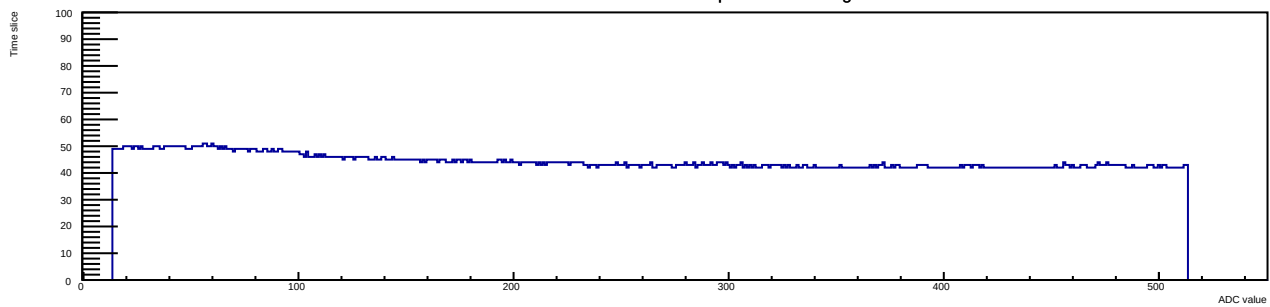
Run 7 Evt 2 Time mcm 0 chip 2 chan 5 swtrig



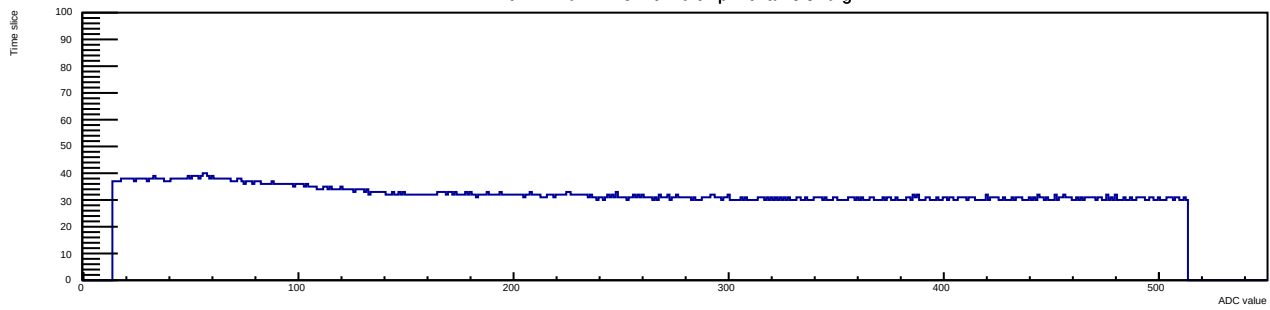
Run 7 Evt 2 Time mcm 0 chip 2 chan 6 swtrig



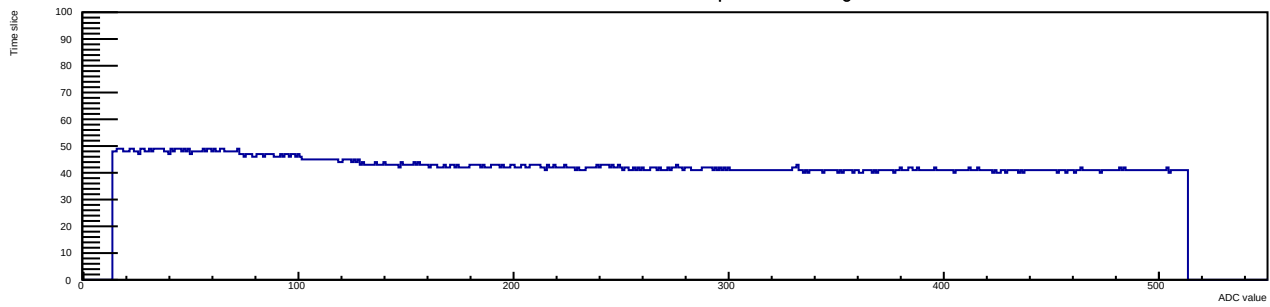
Run 7 Evt 2 Time mcm 0 chip 2 chan 7 swtrig



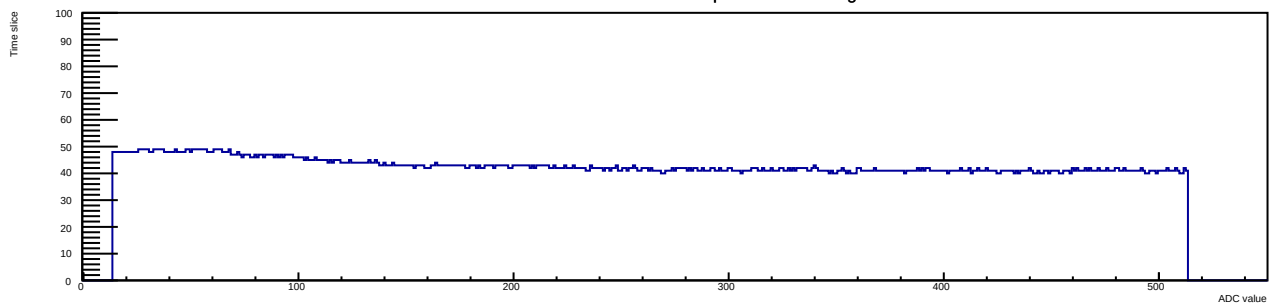
Run 7 Evt 2 Time mcm 0 chip 2 chan 8 swtrig



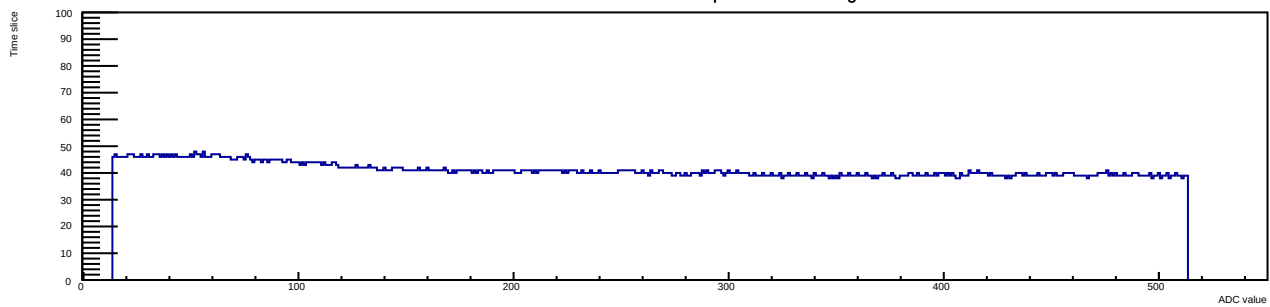
Run 7 Evt 2 Time mcm 0 chip 2 chan 9 swtrig



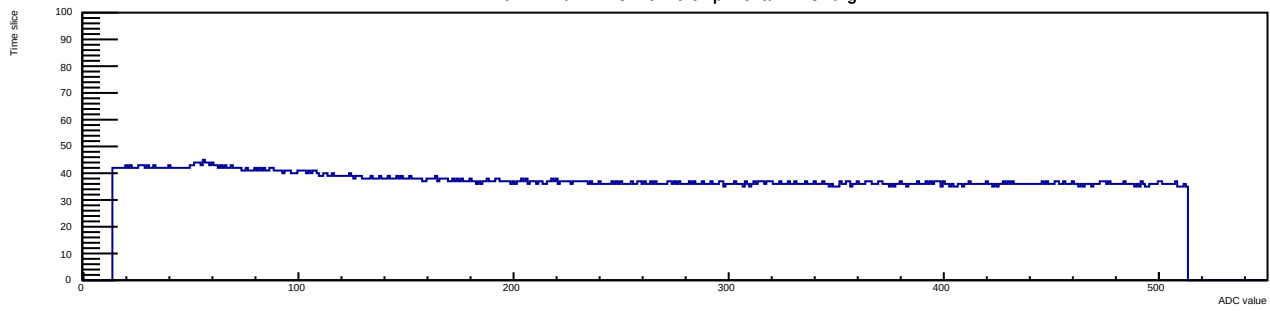
Run 7 Evt 2 Time mcm 0 chip 2 chan 10 swtrig



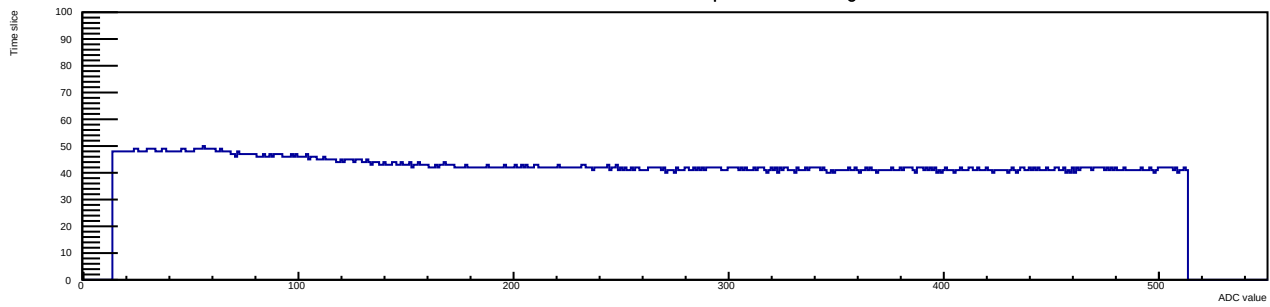
Run 7 Evt 2 Time mcm 0 chip 2 chan 11 swtrig



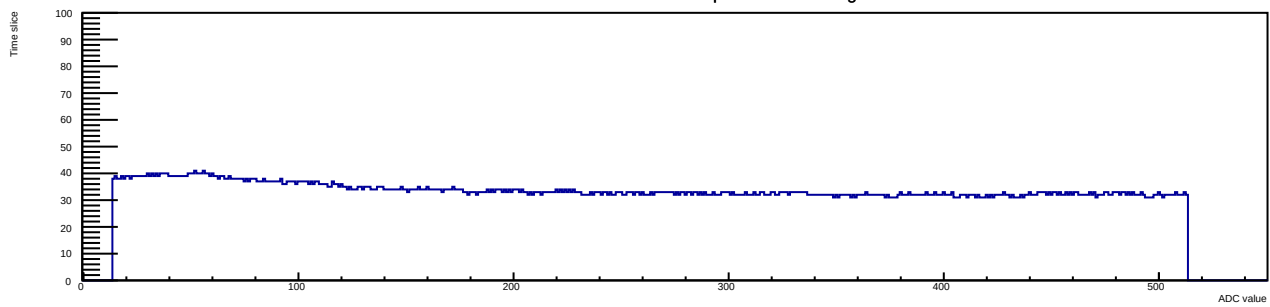
Run 7 Evt 2 Time mcm 0 chip 2 chan 12 swtrig



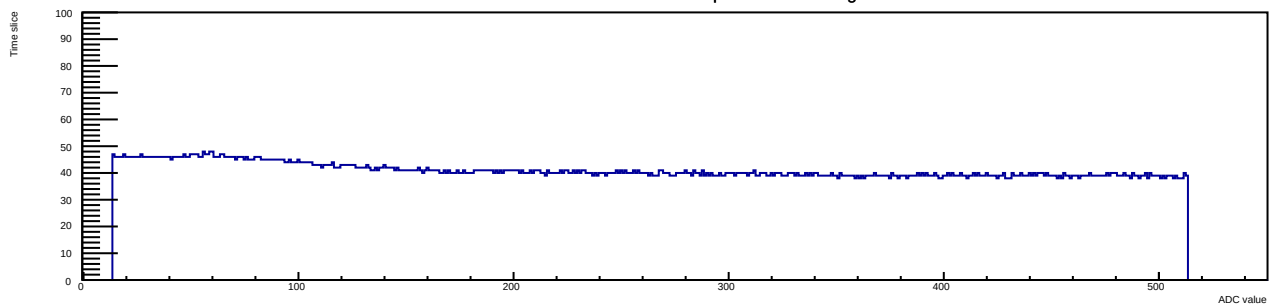
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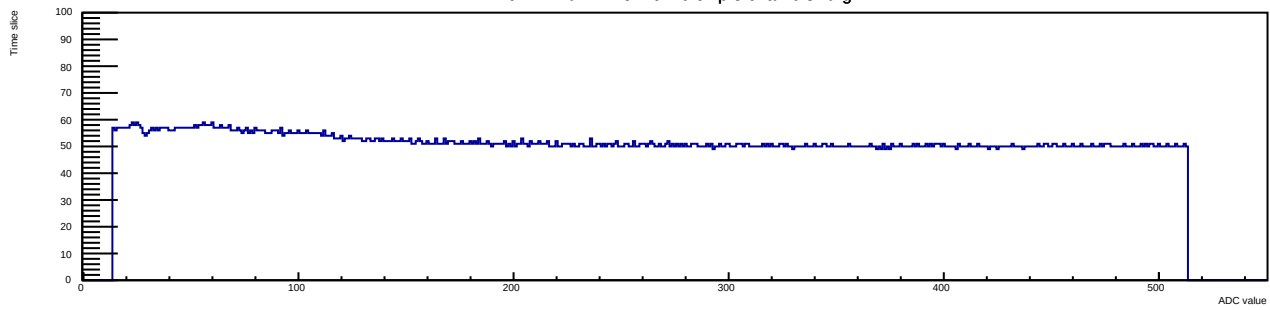
Run 7 Evt 2 Time mcm 0 chip 2 chan 14 swtrig



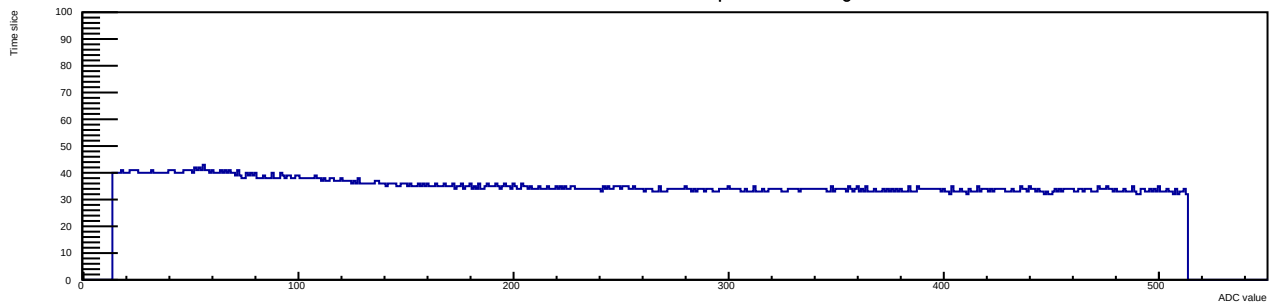
Run 7 Evt 2 Time mcm 0 chip 2 chan 15 swtrig



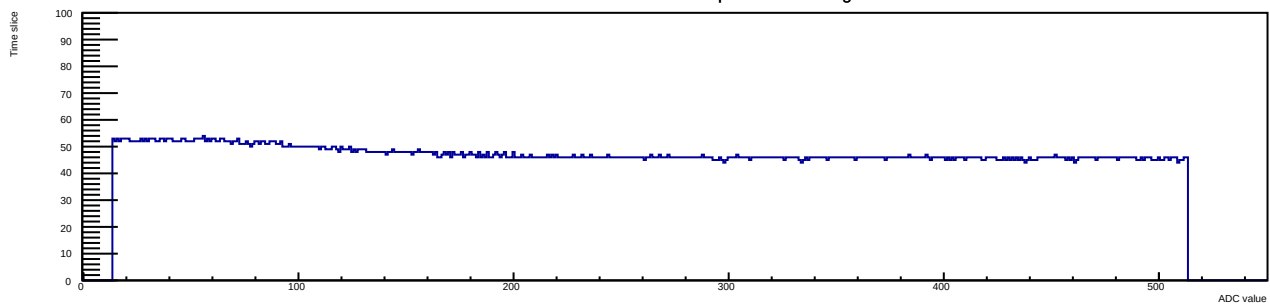
Run 7 Evt 2 Time mcm 0 chip 3 chan 0 swtrig



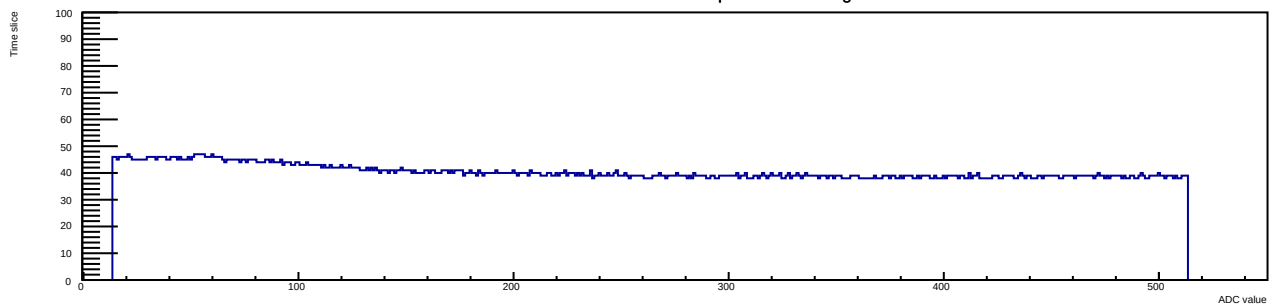
Run 7 Evt 2 Time mcm 0 chip 3 chan 1 swtrig



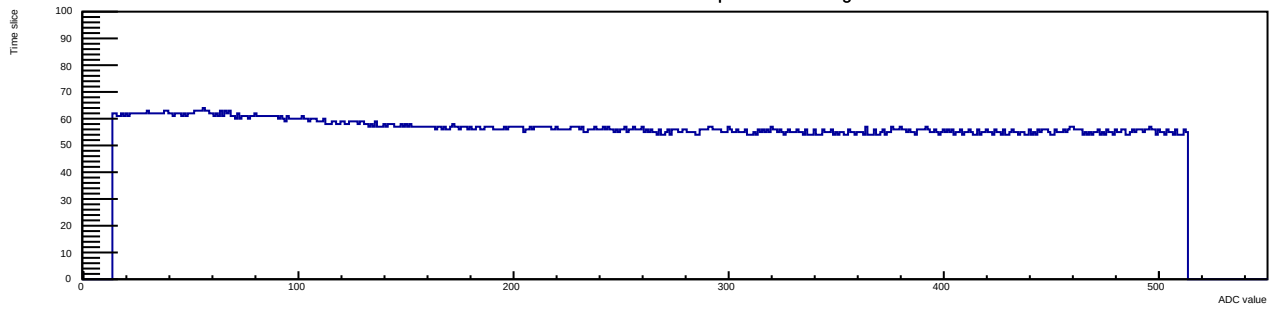
Run 7 Evt 2 Time mcm 0 chip 3 chan 2 swtrig



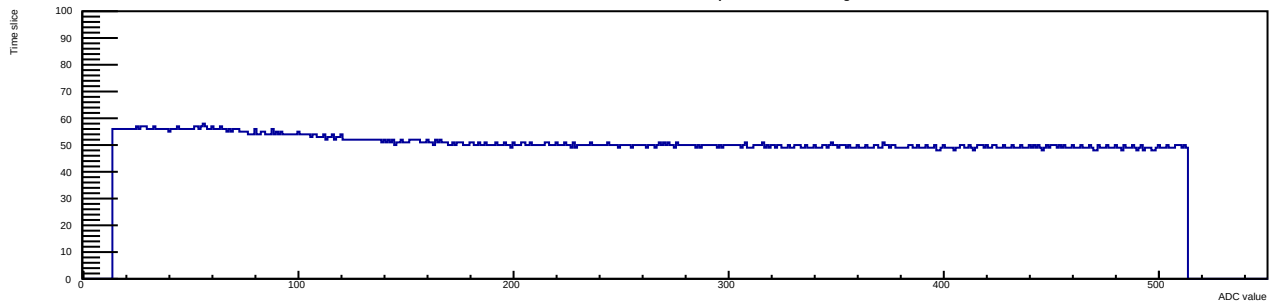
Run 7 Evt 2 Time mcm 0 chip 3 chan 3 swtrig



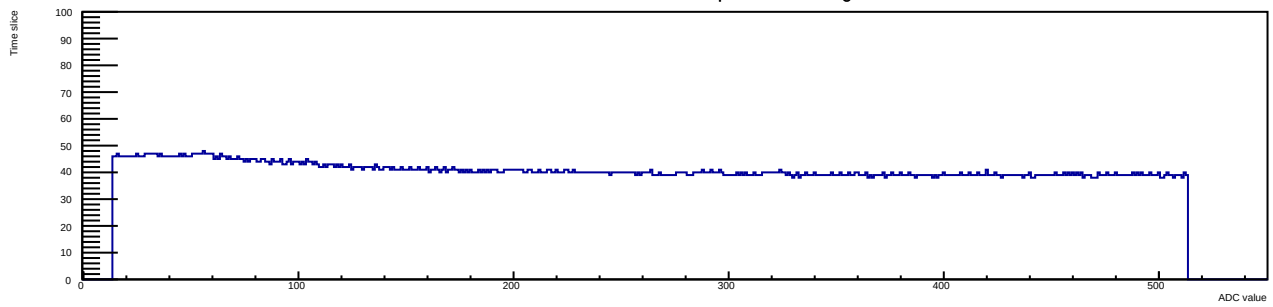
Run 7 Evt 2 Time mcm 0 chip 3 chan 4 swtrig



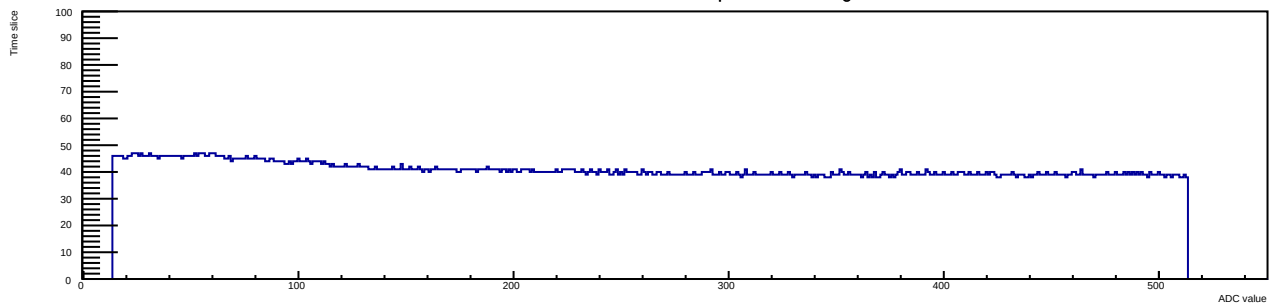
Run 7 Evt 2 Time mcm 0 chip 3 chan 5 swtrig



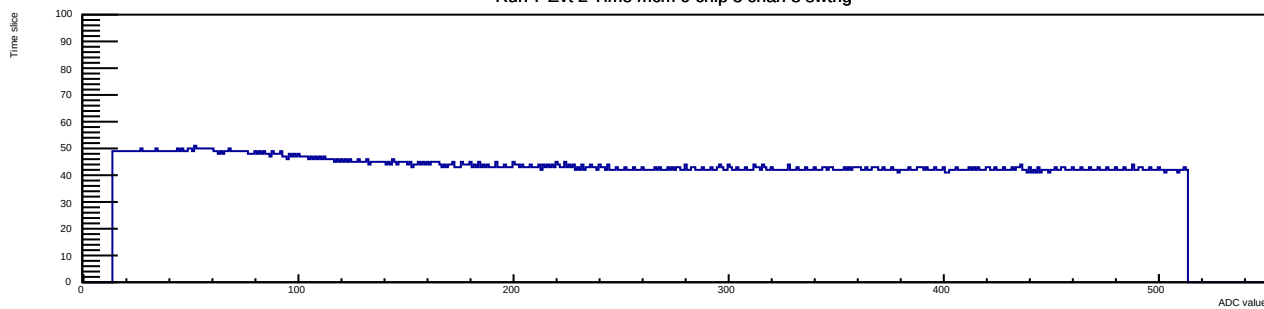
Run 7 Evt 2 Time mcm 0 chip 3 chan 6 swtrig



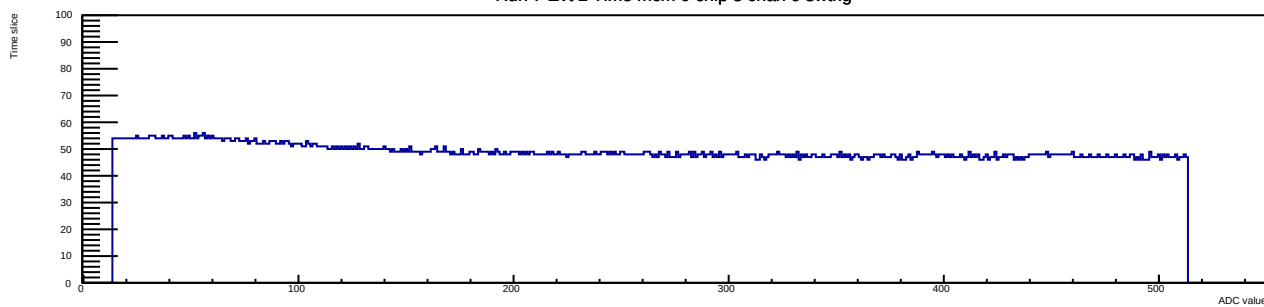
Run 7 Evt 2 Time mcm 0 chip 3 chan 7 swtrig



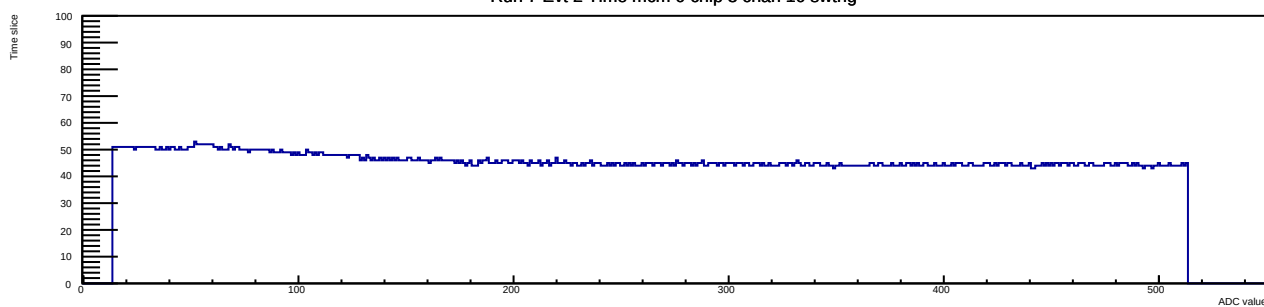
Run 7 Evt 2 Time mcm 0 chip 3 chan 8 swtrig



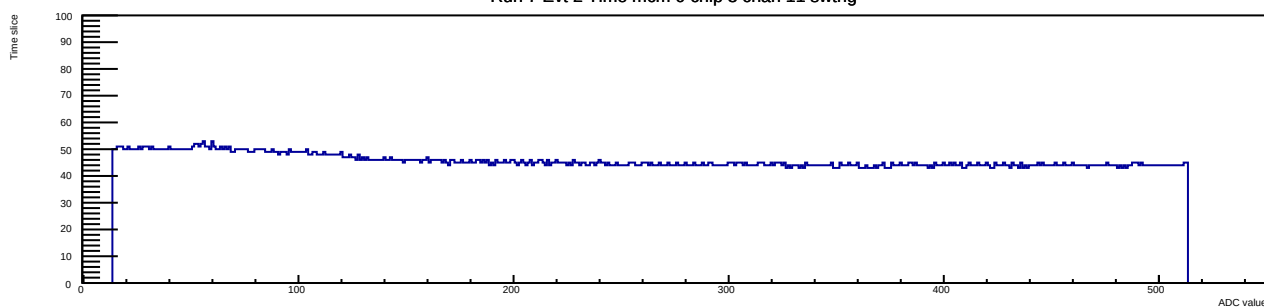
Run 7 Evt 2 Time mcm 0 chip 3 chan 9 swtrig



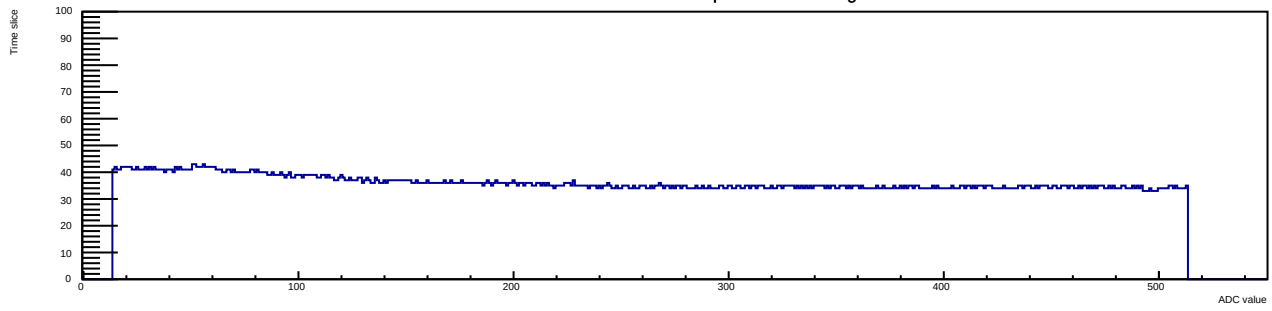
Run 7 Evt 2 Time mcm 0 chip 3 chan 10 swtrig



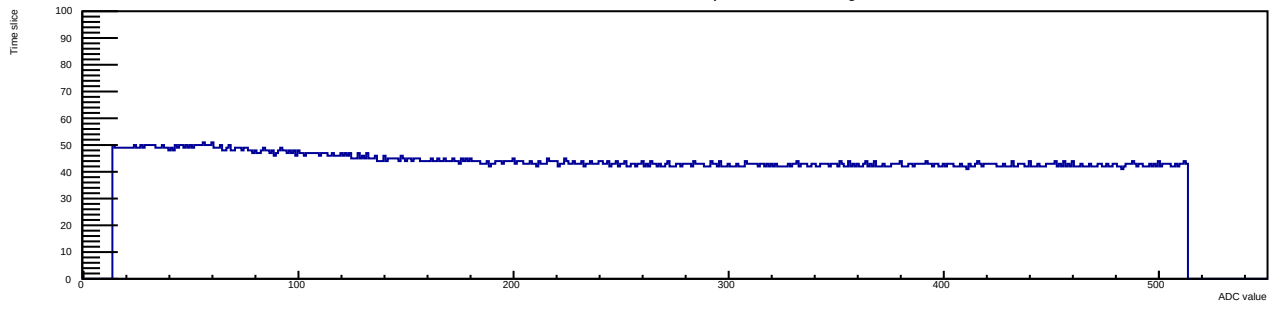
Run 7 Evt 2 Time mcm 0 chip 3 chan 11 swtrig



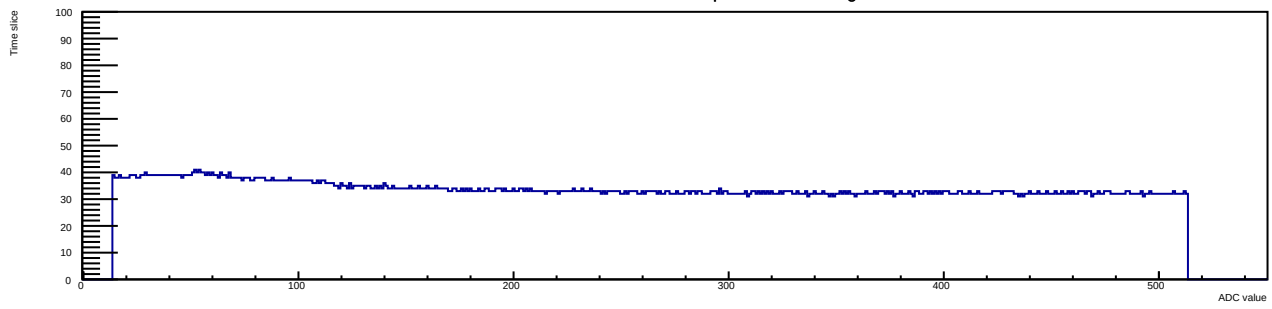
Run 7 Evt 2 Time mcm 0 chip 3 chan 12 swtrig



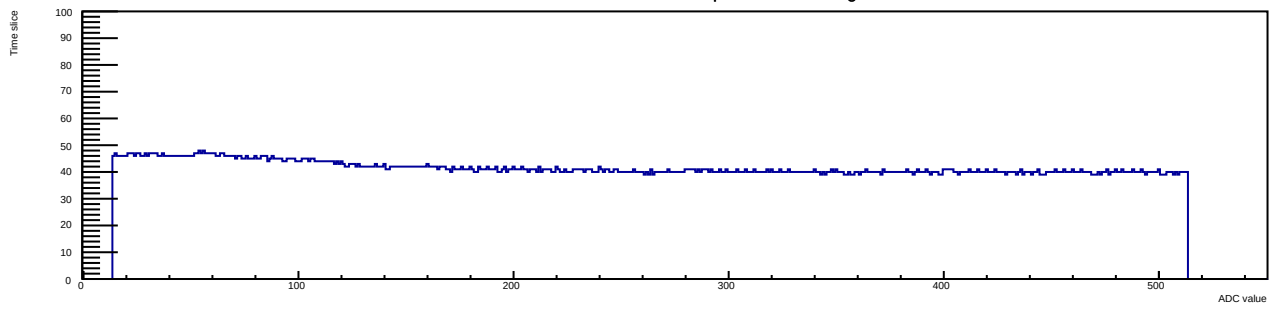
Run 7 Evt 2 Time mcm 0 chip 3 chan 13 swtrig



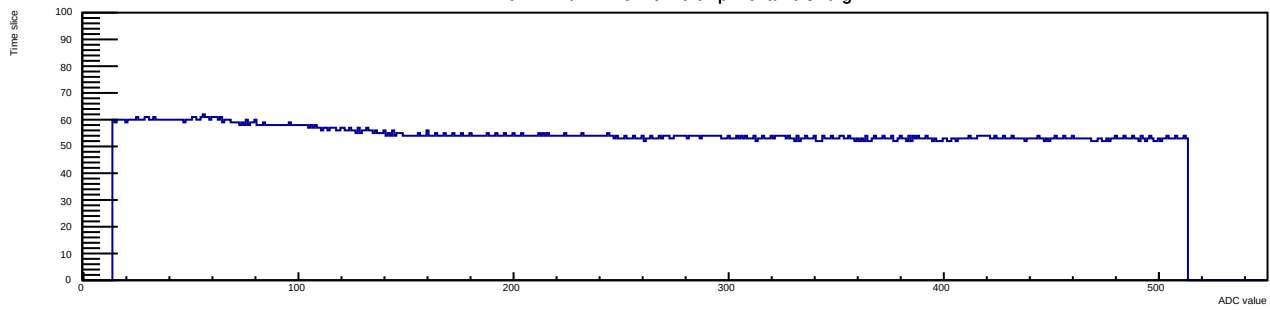
Run 7 Evt 2 Time mcm 0 chip 3 chan 14 swtrig



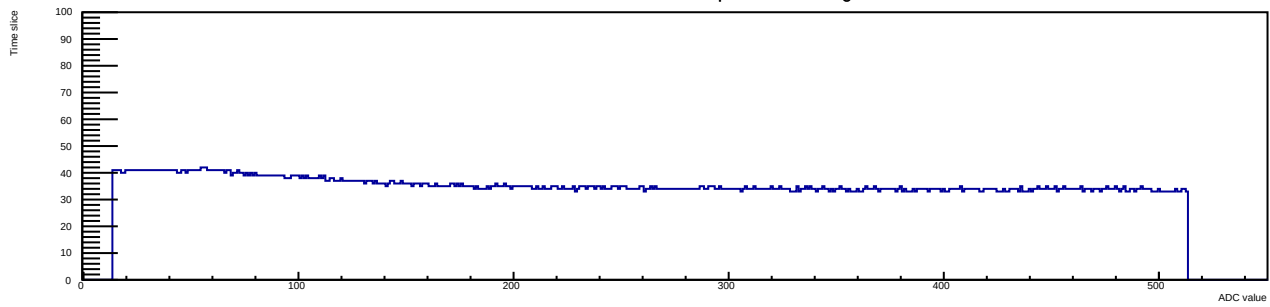
Run 7 Evt 2 Time mcm 0 chip 3 chan 15 swtrig



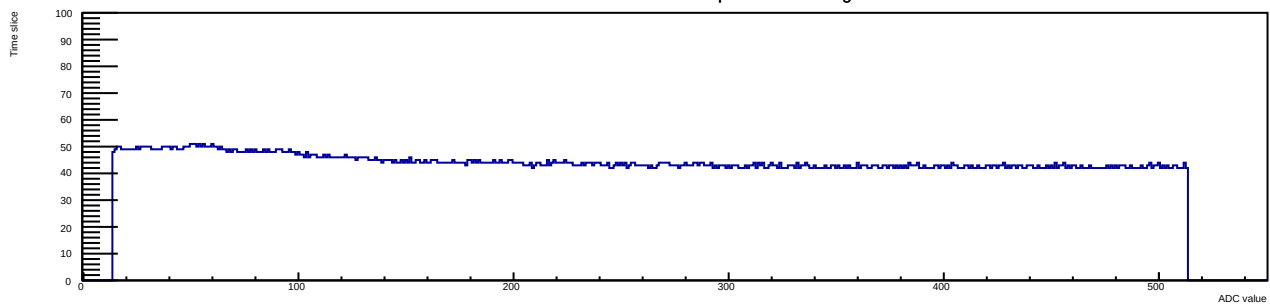
Run 7 Evt 2 Time mcm 0 chip 4 chan 0 swtrig



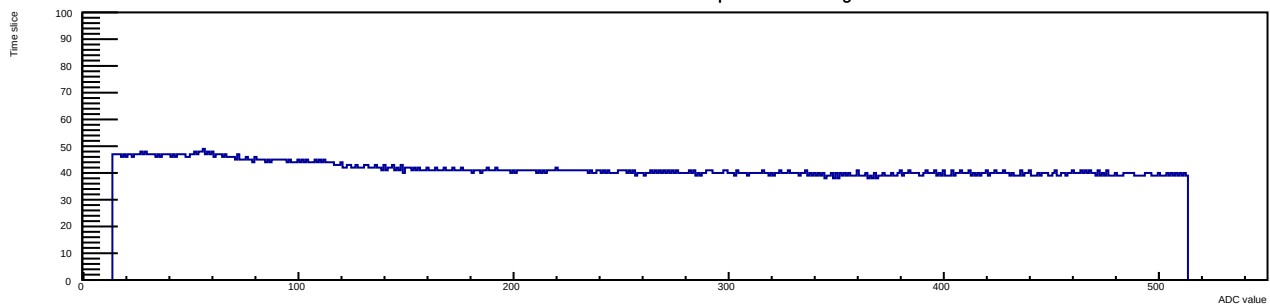
Run 7 Evt 2 Time mcm 0 chip 4 chan 1 swtrig



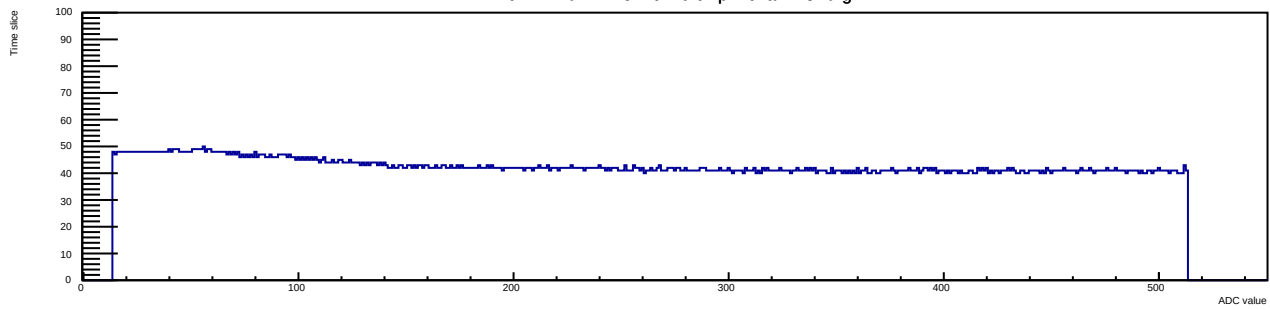
Run 7 Evt 2 Time mcm 0 chip 4 chan 2 swtrig



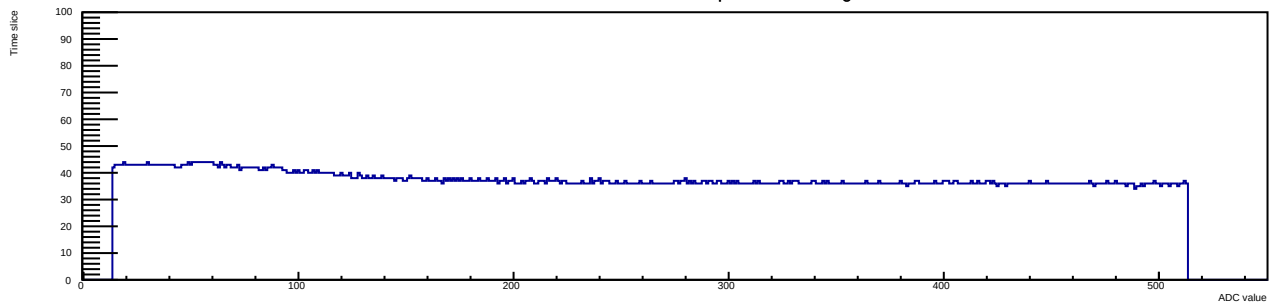
Run 7 Evt 2 Time mcm 0 chip 4 chan 3 swtrig



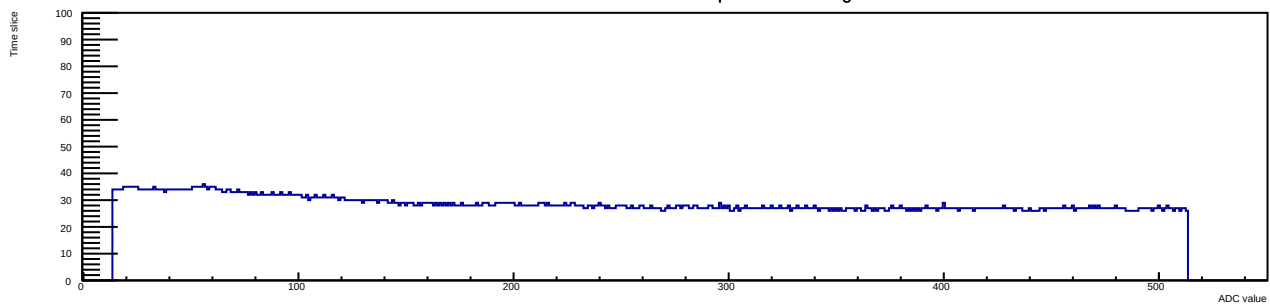
Run 7 Evt 2 Time mcm 0 chip 4 chan 4 swtrig



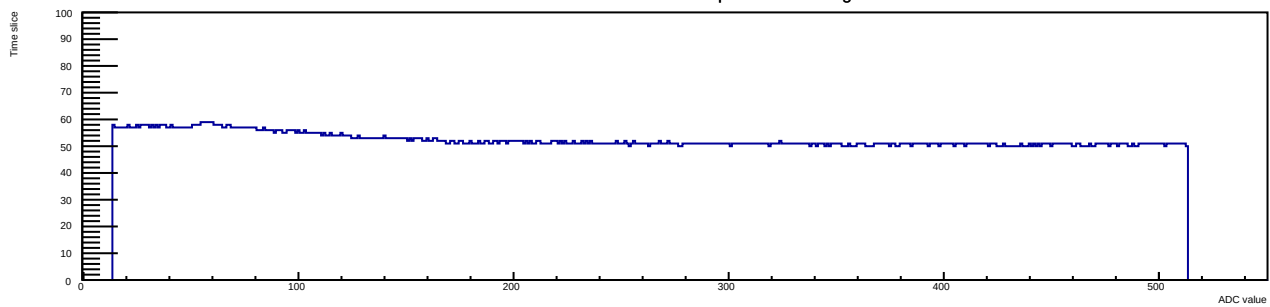
Run 7 Evt 2 Time mcm 0 chip 4 chan 5 swtrig



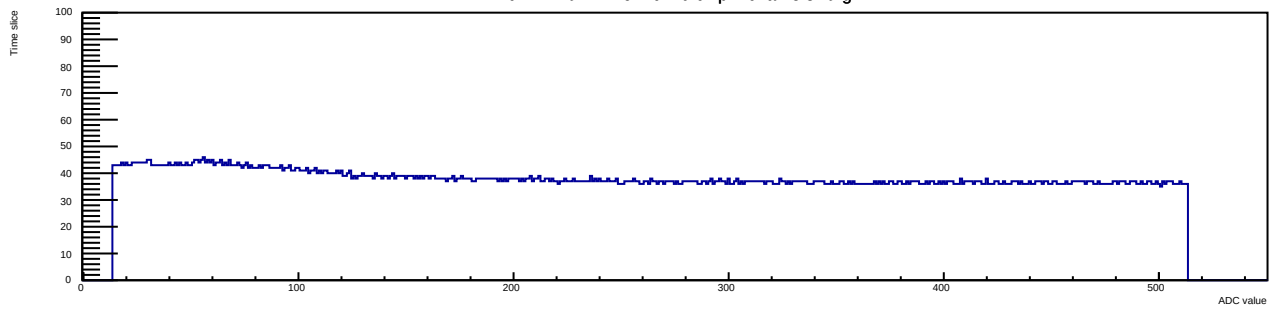
Run 7 Evt 2 Time mcm 0 chip 4 chan 6 swtrig



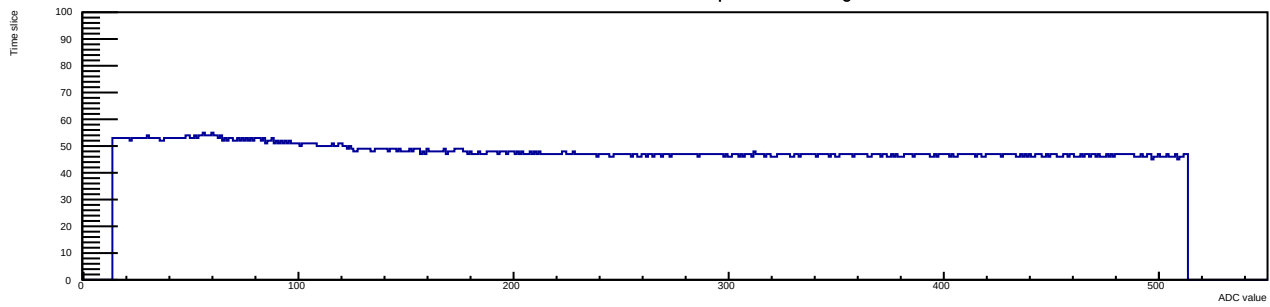
Run 7 Evt 2 Time mcm 0 chip 4 chan 7 swtrig



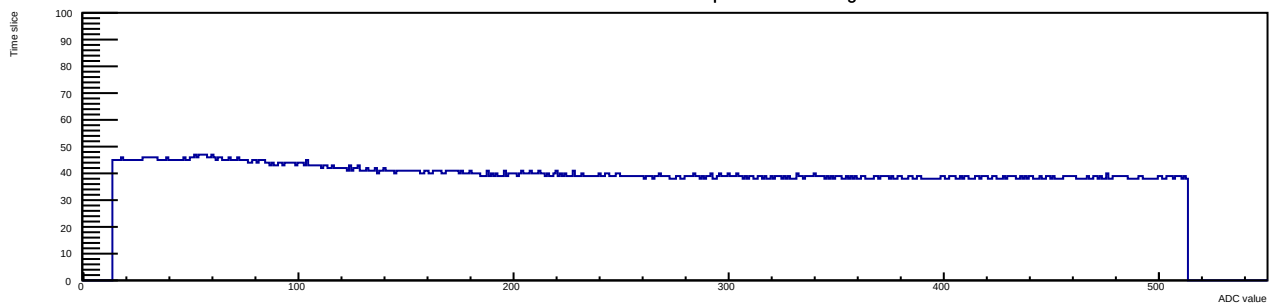
Run 7 Evt 2 Time mcm 0 chip 4 chan 8 swtrig



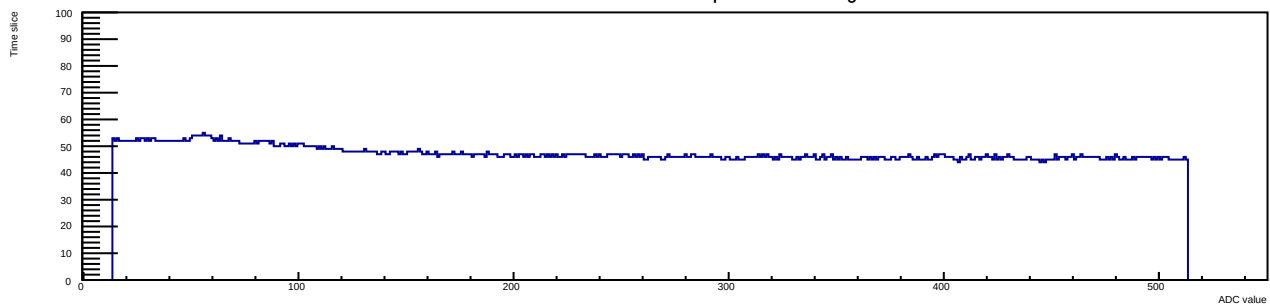
Run 7 Evt 2 Time mcm 0 chip 4 chan 9 swtrig



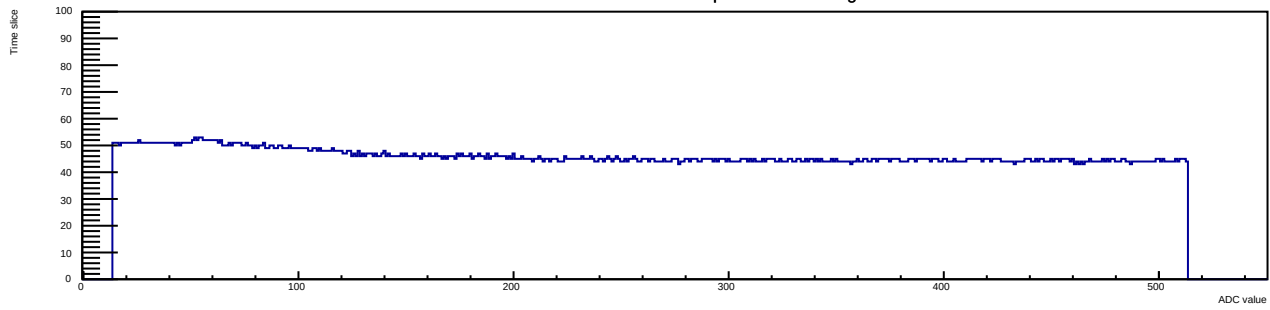
Run 7 Evt 2 Time mcm 0 chip 4 chan 10 swtrig



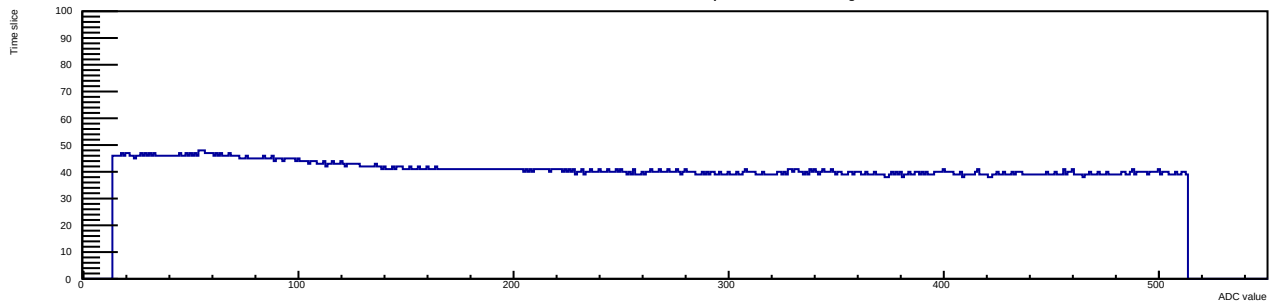
Run 7 Evt 2 Time mcm 0 chip 4 chan 11 swtrig



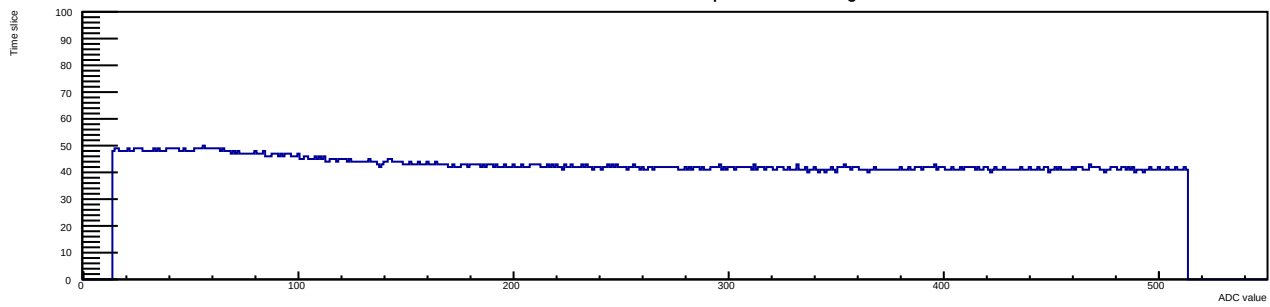
Run 7 Evt 2 Time mcm 0 chip 4 chan 12 swtrig



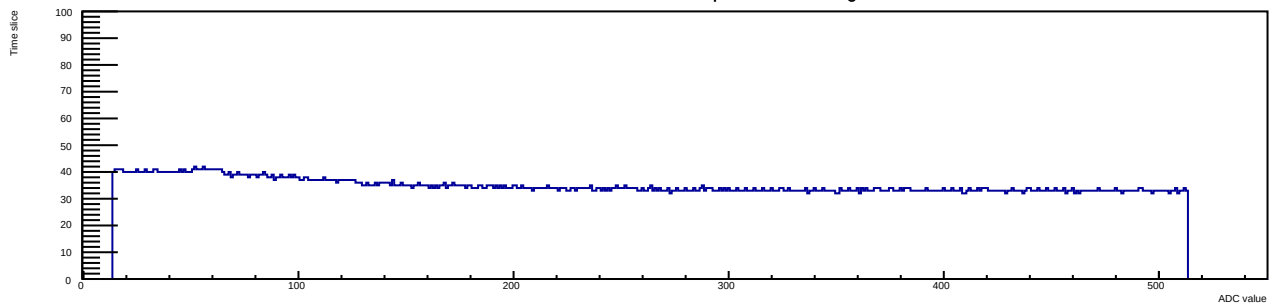
Run 7 Evt 2 Time mcm 0 chip 4 chan 13 swtrig



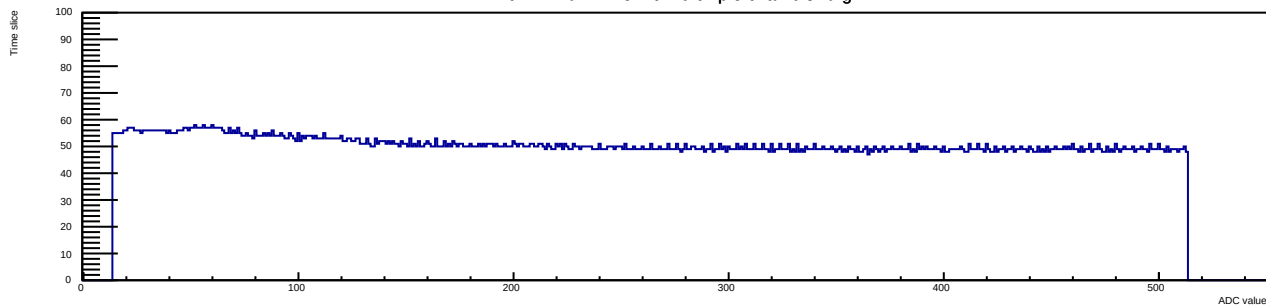
Run 7 Evt 2 Time mcm 0 chip 4 chan 14 swtrig



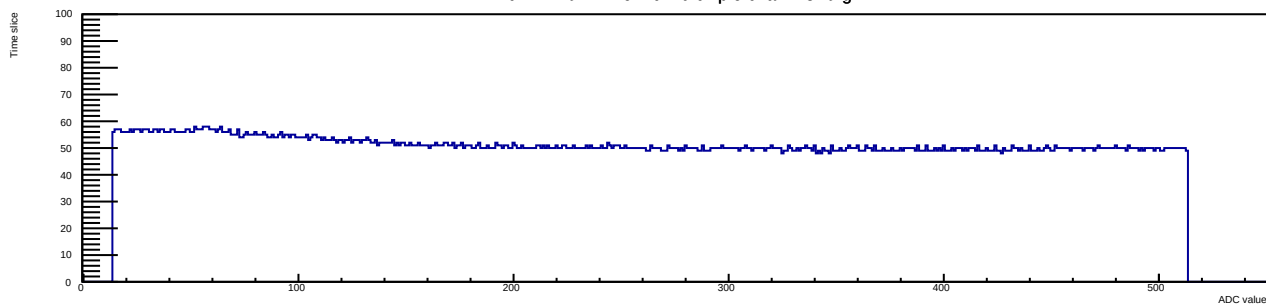
Run 7 Evt 2 Time mcm 0 chip 4 chan 15 swtrig



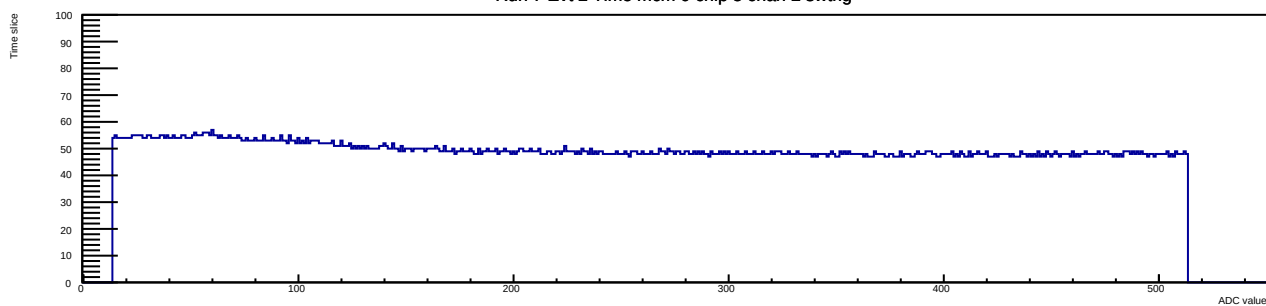
Run 7 Evt 2 Time mcm 0 chip 5 chan 0 swtrig



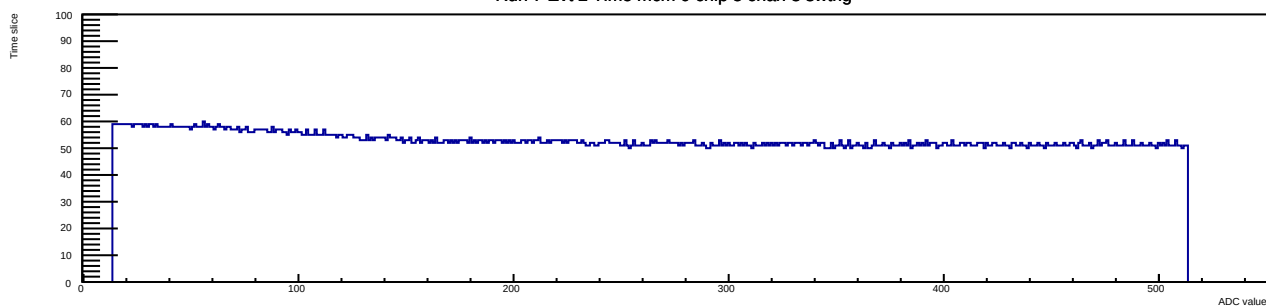
Run 7 Evt 2 Time mcm 0 chip 5 chan 1 swtrig



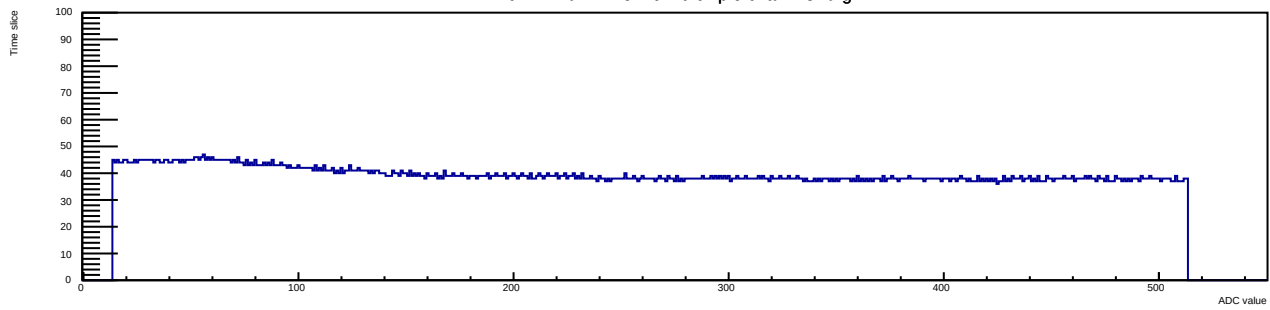
Run 7 Evt 2 Time mcm 0 chip 5 chan 2 swtrig



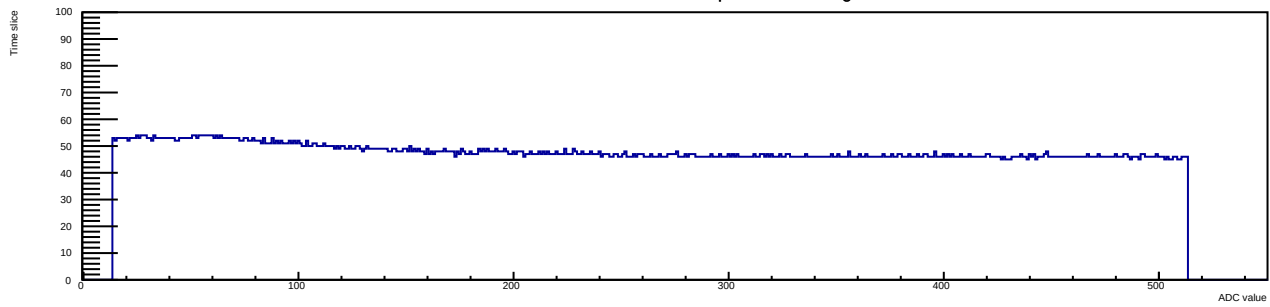
Run 7 Evt 2 Time mcm 0 chip 5 chan 3 swtrig



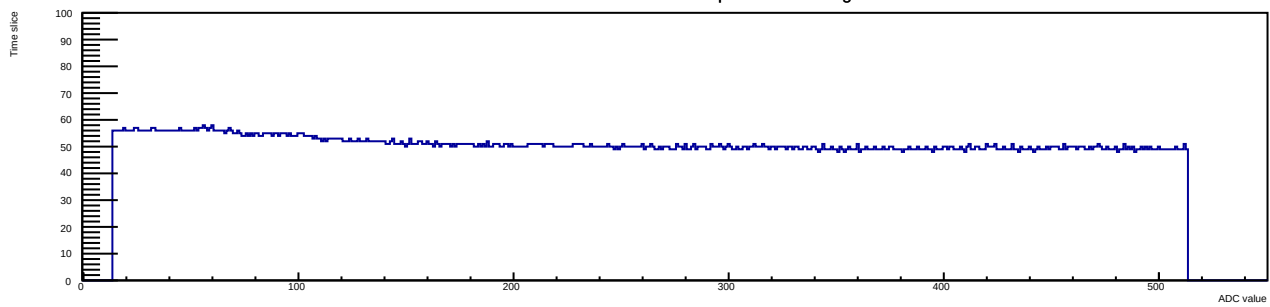
Run 7 Evt 2 Time mcm 0 chip 5 chan 4 swtrig



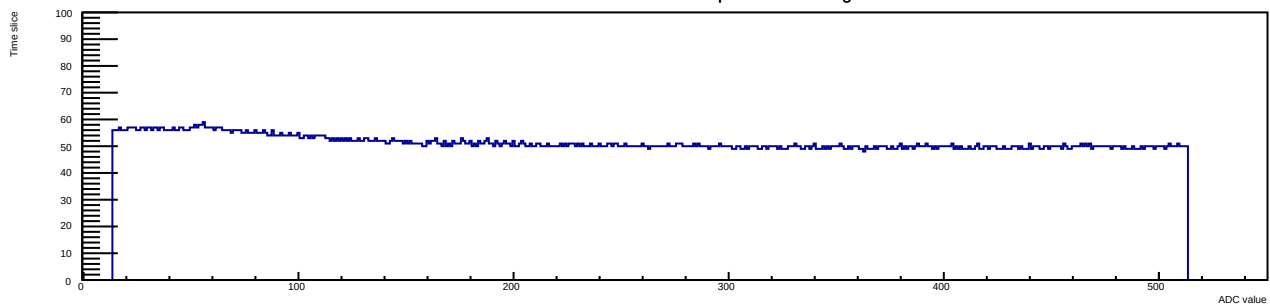
Run 7 Evt 2 Time mcm 0 chip 5 chan 5 swtrig



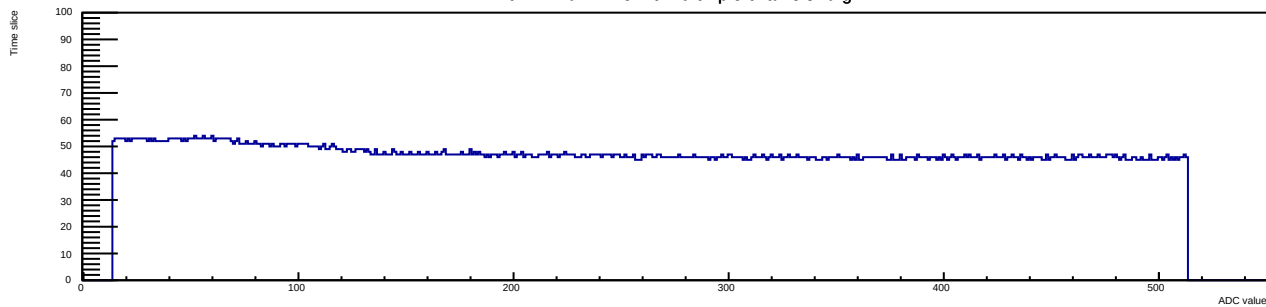
Run 7 Evt 2 Time mcm 0 chip 5 chan 6 swtrig



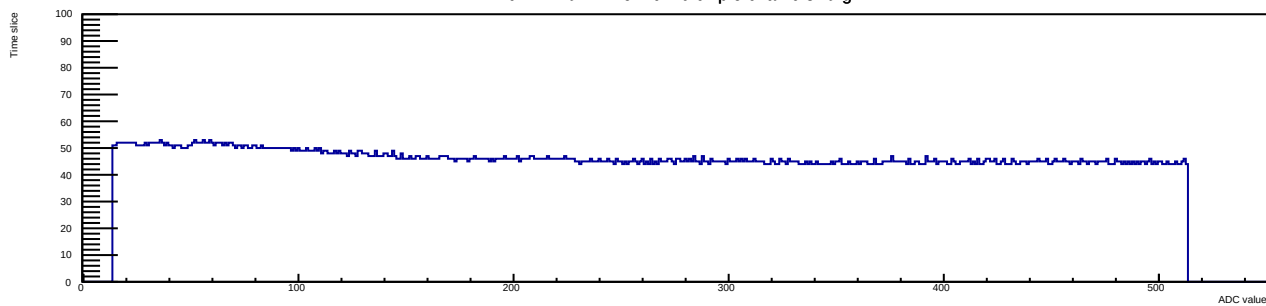
Run 7 Evt 2 Time mcm 0 chip 5 chan 7 swtrig



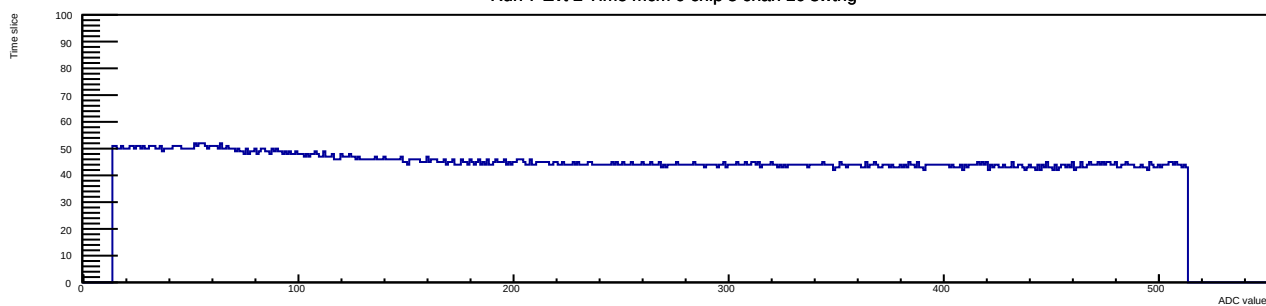
Run 7 Evt 2 Time mcm 0 chip 5 chan 8 swtrig



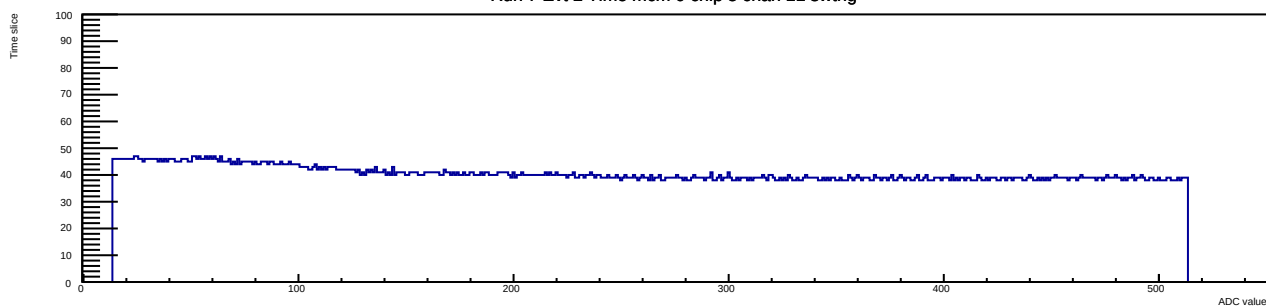
Run 7 Evt 2 Time mcm 0 chip 5 chan 9 swtrig



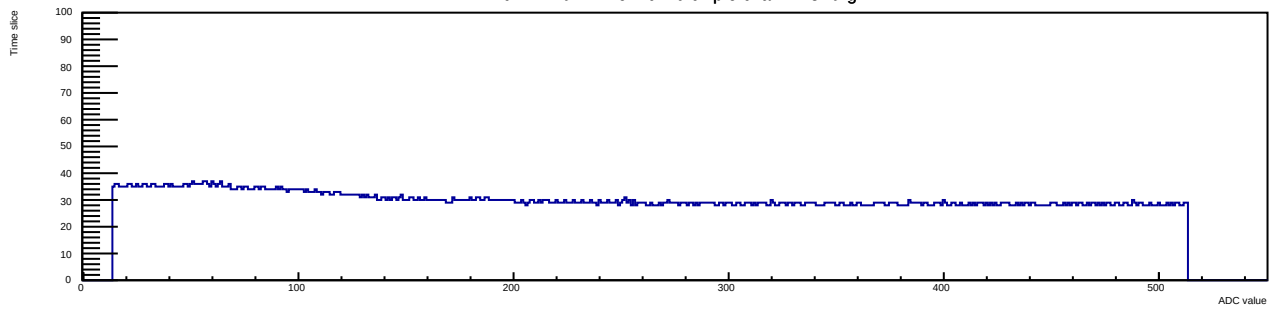
Run 7 Evt 2 Time mcm 0 chip 5 chan 10 swtrig



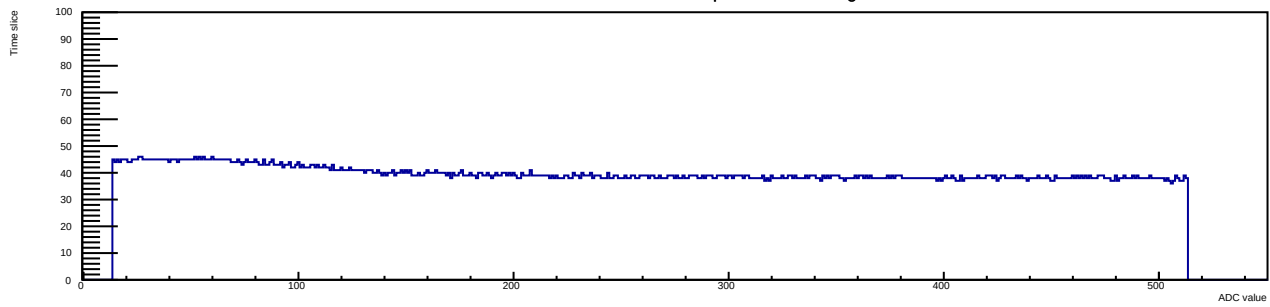
Run 7 Evt 2 Time mcm 0 chip 5 chan 11 swtrig



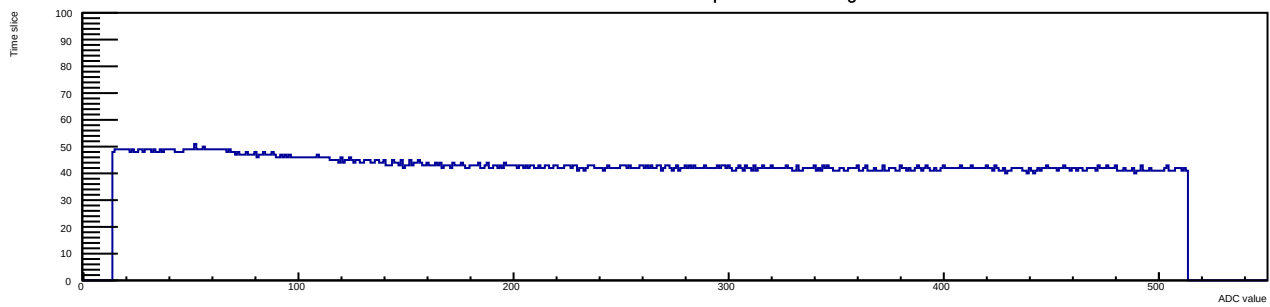
Run 7 Evt 2 Time mcm 0 chip 5 chan 12 swtrig



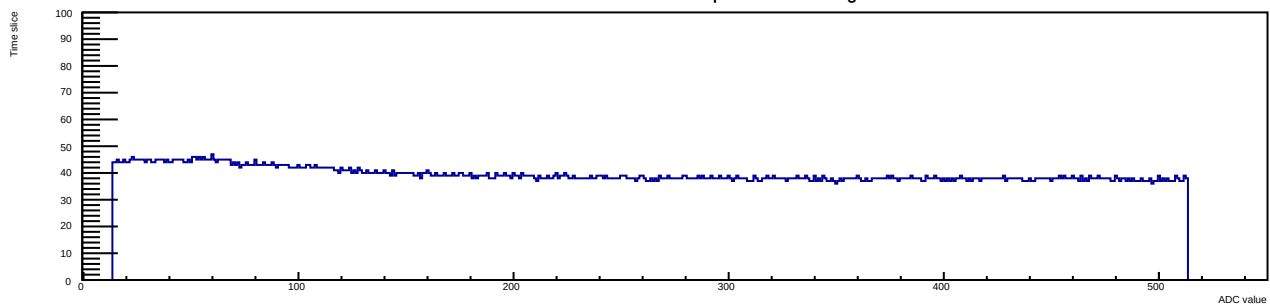
Run 7 Evt 2 Time mcm 0 chip 5 chan 13 swtrig



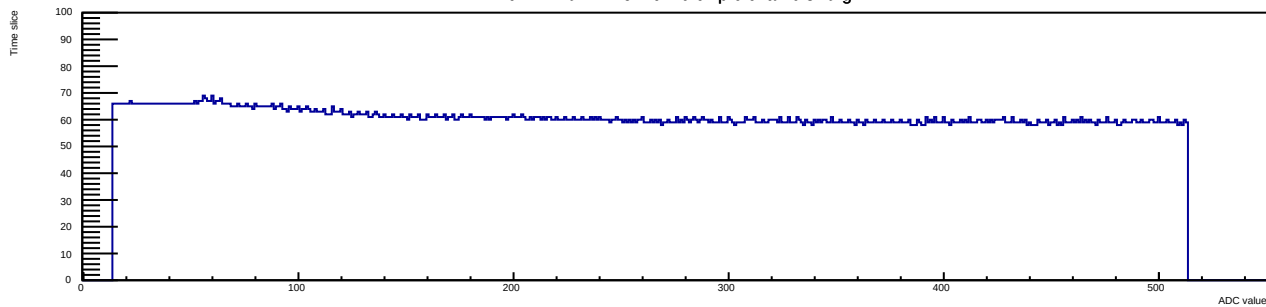
Run 7 Evt 2 Time mcm 0 chip 5 chan 14 swtrig



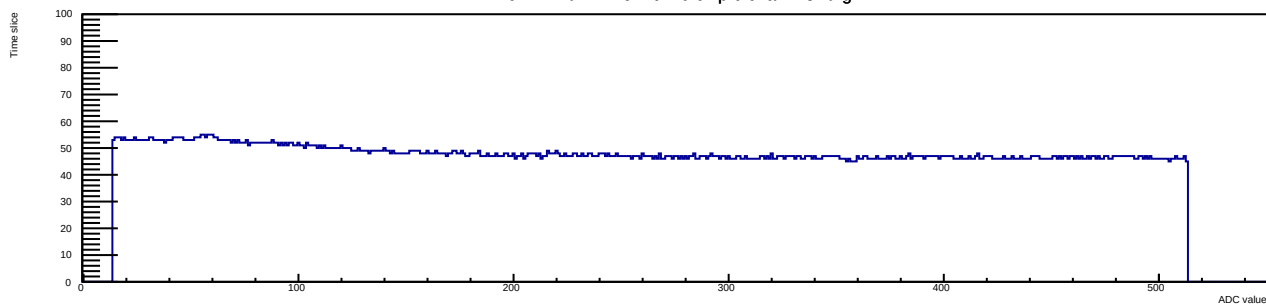
Run 7 Evt 2 Time mcm 0 chip 5 chan 15 swtrig



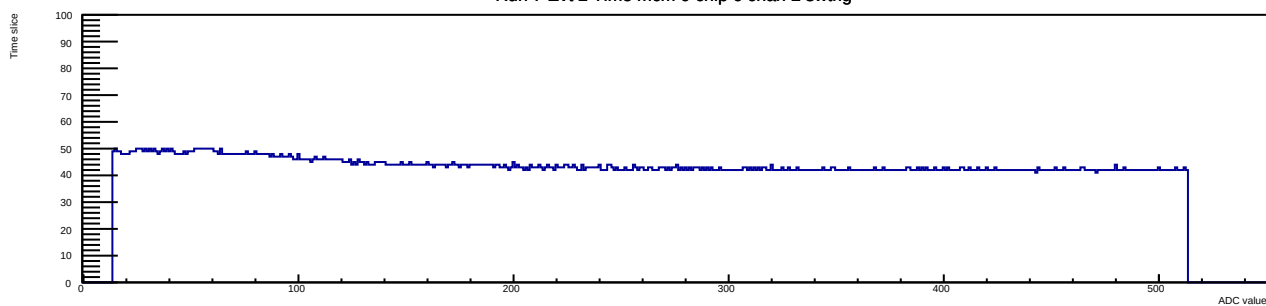
Run 7 Evt 2 Time mcm 0 chip 6 chan 0 swtrig



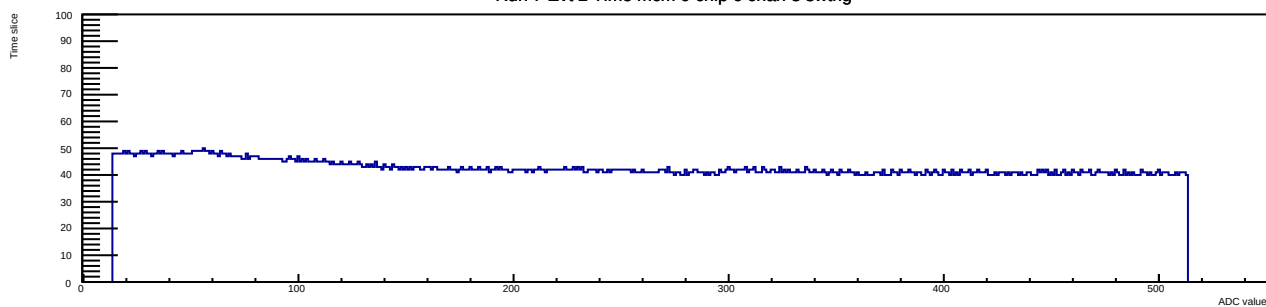
Run 7 Evt 2 Time mcm 0 chip 6 chan 1 swtrig



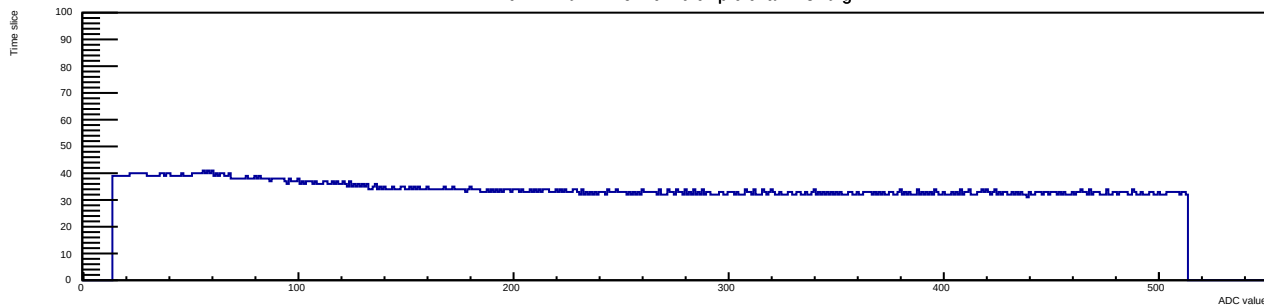
Run 7 Evt 2 Time mcm 0 chip 6 chan 2 swtrig



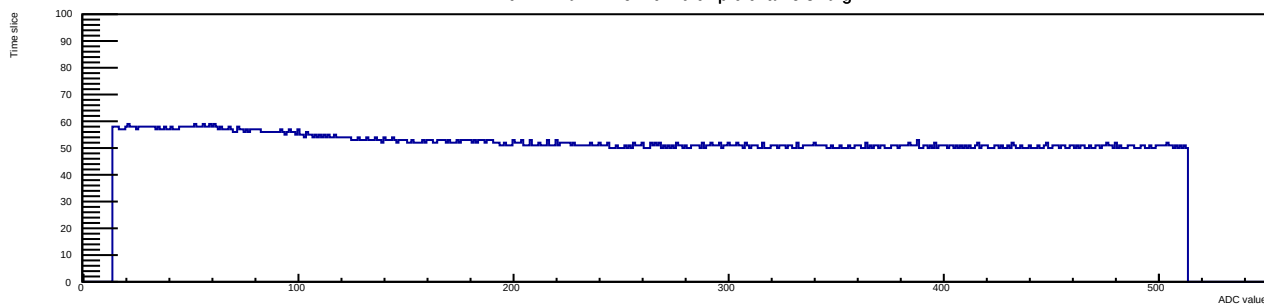
Run 7 Evt 2 Time mcm 0 chip 6 chan 3 swtrig



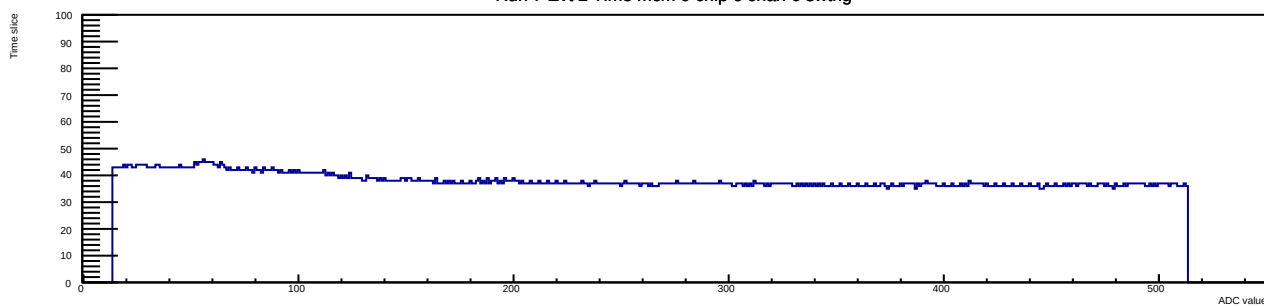
Run 7 Evt 2 Time mcm 0 chip 6 chan 4 swtrig



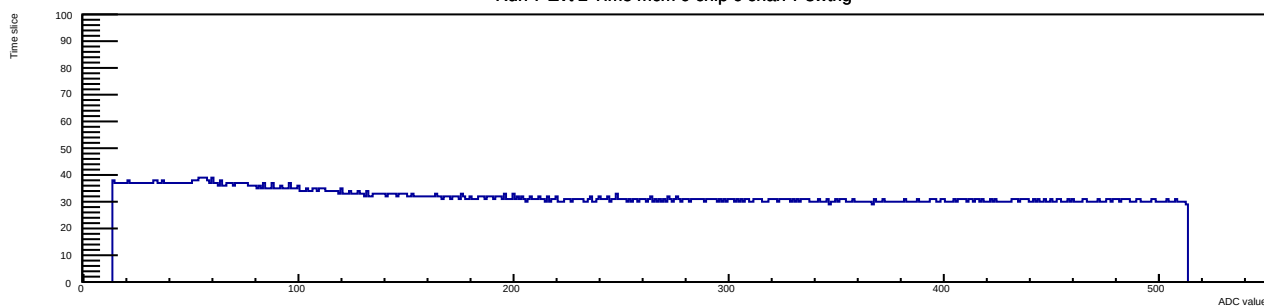
Run 7 Evt 2 Time mcm 0 chip 6 chan 5 swtrig



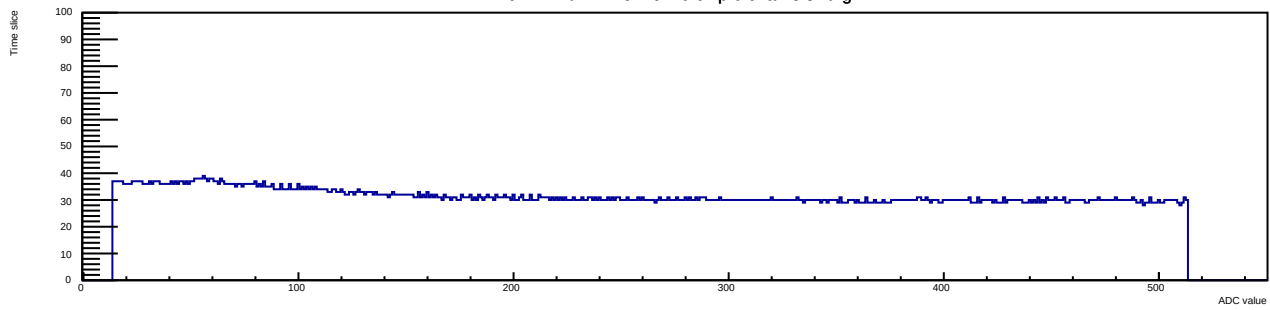
Run 7 Evt 2 Time mcm 0 chip 6 chan 6 swtrig



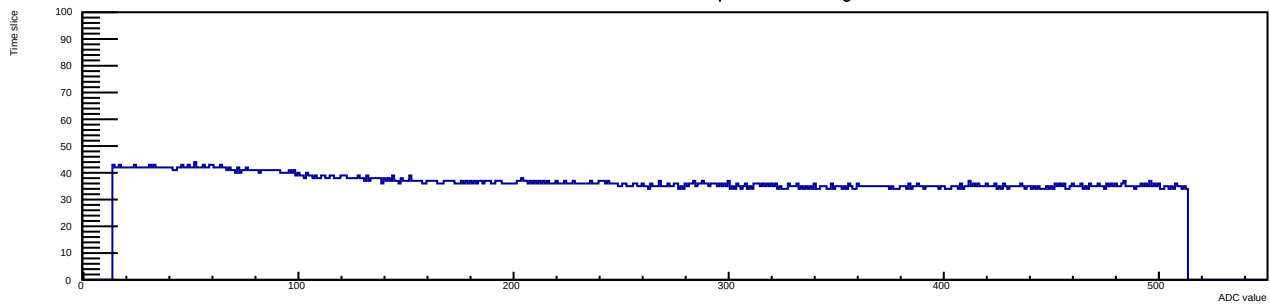
Run 7 Evt 2 Time mcm 0 chip 6 chan 7 swtrig



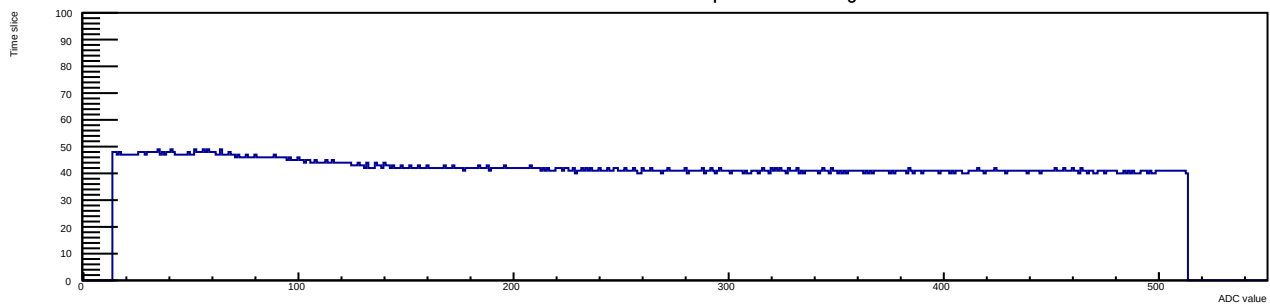
Run 7 Evt 2 Time mcm 0 chip 6 chan 8 swtrig



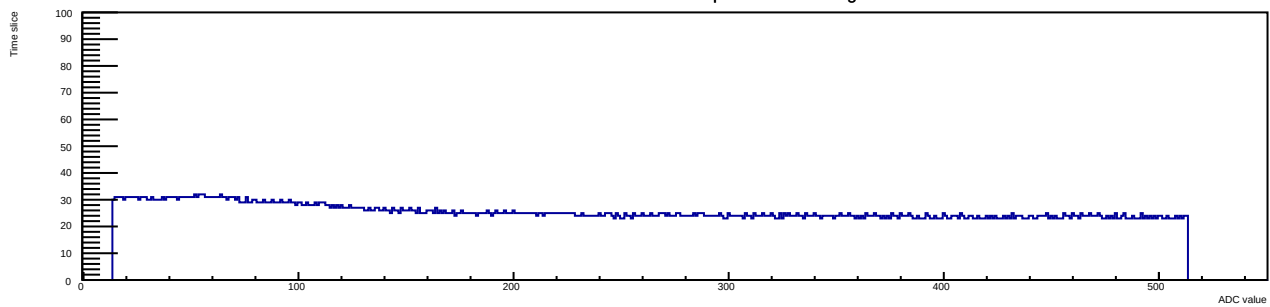
Run 7 Evt 2 Time mcm 0 chip 6 chan 9 swtrig



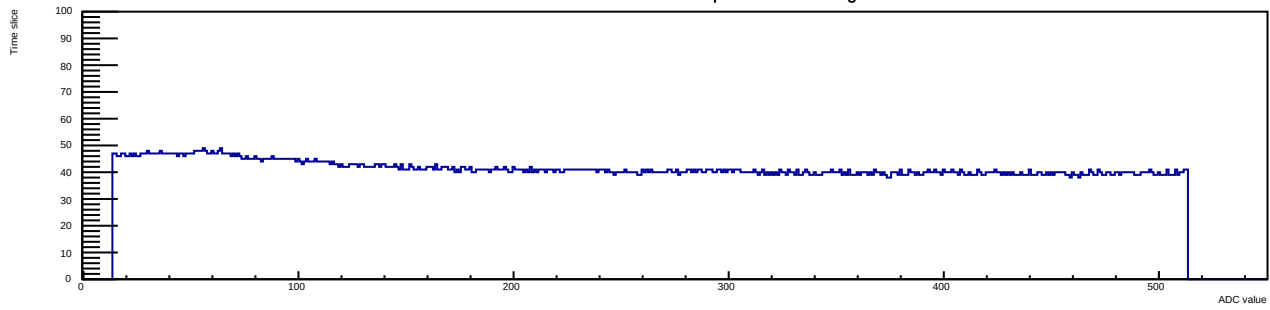
Run 7 Evt 2 Time mcm 0 chip 6 chan 10 swtrig



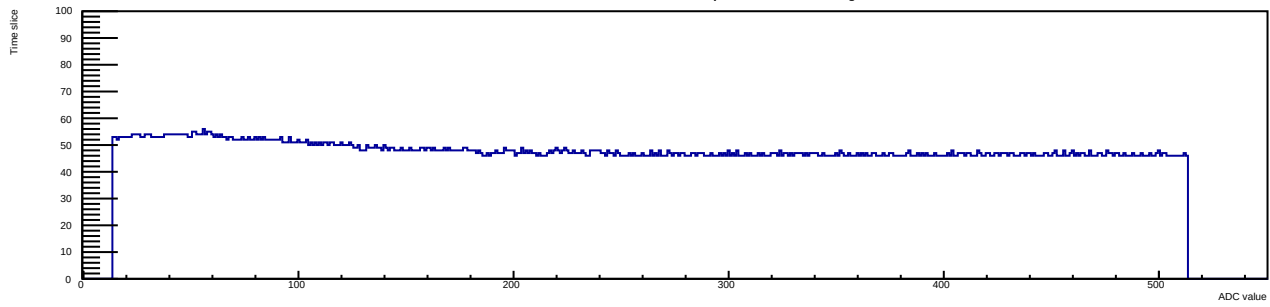
Run 7 Evt 2 Time mcm 0 chip 6 chan 11 swtrig



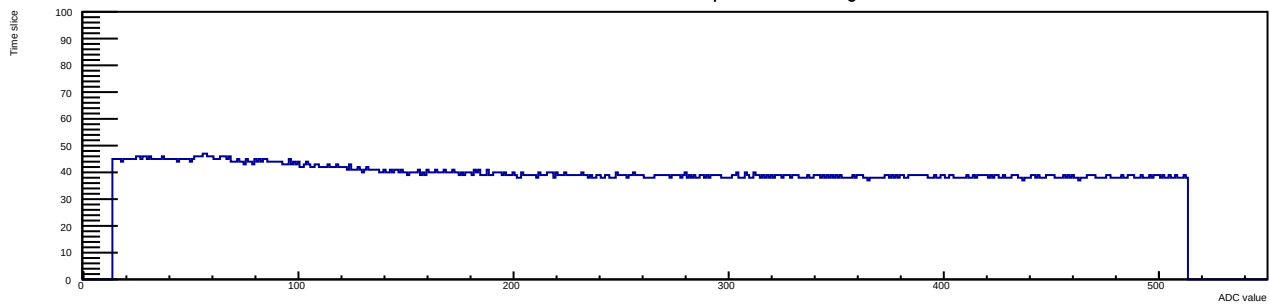
Run 7 Evt 2 Time mcm 0 chip 6 chan 12 swtrig



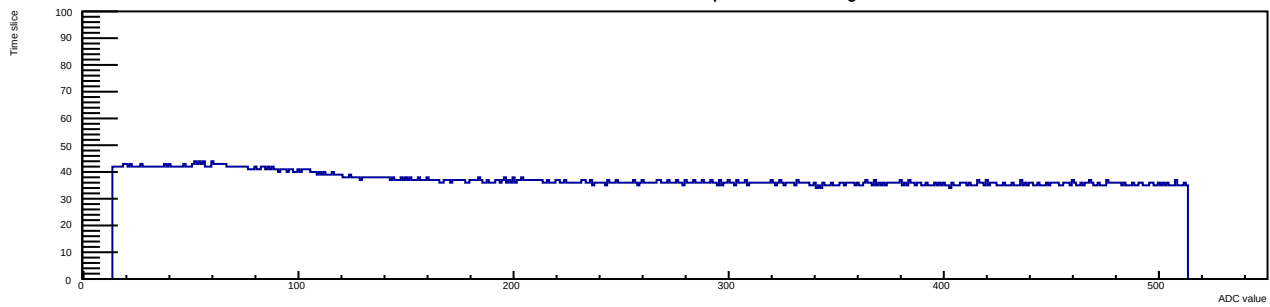
Run 7 Evt 2 Time mcm 0 chip 6 chan 13 swtrig



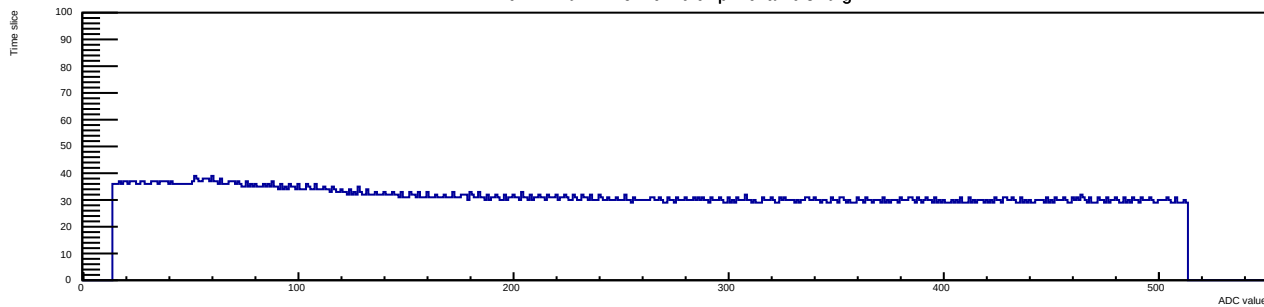
Run 7 Evt 2 Time mcm 0 chip 6 chan 14 swtrig



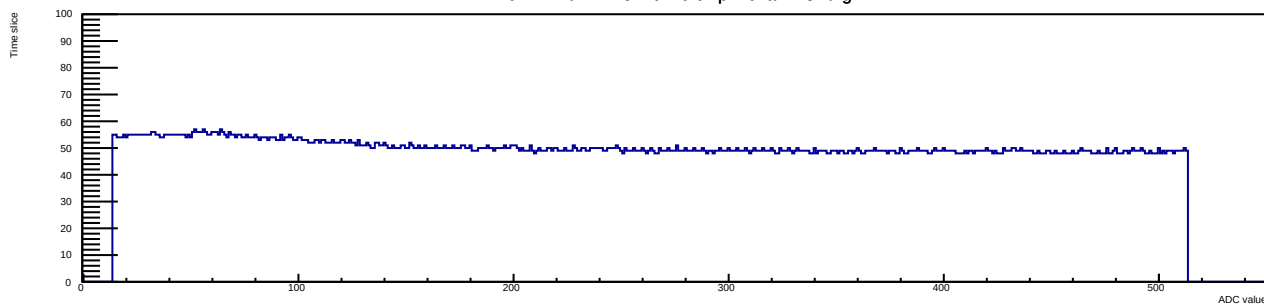
Run 7 Evt 2 Time mcm 0 chip 6 chan 15 swtrig



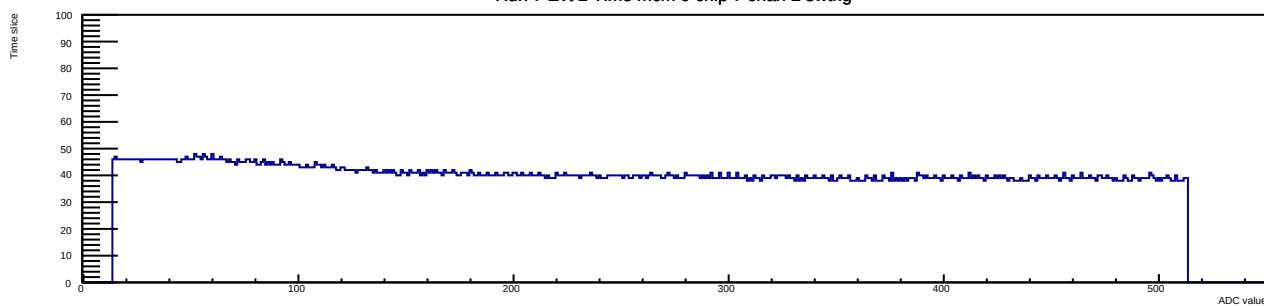
Run 7 Evt 2 Time mcm 0 chip 7 chan 0 swtrig



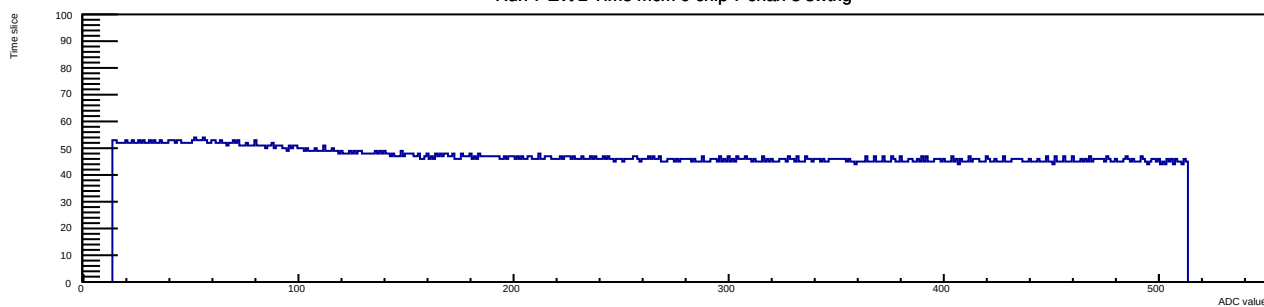
Run 7 Evt 2 Time mcm 0 chip 7 chan 1 swtrig



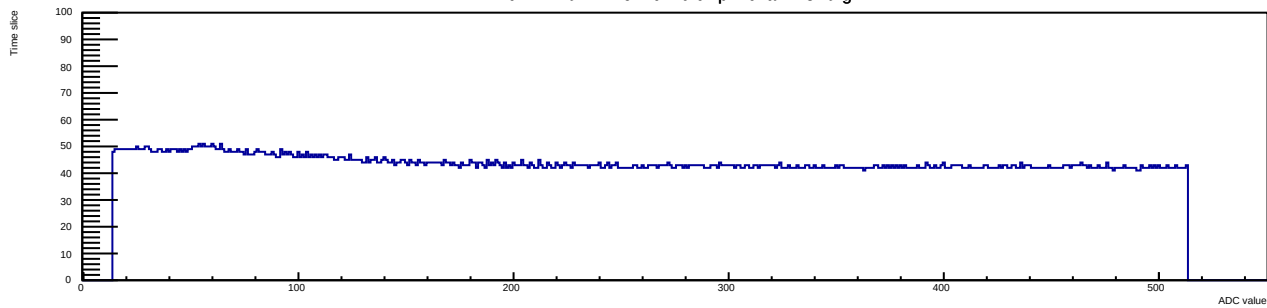
Run 7 Evt 2 Time mcm 0 chip 7 chan 2 swtrig



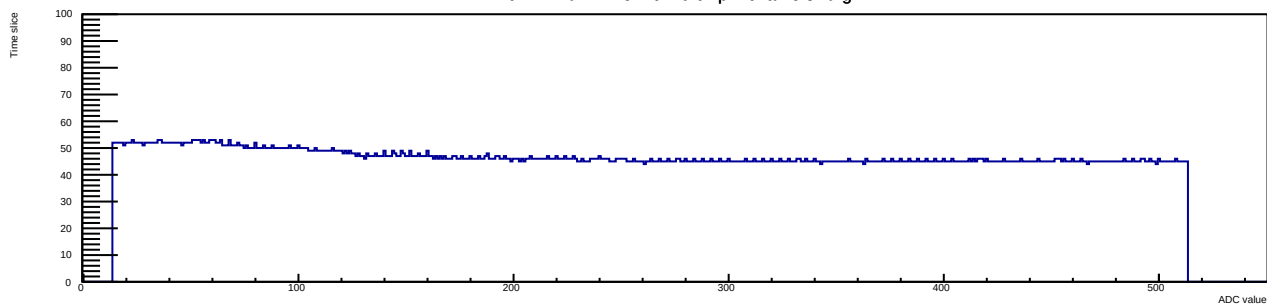
Run 7 Evt 2 Time mcm 0 chip 7 chan 3 swtrig



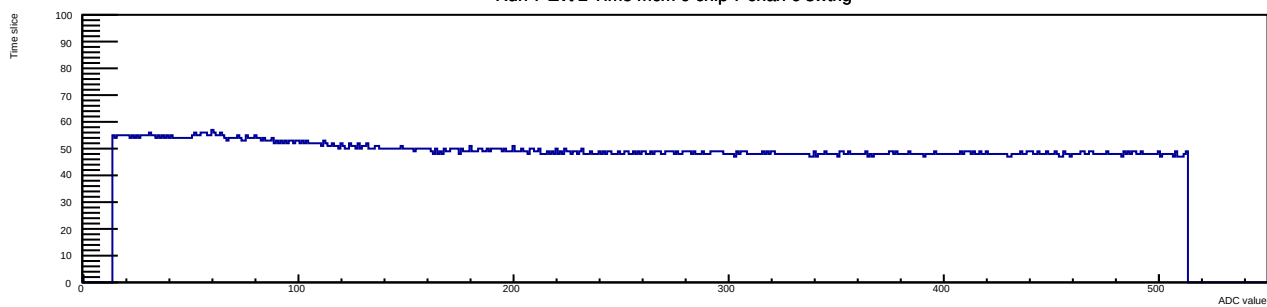
Run 7 Evt 2 Time mcm 0 chip 7 chan 4 swtrig



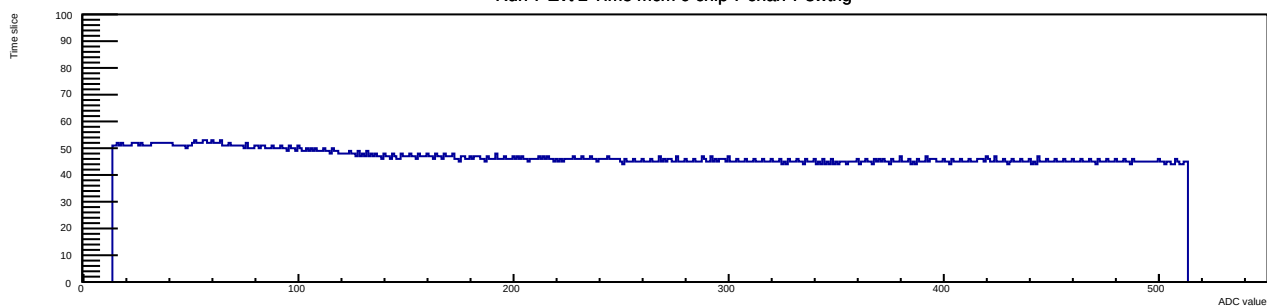
Run 7 Evt 2 Time mcm 0 chip 7 chan 5 swtrig



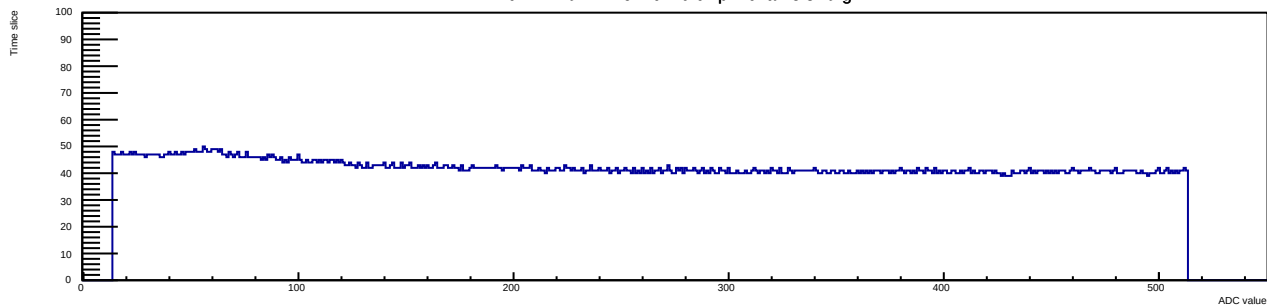
Run 7 Evt 2 Time mcm 0 chip 7 chan 6 swtrig



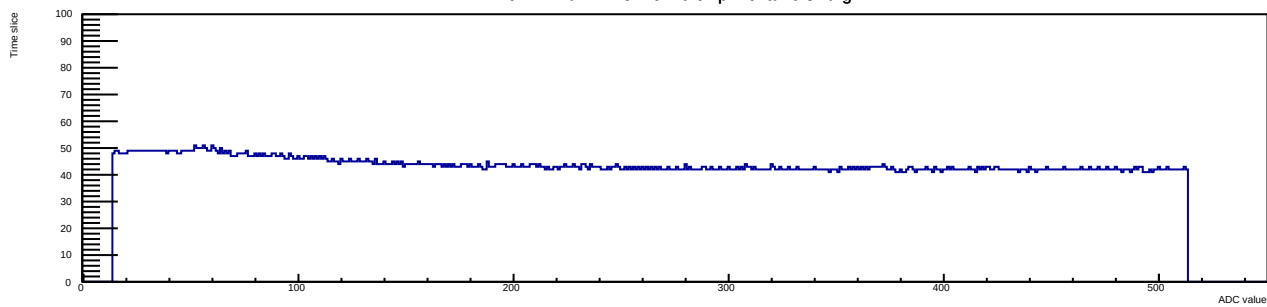
Run 7 Evt 2 Time mcm 0 chip 7 chan 7 swtrig



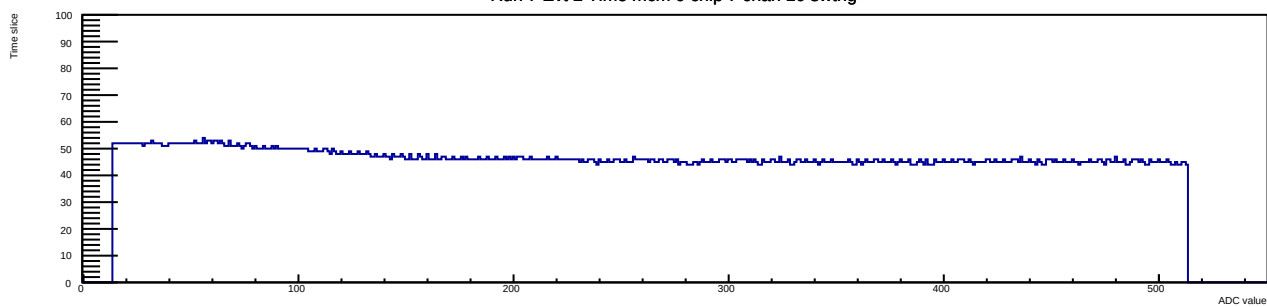
Run 7 Evt 2 Time mcm 0 chip 7 chan 8 swtrig



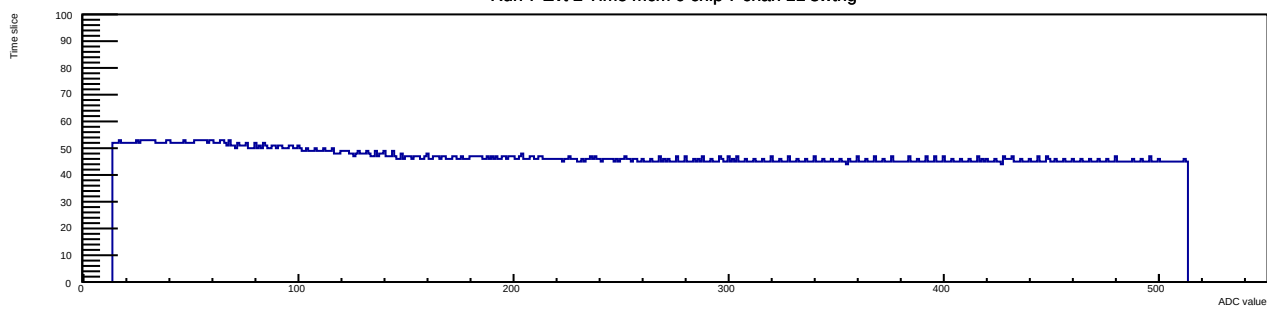
Run 7 Evt 2 Time mcm 0 chip 7 chan 9 swtrig



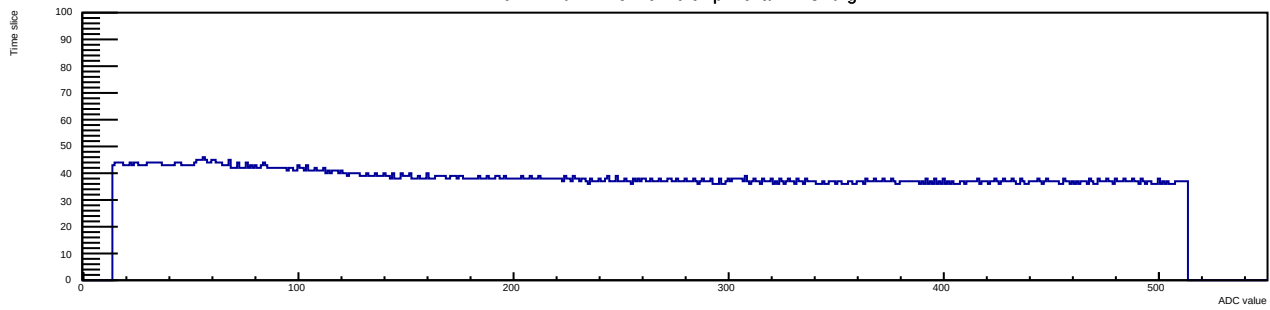
Run 7 Evt 2 Time mcm 0 chip 7 chan 10 swtrig



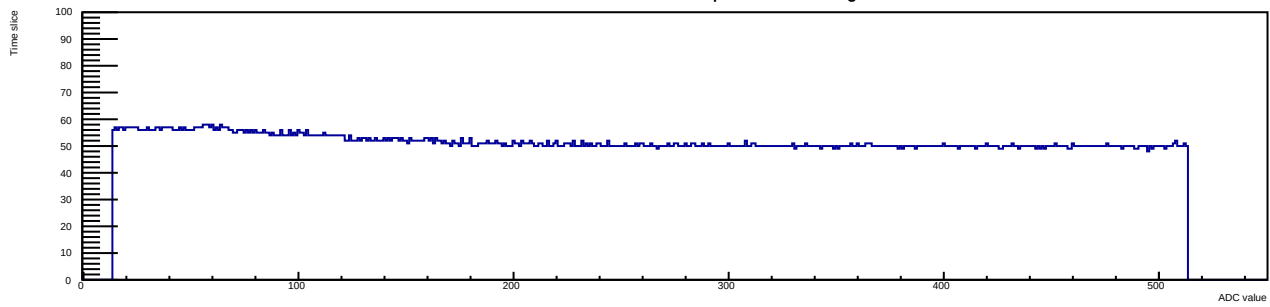
Run 7 Evt 2 Time mcm 0 chip 7 chan 11 swtrig



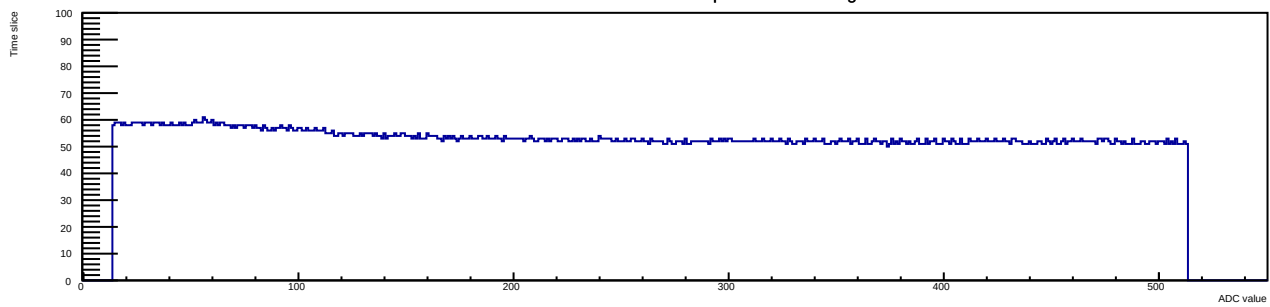
Run 7 Evt 2 Time mcm 0 chip 7 chan 12 swtrig



Run 7 Evt 2 Time mcm 0 chip 7 chan 13 swtrig



Run 7 Evt 2 Time mcm 0 chip 7 chan 14 swtrig



Run 7 Evt 2 Time mcm 0 chip 7 chan 15 swtrig

