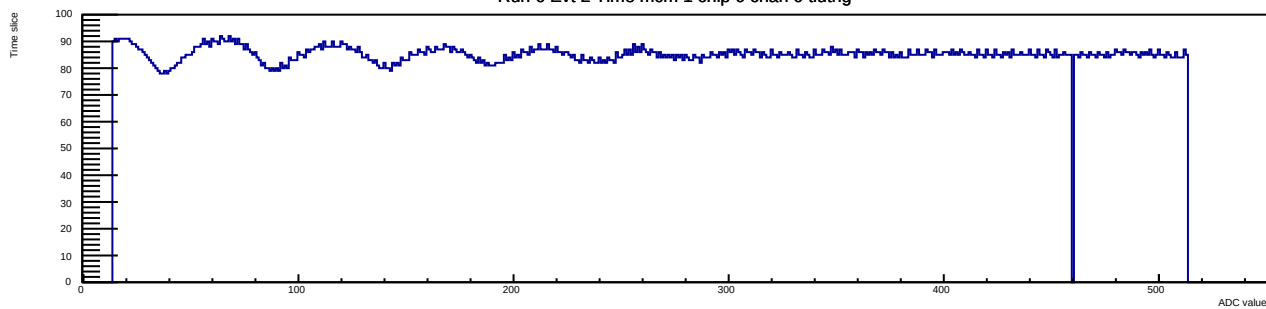
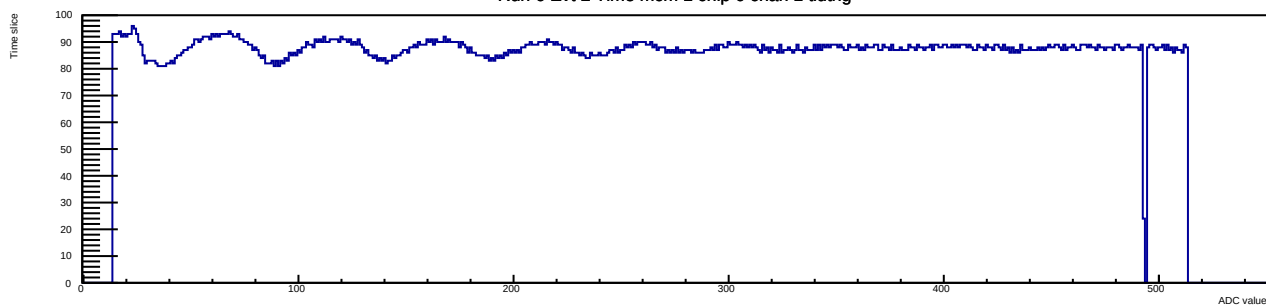


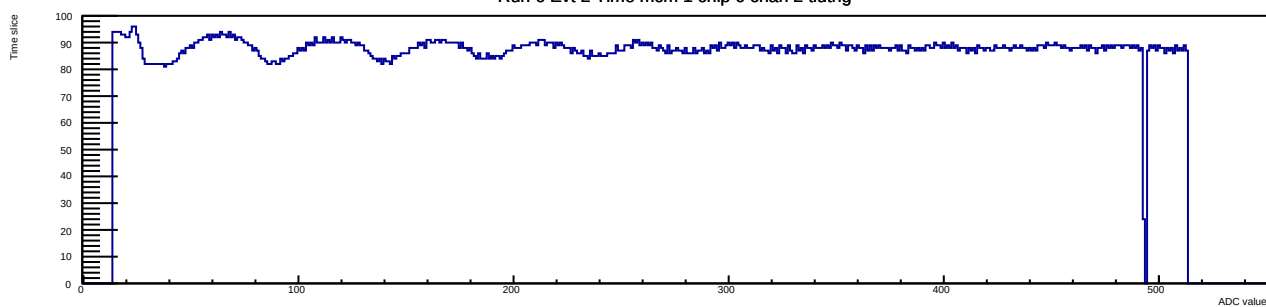
Run 6 Evt 2 Time mcm 1 chip 0 chan 0 tlutrig



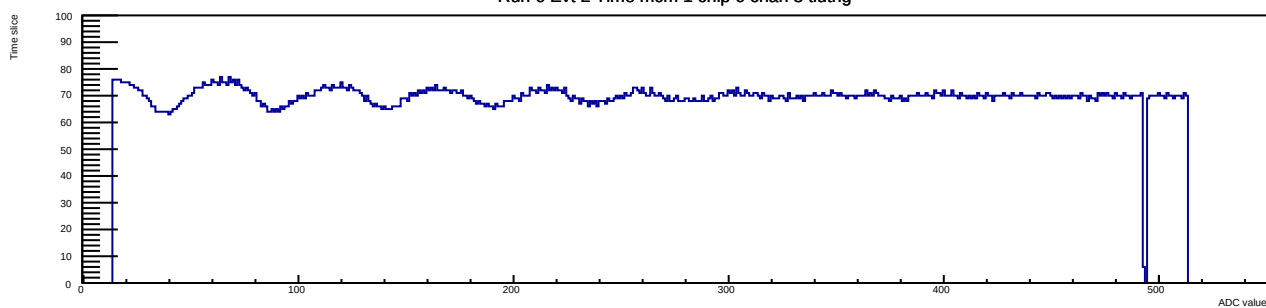
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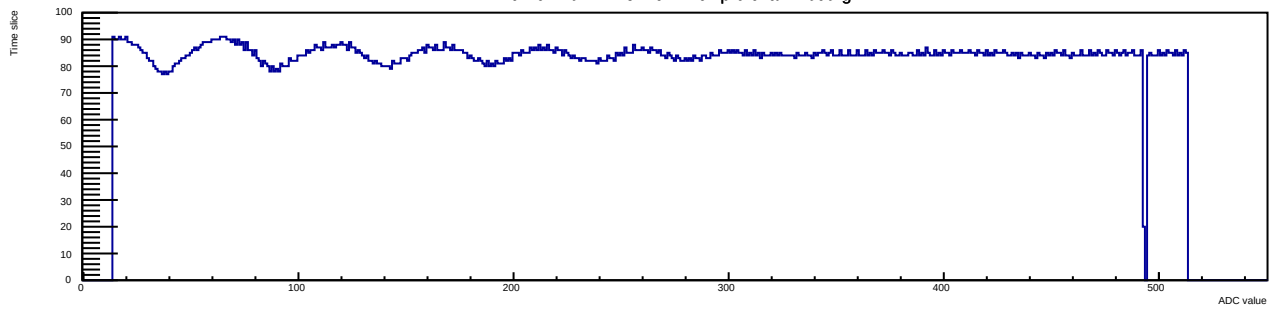
Run 6 Evt 2 Time mcm 1 chip 0 chan 2 tlutrig



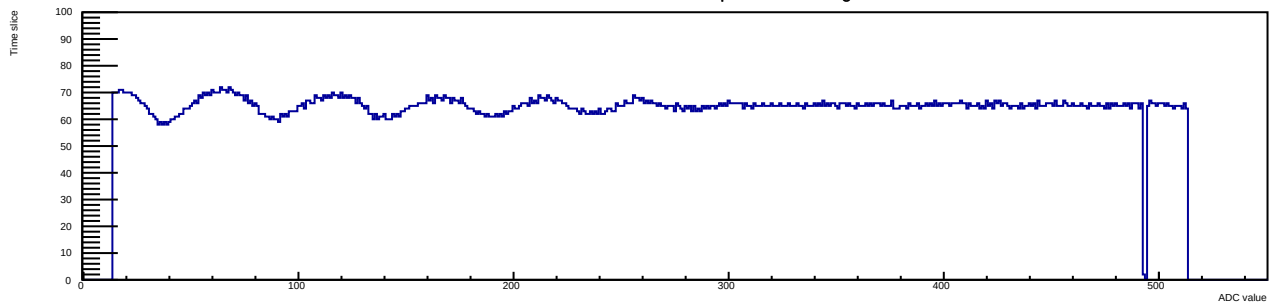
Run 6 Evt 2 Time mcm 1 chip 0 chan 3 tlutrig



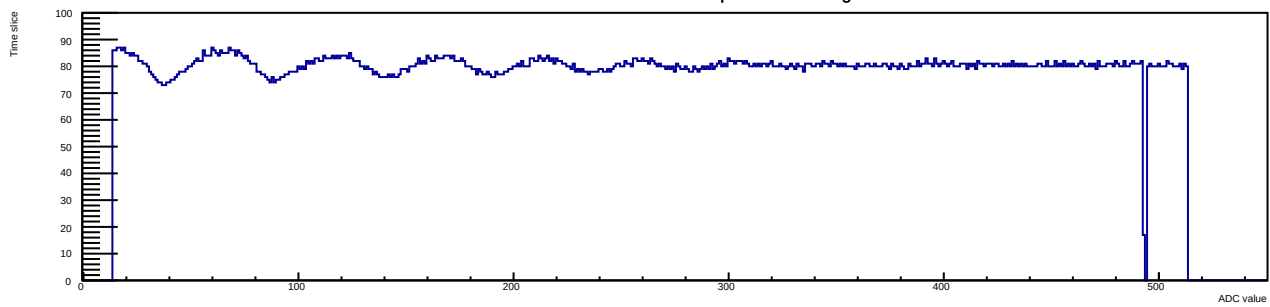
Run 6 Evt 2 Time mcm 1 chip 0 chan 4 tlutrig



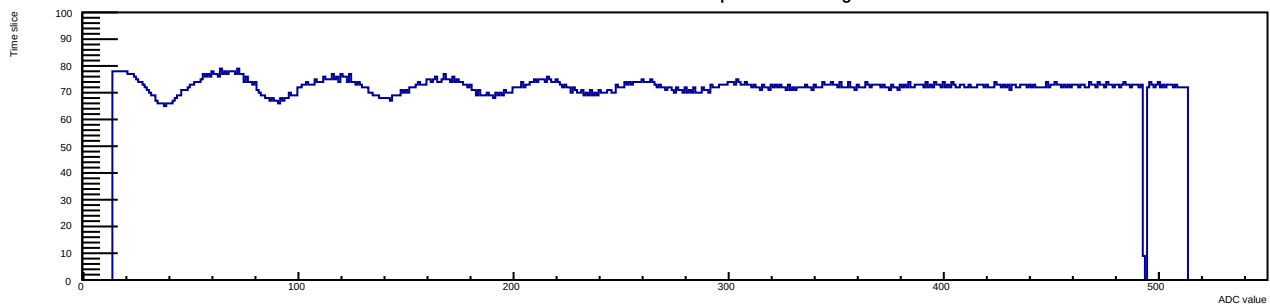
Run 6 Evt 2 Time mcm 1 chip 0 chan 5 tlutrig



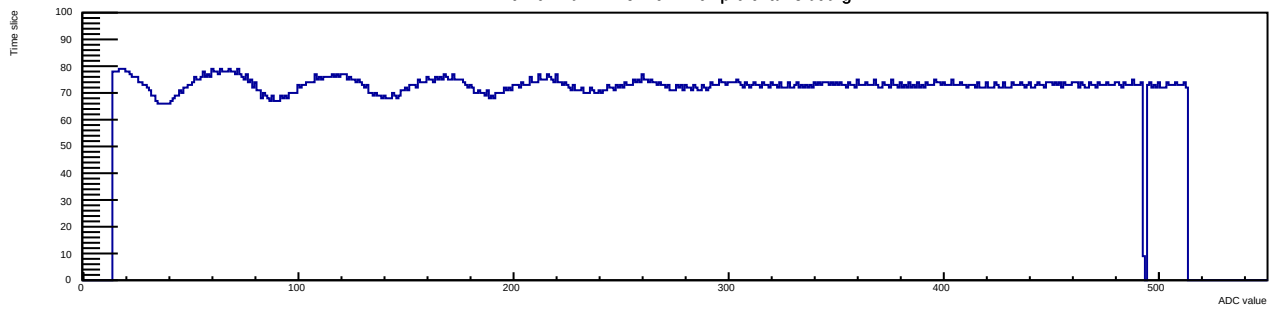
Run 6 Evt 2 Time mcm 1 chip 0 chan 6 tlutrig



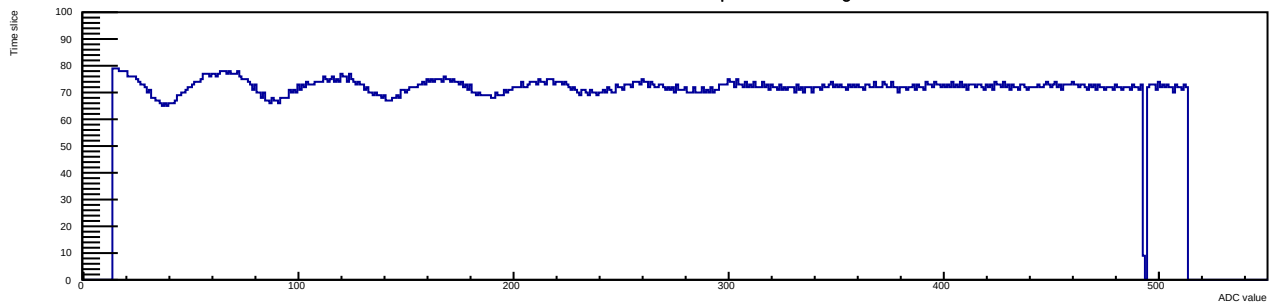
Run 6 Evt 2 Time mcm 1 chip 0 chan 7 tlutrig



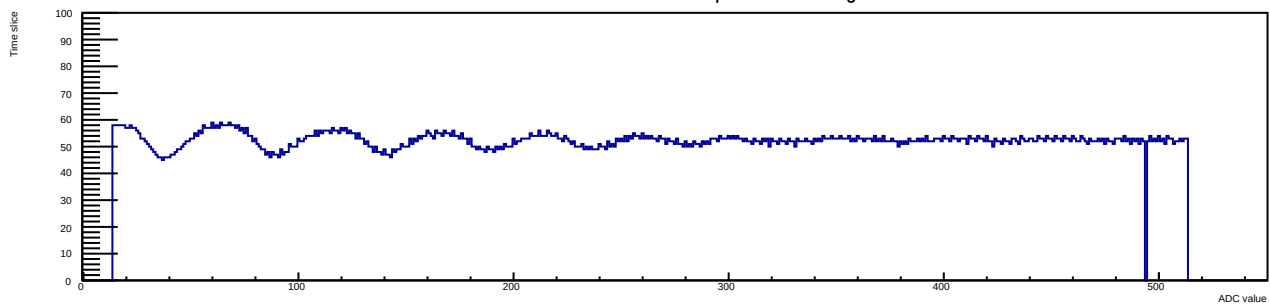
Run 6 Evt 2 Time mcm 1 chip 0 chan 8 tlutrig



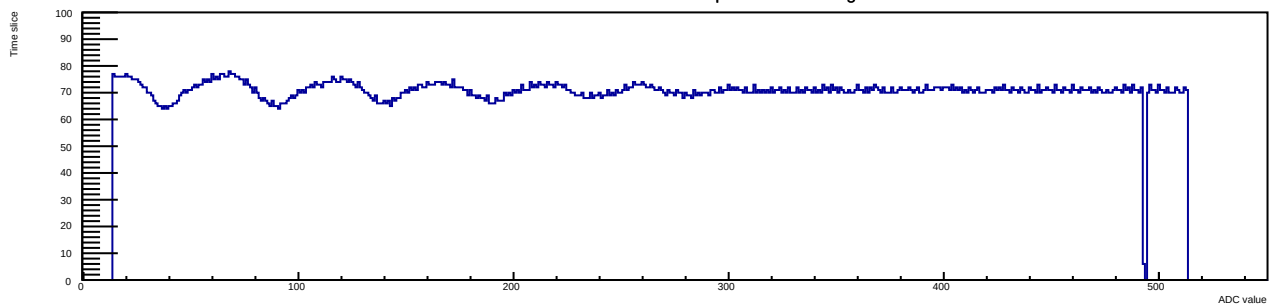
Run 6 Evt 2 Time mcm 1 chip 0 chan 9 tlutrig



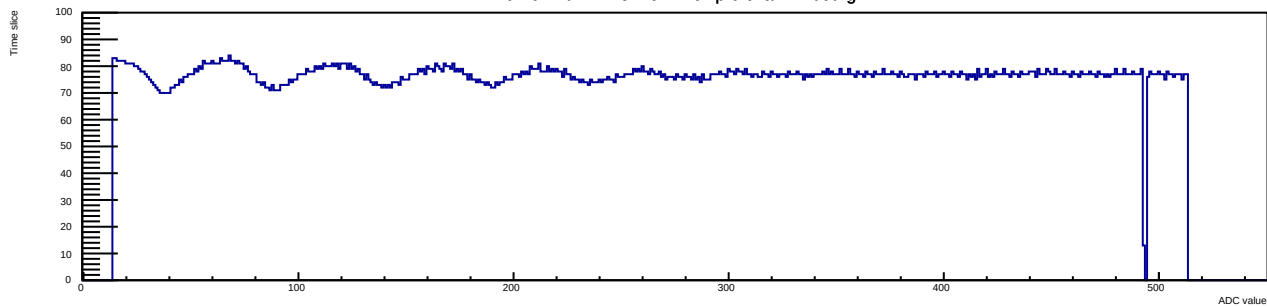
Run 6 Evt 2 Time mcm 1 chip 0 chan 10 tlutrig



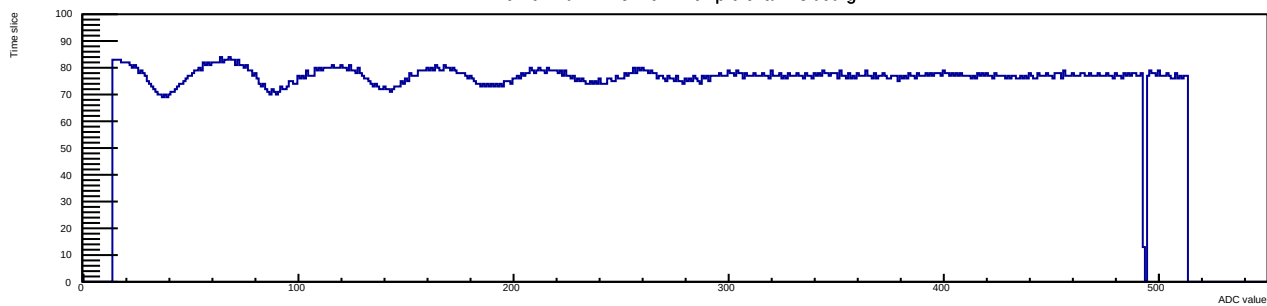
Run 6 Evt 2 Time mcm 1 chip 0 chan 11 tlutrig



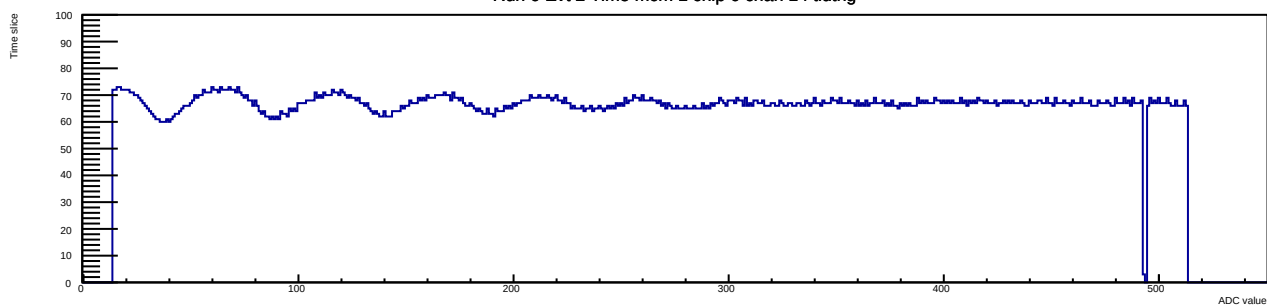
Run 6 Evt 2 Time mcm 1 chip 0 chan 12 tlutrig



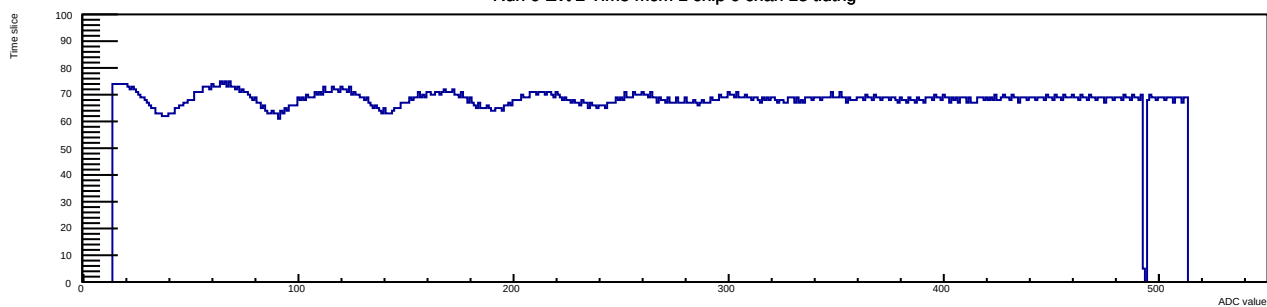
Run 6 Evt 2 Time mcm 1 chip 0 chan 13 tlutrig



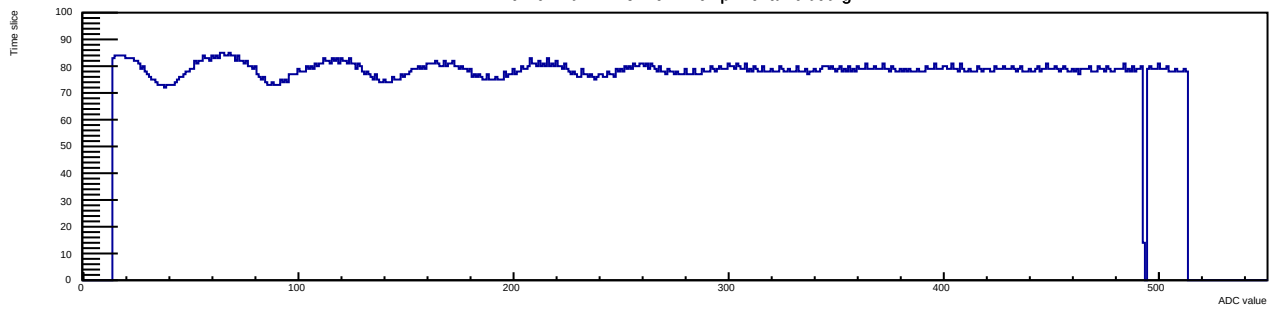
Run 6 Evt 2 Time mcm 1 chip 0 chan 14 tlutrig



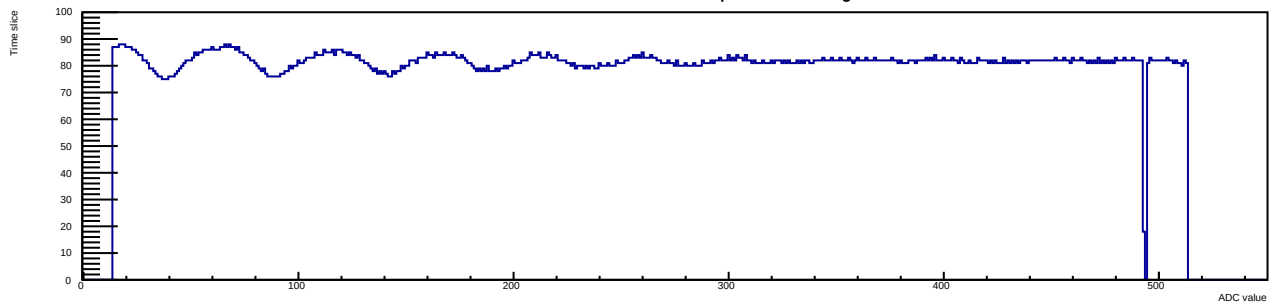
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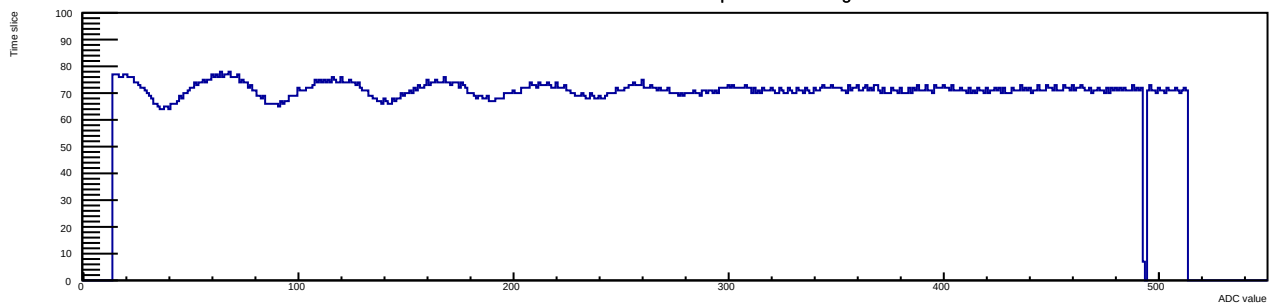
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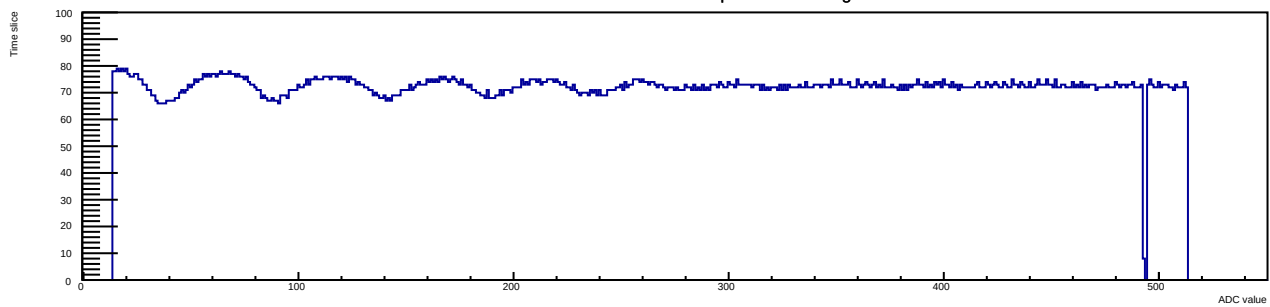
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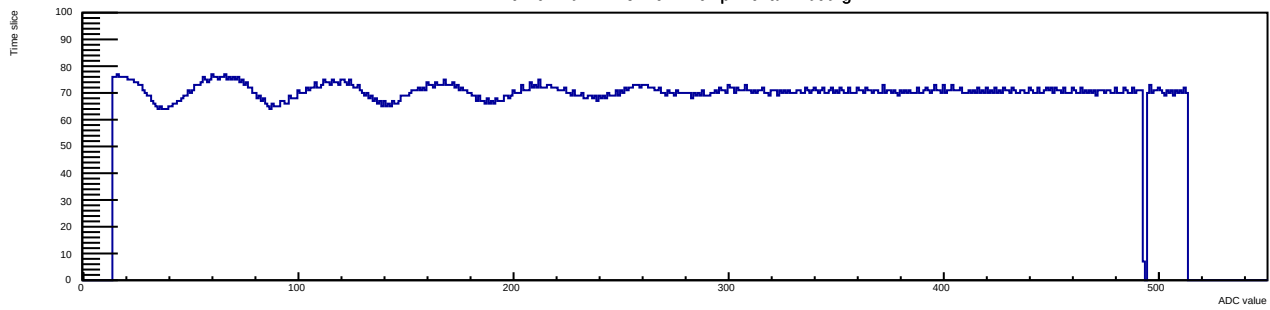
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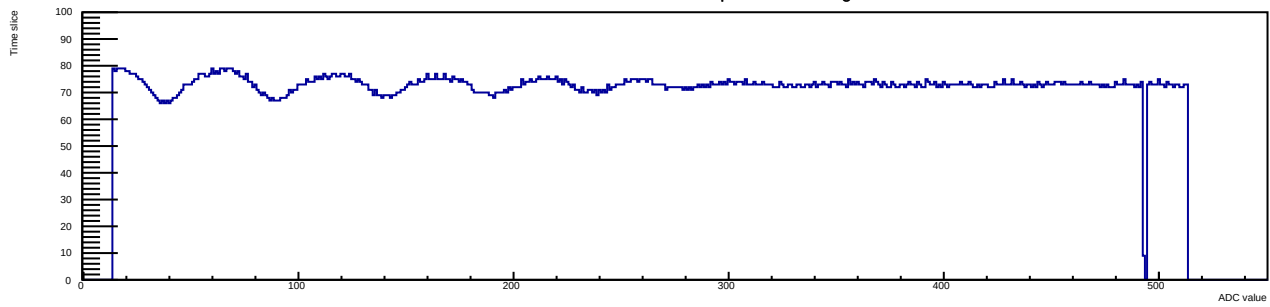
Run 6 Evt 2 Time mcm 1 chip 1 chan 3 tlutrig



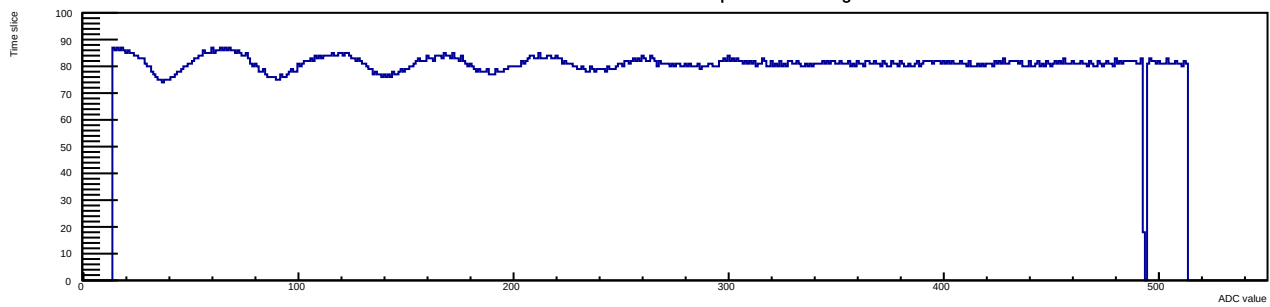
Run 6 Evt 2 Time mcm 1 chip 1 chan 4 tlutrig



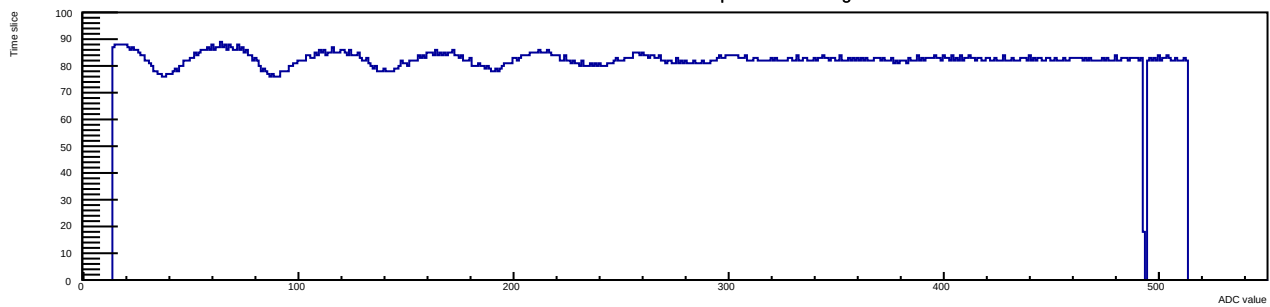
Run 6 Evt 2 Time mcm 1 chip 1 chan 5 tlutrig



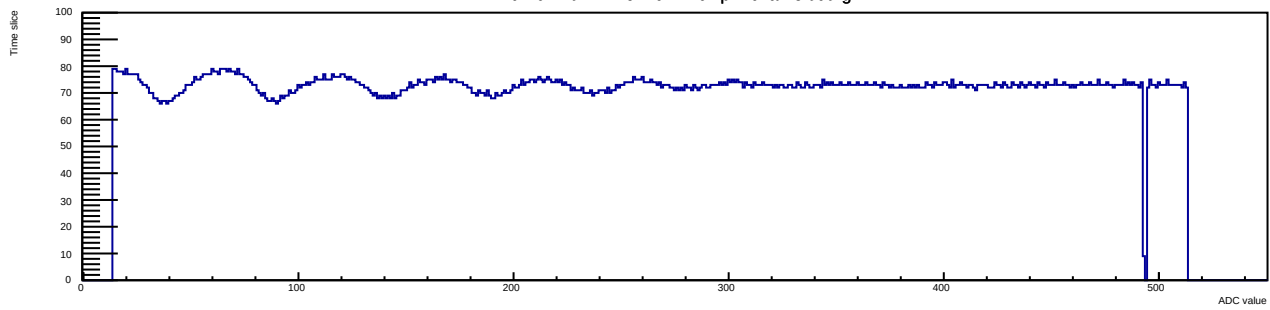
Run 6 Evt 2 Time mcm 1 chip 1 chan 6 tlutrig



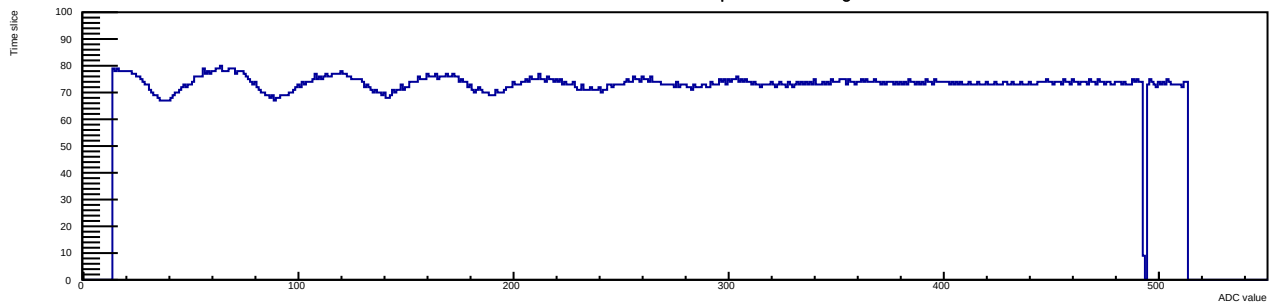
Run 6 Evt 2 Time mcm 1 chip 1 chan 7 tlutrig



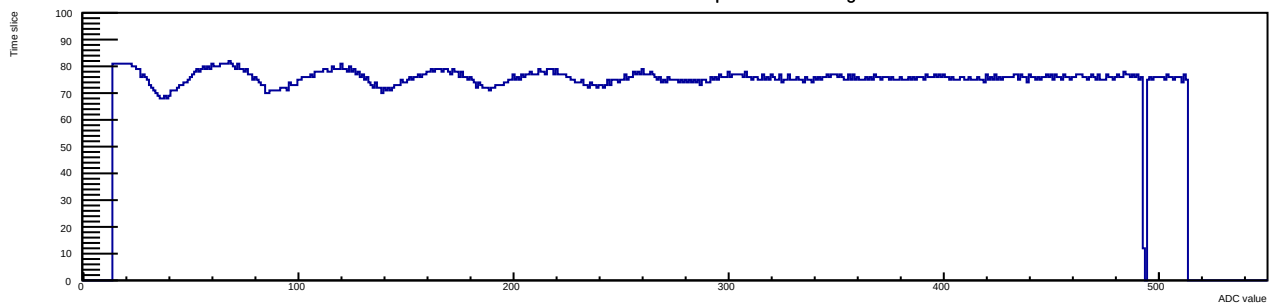
Run 6 Evt 2 Time mcm 1 chip 1 chan 8 tlutrig



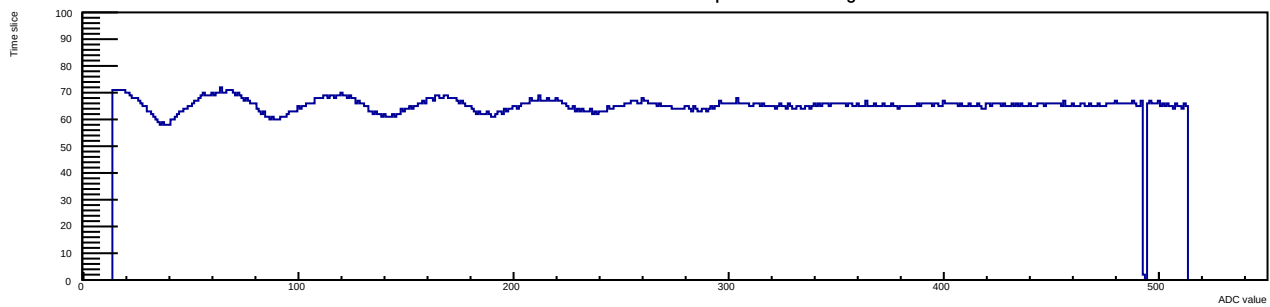
Run 6 Evt 2 Time mcm 1 chip 1 chan 9 tlutrig



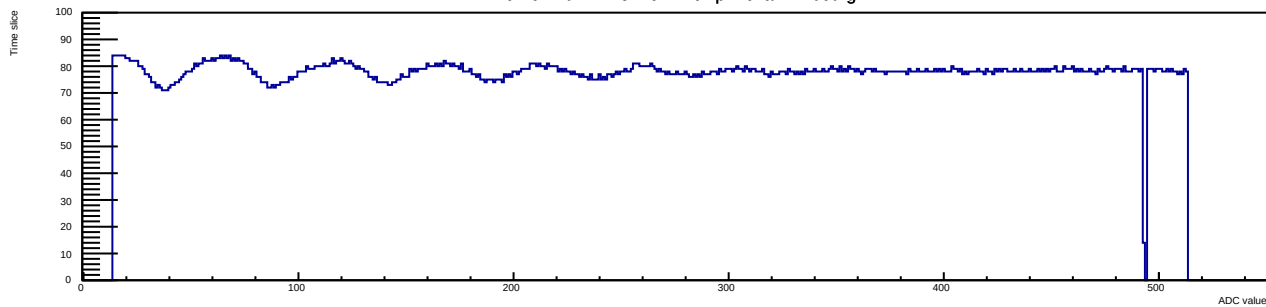
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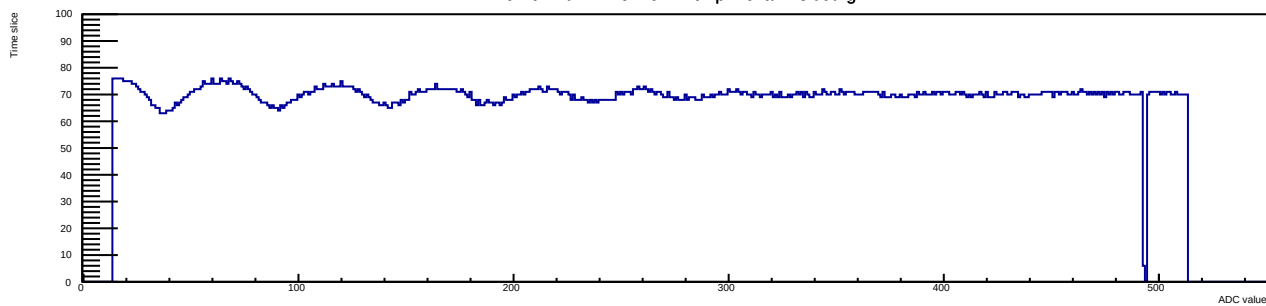
Run 6 Evt 2 Time mcm 1 chip 1 chan 11 tlutrig



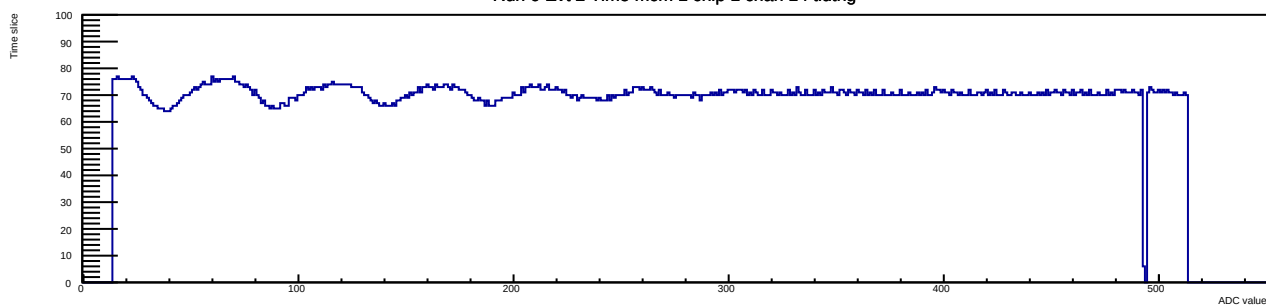
Run 6 Evt 2 Time mcm 1 chip 1 chan 12 tlutrig



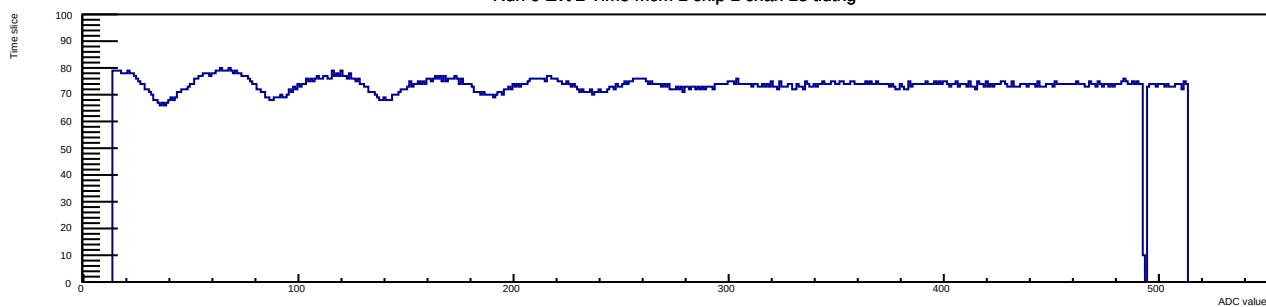
Run 6 Evt 2 Time mcm 1 chip 1 chan 13 tlutrig



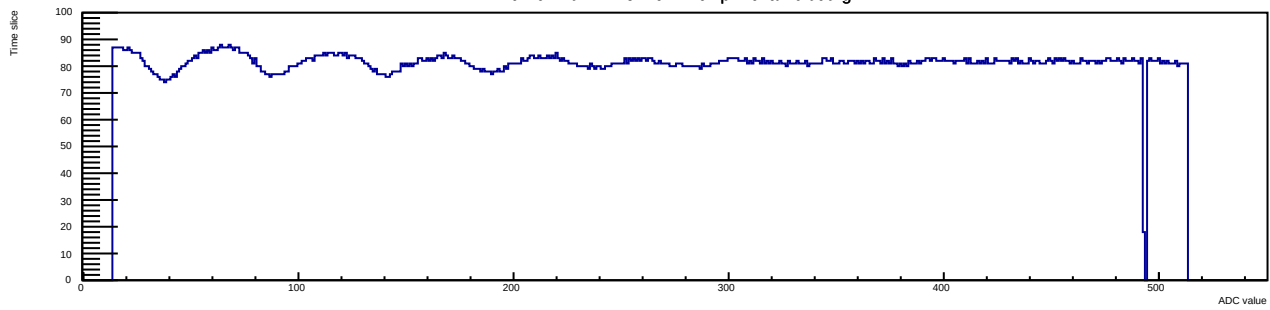
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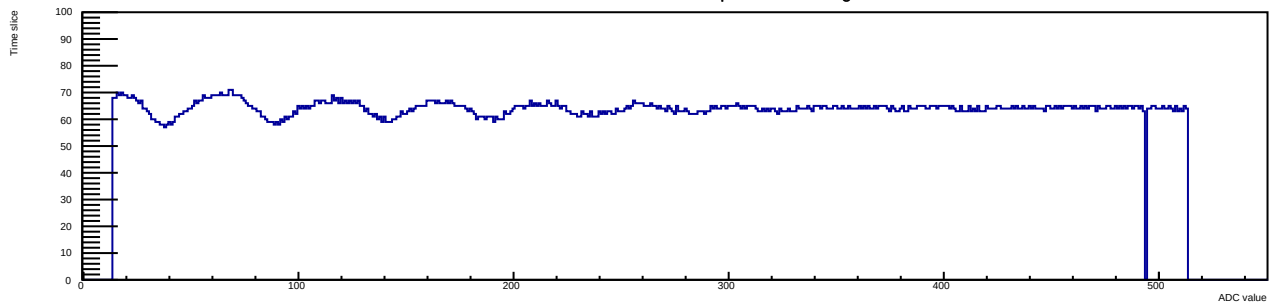
Run 6 Evt 2 Time mcm 1 chip 1 chan 15 tlutrig



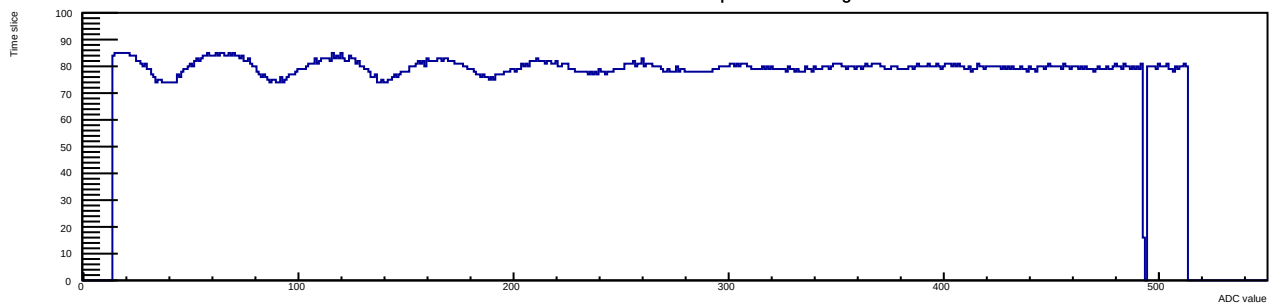
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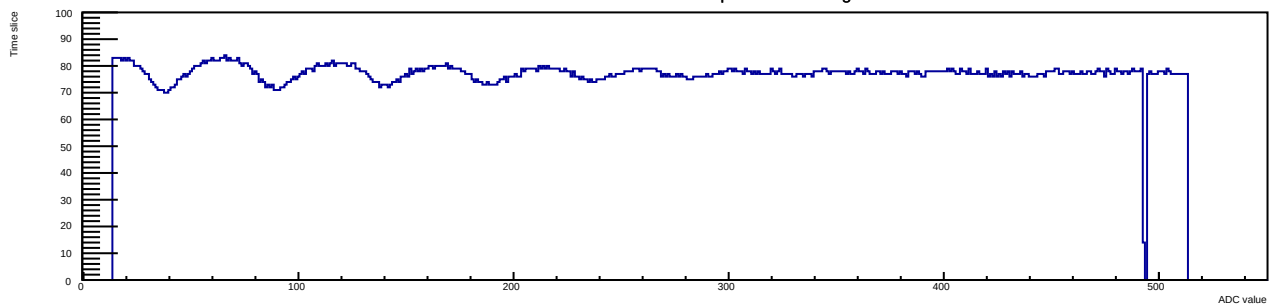
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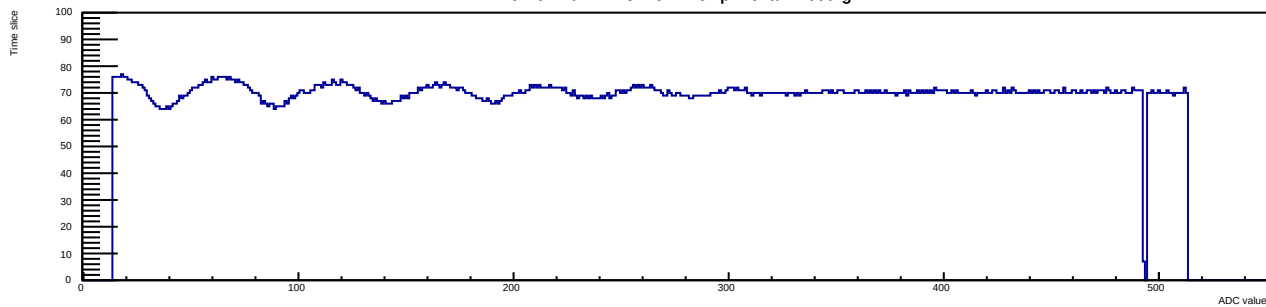
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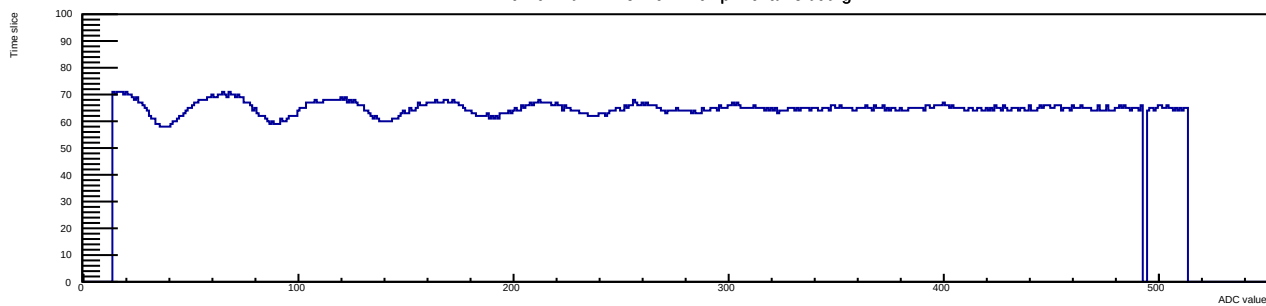
Run 6 Evt 2 Time mcm 1 chip 2 chan 3 tlutrig



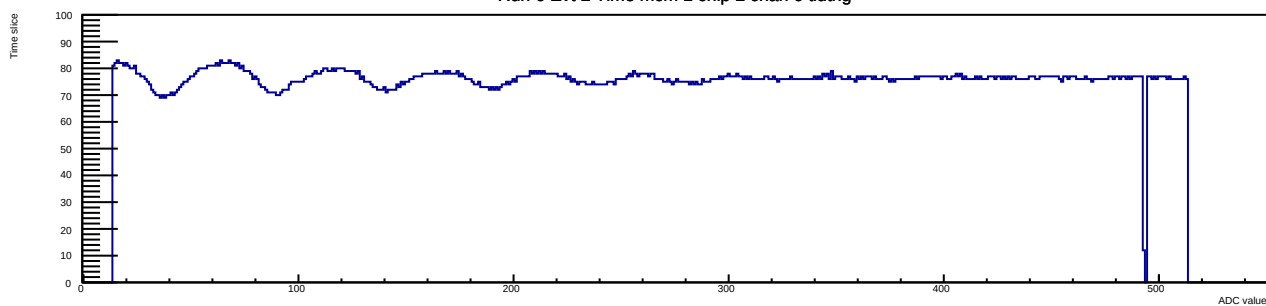
Run 6 Evt 2 Time mcm 1 chip 2 chan 4 tlutrig



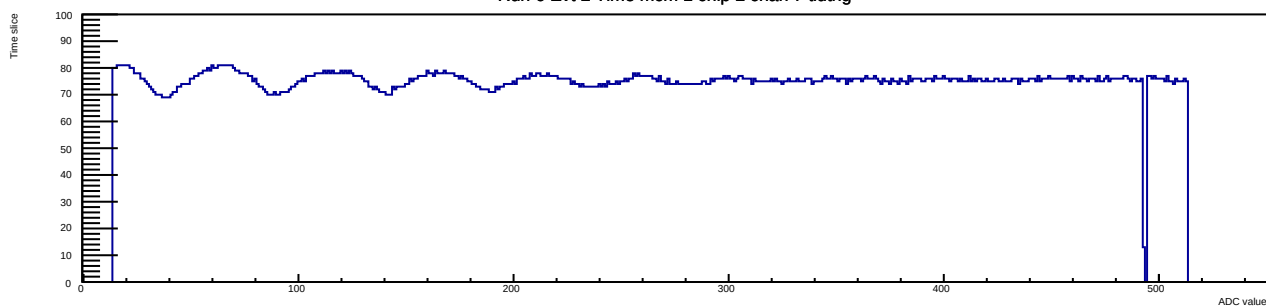
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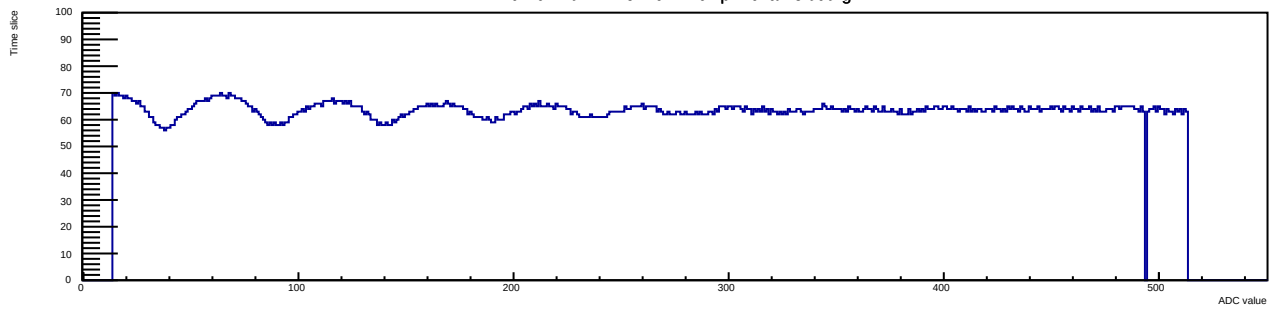
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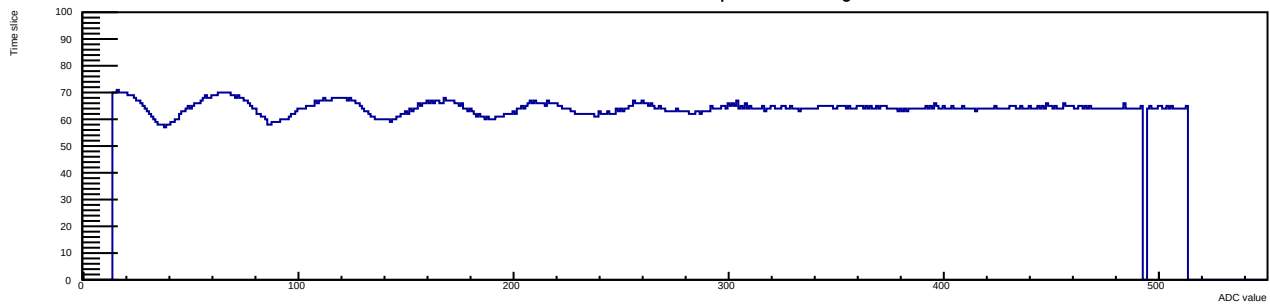
Run 6 Evt 2 Time mcm 1 chip 2 chan 7 tlutrig



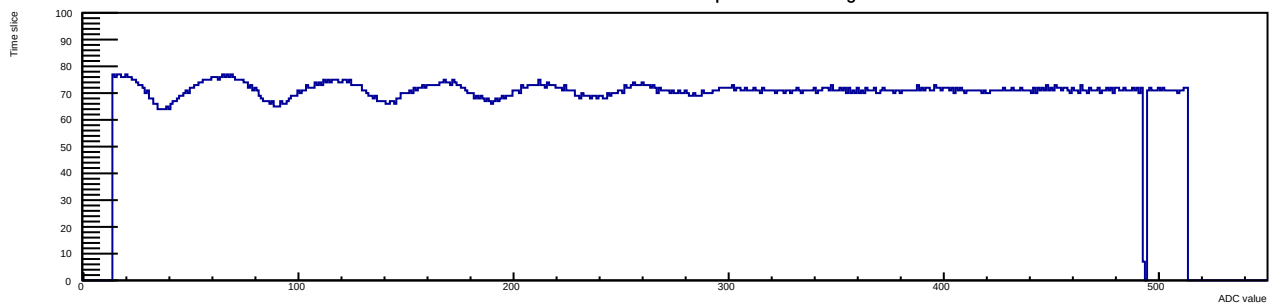
Run 6 Evt 2 Time mcm 1 chip 2 chan 8 tlutrig



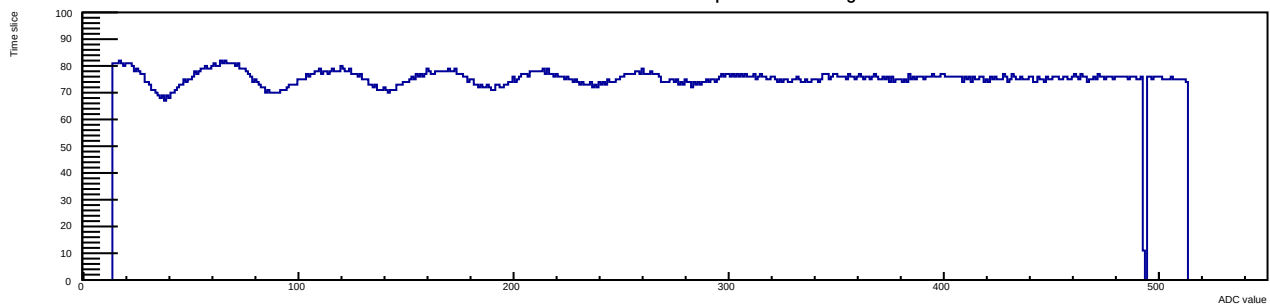
Run 6 Evt 2 Time mcm 1 chip 2 chan 9 tlutrig



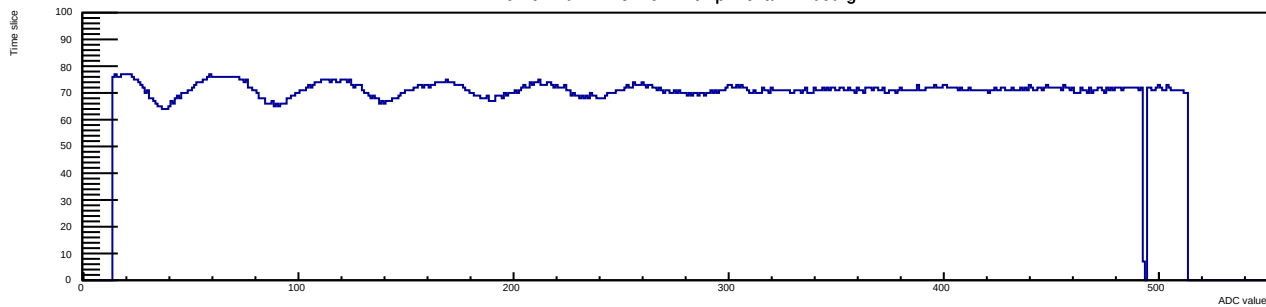
Run 6 Evt 2 Time mcm 1 chip 2 chan 10 tlutrig



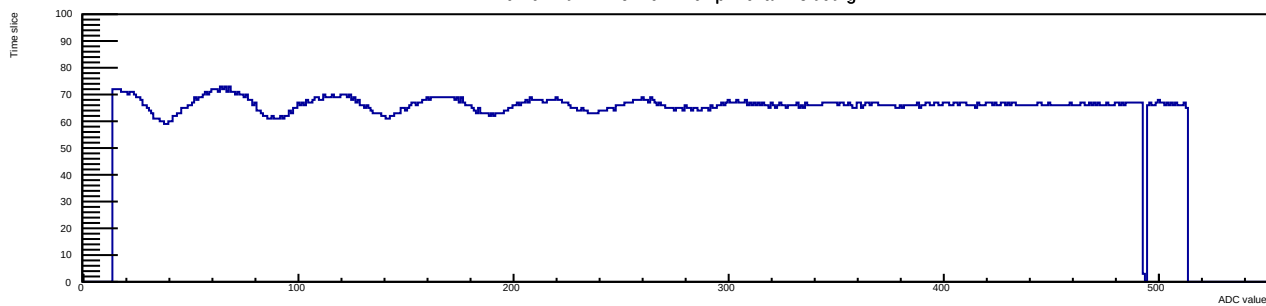
Run 6 Evt 2 Time mcm 1 chip 2 chan 11 tlutrig



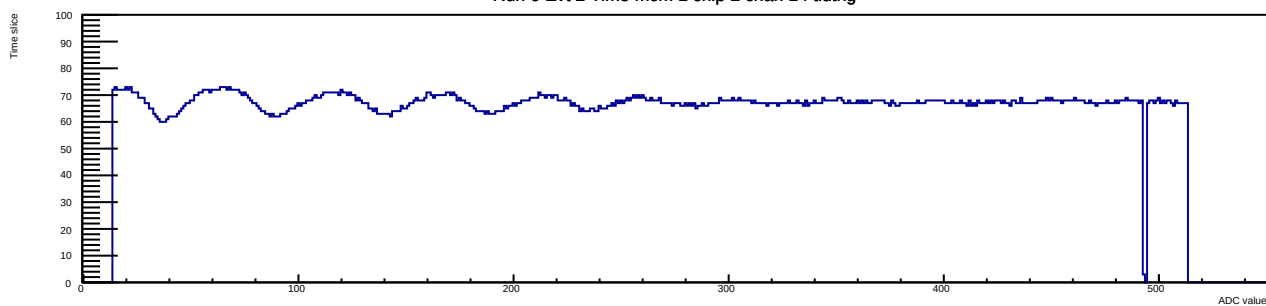
Run 6 Evt 2 Time mcm 1 chip 2 chan 12 tlutrig



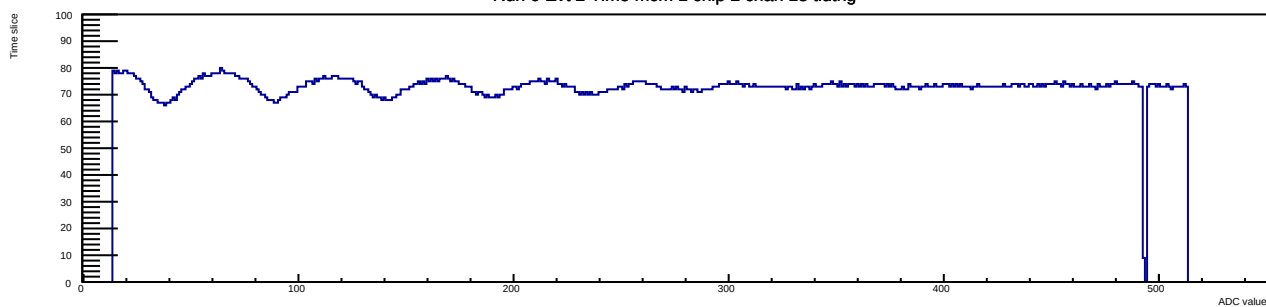
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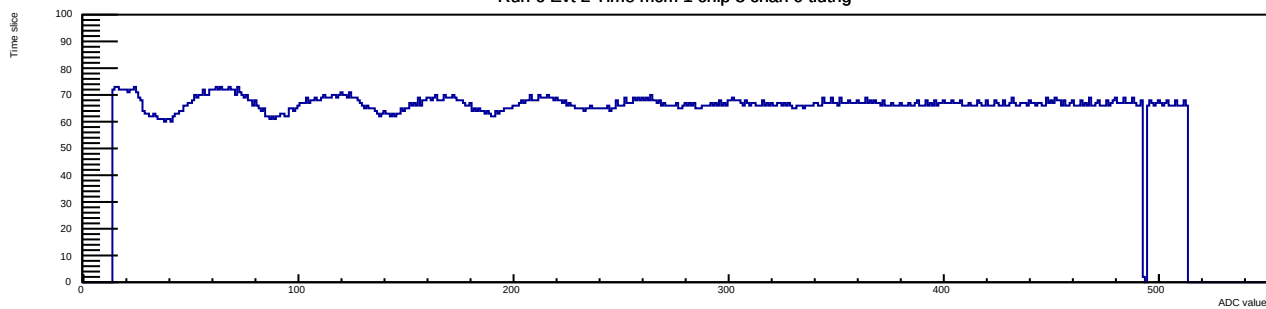
Run 6 Evt 2 Time mcm 1 chip 2 chan 14 tlutrig



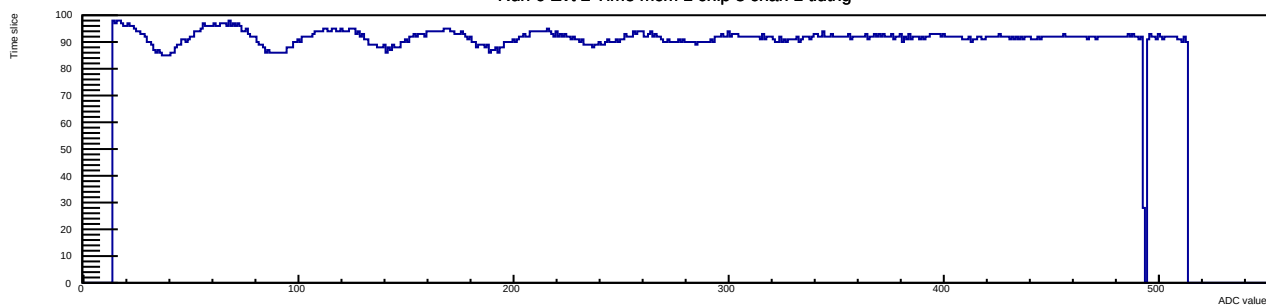
Run 6 Evt 2 Time mcm 1 chip 2 chan 15 tlutrig



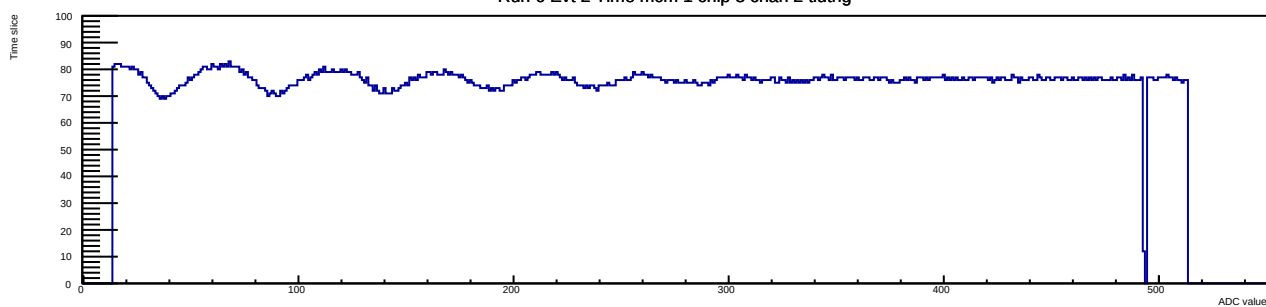
Run 6 Evt 2 Time mcm 1 chip 3 chan 0 tlutrig



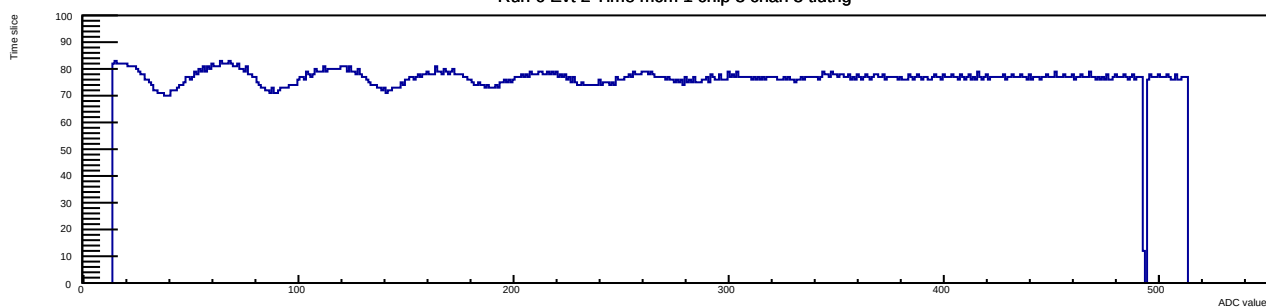
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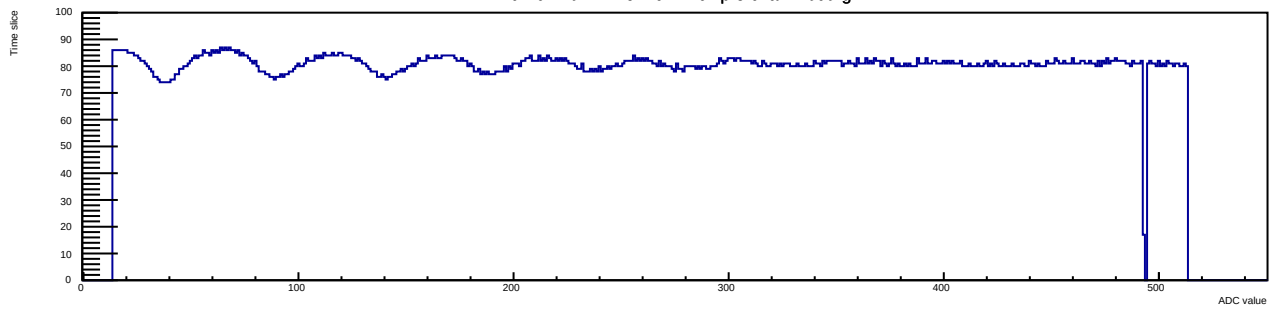
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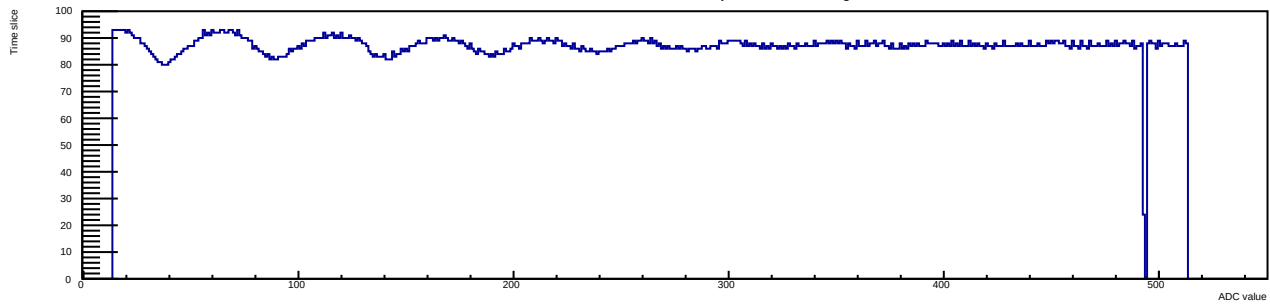
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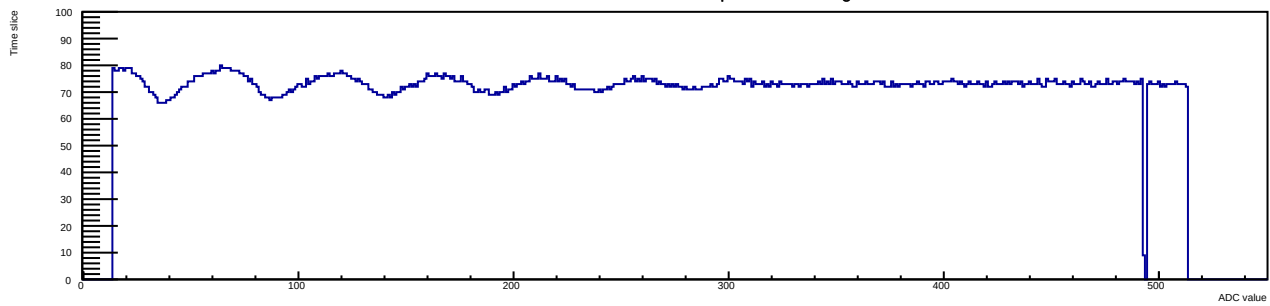
Run 6 Evt 2 Time mcm 1 chip 3 chan 4 tlutrig



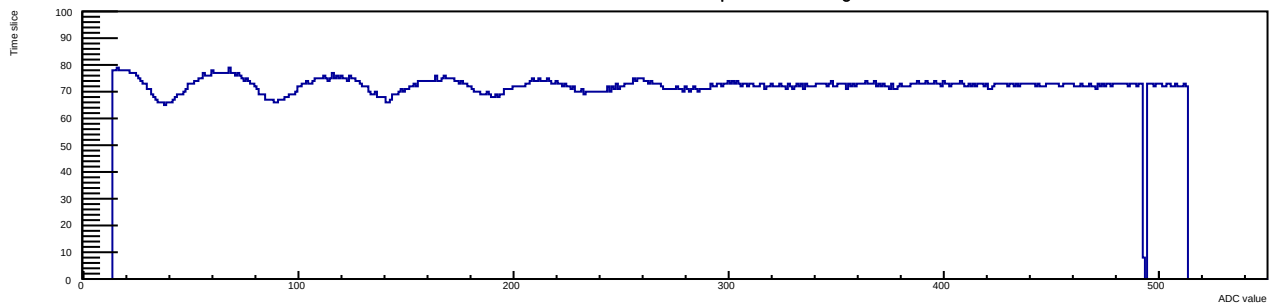
Run 6 Evt 2 Time mcm 1 chip 3 chan 5 tlutrig



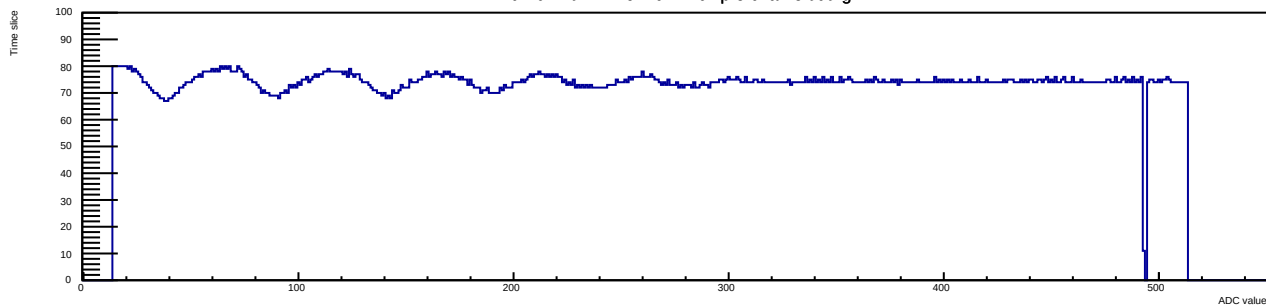
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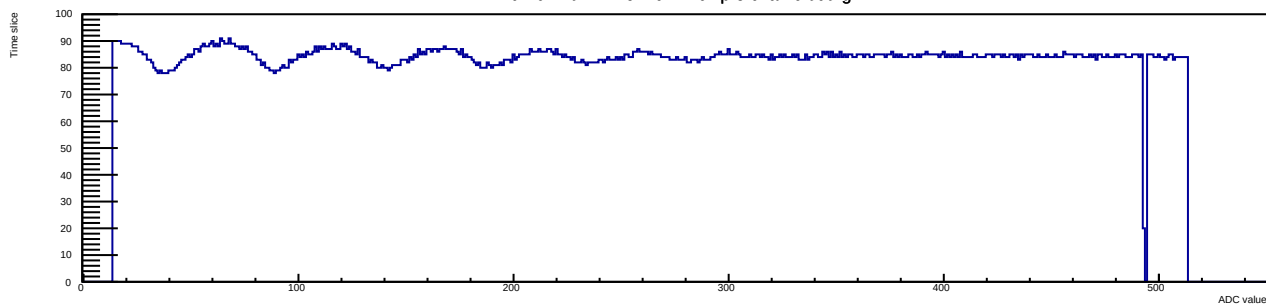
Run 6 Evt 2 Time mcm 1 chip 3 chan 7 tlutrig



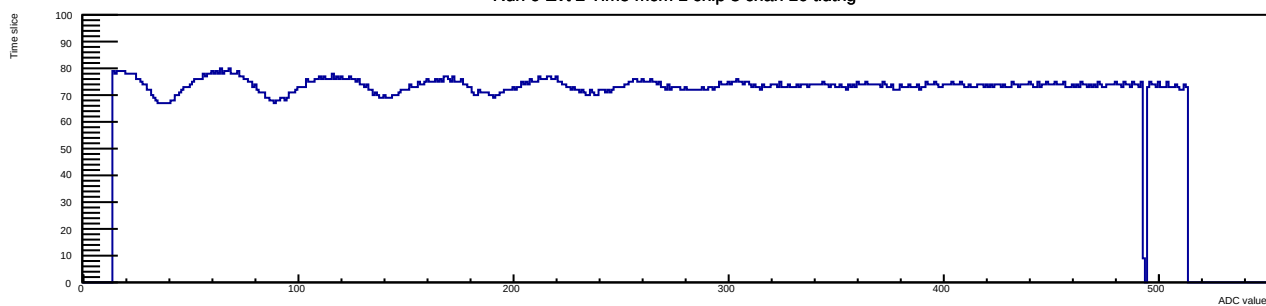
Run 6 Evt 2 Time mcm 1 chip 3 chan 8 tlutrig



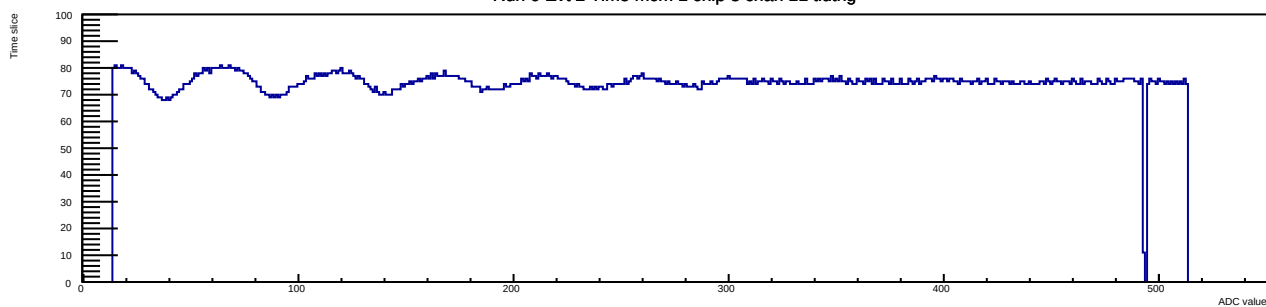
Run 6 Evt 2 Time mcm 1 chip 3 chan 9 tlutrig



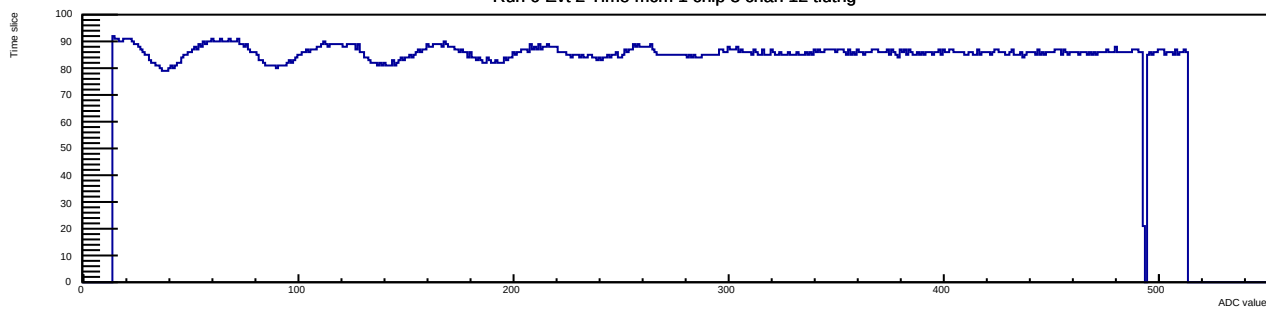
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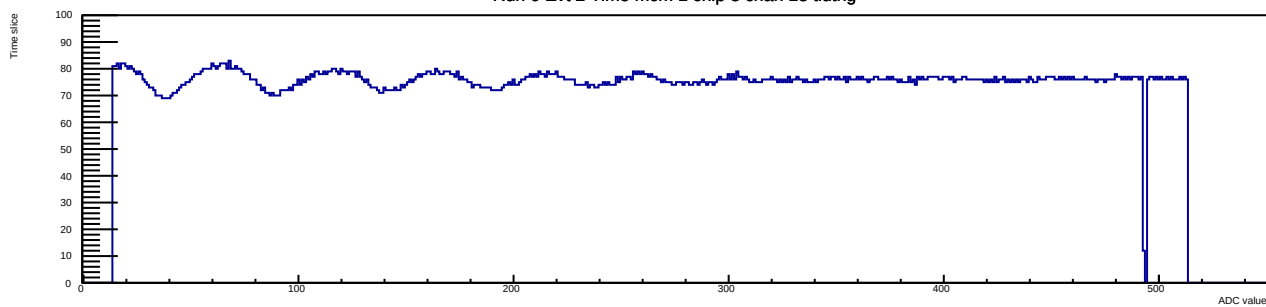
Run 6 Evt 2 Time mcm 1 chip 3 chan 11 tlutrig



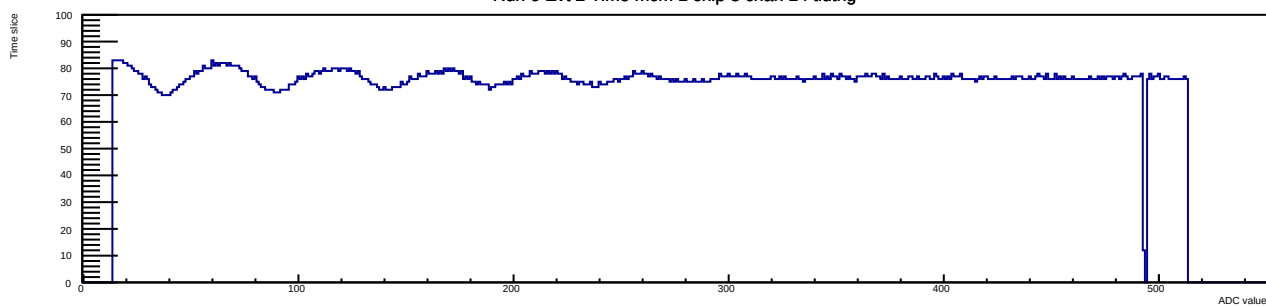
Run 6 Evt 2 Time mcm 1 chip 3 chan 12 tlutrig



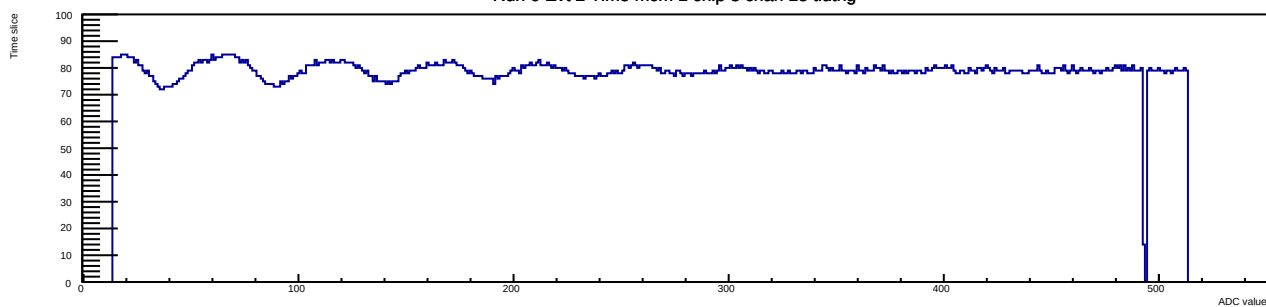
Run 6 Evt 2 Time mcm 1 chip 3 chan 13 tlutrig



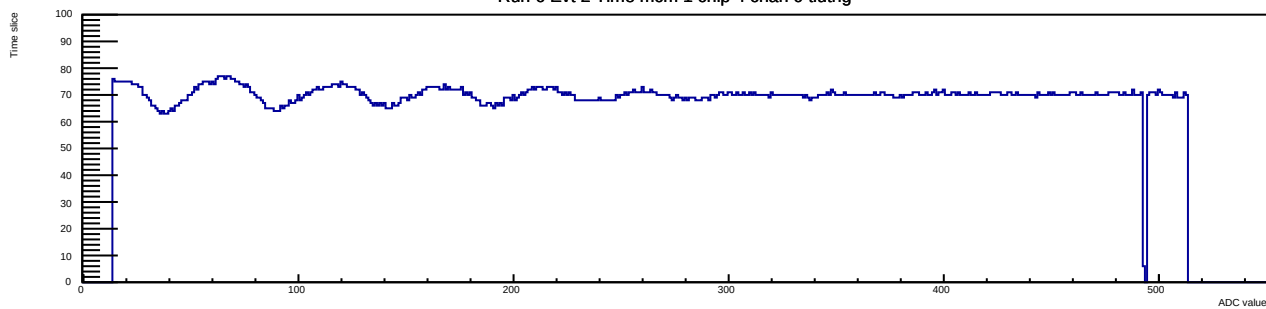
Run 6 Evt 2 Time mcm 1 chip 3 chan 14 tlutrig



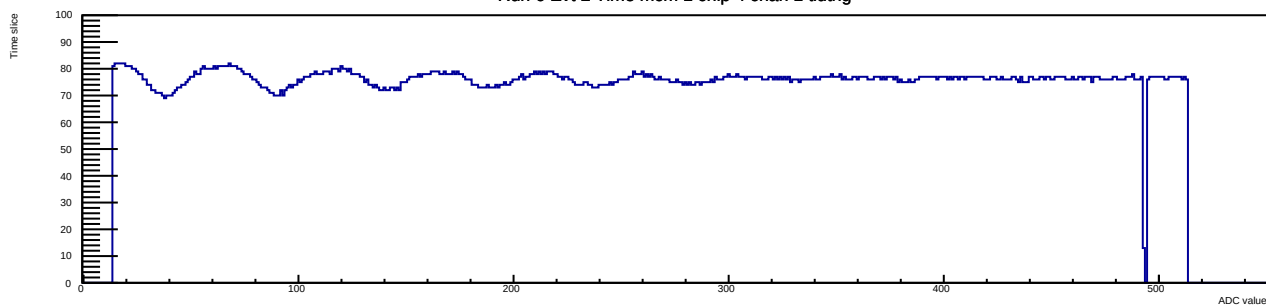
Run 6 Evt 2 Time mcm 1 chip 3 chan 15 tlutrig



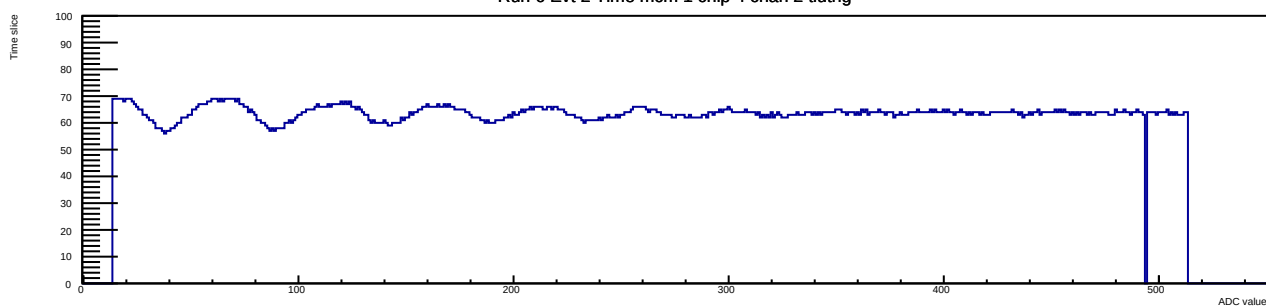
Run 6 Evt 2 Time mcm 1 chip 4 chan 0 tlutrig



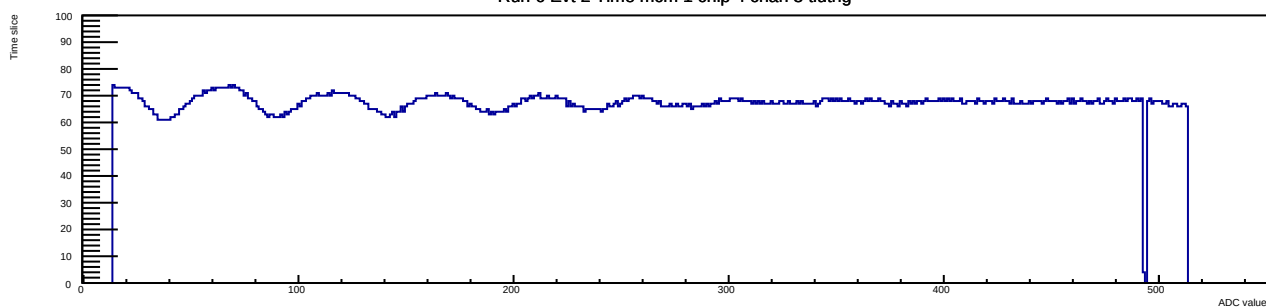
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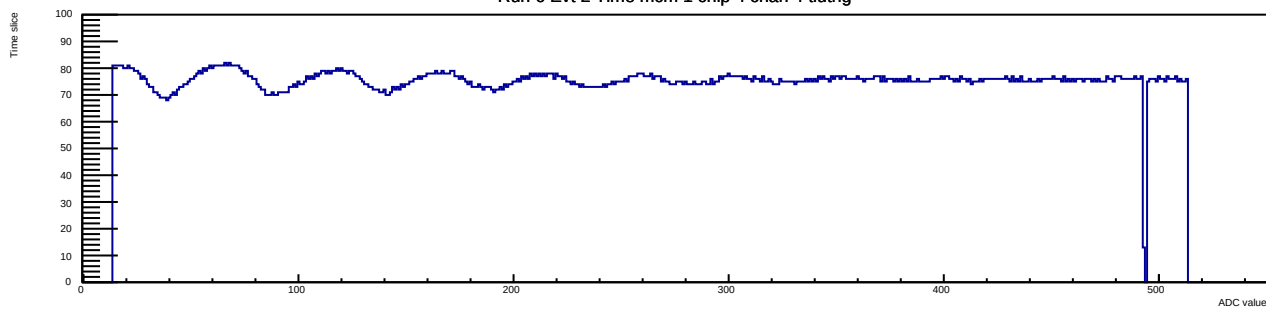
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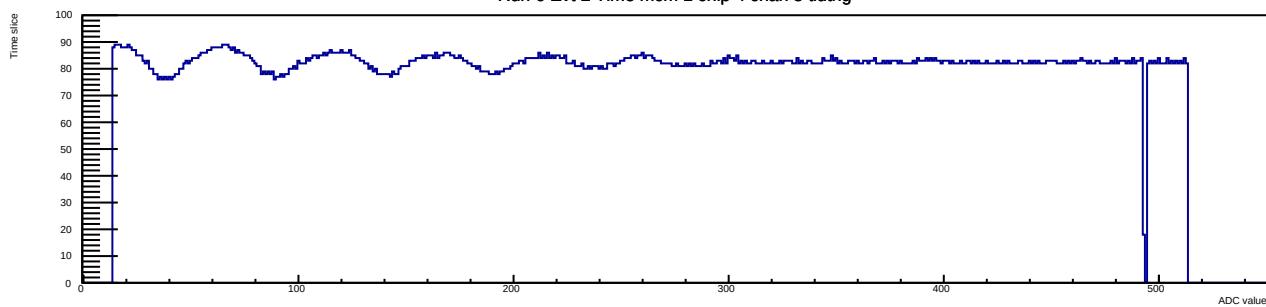
Run 6 Evt 2 Time mcm 1 chip 4 chan 3 tlutrig



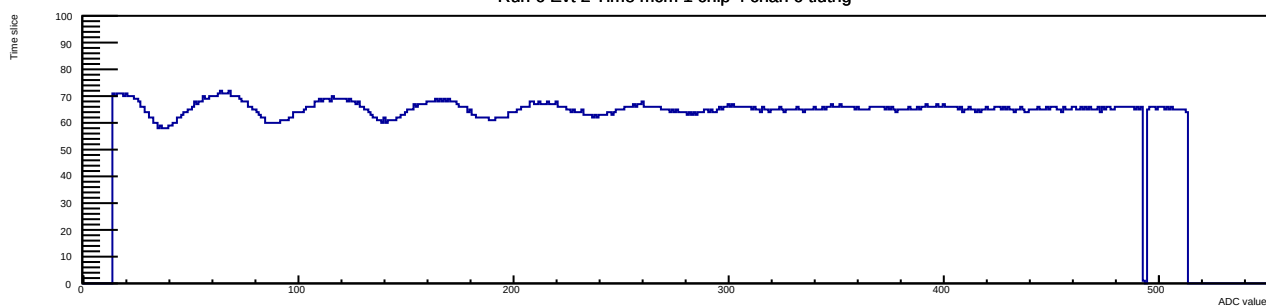
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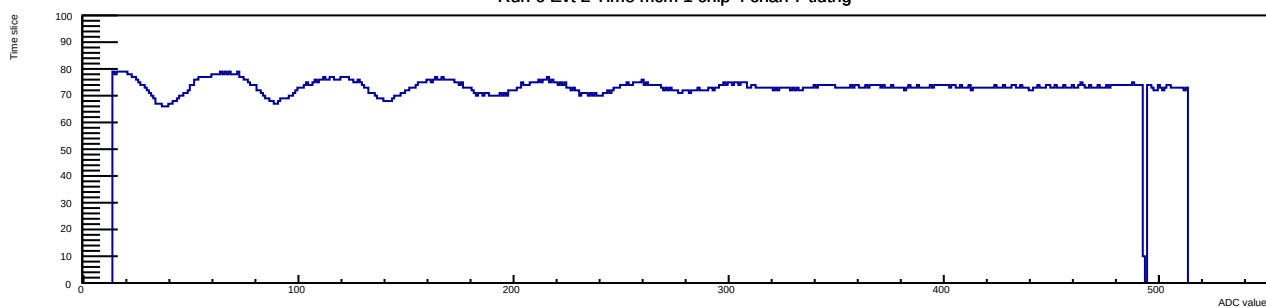
Run 6 Evt 2 Time mcm 1 chip 4 chan 5 tlutrig



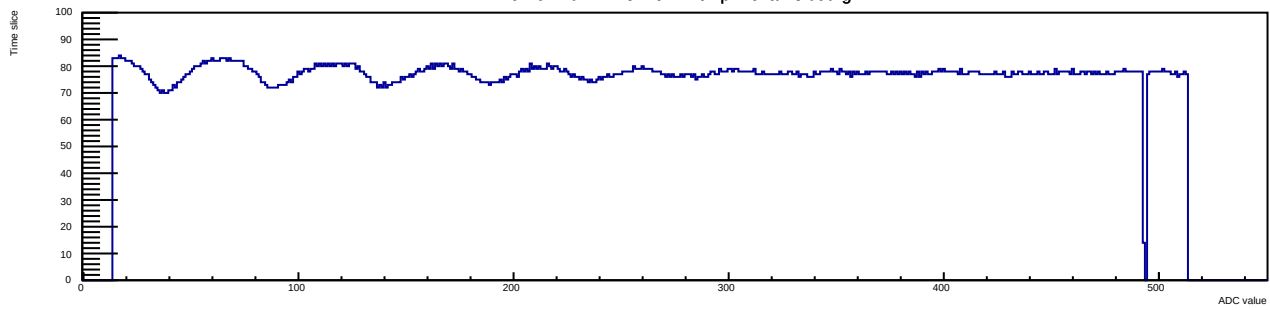
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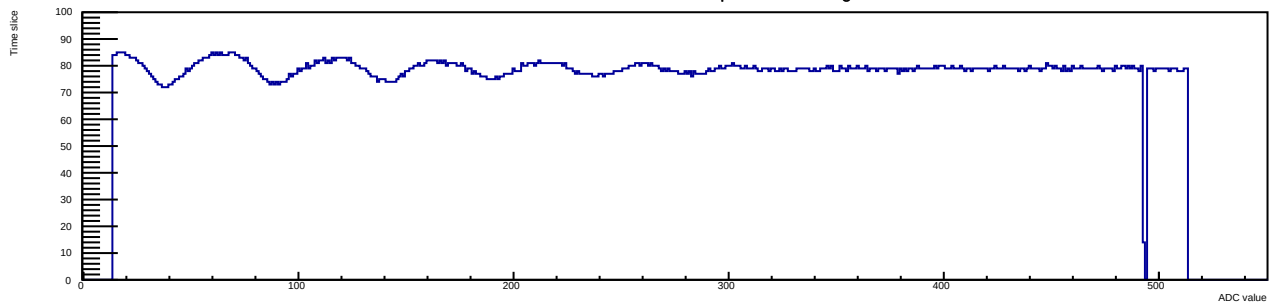
Run 6 Evt 2 Time mcm 1 chip 4 chan 7 tlutrig



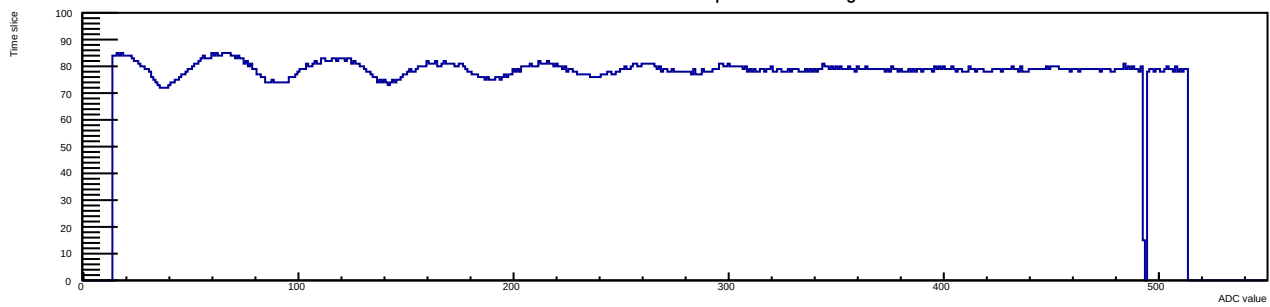
Run 6 Evt 2 Time mcm 1 chip 4 chan 8 tlutrig



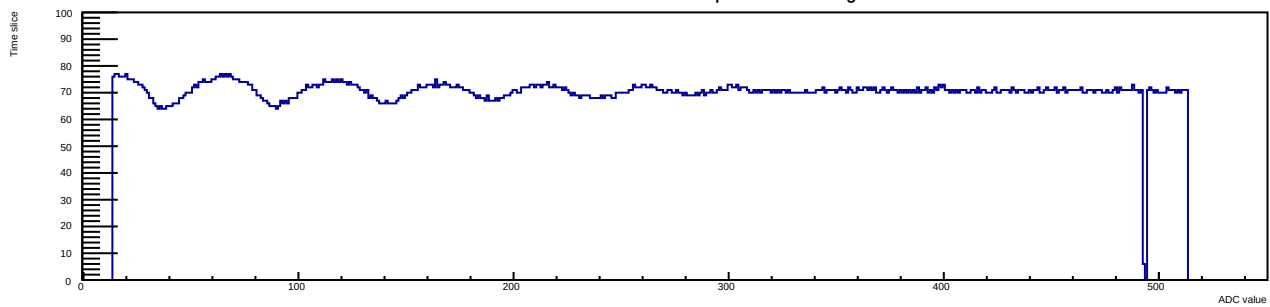
Run 6 Evt 2 Time mcm 1 chip 4 chan 9 tlutrig



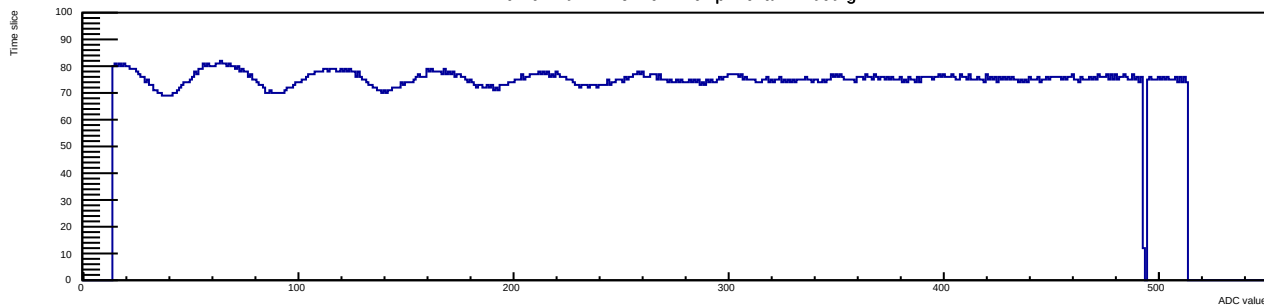
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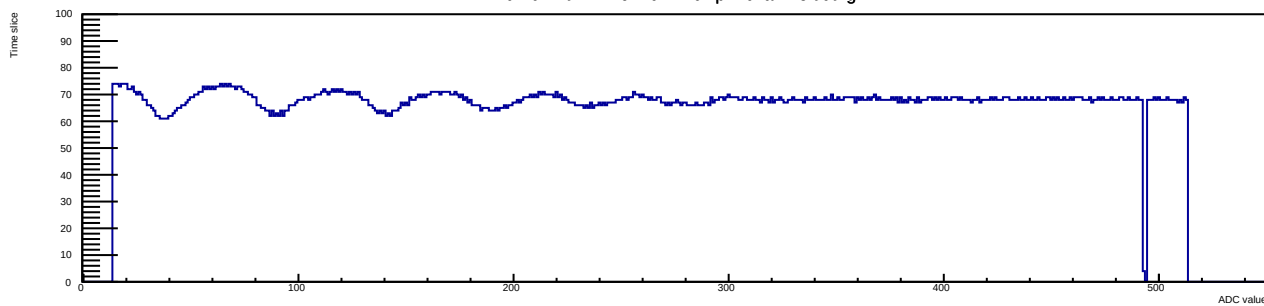
Run 6 Evt 2 Time mcm 1 chip 4 chan 11 tlutrig



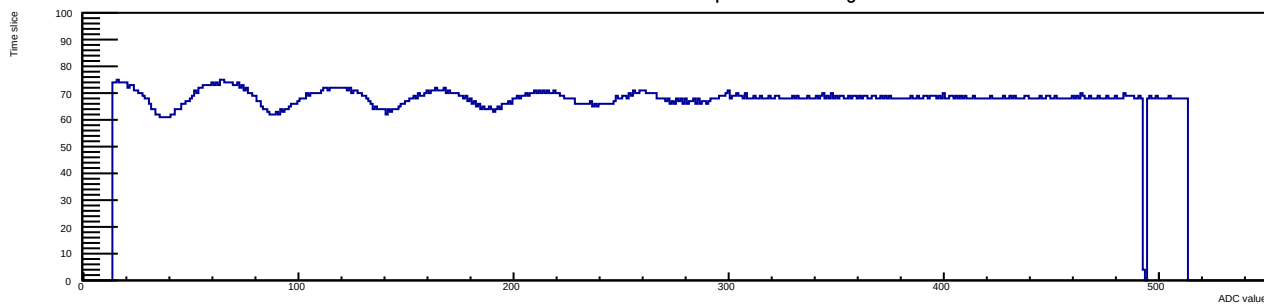
Run 6 Evt 2 Time mcm 1 chip 4 chan 12 tlutrig



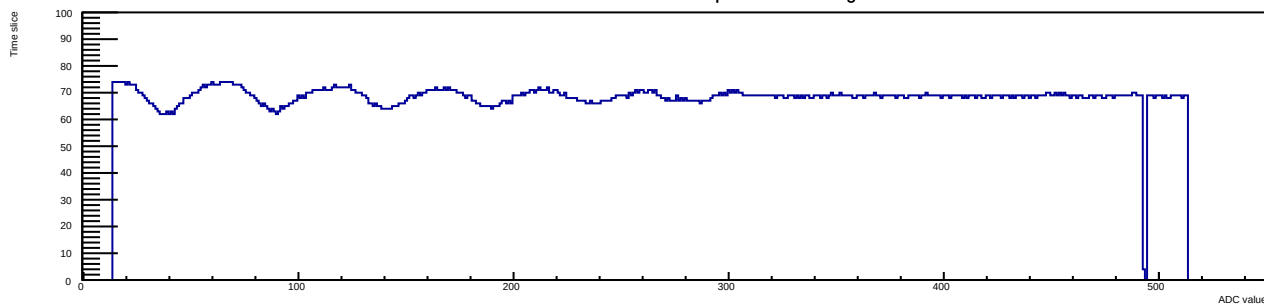
Run 6 Evt 2 Time mcm 1 chip 4 chan 13 tlutrig



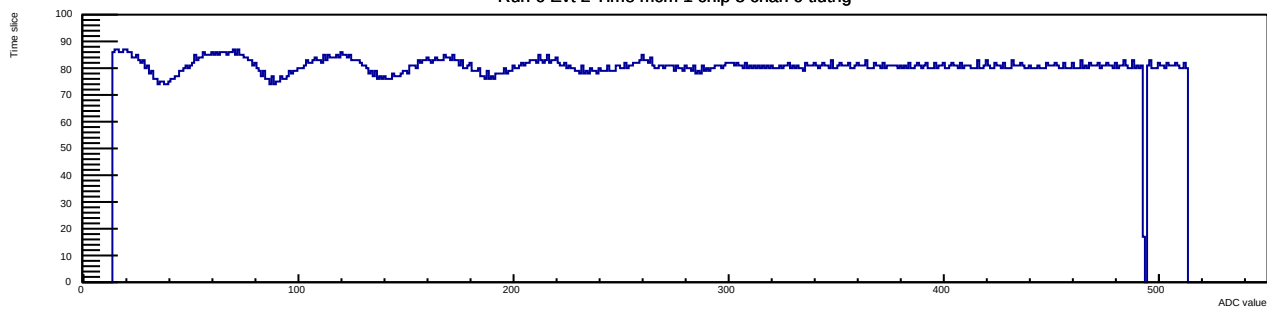
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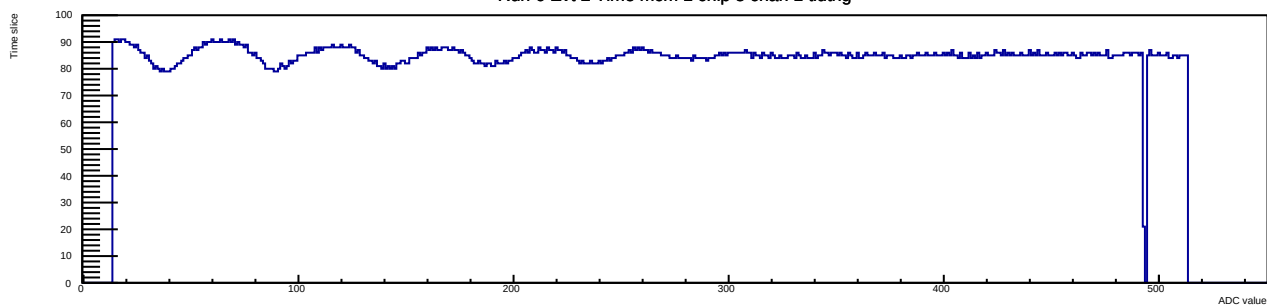
Run 6 Evt 2 Time mcm 1 chip 4 chan 15 tlutrig



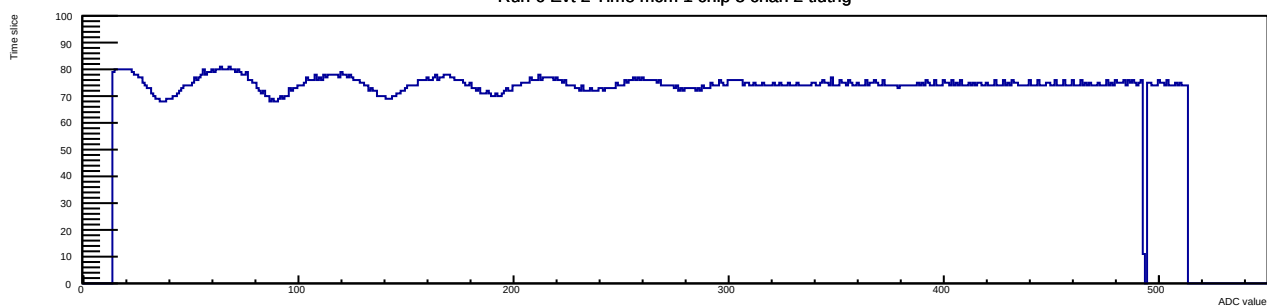
Run 6 Evt 2 Time mcm 1 chip 5 chan 0 tlutrig



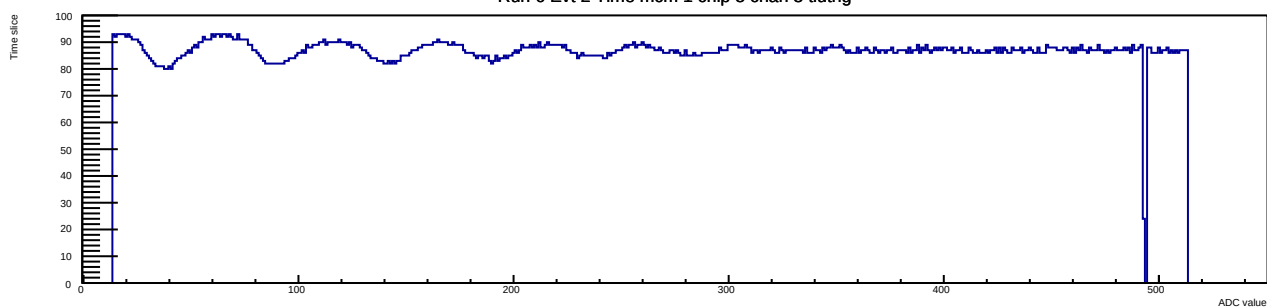
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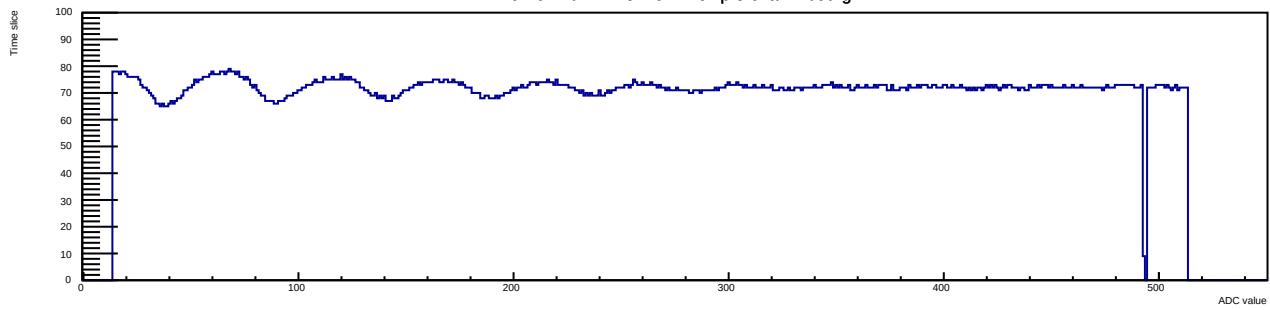
Run 6 Evt 2 Time mcm 1 chip 5 chan 2 tlutrig



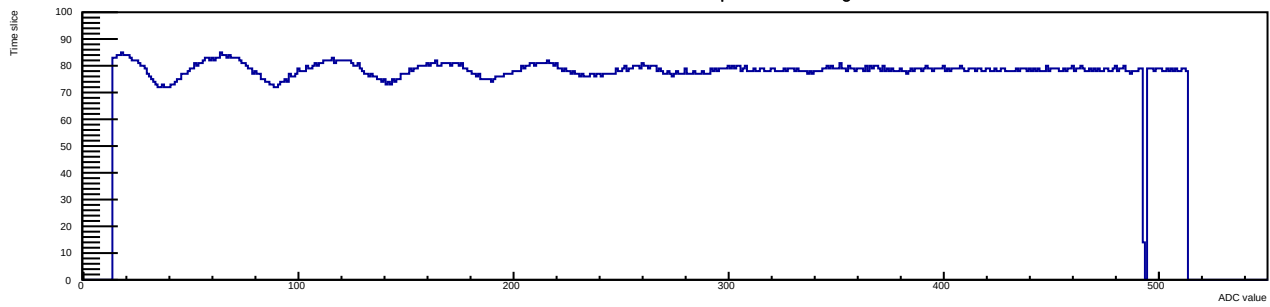
Run 6 Evt 2 Time mcm 1 chip 5 chan 3 tlutrig



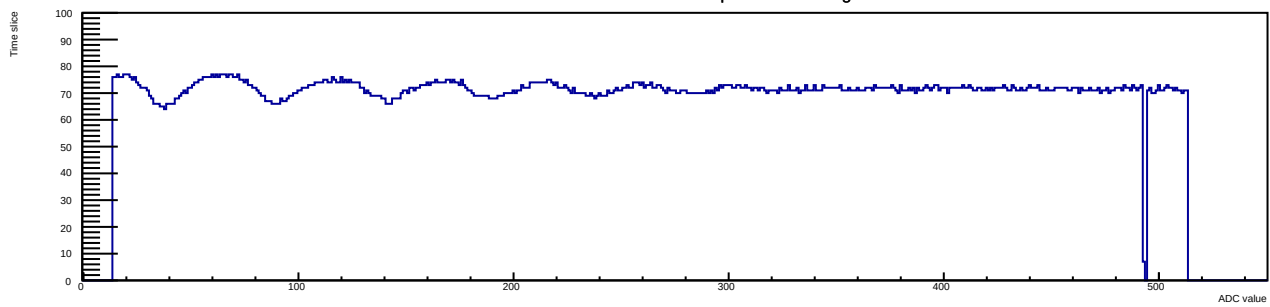
Run 6 Evt 2 Time mcm 1 chip 5 chan 4 tlutrig



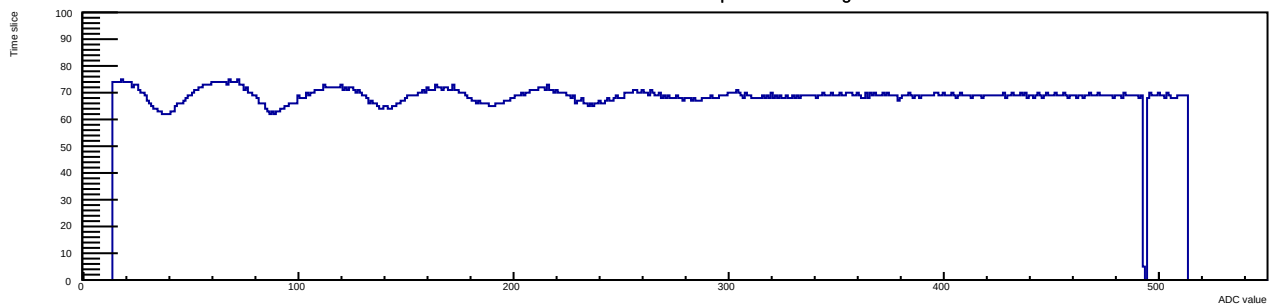
Run 6 Evt 2 Time mcm 1 chip 5 chan 5 tlutrig



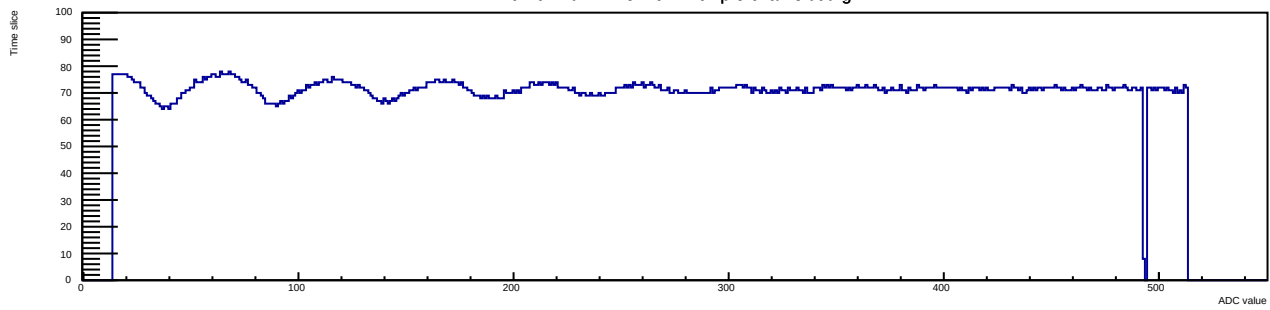
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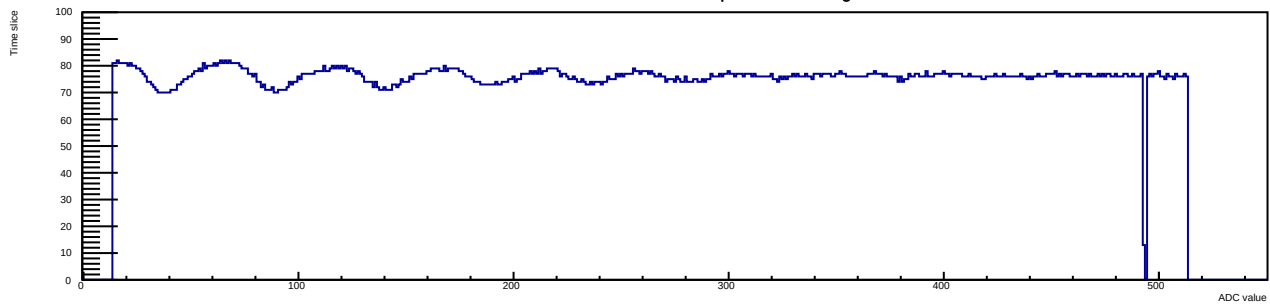
Run 6 Evt 2 Time mcm 1 chip 5 chan 7 tlutrig



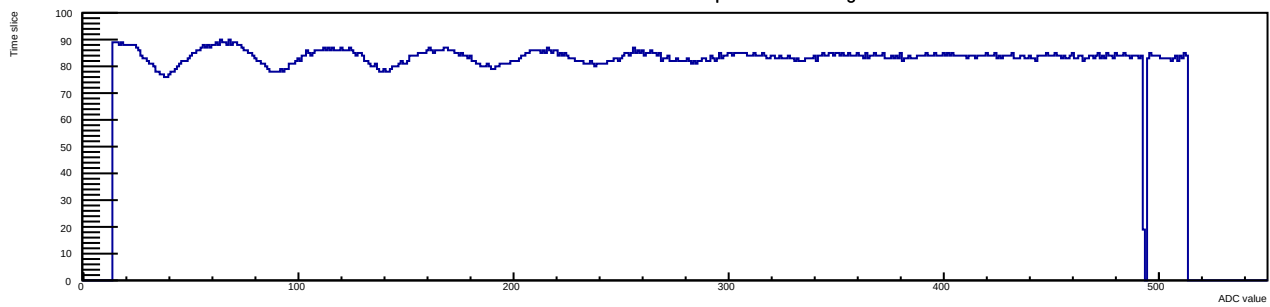
Run 6 Evt 2 Time mcm 1 chip 5 chan 8 tlutrig



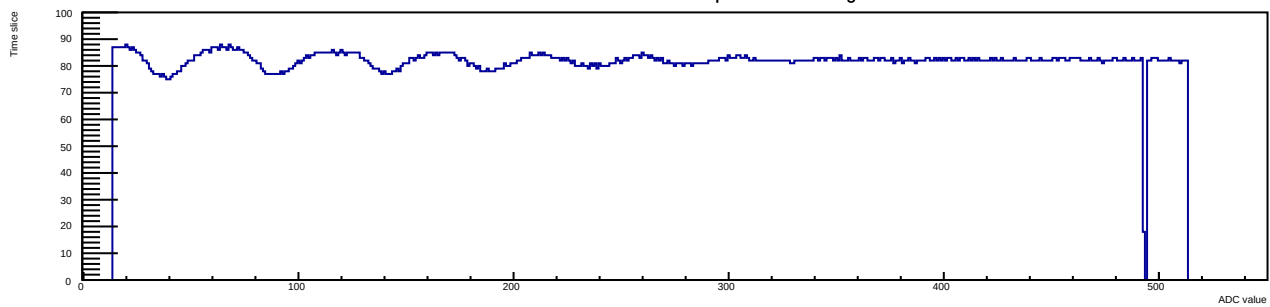
Run 6 Evt 2 Time mcm 1 chip 5 chan 9 tlutrig



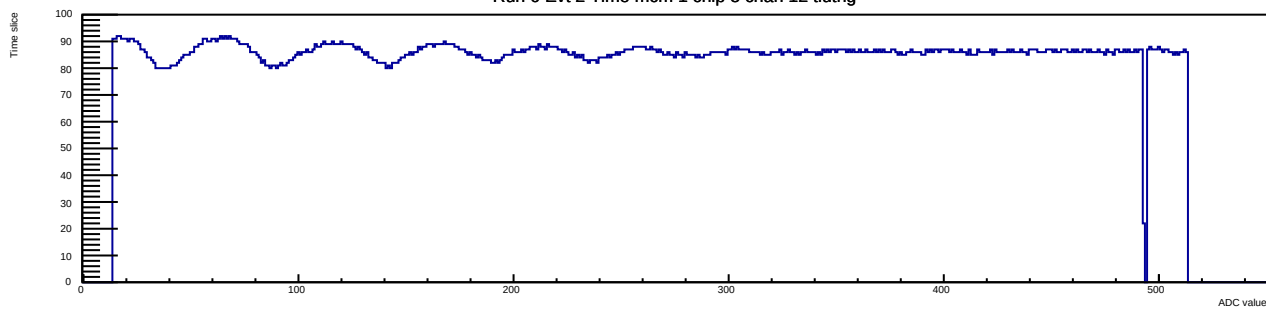
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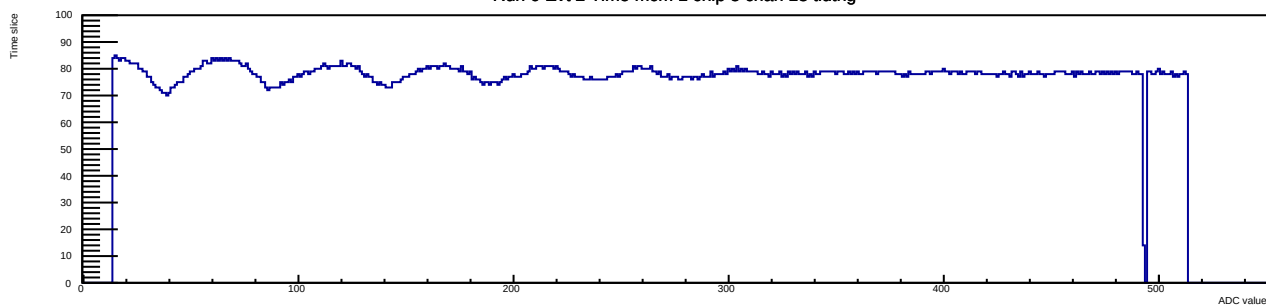
Run 6 Evt 2 Time mcm 1 chip 5 chan 11 tlutrig



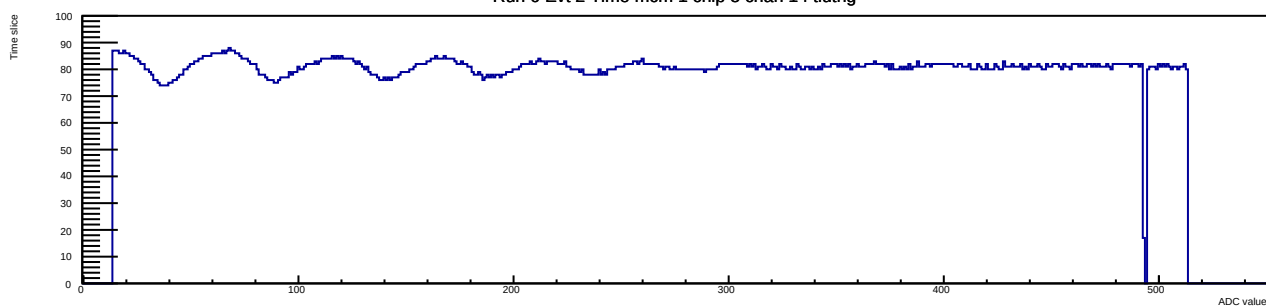
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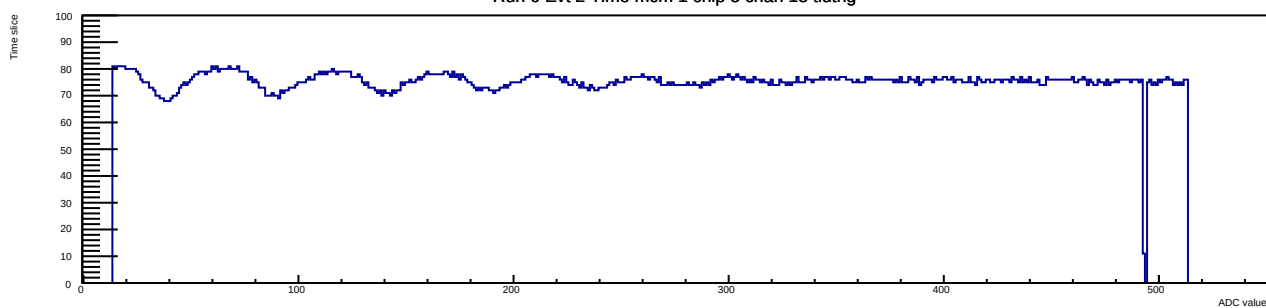
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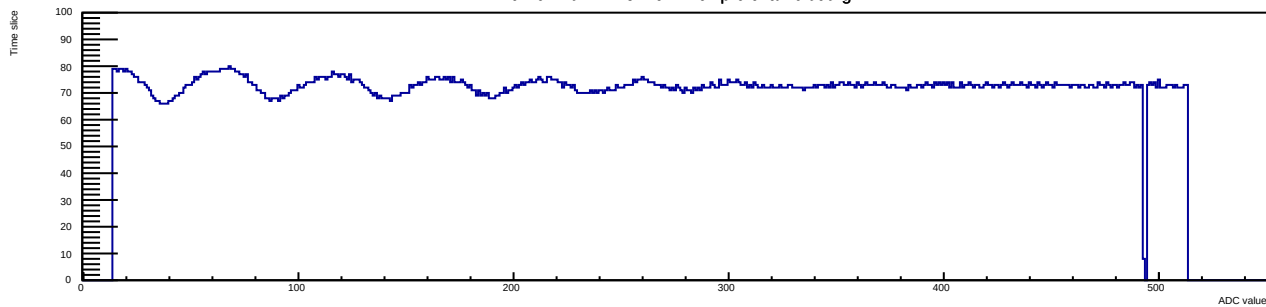
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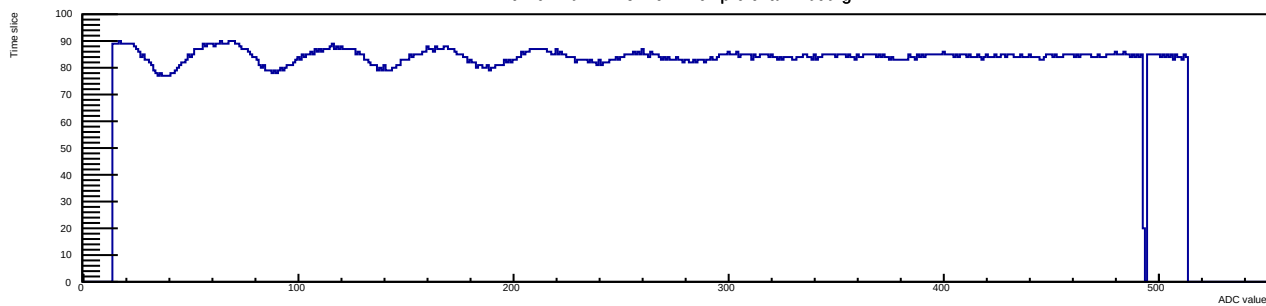
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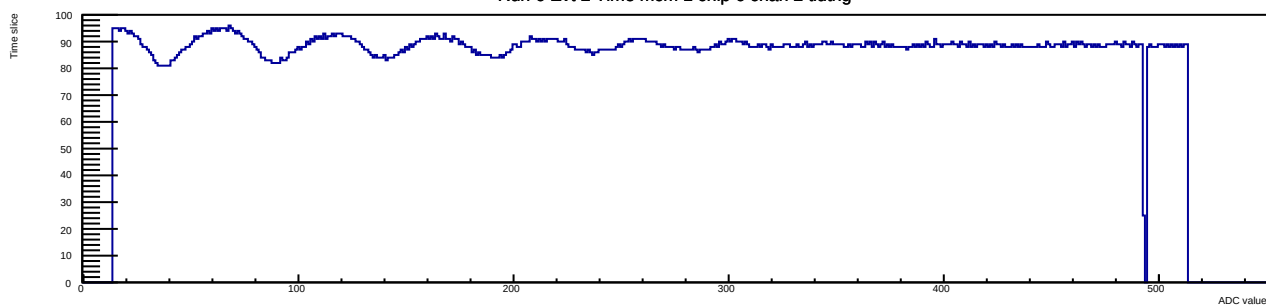
Run 6 Evt 2 Time mcm 1 chip 6 chan 0 tlutrig



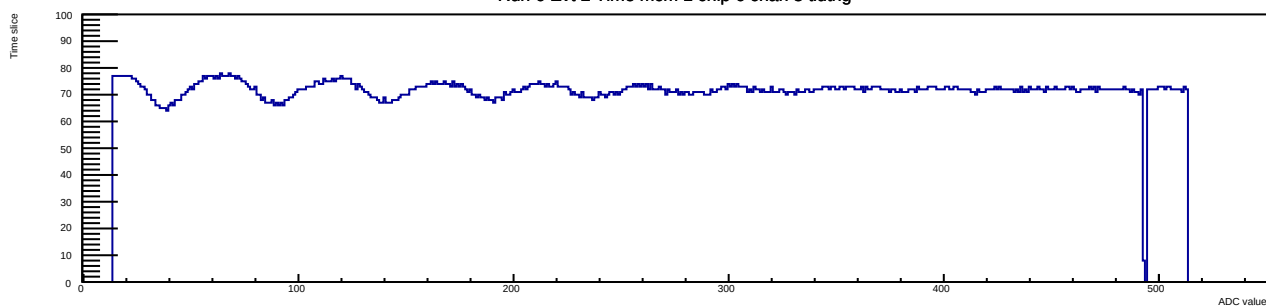
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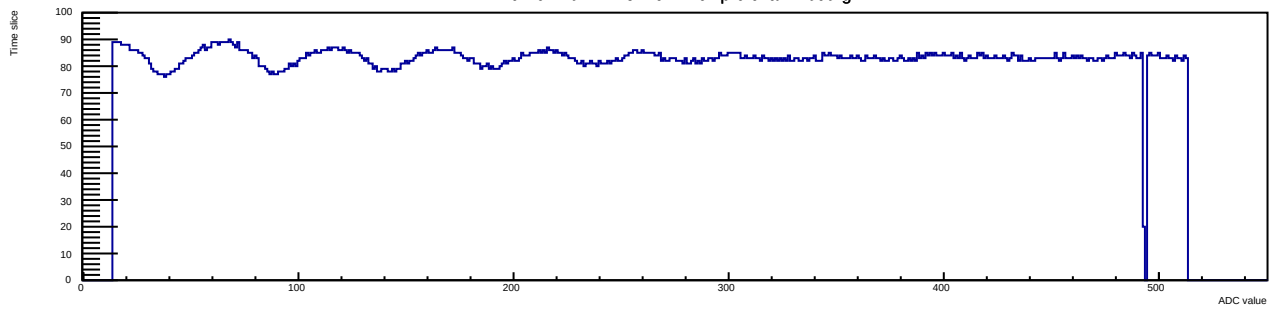
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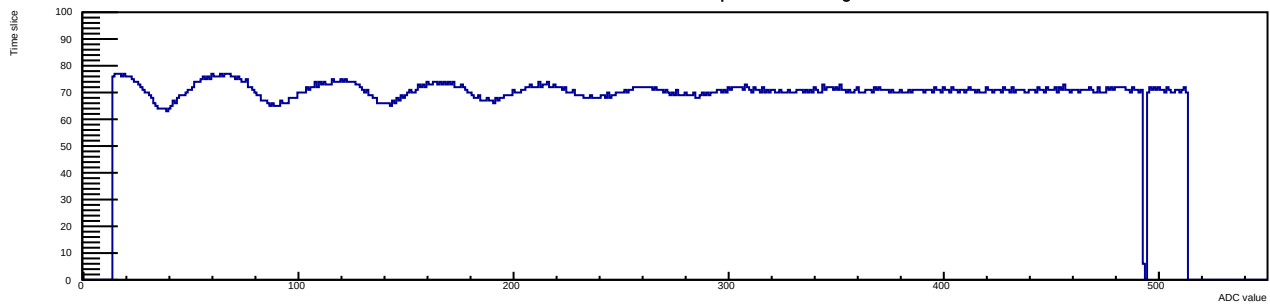
Run 6 Evt 2 Time mcm 1 chip 6 chan 3 tlutrig



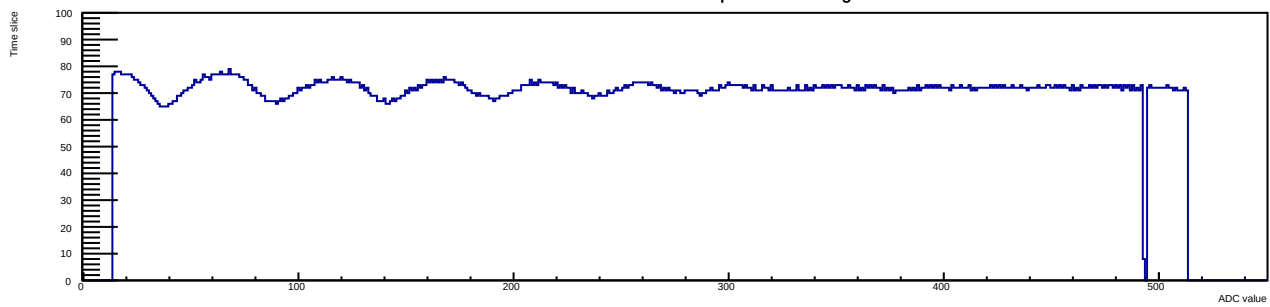
Run 6 Evt 2 Time mcm 1 chip 6 chan 4 tlutrig



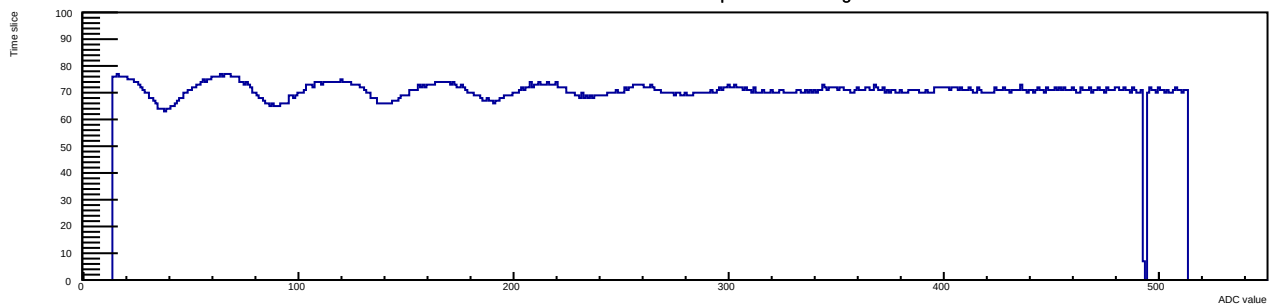
Run 6 Evt 2 Time mcm 1 chip 6 chan 5 tlutrig



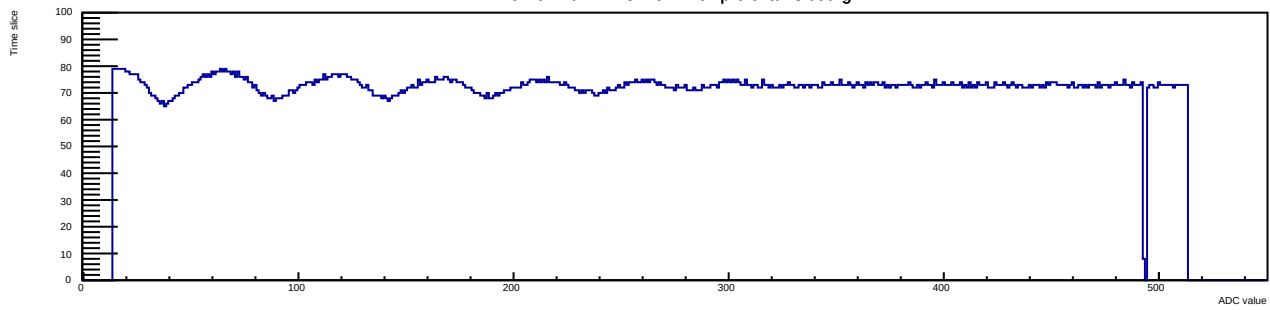
Run 6 Evt 2 Time mcm 1 chip 6 chan 6 tlutrig



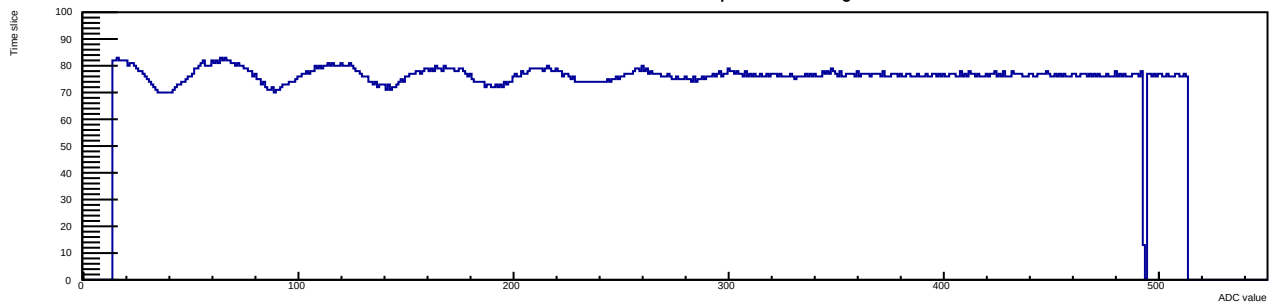
Run 6 Evt 2 Time mcm 1 chip 6 chan 7 tlutrig



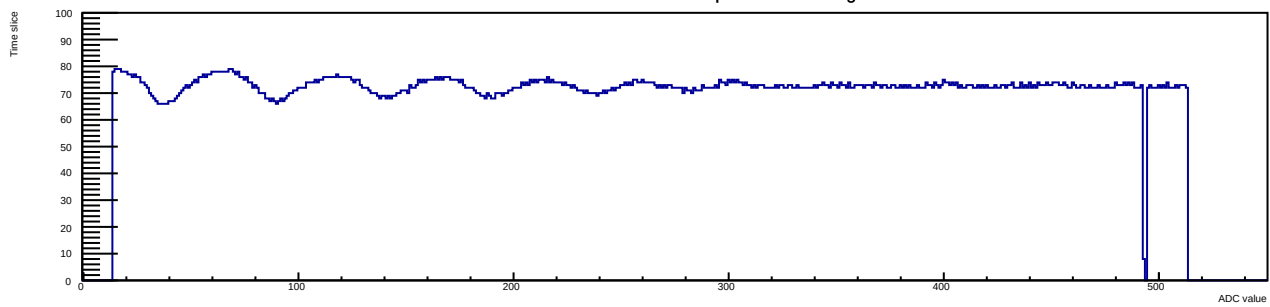
Run 6 Evt 2 Time mcm 1 chip 6 chan 8 tlutrig



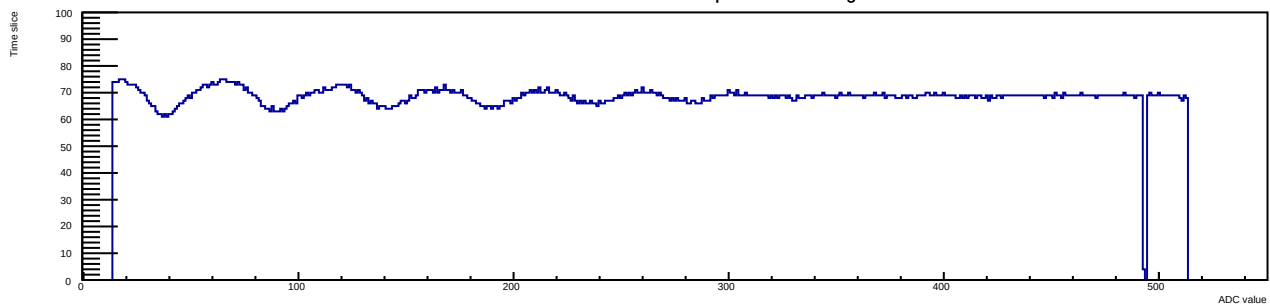
Run 6 Evt 2 Time mcm 1 chip 6 chan 9 tlutrig



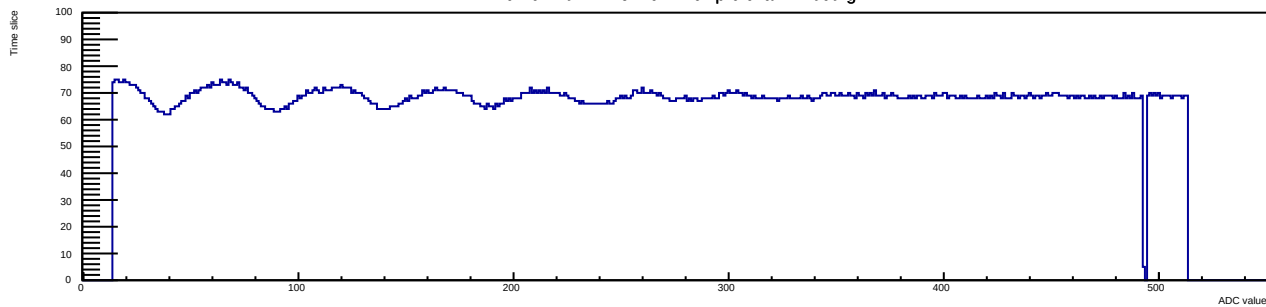
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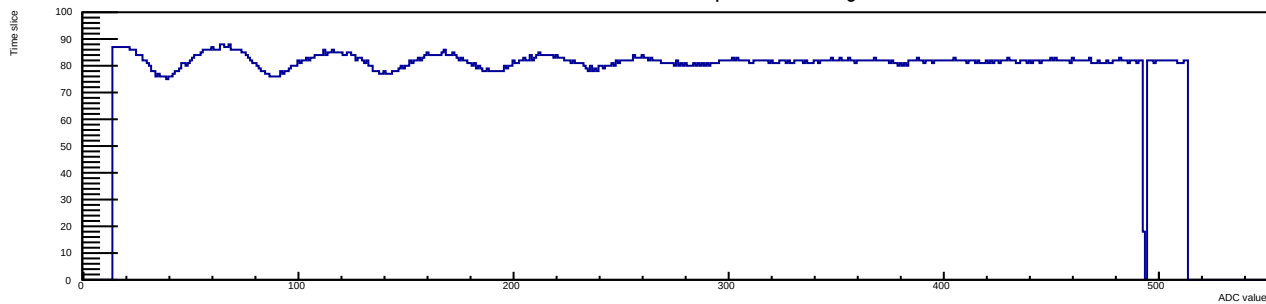
Run 6 Evt 2 Time mcm 1 chip 6 chan 11 tlutrig



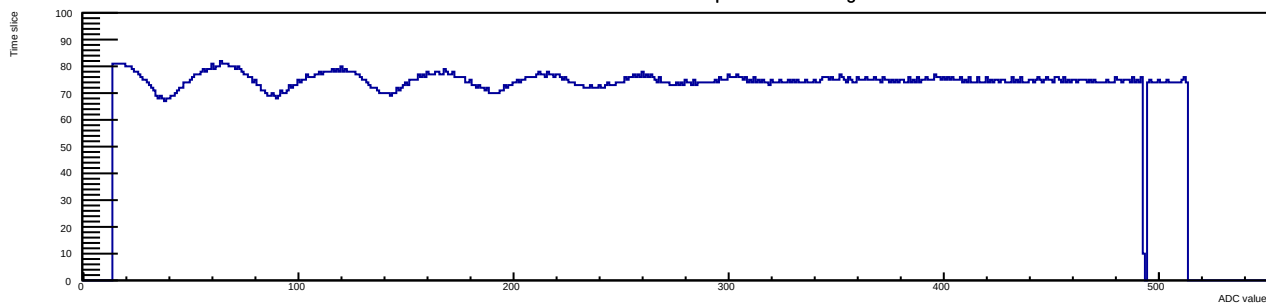
Run 6 Evt 2 Time mcm 1 chip 6 chan 12 tlutrig



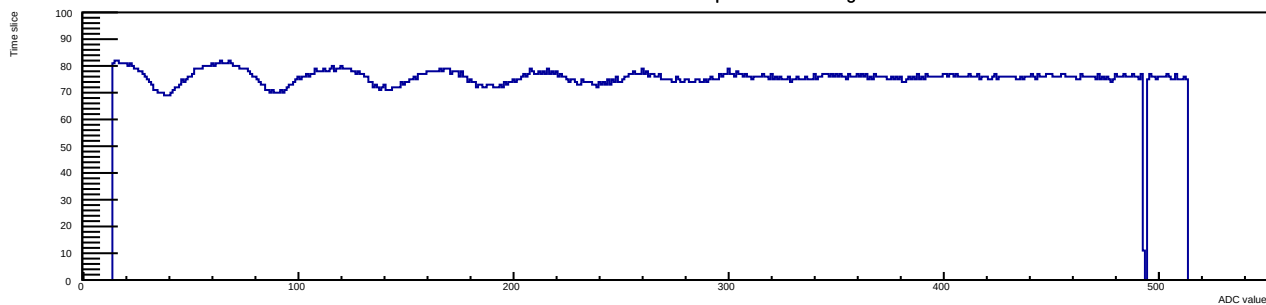
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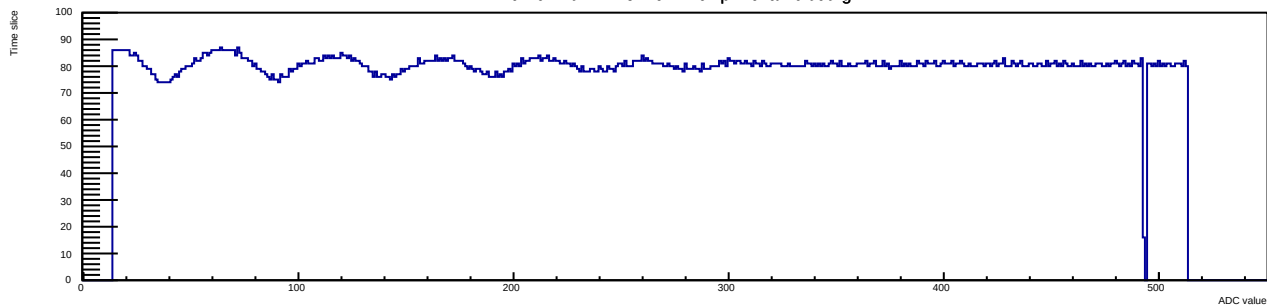
Run 6 Evt 2 Time mcm 1 chip 6 chan 14 tlutrig



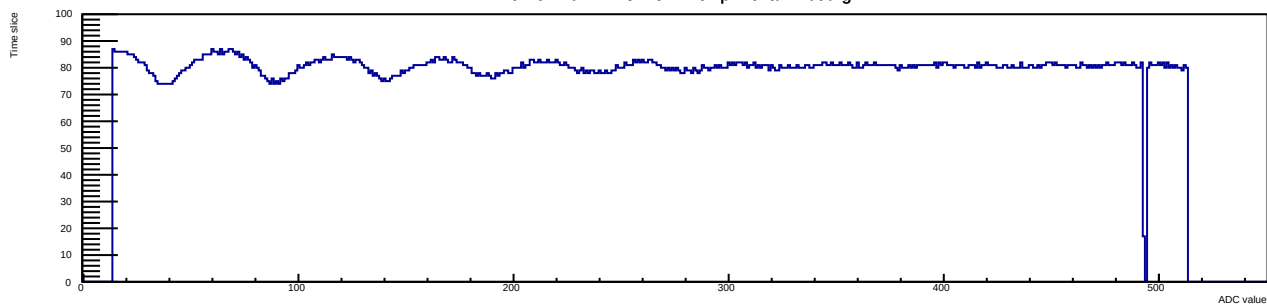
Run 6 Evt 2 Time mcm 1 chip 6 chan 15 tlutrig



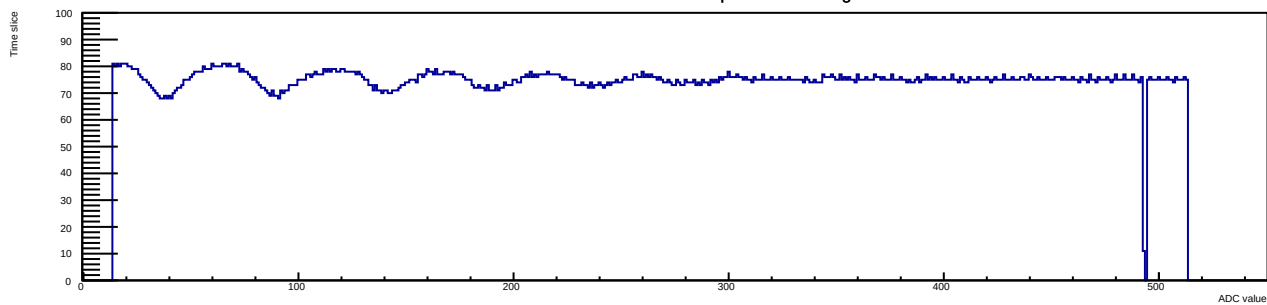
Run 6 Evt 2 Time mcm 1 chip 7 chan 0 tlutrig



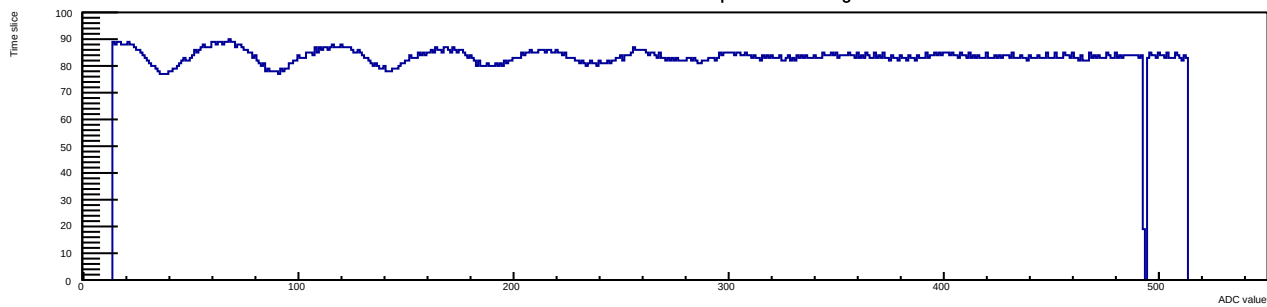
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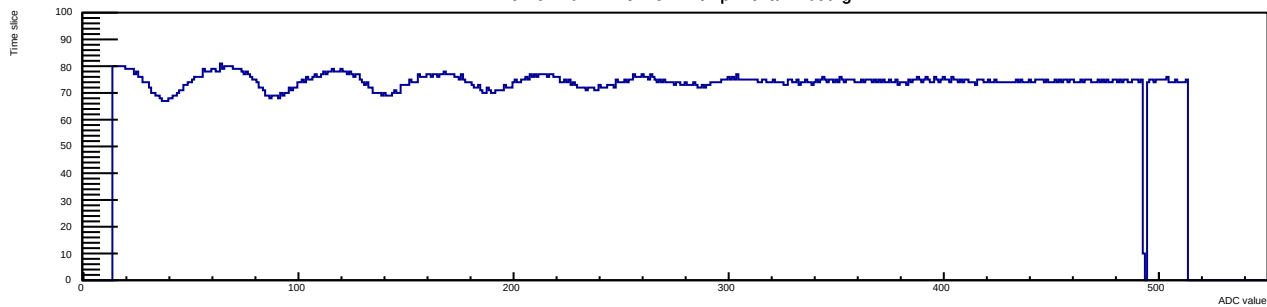
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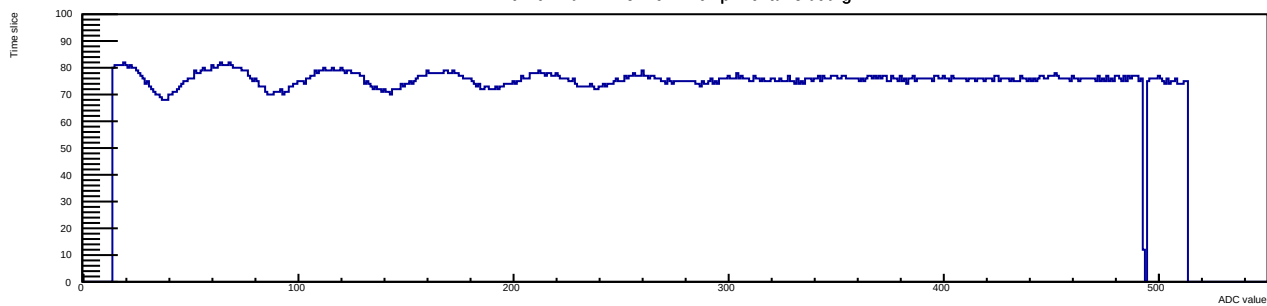
Run 6 Evt 2 Time mcm 1 chip 7 chan 3 tlutrig



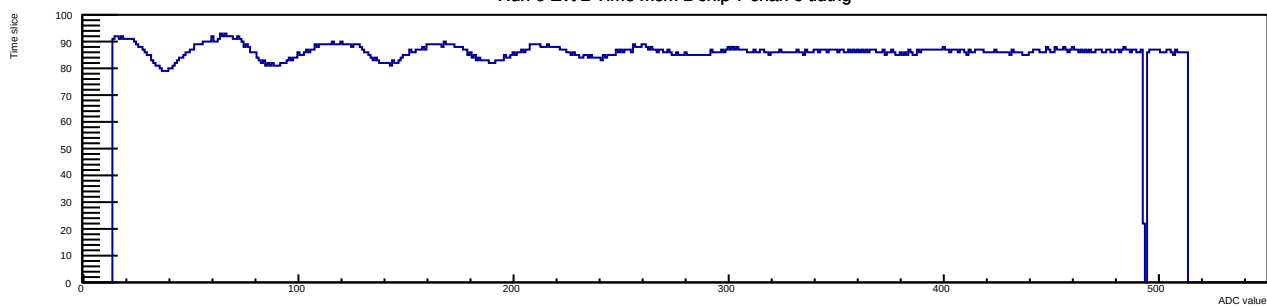
Run 6 Evt 2 Time mcm 1 chip 7 chan 4 tlutrig



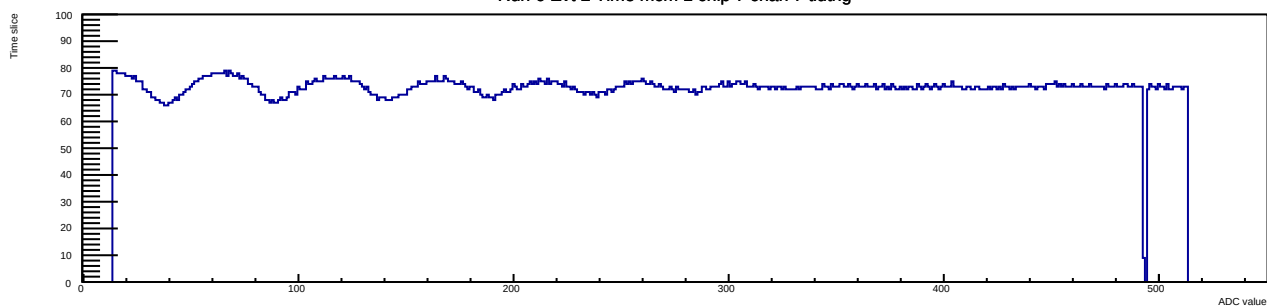
Run 6 Evt 2 Time mcm 1 chip 7 chan 5 tlutrig



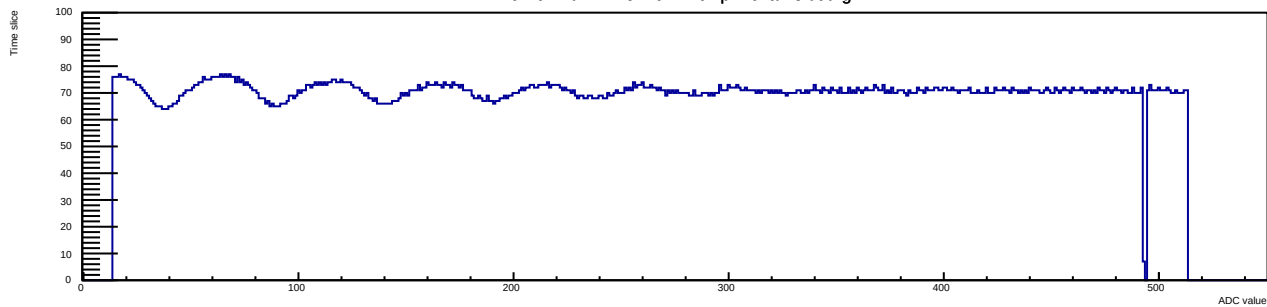
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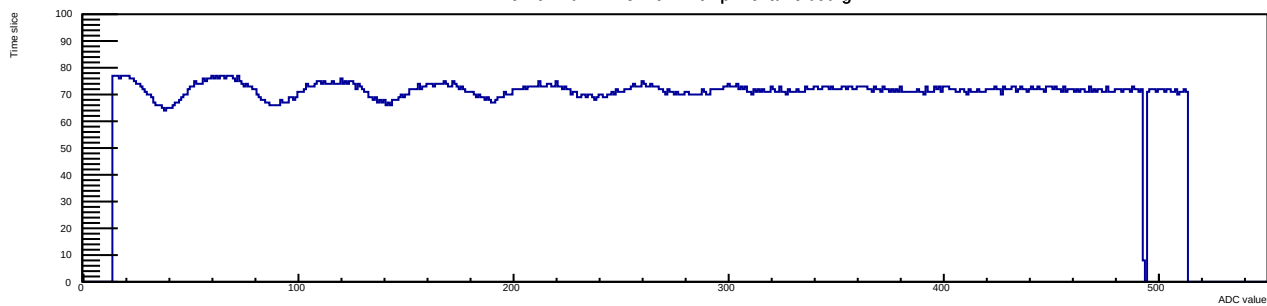
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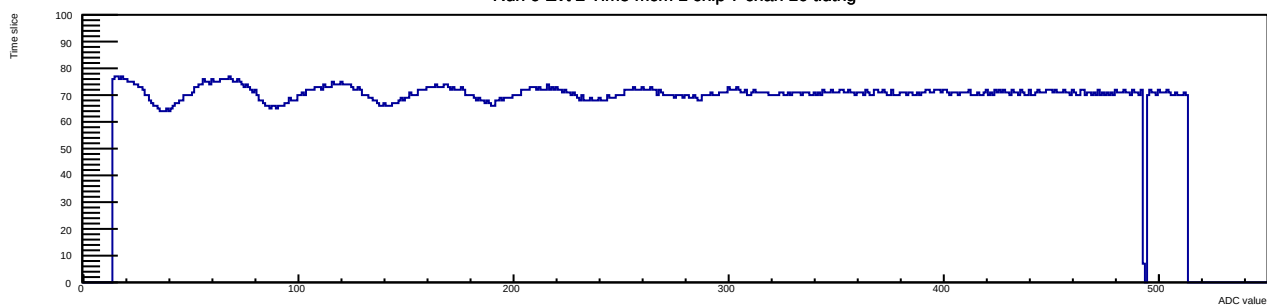
Run 6 Evt 2 Time mcm 1 chip 7 chan 8 tlutrig



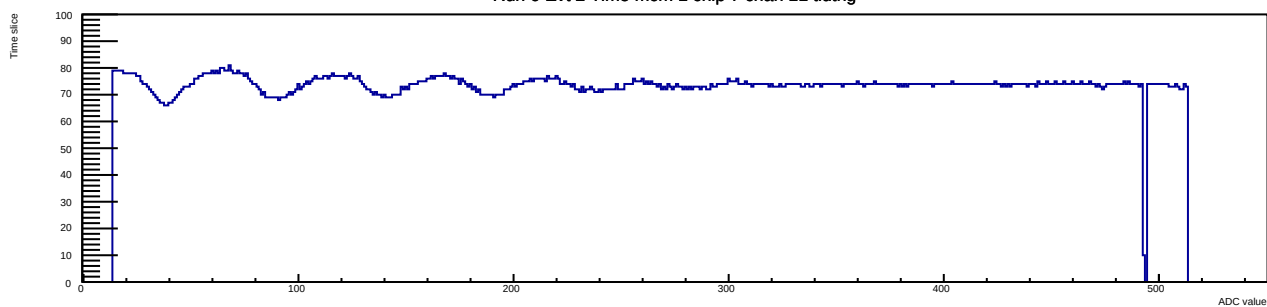
Run 6 Evt 2 Time mcm 1 chip 7 chan 9 tlutrig



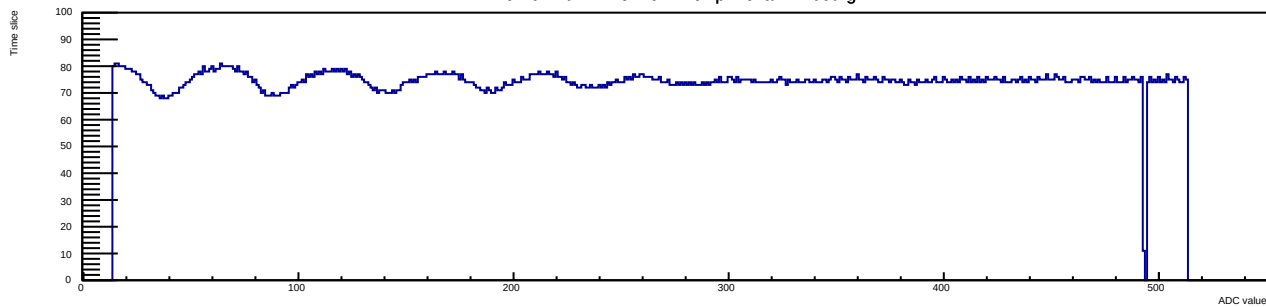
Run 6 Evt 2 Time mcm 1 chip 7 chan 10 tlutrig



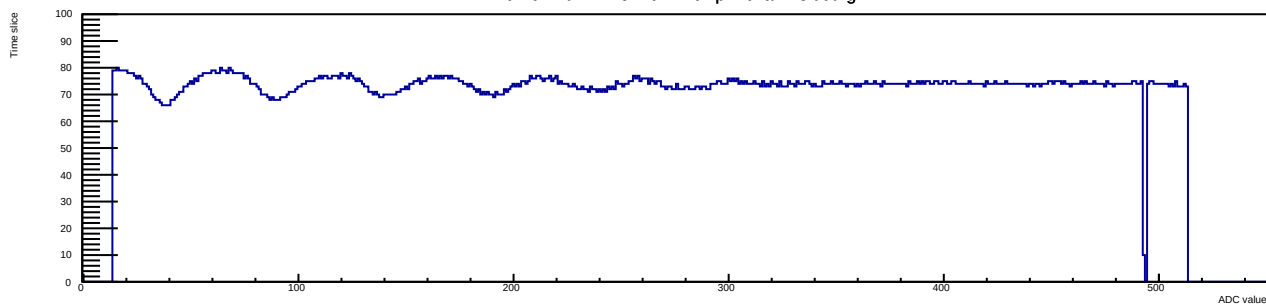
Run 6 Evt 2 Time mcm 1 chip 7 chan 11 tlutrig



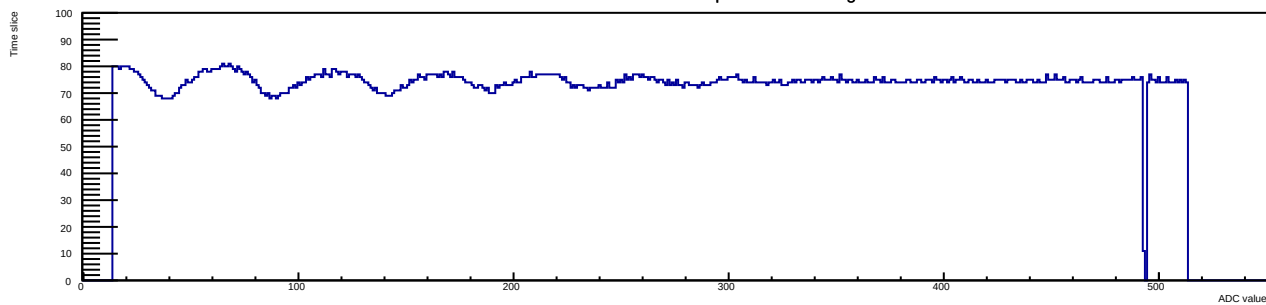
Run 6 Evt 2 Time mcm 1 chip 7 chan 12 tlutrig



Run 6 Evt 2 Time mcm 1 chip 7 chan 13 tlutrig



Run 6 Evt 2 Time mcm 1 chip 7 chan 14 tlutrig



Run 6 Evt 2 Time mcm 1 chip 7 chan 15 tlutrig

