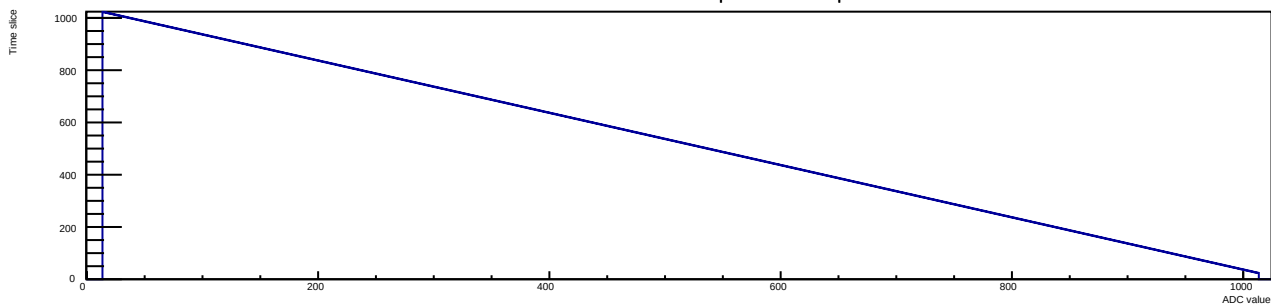
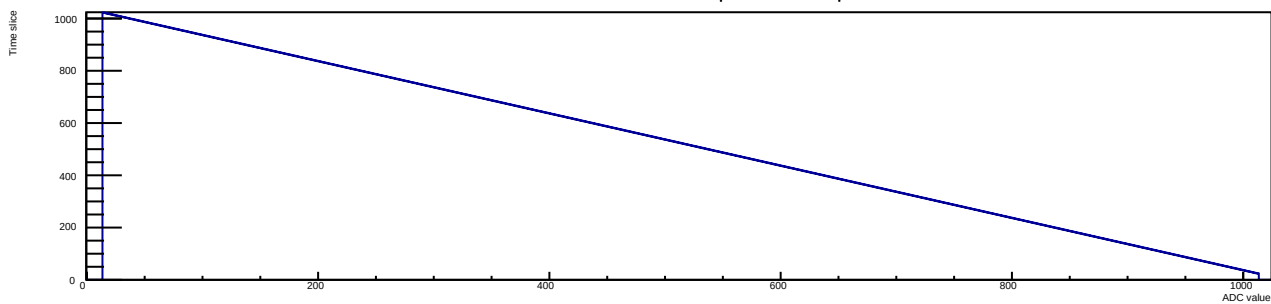


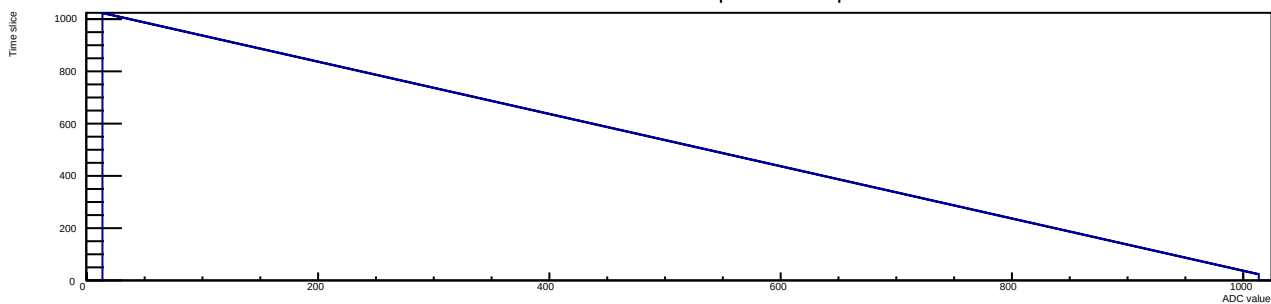
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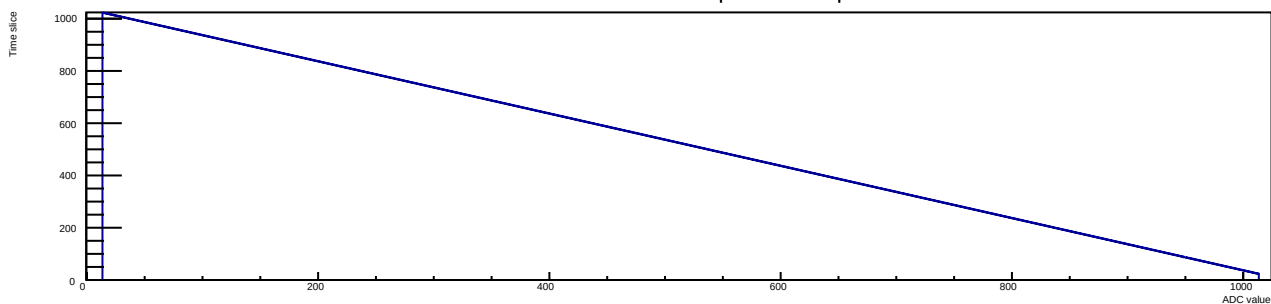
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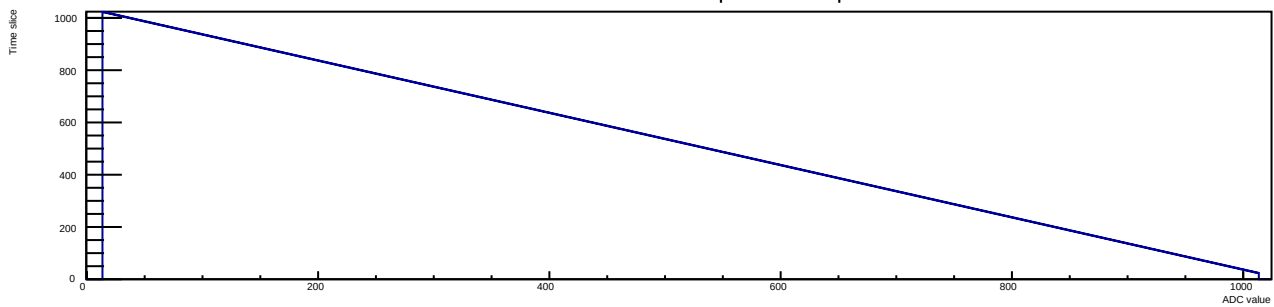
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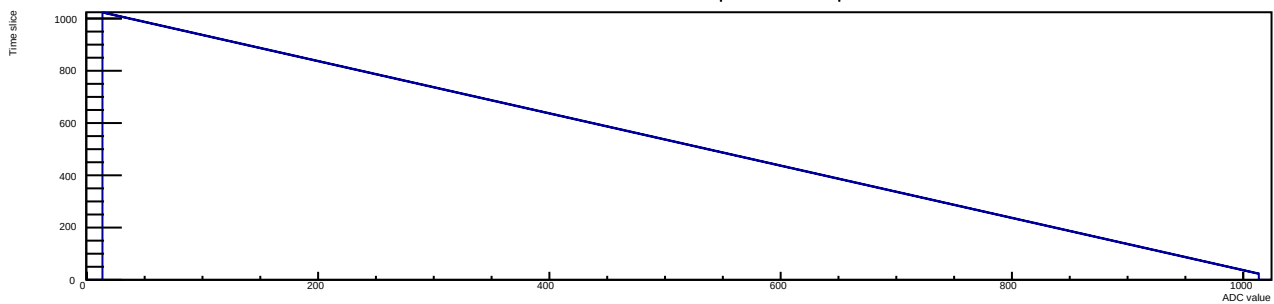
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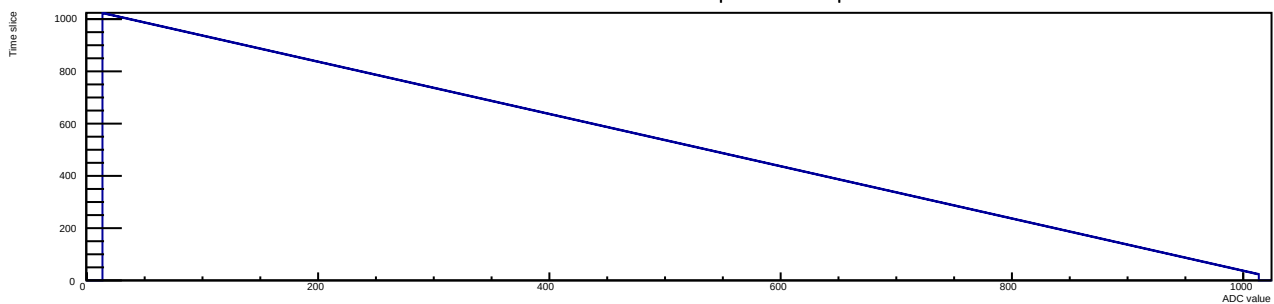
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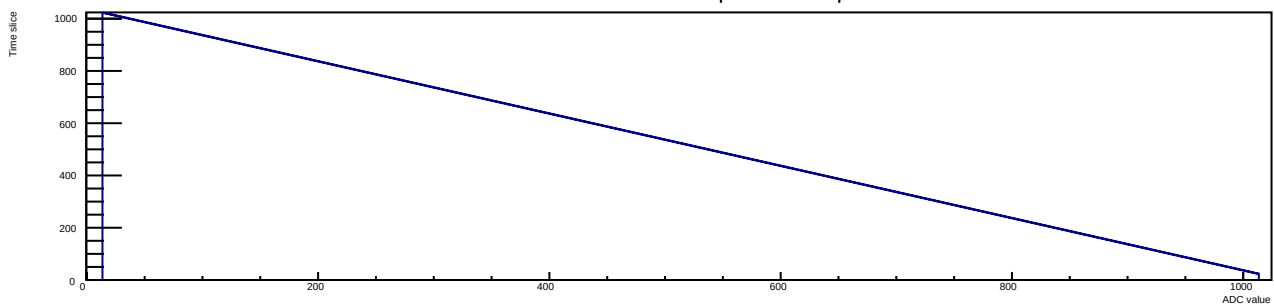
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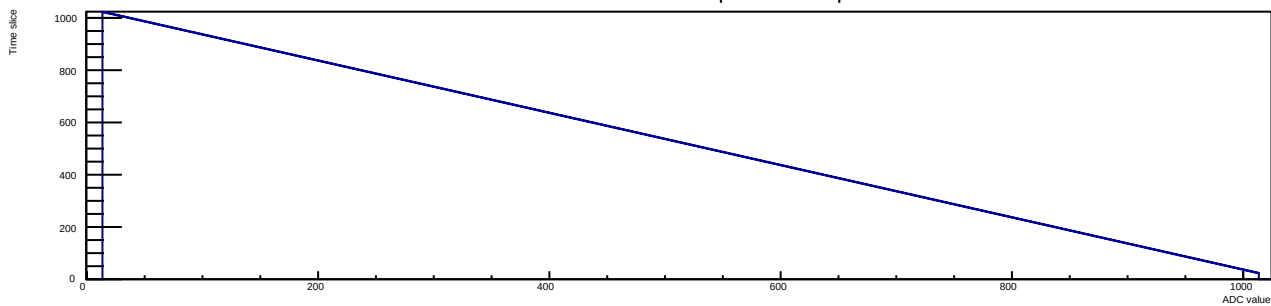
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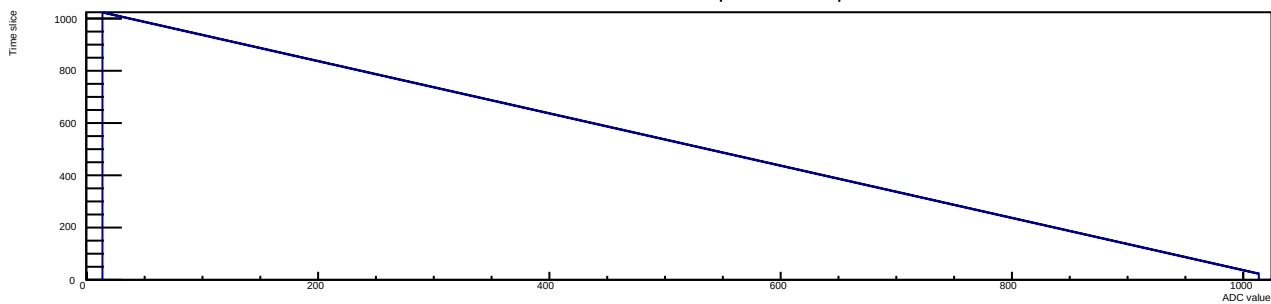
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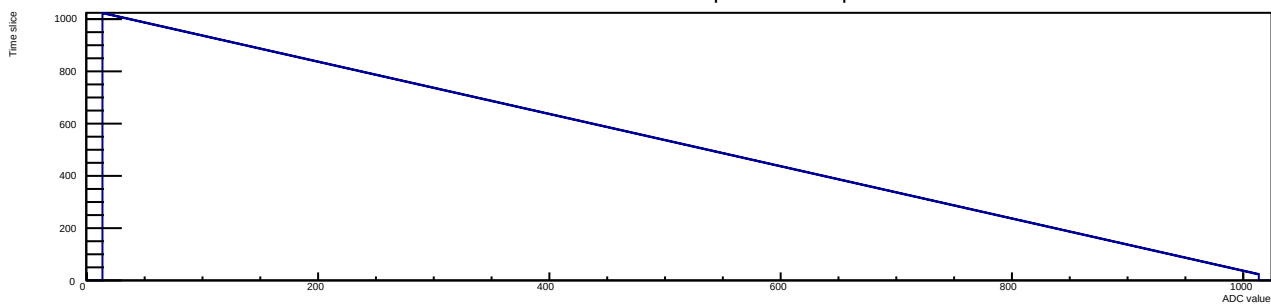
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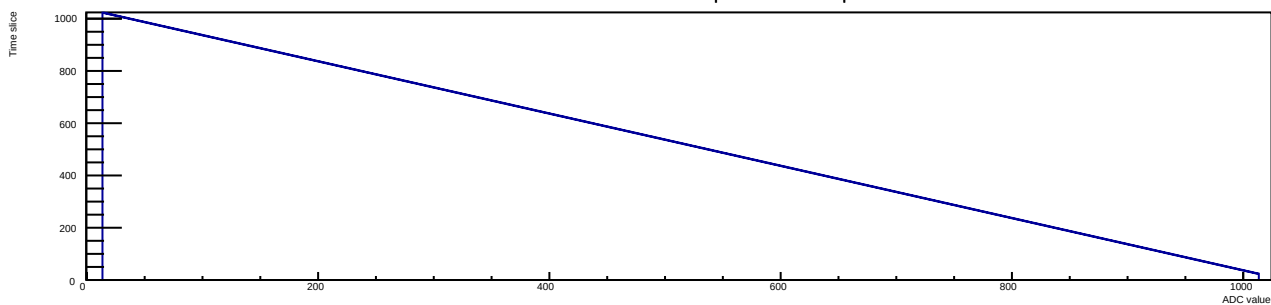
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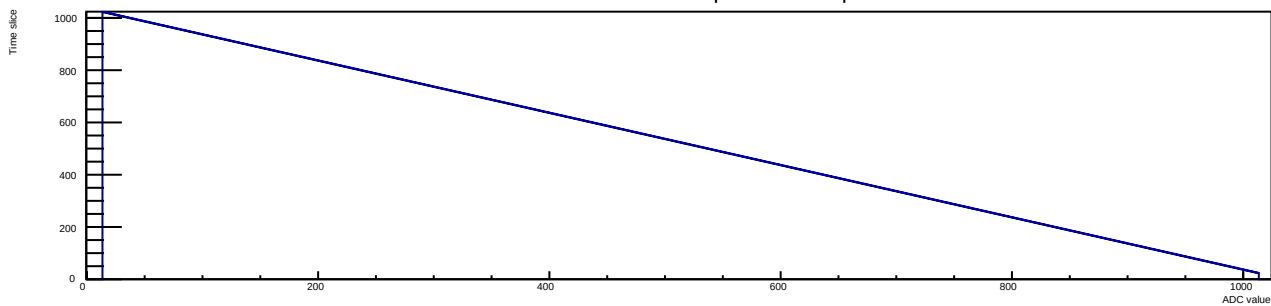
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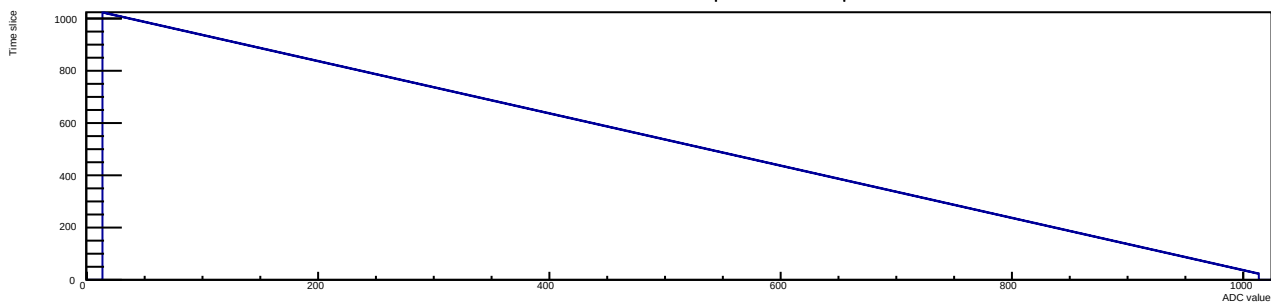
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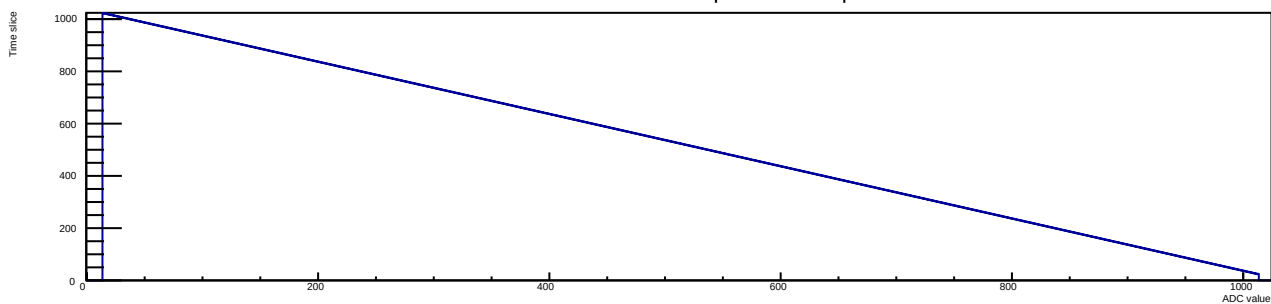
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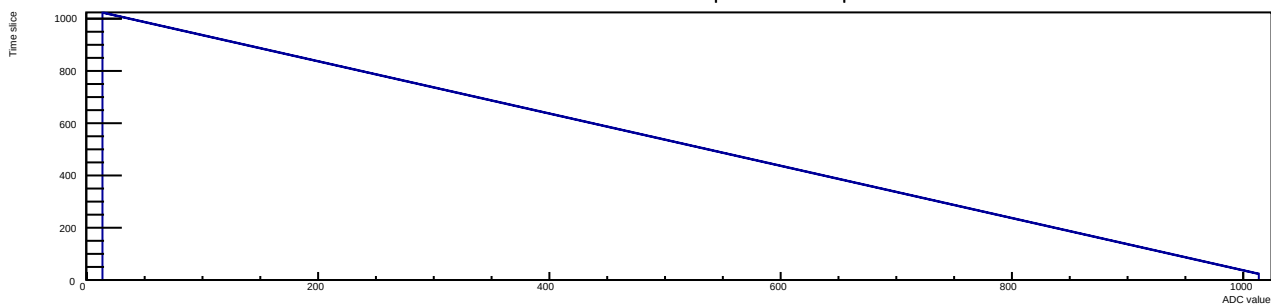
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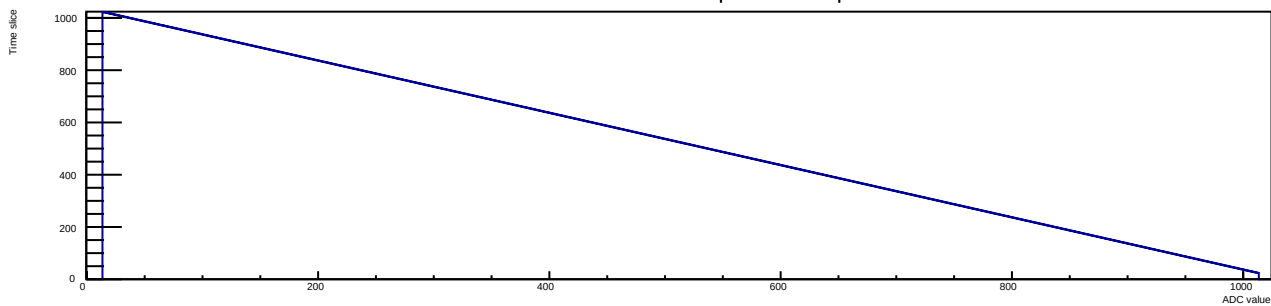
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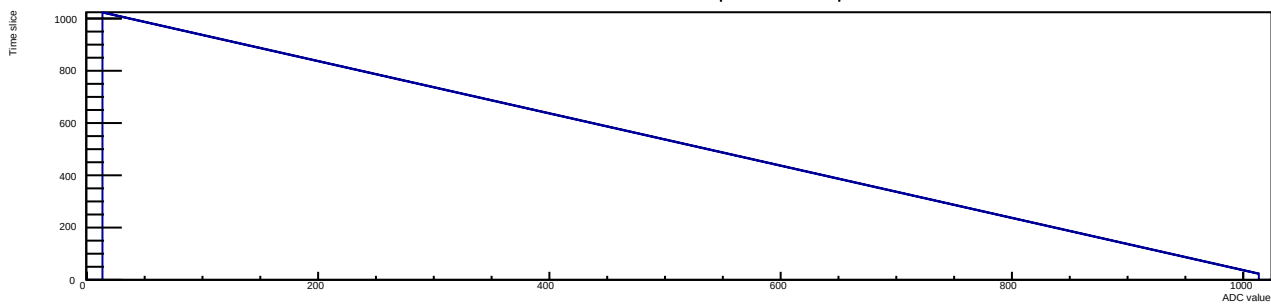
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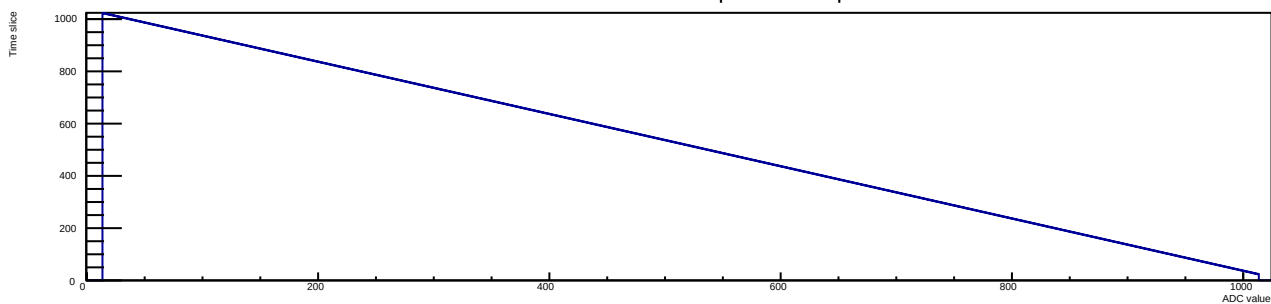
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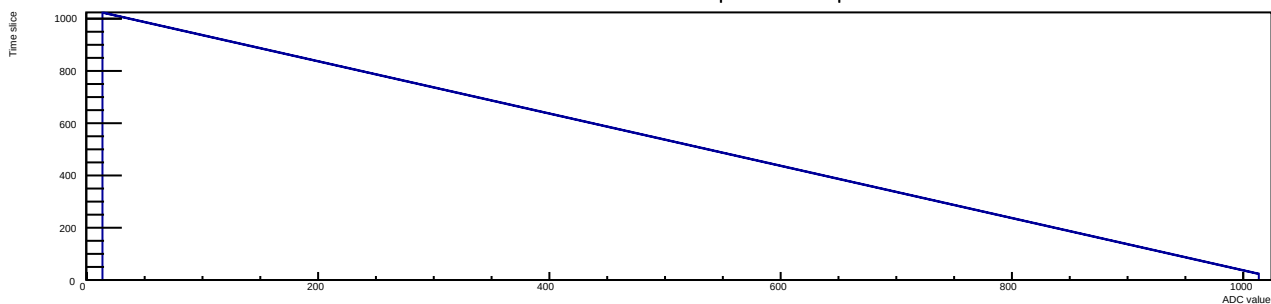
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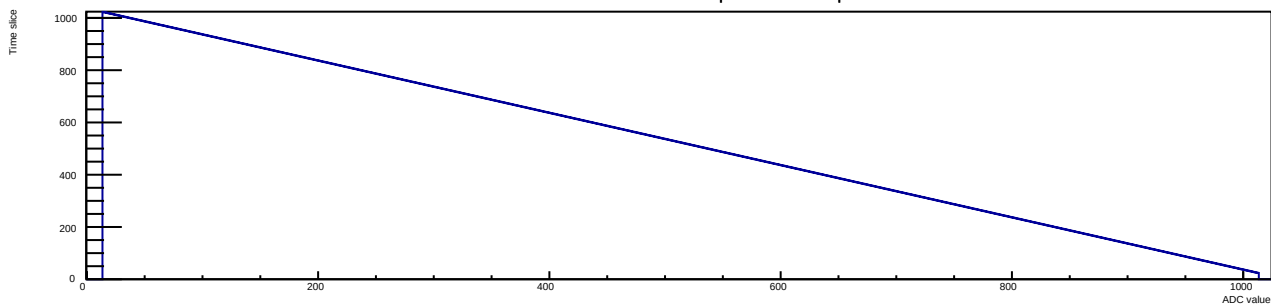
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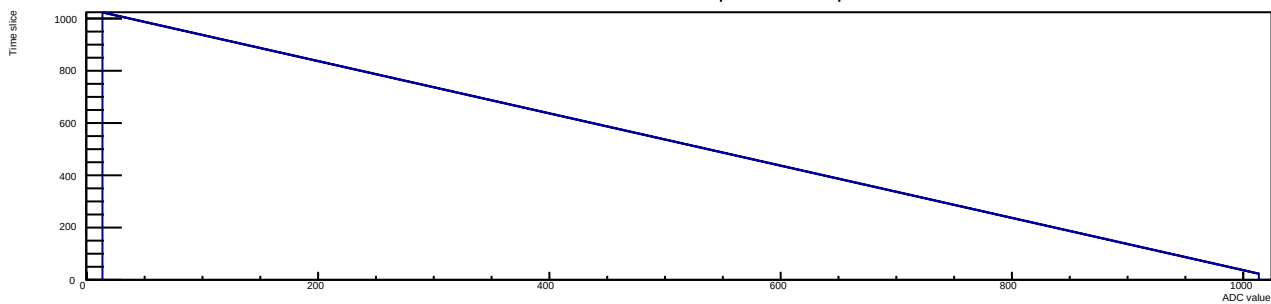
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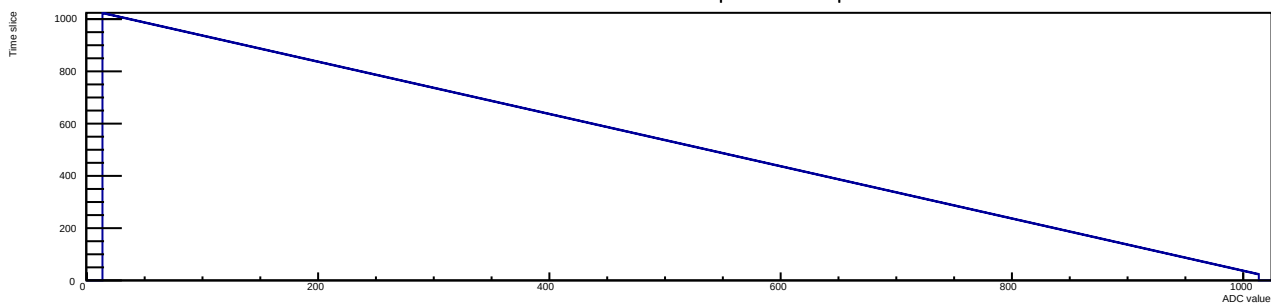
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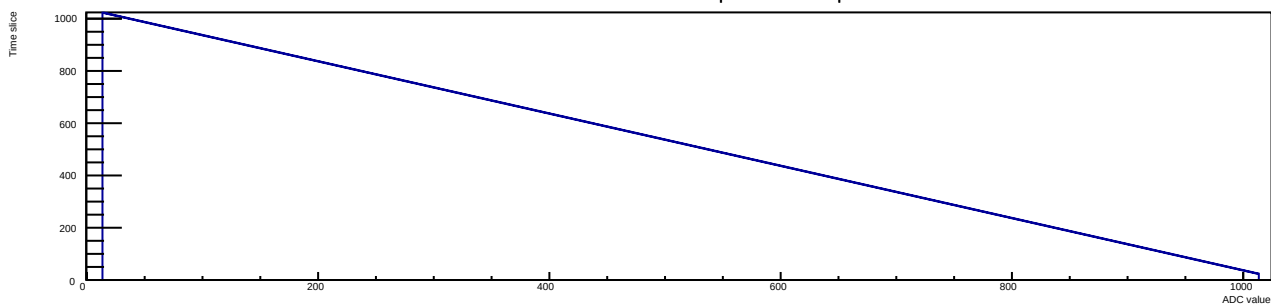
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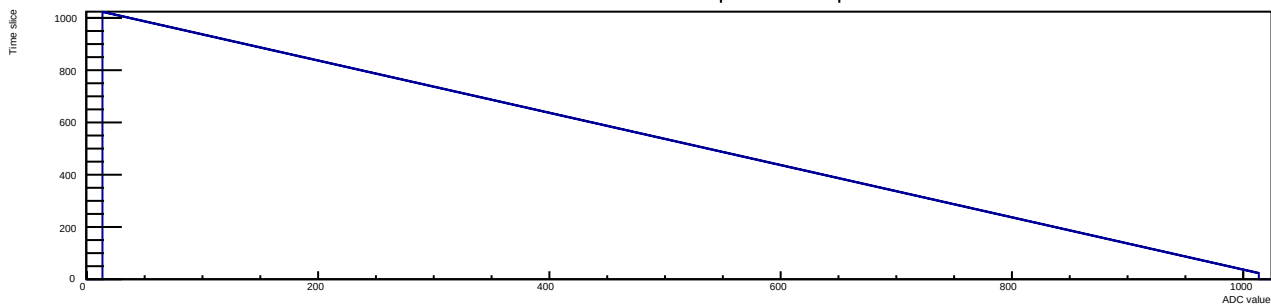
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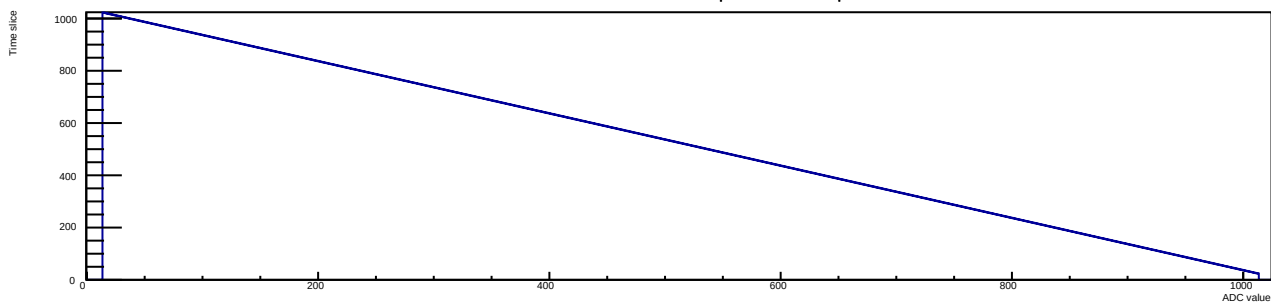
Run 18 Evt 4 Time mcm 0 chip 1 chan 7 ramps-1



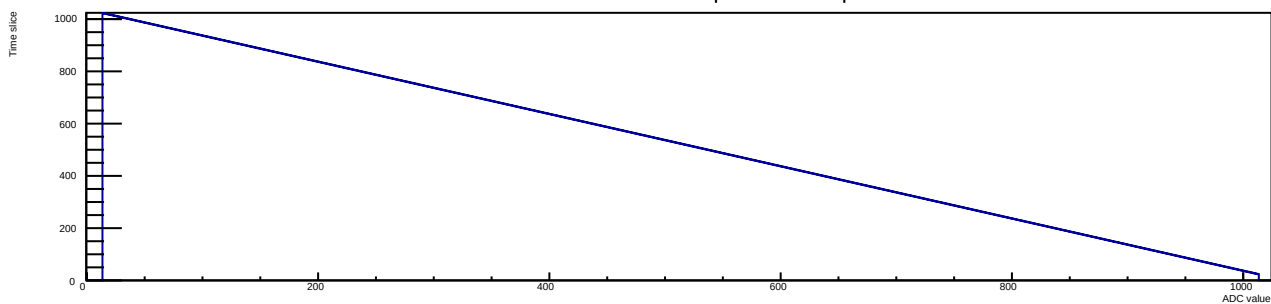
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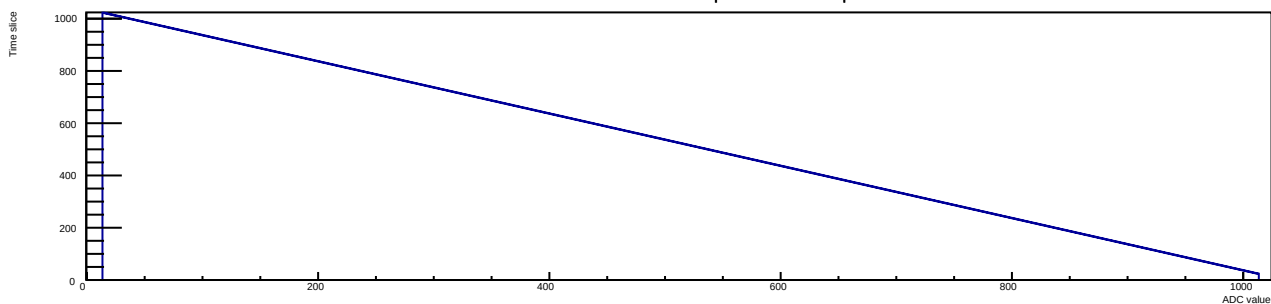
Run 18 Evt 4 Time mcm 0 chip 1 chan 9 ramps-1



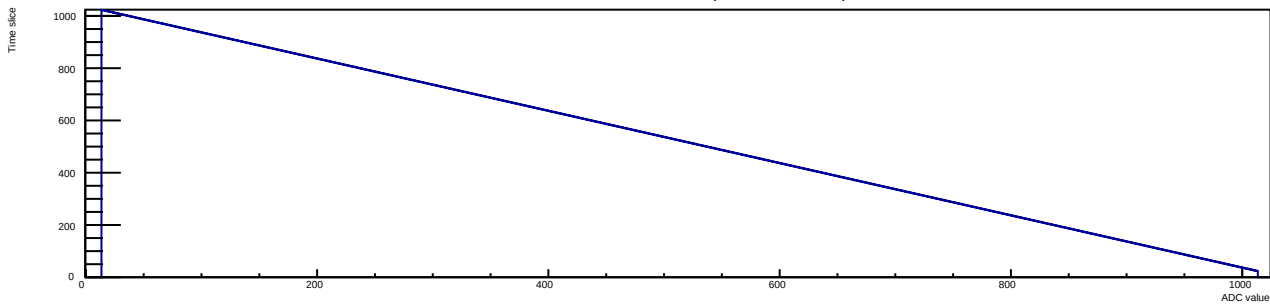
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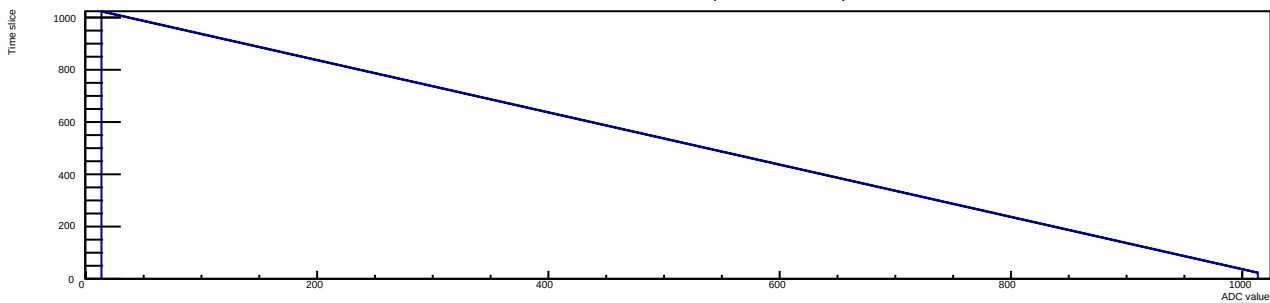
Run 18 Evt 4 Time mcm 0 chip 1 chan 11 ramps-1



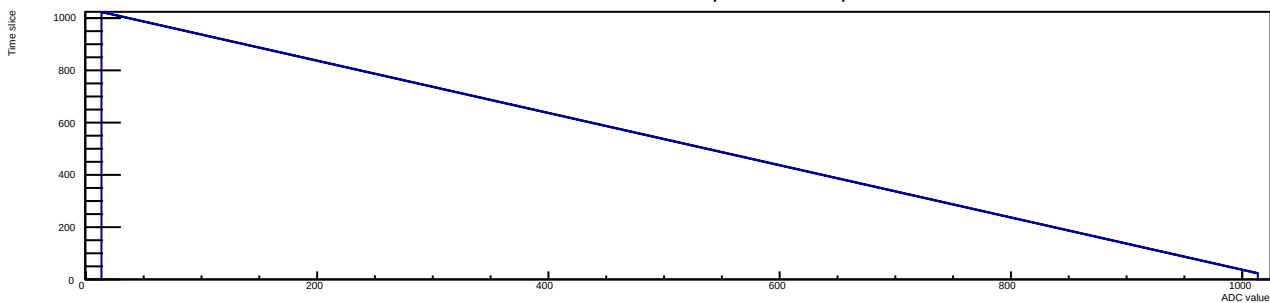
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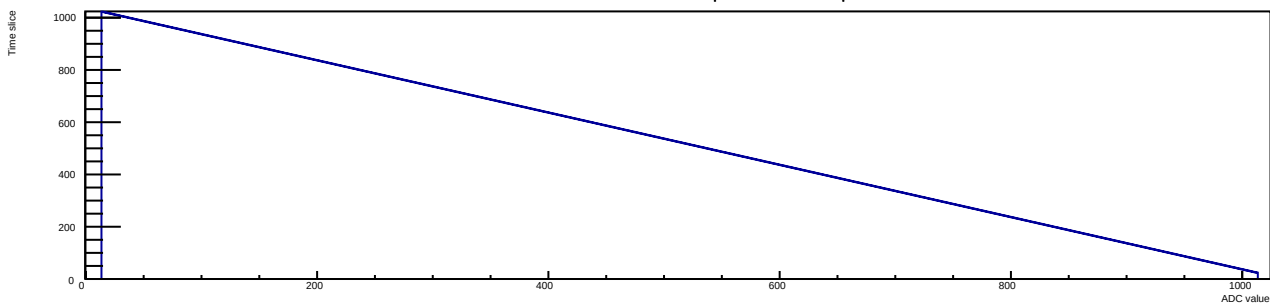
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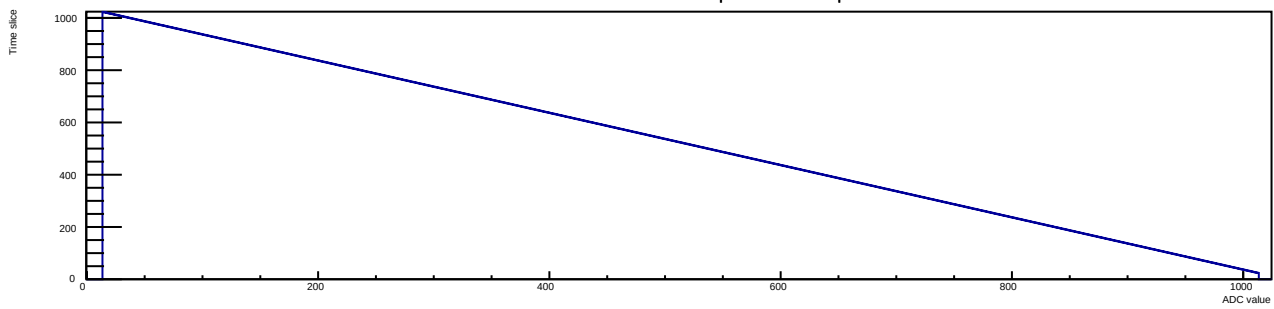
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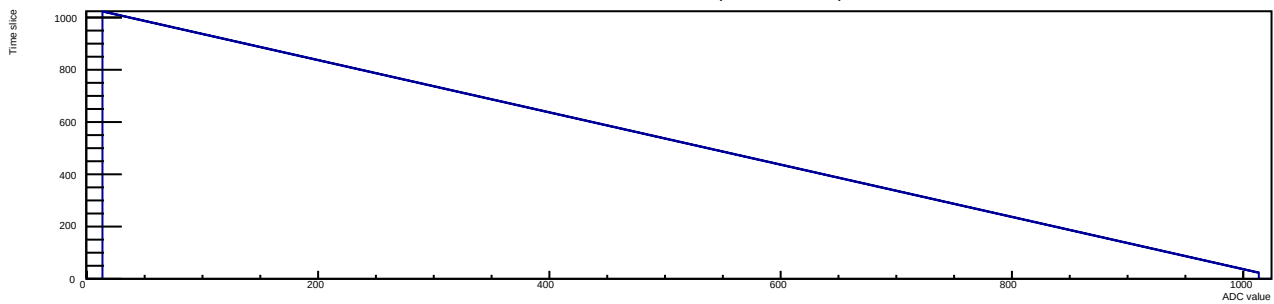
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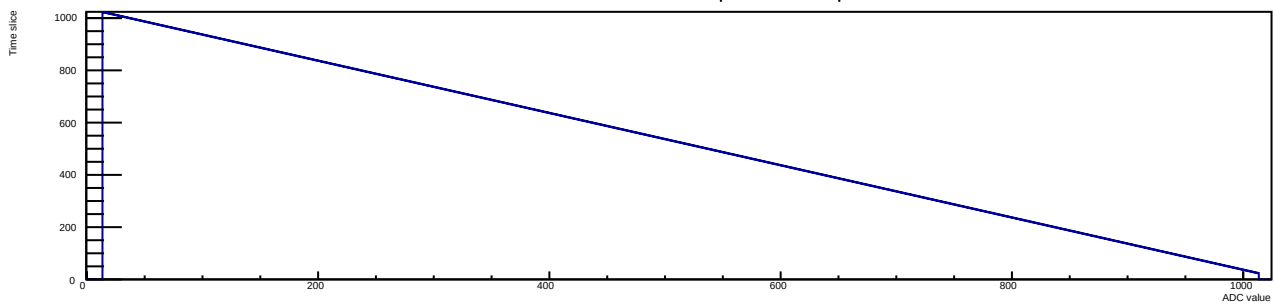
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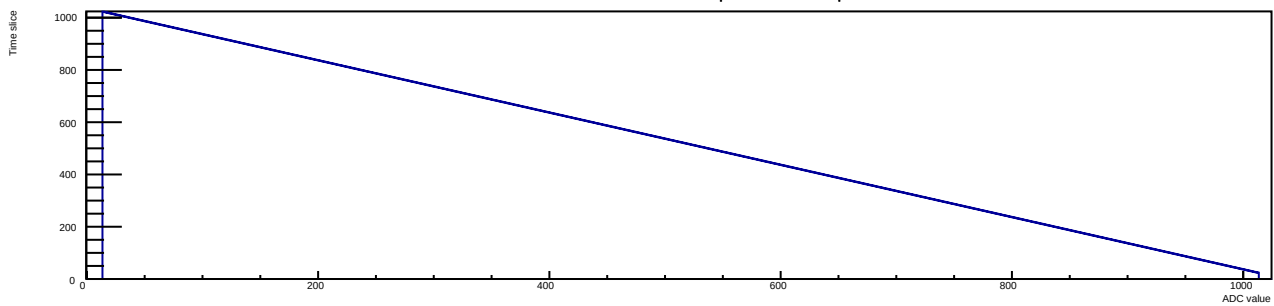
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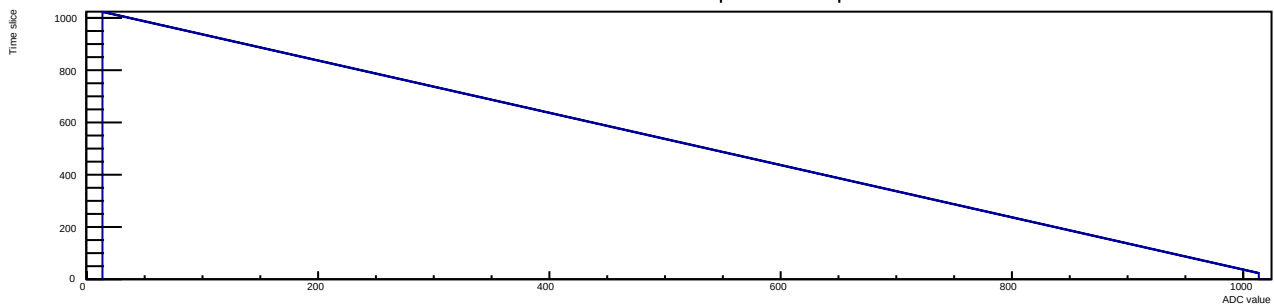
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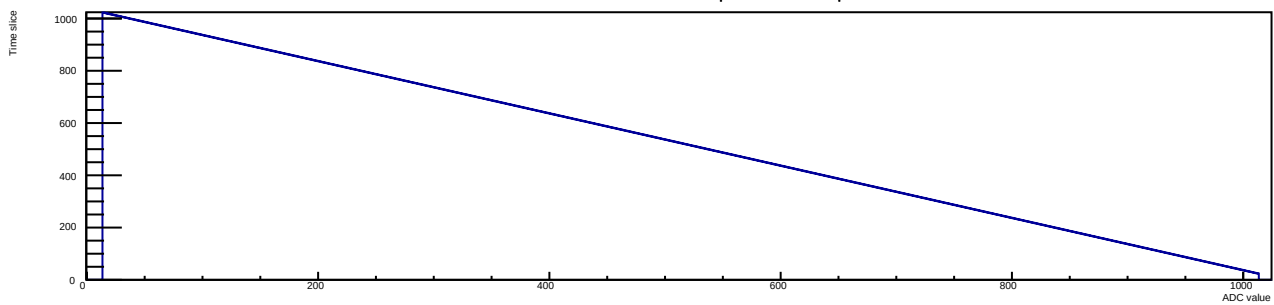
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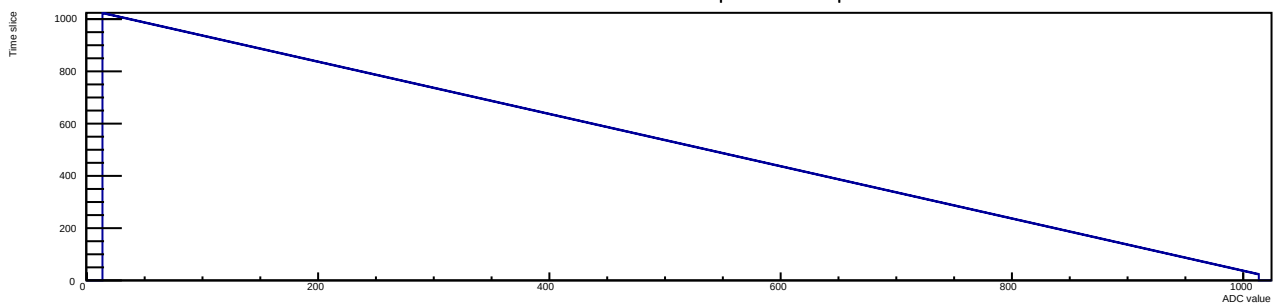
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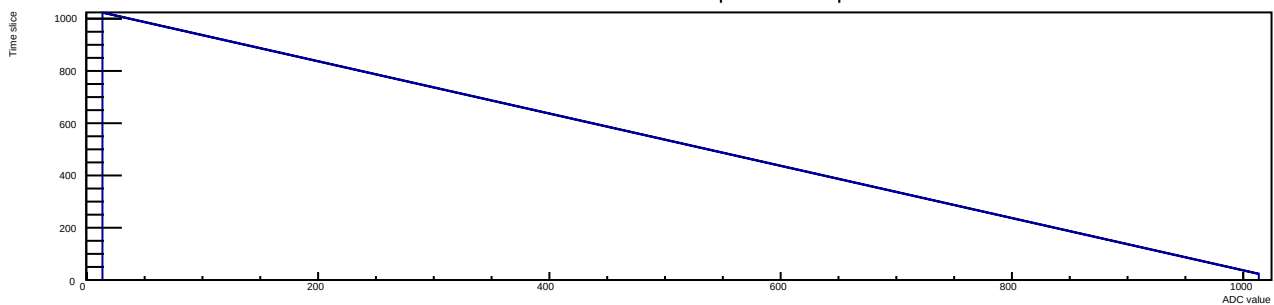
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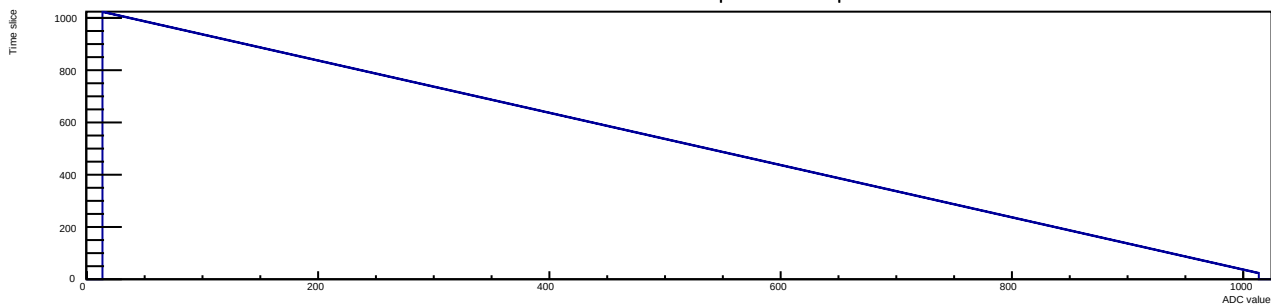
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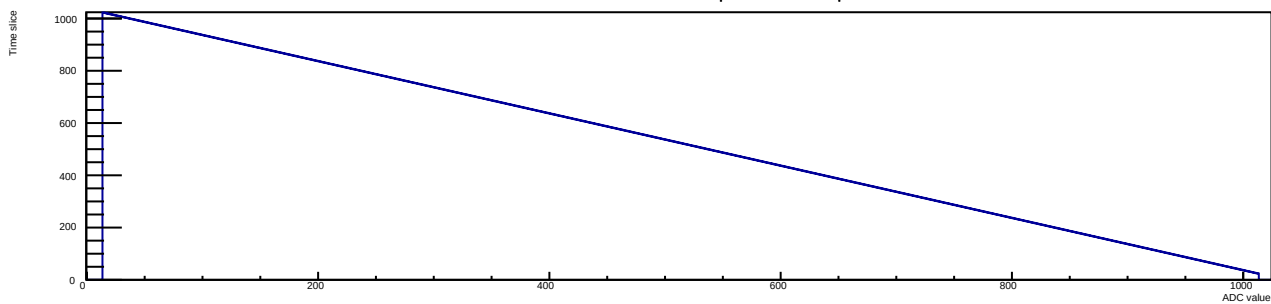
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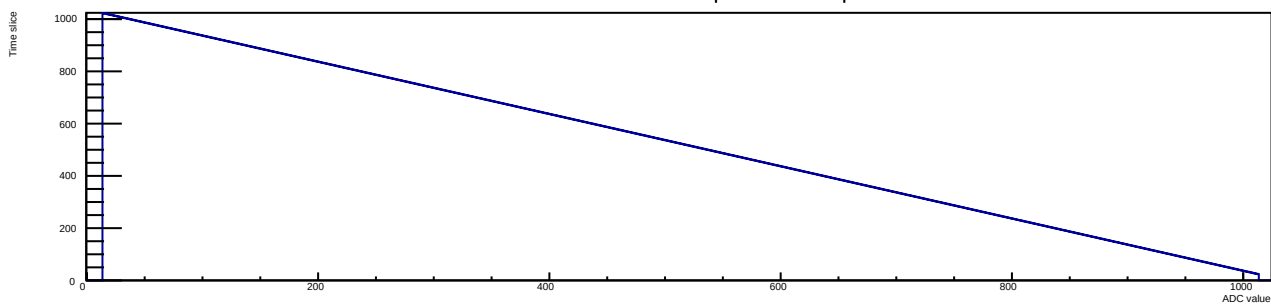
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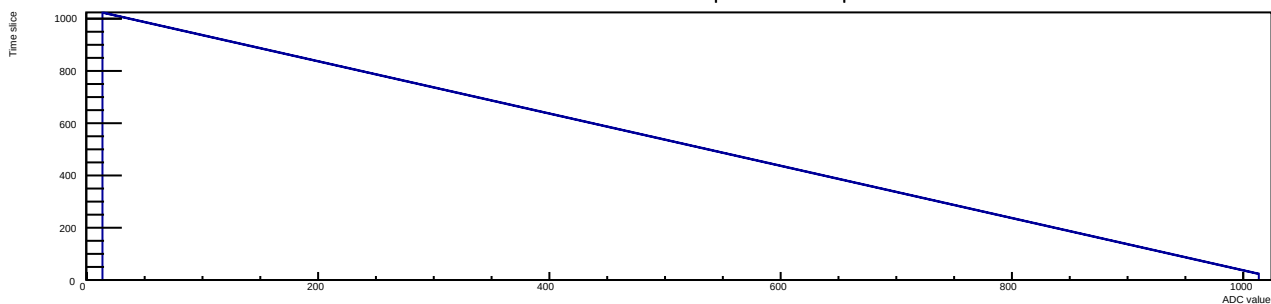
Run 18 Evt 4 Time mcm 0 chip 2 chan 9 ramps-1



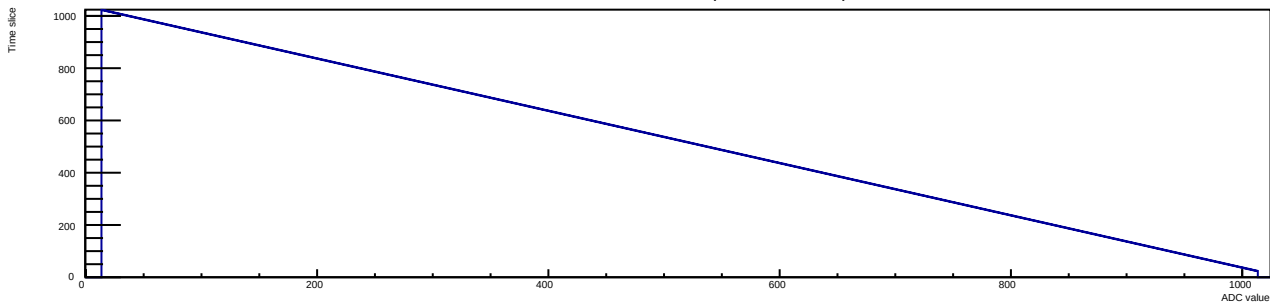
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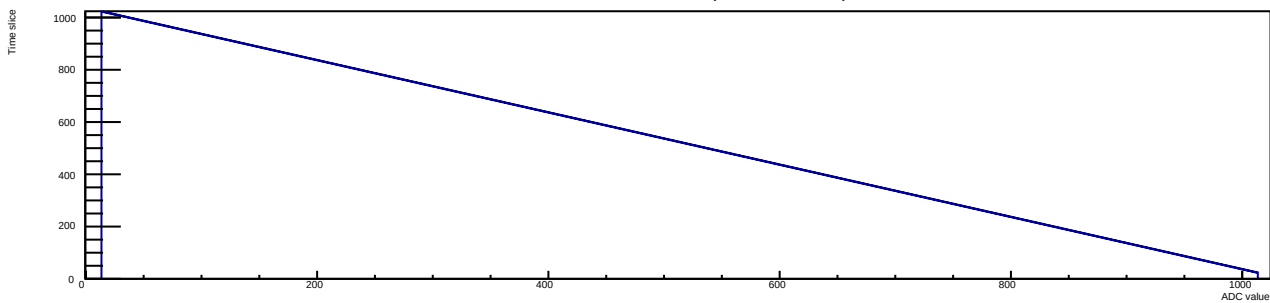
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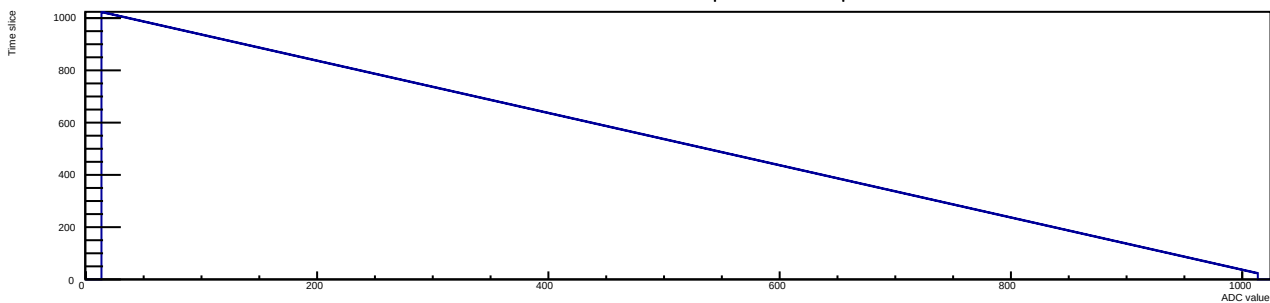
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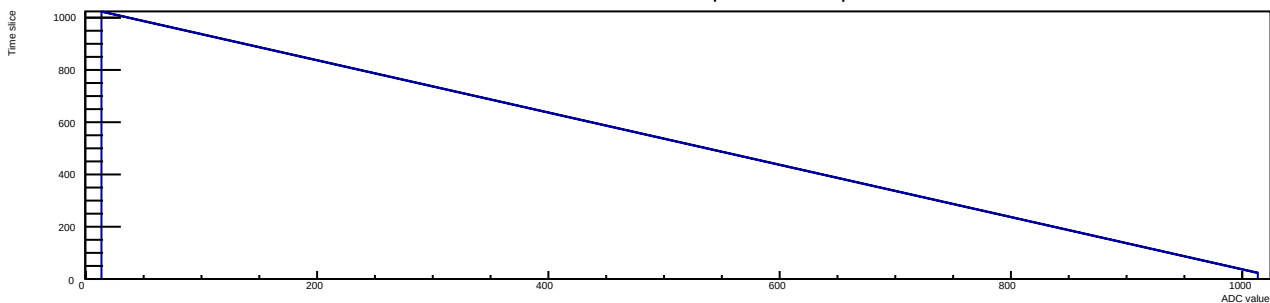
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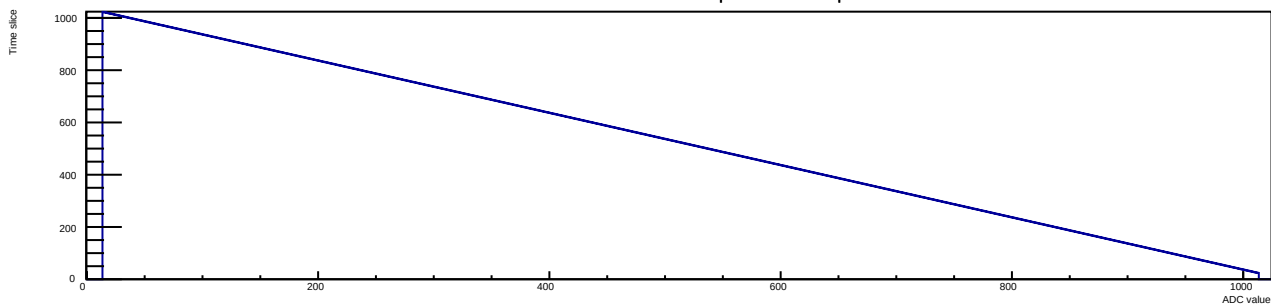
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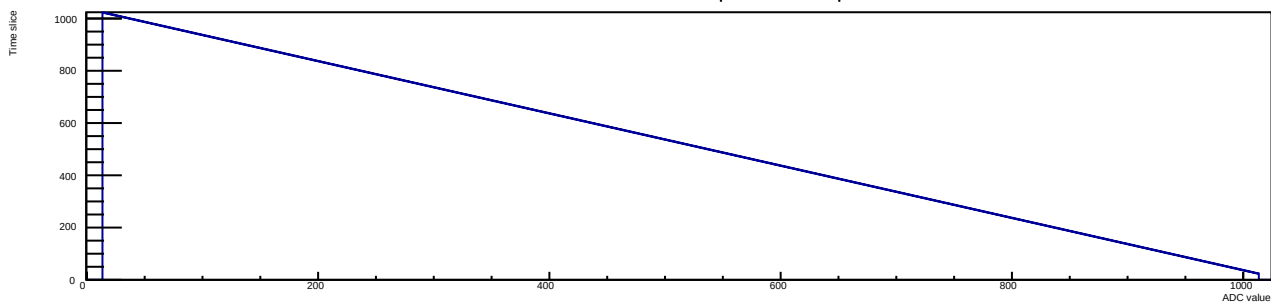
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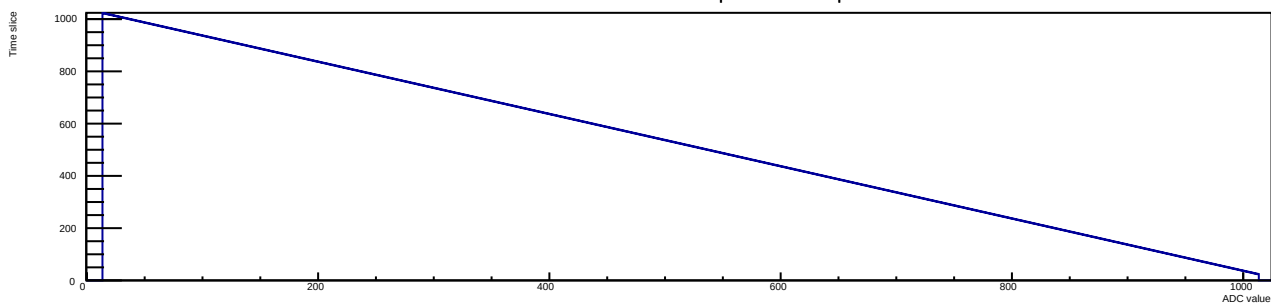
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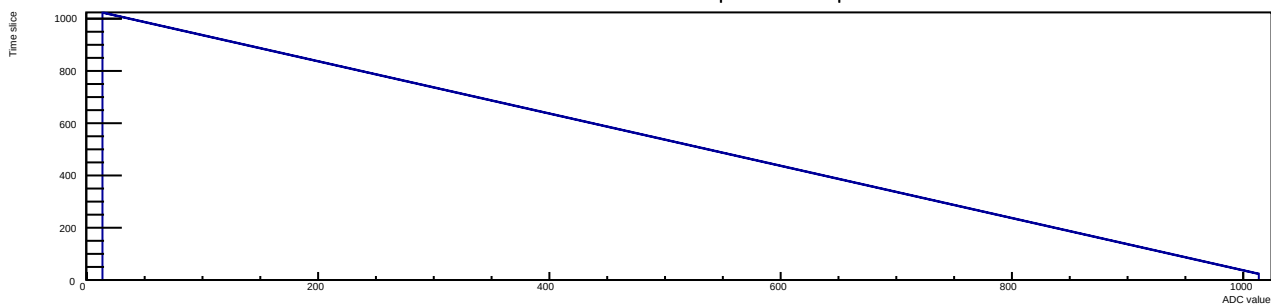
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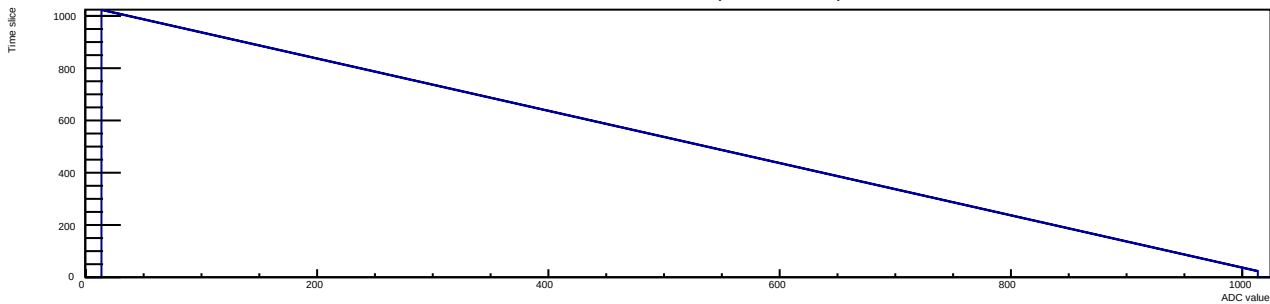
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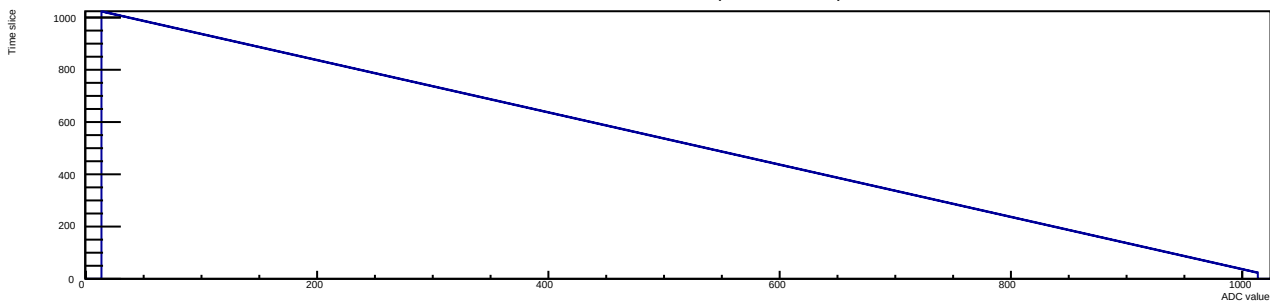
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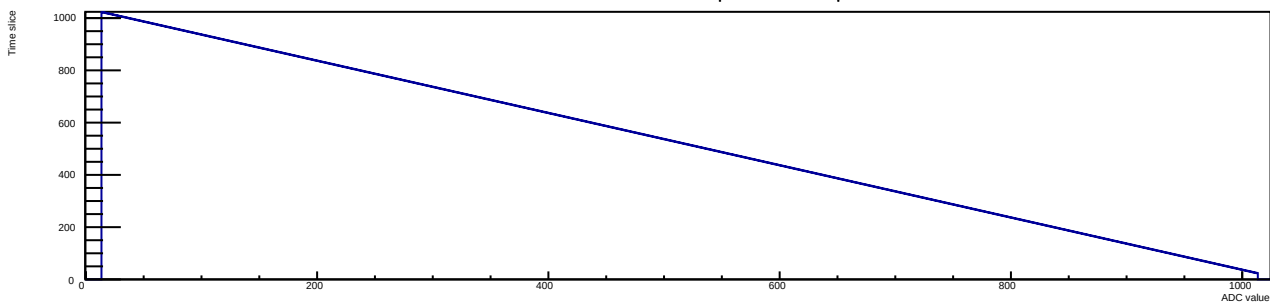
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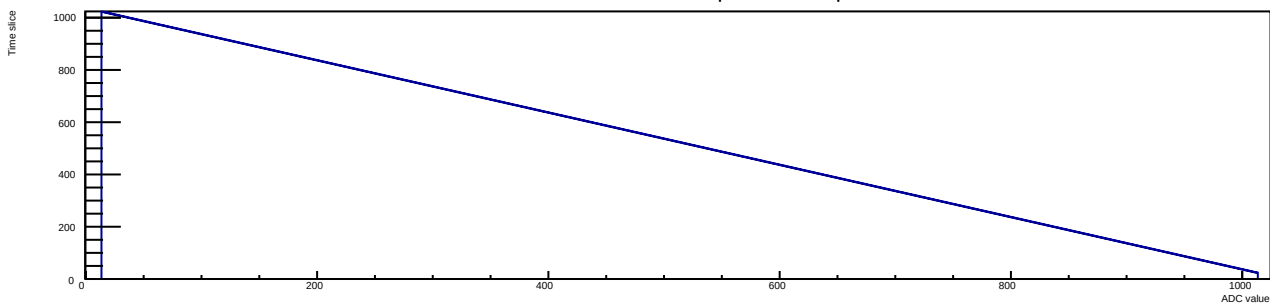
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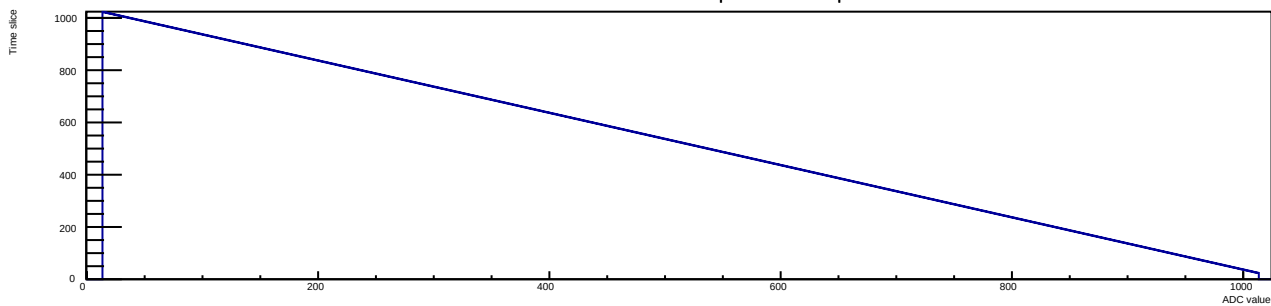
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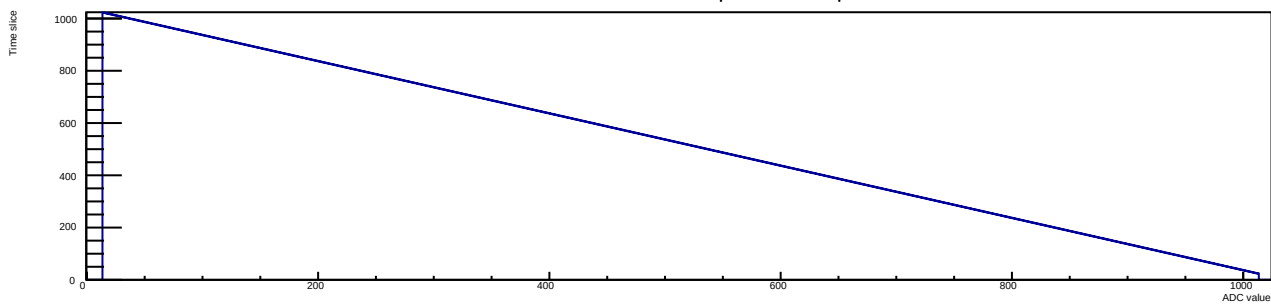
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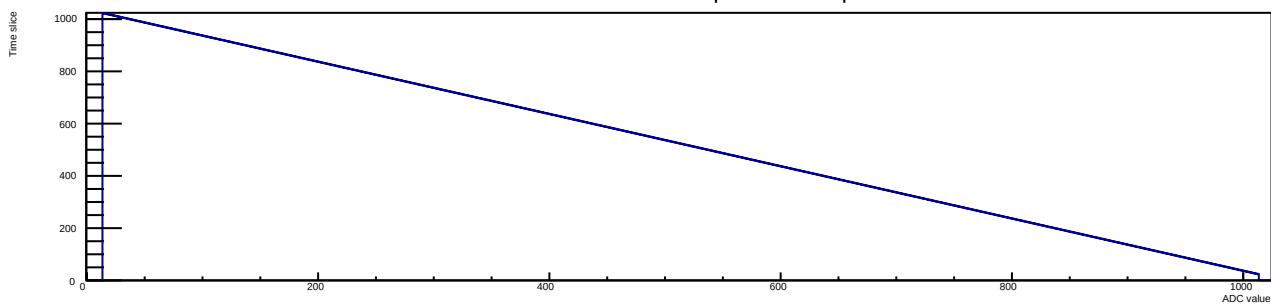
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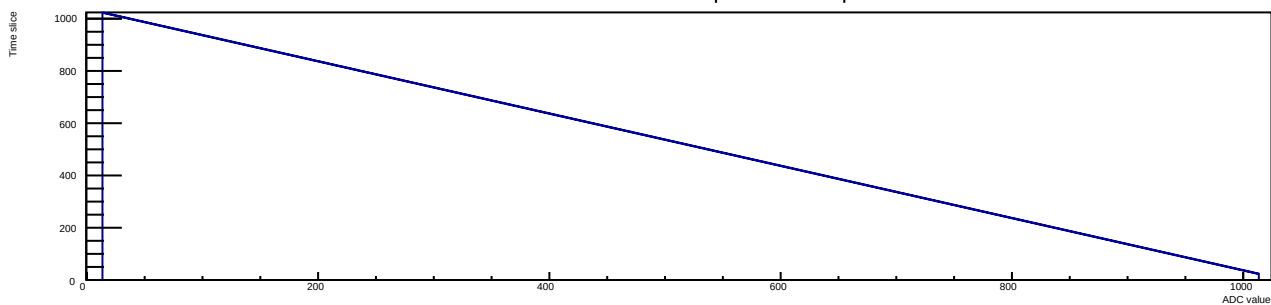
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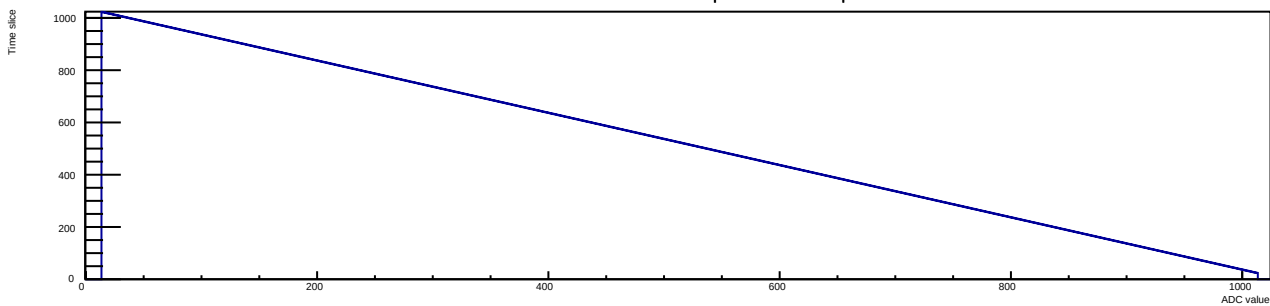
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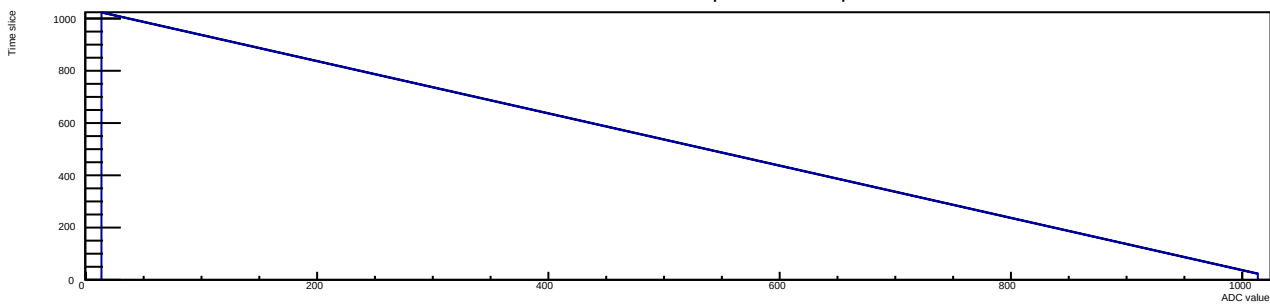
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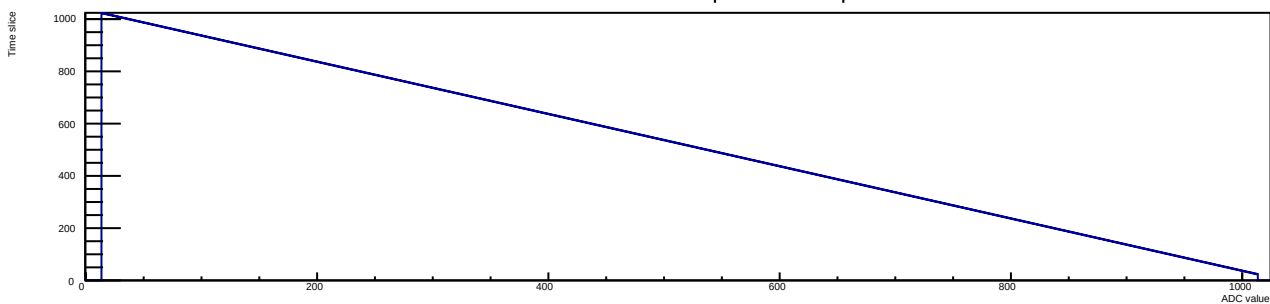
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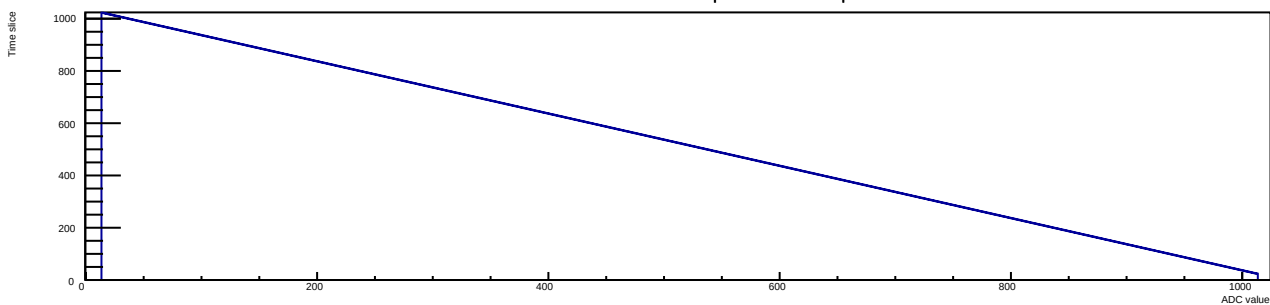
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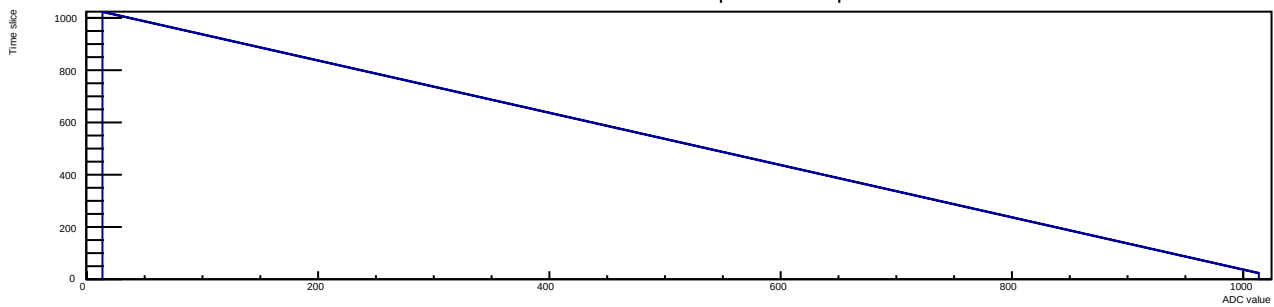
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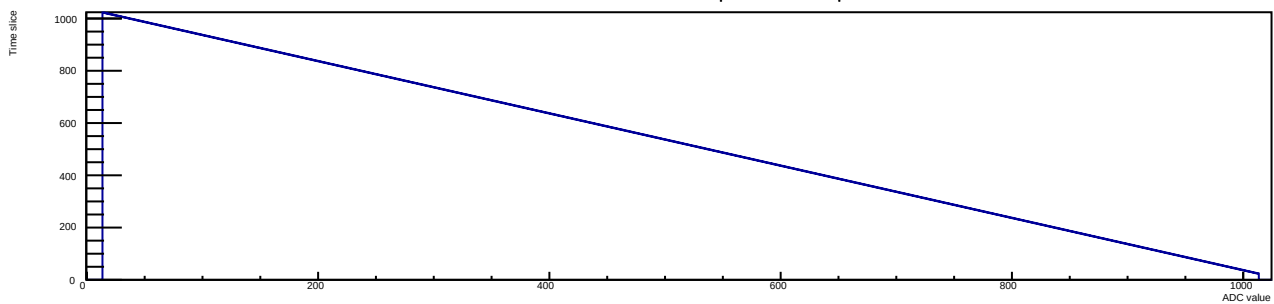
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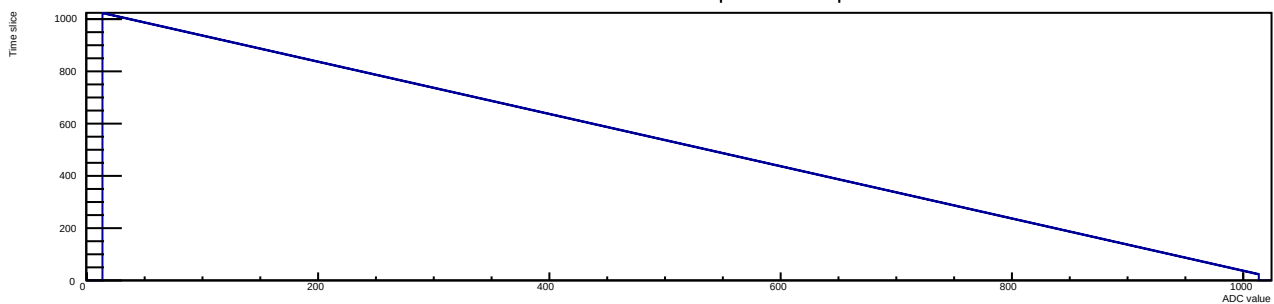
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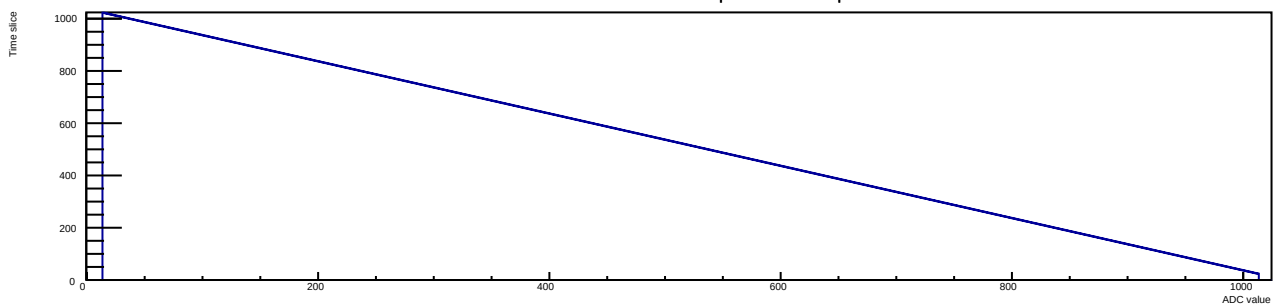
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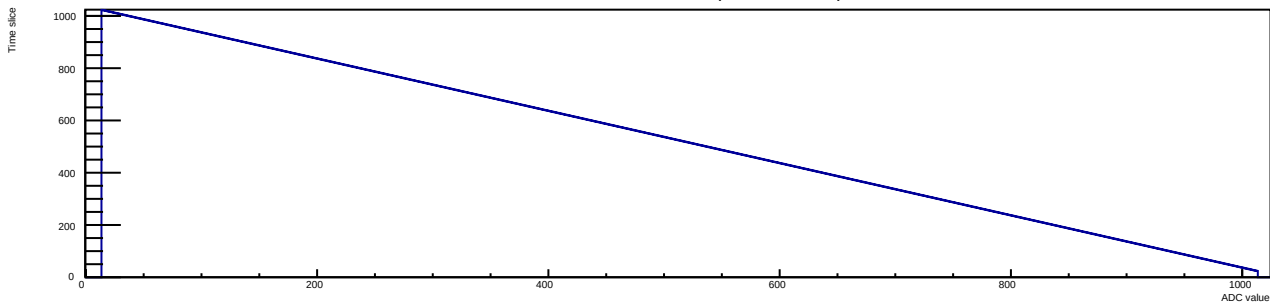
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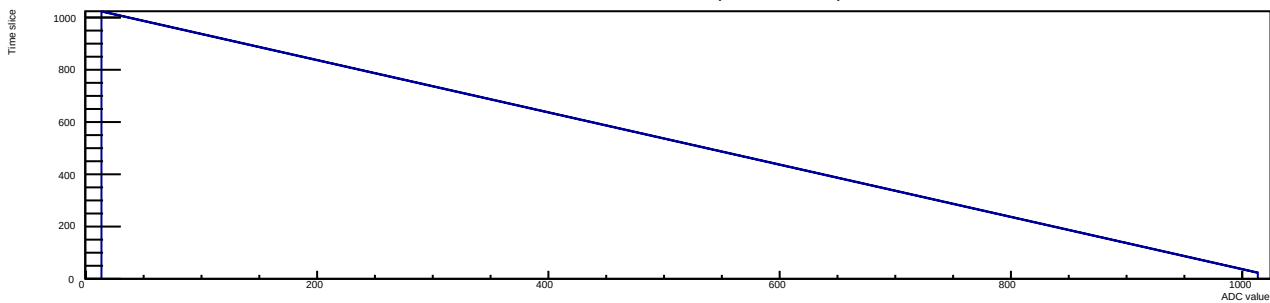
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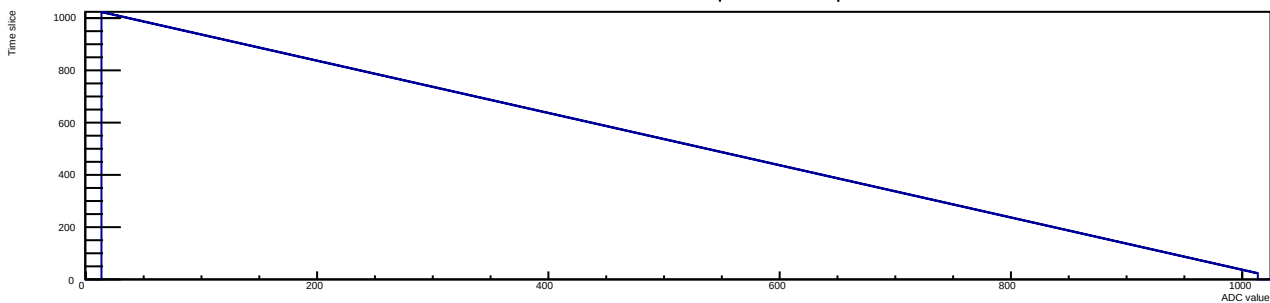
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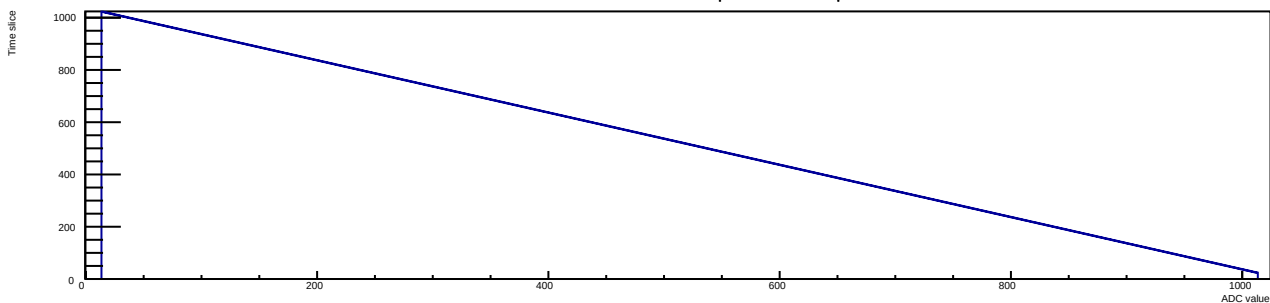
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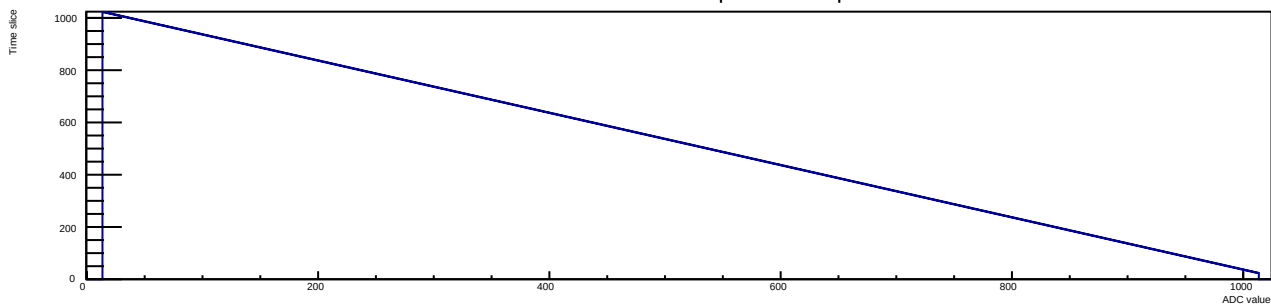
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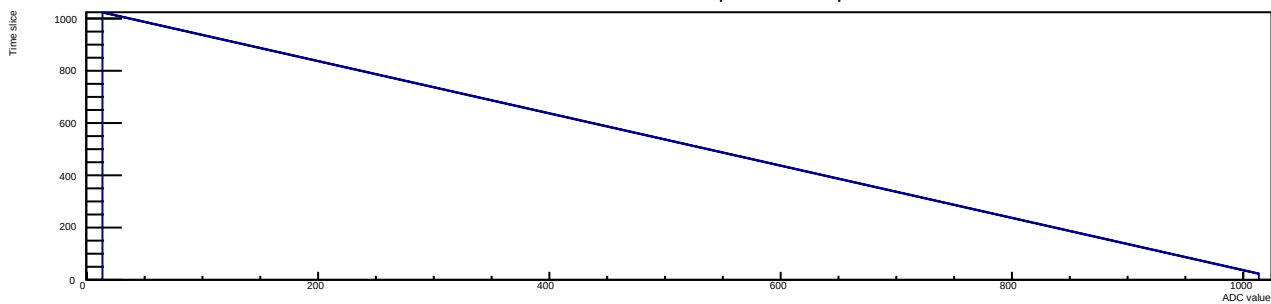
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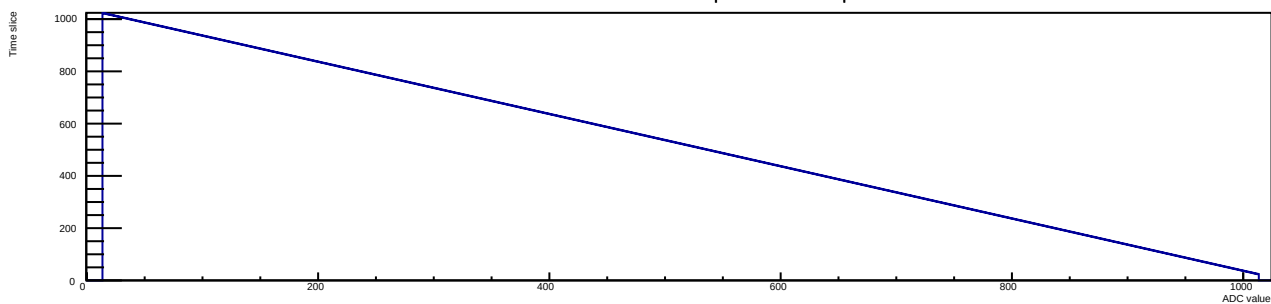
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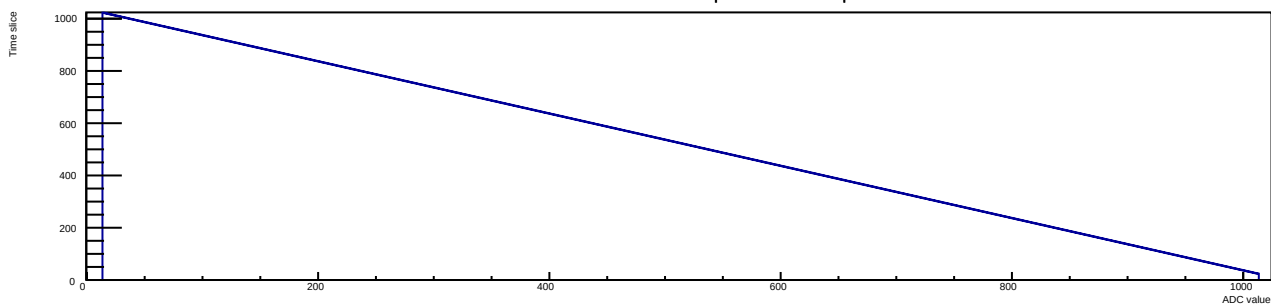
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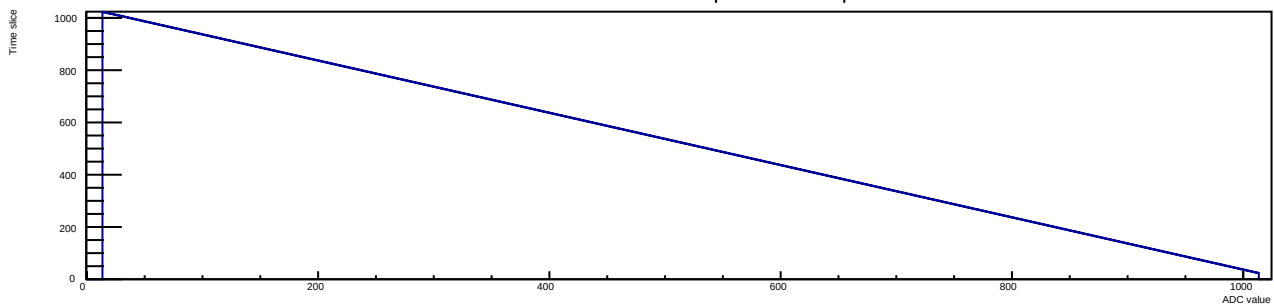
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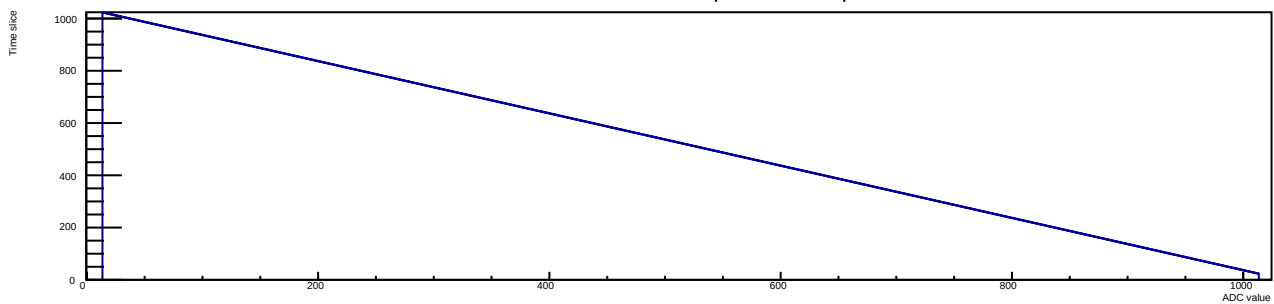
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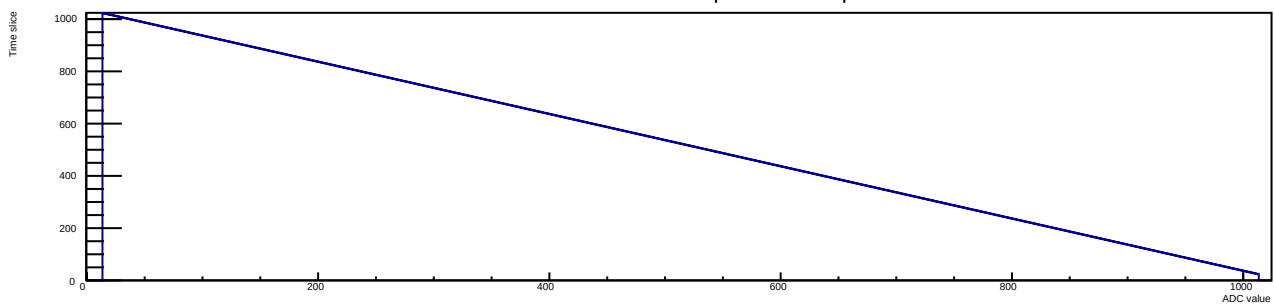
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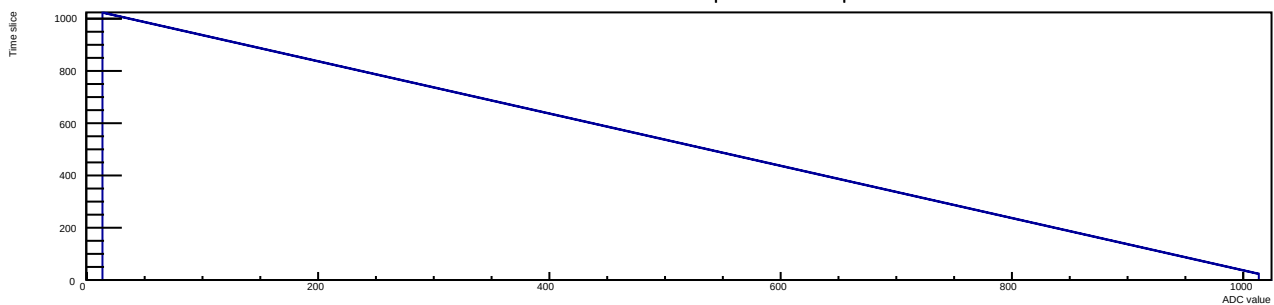
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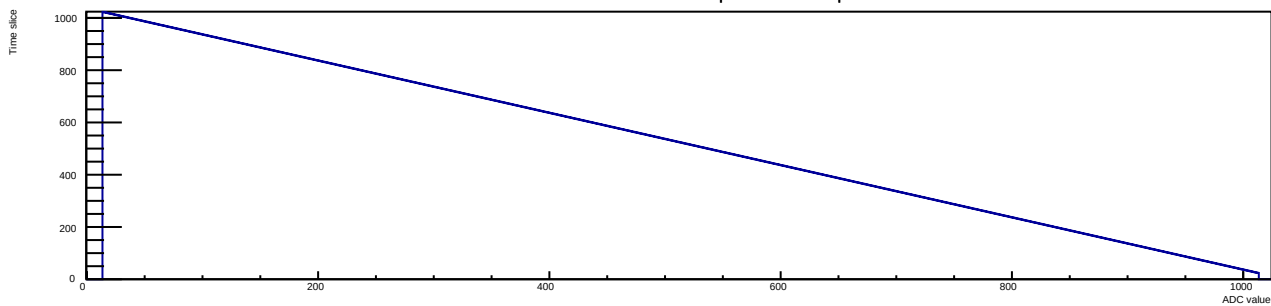
Run 18 Evt 4 Time mcm 0 chip 4 chan 14 ramps-1



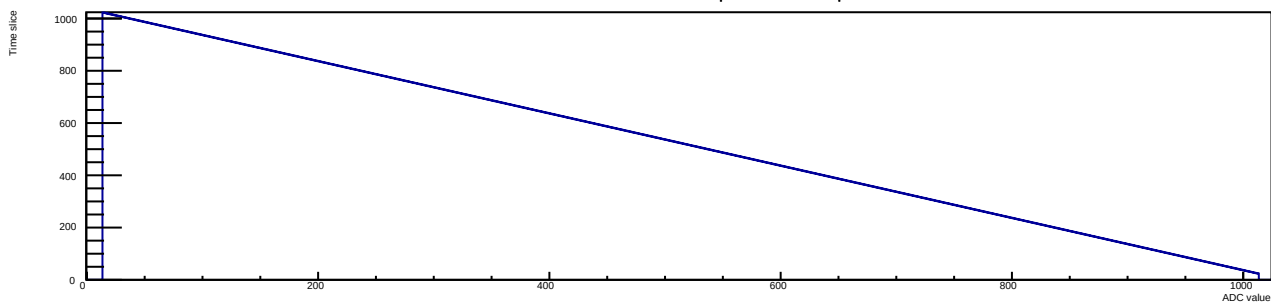
Run 18 Evt 4 Time mcm 0 chip 4 chan 15 ramps-1



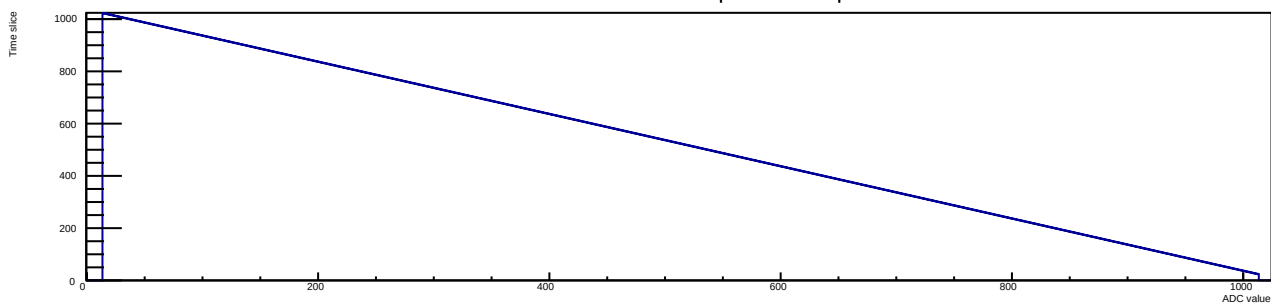
Run 18 Evt 4 Time mcm 0 chip 5 chan 0 ramps-1



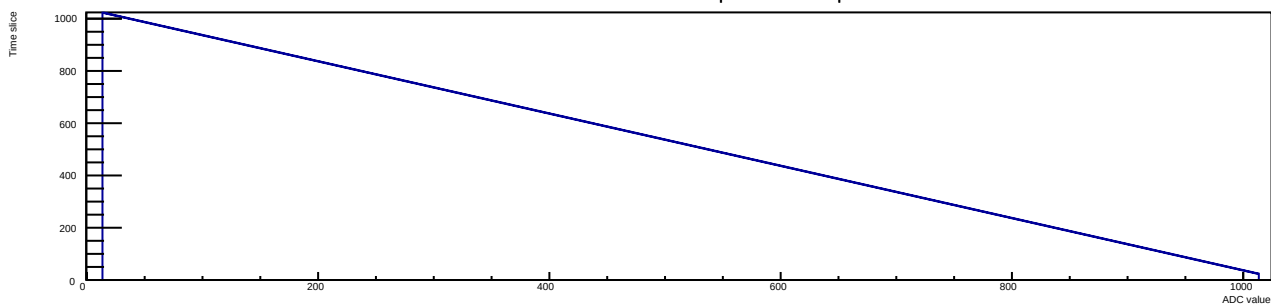
Run 18 Evt 4 Time mcm 0 chip 5 chan 1 ramps-1



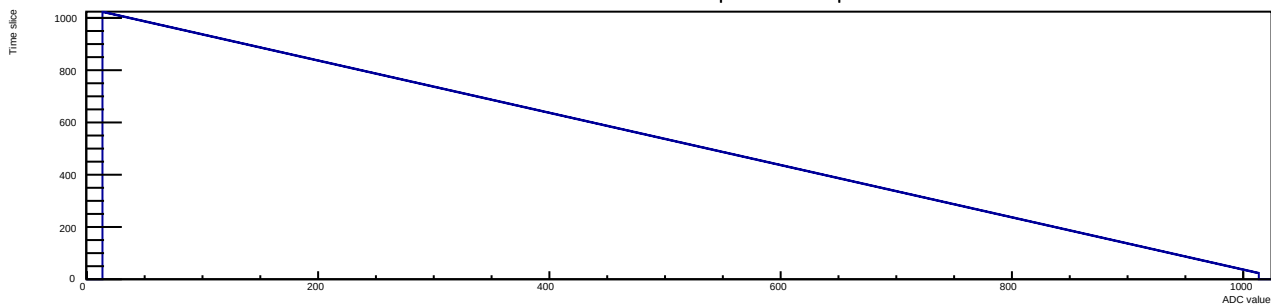
Run 18 Evt 4 Time mcm 0 chip 5 chan 2 ramps-1



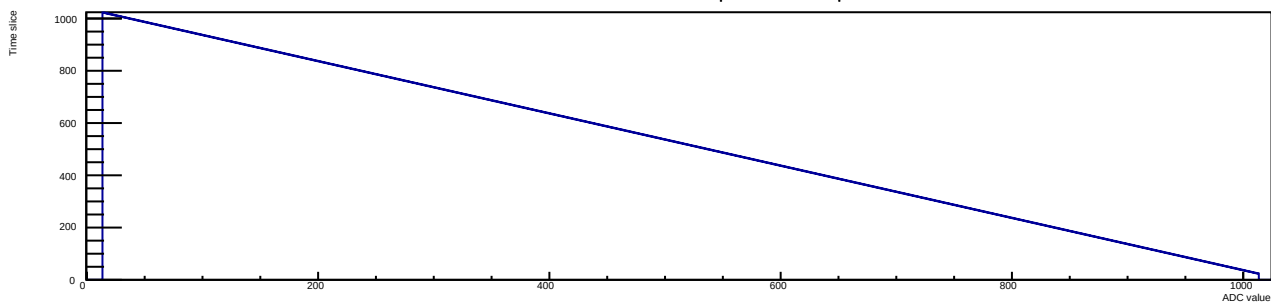
Run 18 Evt 4 Time mcm 0 chip 5 chan 3 ramps-1



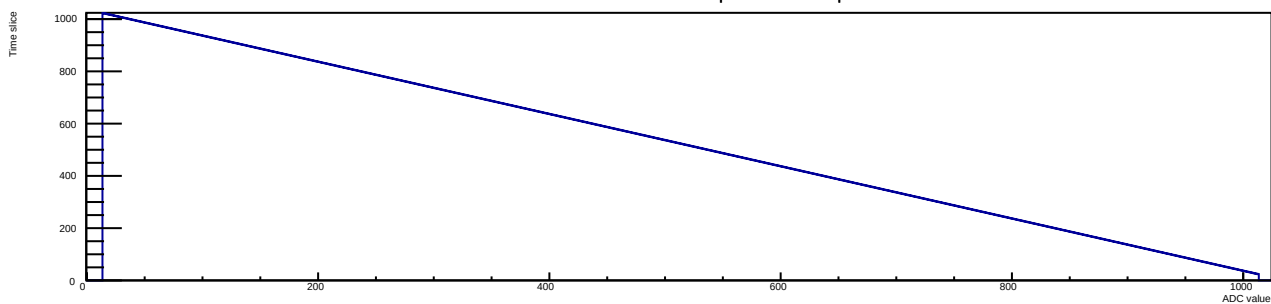
Run 18 Evt 4 Time mcm 0 chip 5 chan 4 ramps-1



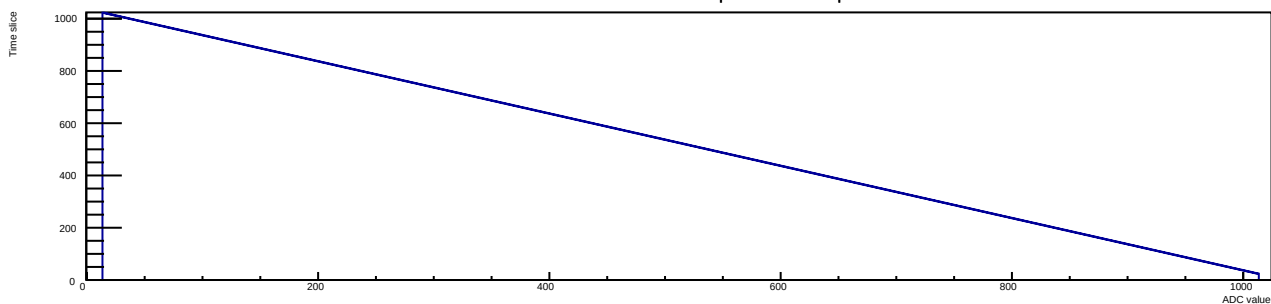
Run 18 Evt 4 Time mcm 0 chip 5 chan 5 ramps-1



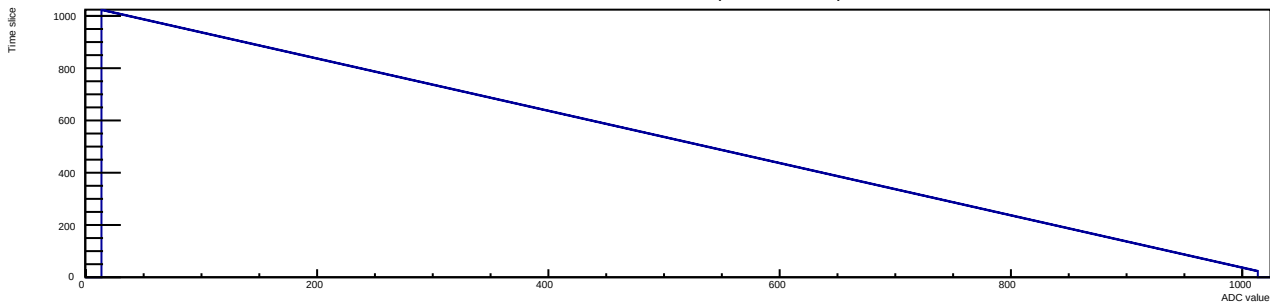
Run 18 Evt 4 Time mcm 0 chip 5 chan 6 ramps-1



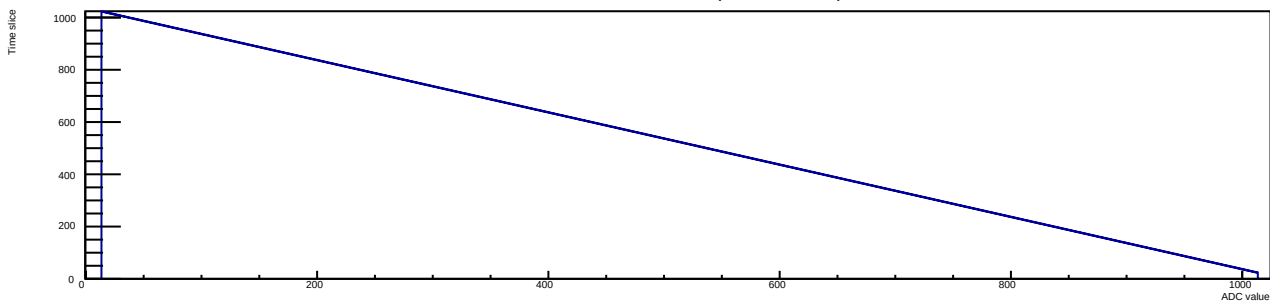
Run 18 Evt 4 Time mcm 0 chip 5 chan 7 ramps-1



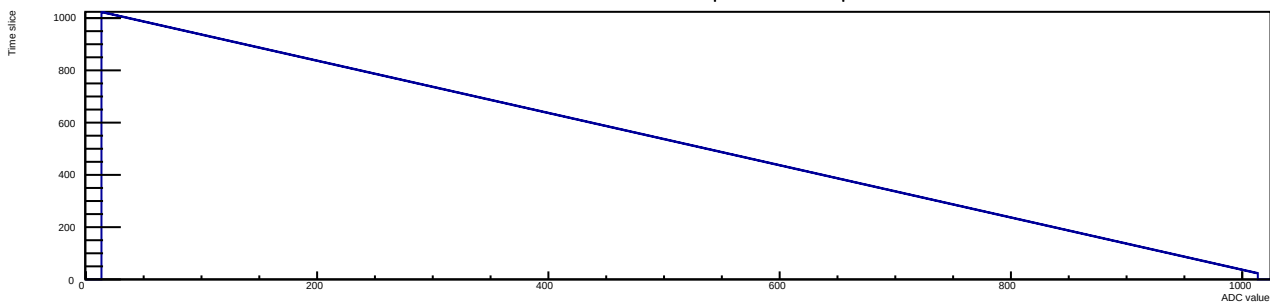
Run 18 Evt 4 Time mcm 0 chip 5 chan 8 ramps-1



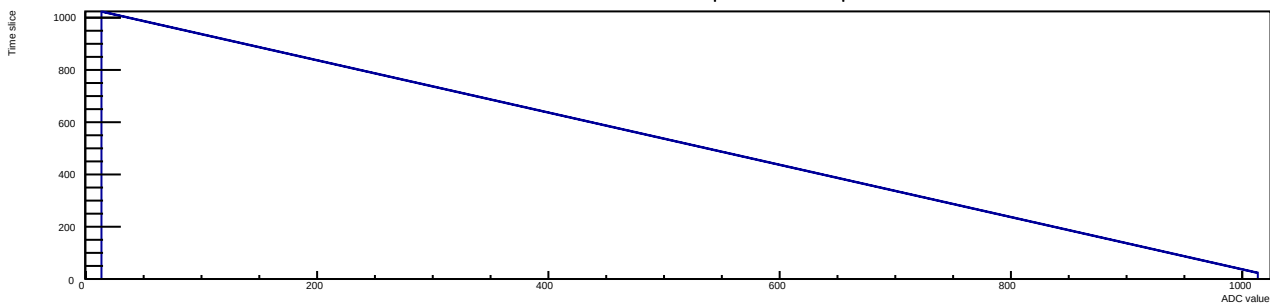
Run 18 Evt 4 Time mcm 0 chip 5 chan 9 ramps-1



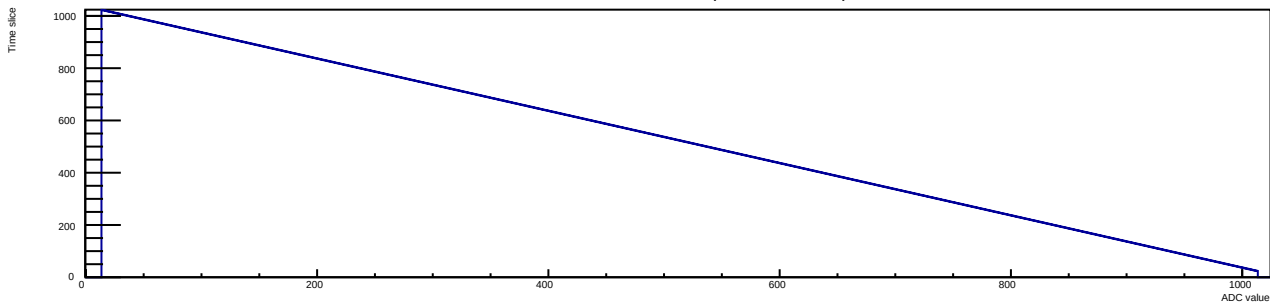
Run 18 Evt 4 Time mcm 0 chip 5 chan 10 ramps-1



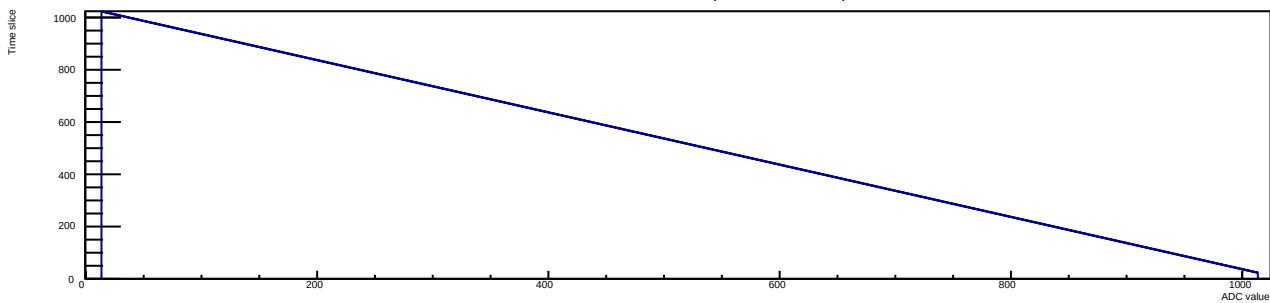
Run 18 Evt 4 Time mcm 0 chip 5 chan 11 ramps-1



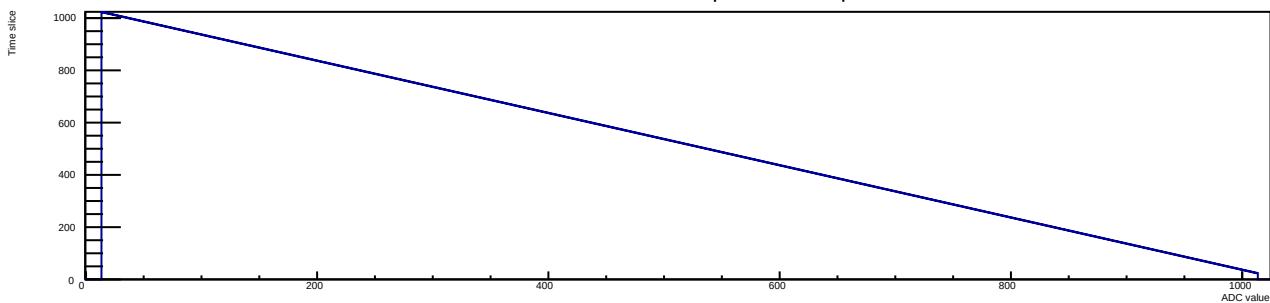
Run 18 Evt 4 Time mcm 0 chip 5 chan 12 ramps-1



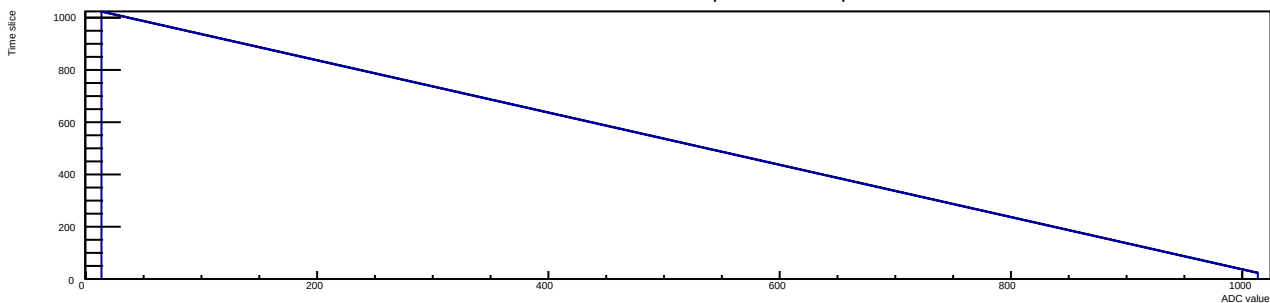
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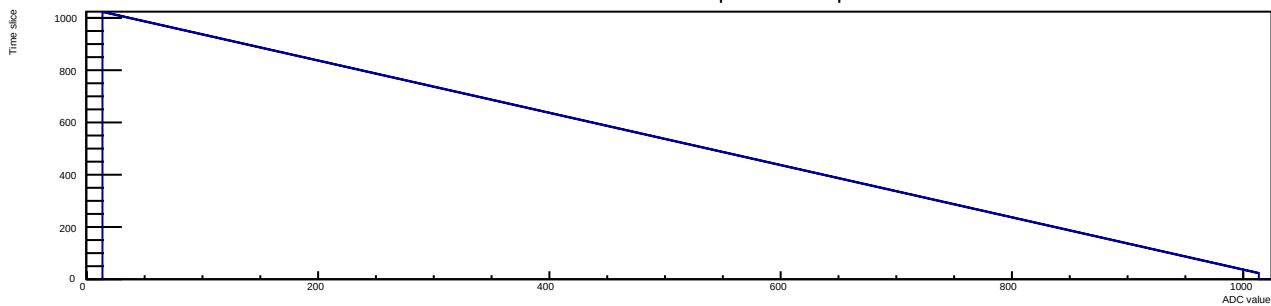
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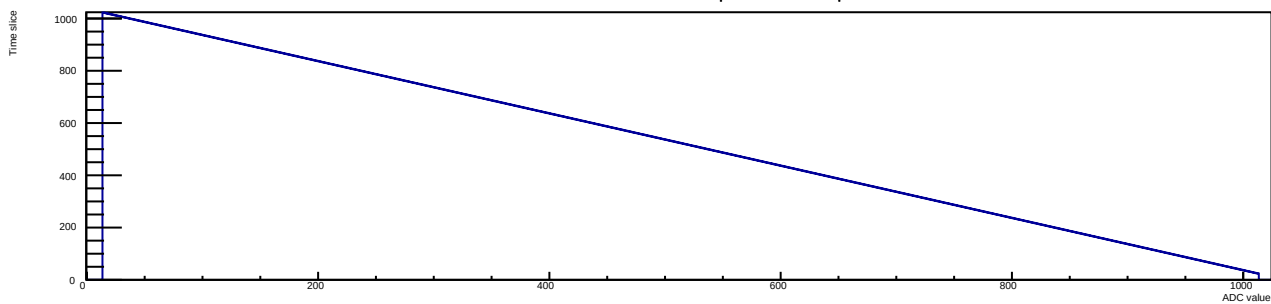
Run 18 Evt 4 Time mcm 0 chip 5 chan 15 ramps-1



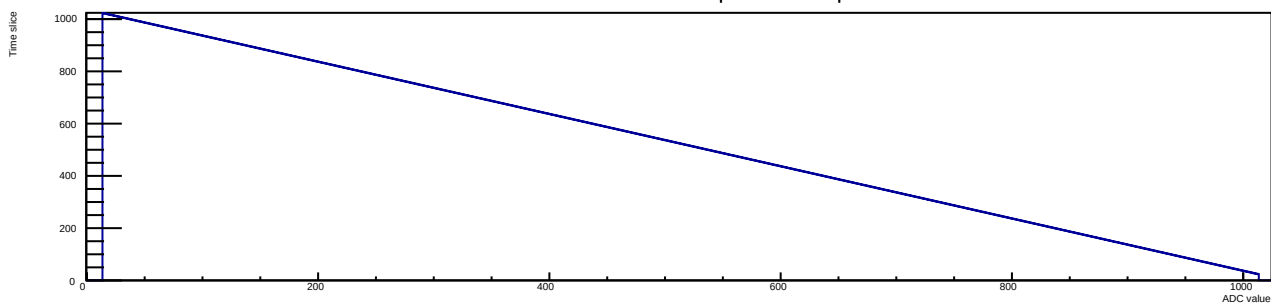
Run 18 Evt 4 Time mcm 0 chip 6 chan 0 ramps-1



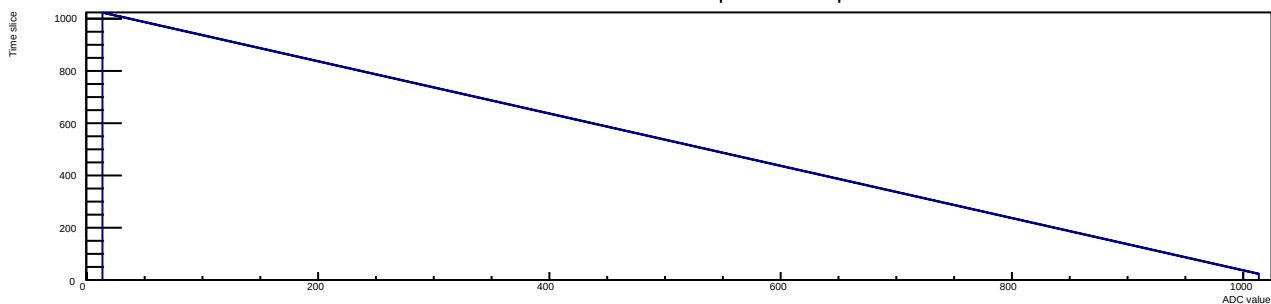
Run 18 Evt 4 Time mcm 0 chip 6 chan 1 ramps-1



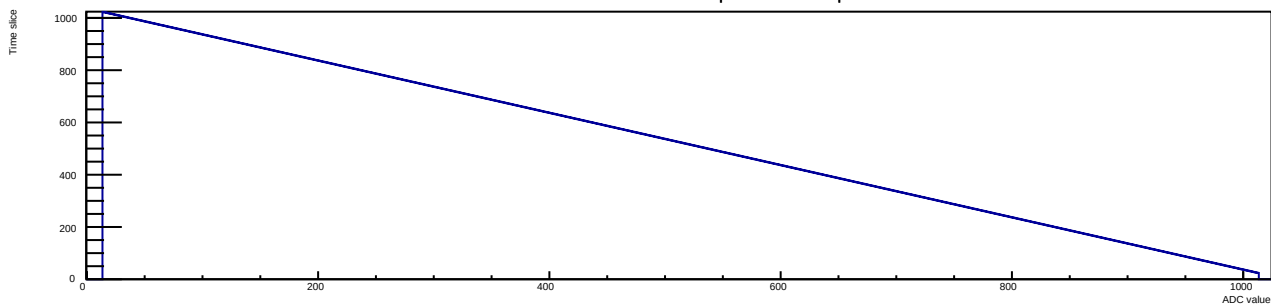
Run 18 Evt 4 Time mcm 0 chip 6 chan 2 ramps-1



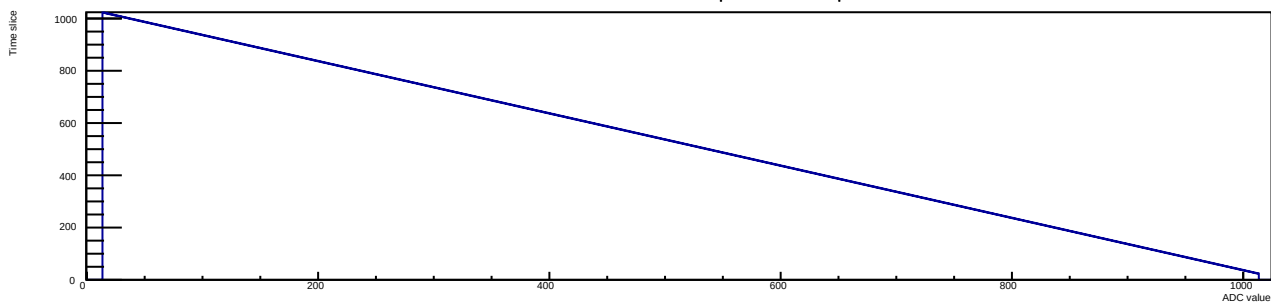
Run 18 Evt 4 Time mcm 0 chip 6 chan 3 ramps-1



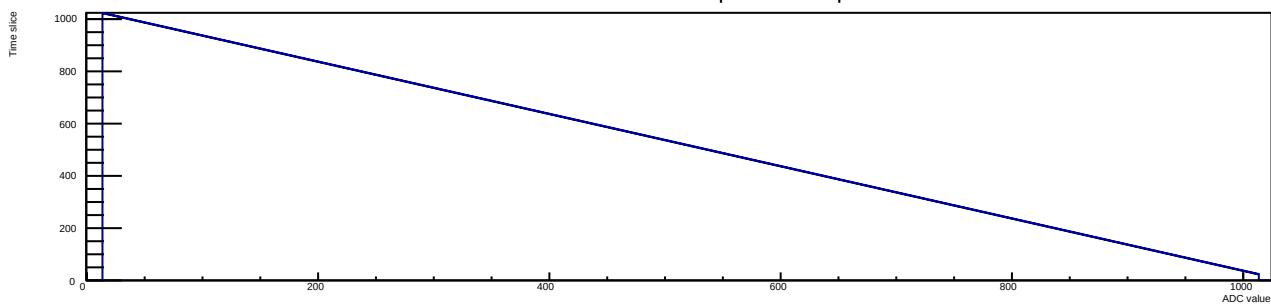
Run 18 Evt 4 Time mcm 0 chip 6 chan 4 ramps-1



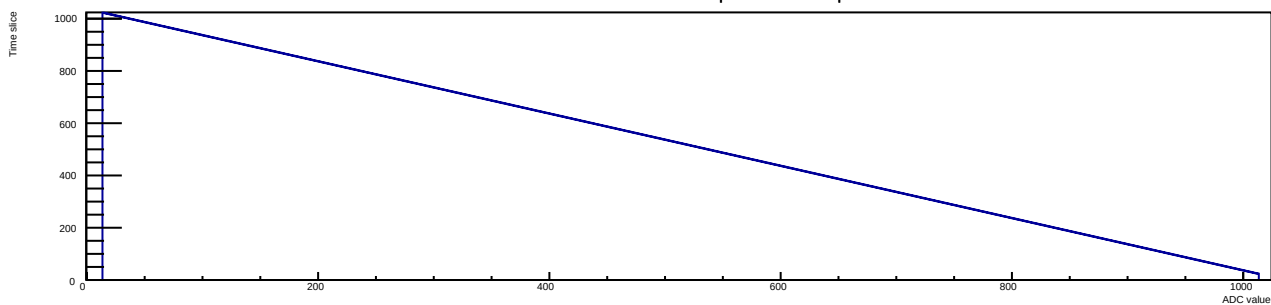
Run 18 Evt 4 Time mcm 0 chip 6 chan 5 ramps-1



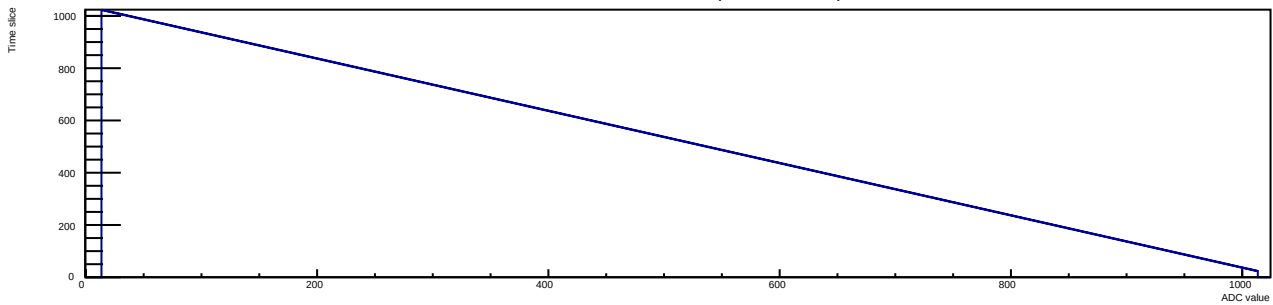
Run 18 Evt 4 Time mcm 0 chip 6 chan 6 ramps-1



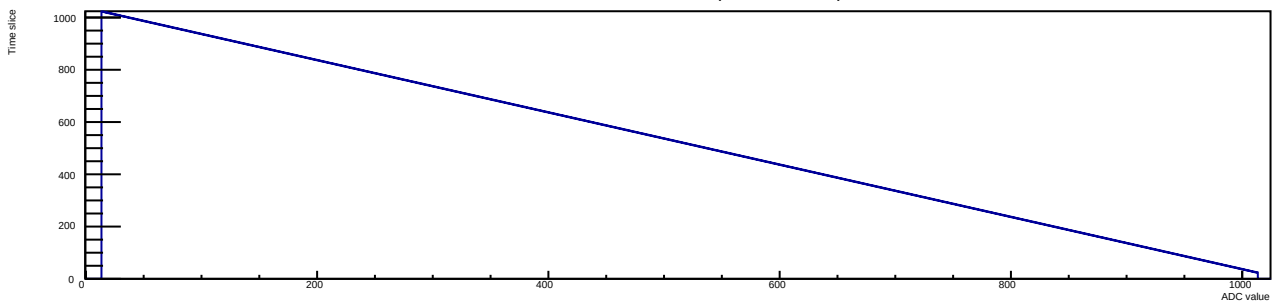
Run 18 Evt 4 Time mcm 0 chip 6 chan 7 ramps-1



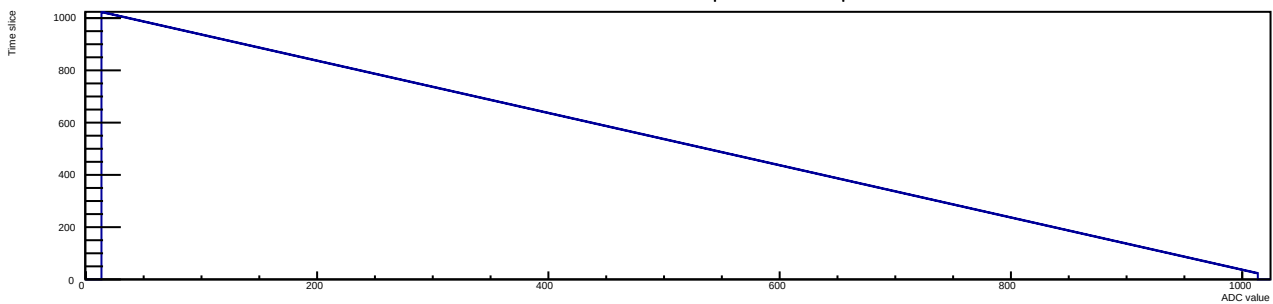
Run 18 Evt 4 Time mcm 0 chip 6 chan 8 ramps-1



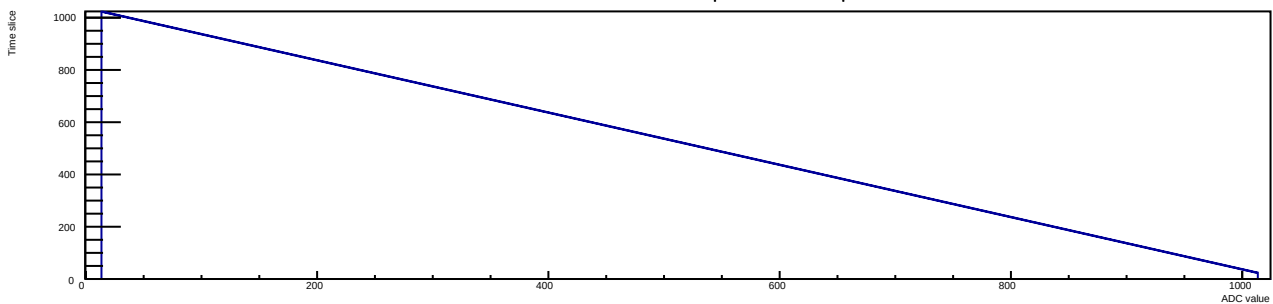
Run 18 Evt 4 Time mcm 0 chip 6 chan 9 ramps-1



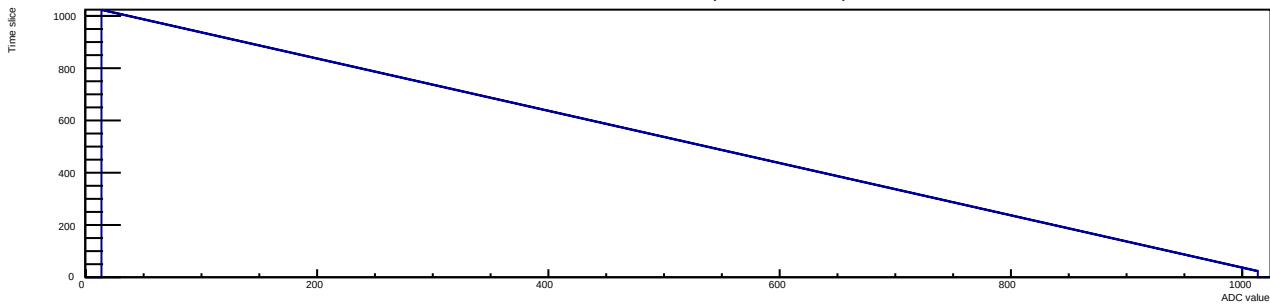
Run 18 Evt 4 Time mcm 0 chip 6 chan 10 ramps-1



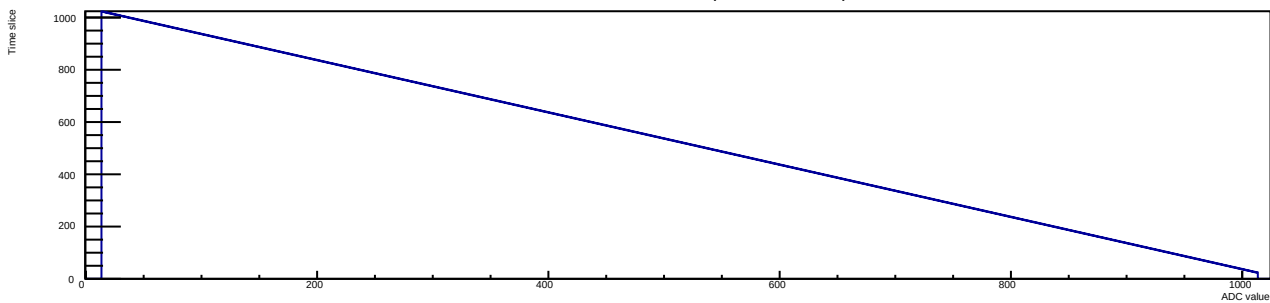
Run 18 Evt 4 Time mcm 0 chip 6 chan 11 ramps-1



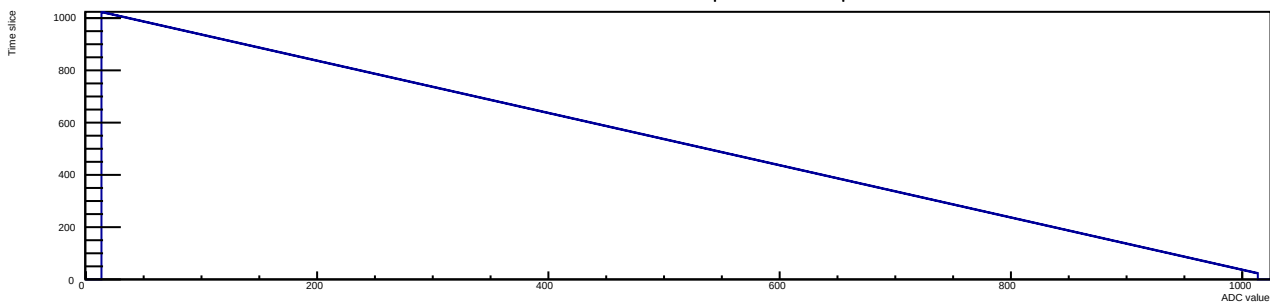
Run 18 Evt 4 Time mcm 0 chip 6 chan 12 ramps-1



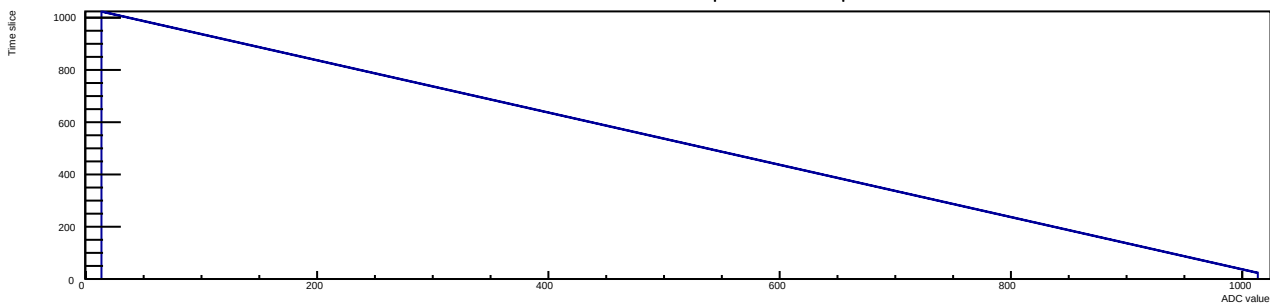
Run 18 Evt 4 Time mcm 0 chip 6 chan 13 ramps-1



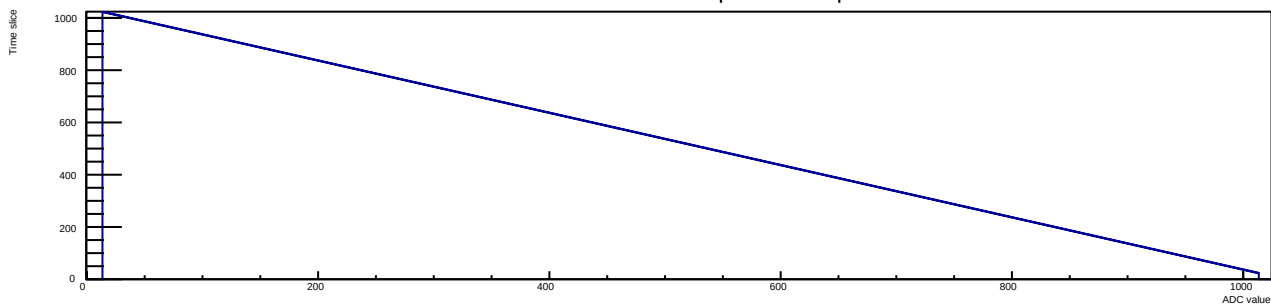
Run 18 Evt 4 Time mcm 0 chip 6 chan 14 ramps-1



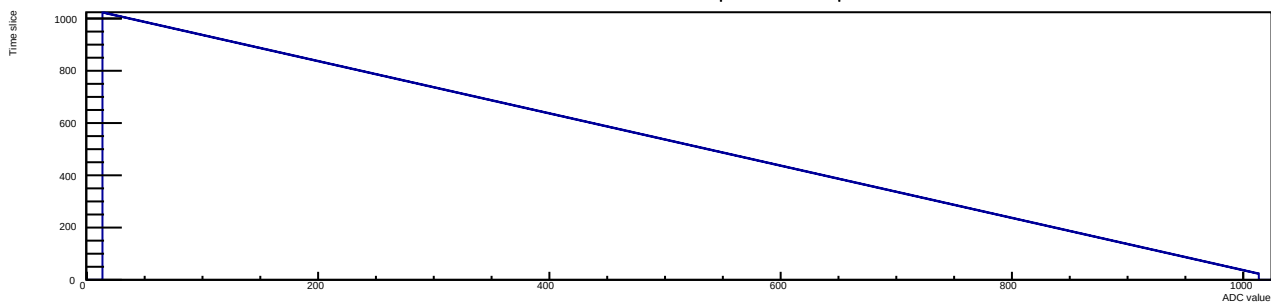
Run 18 Evt 4 Time mcm 0 chip 6 chan 15 ramps-1



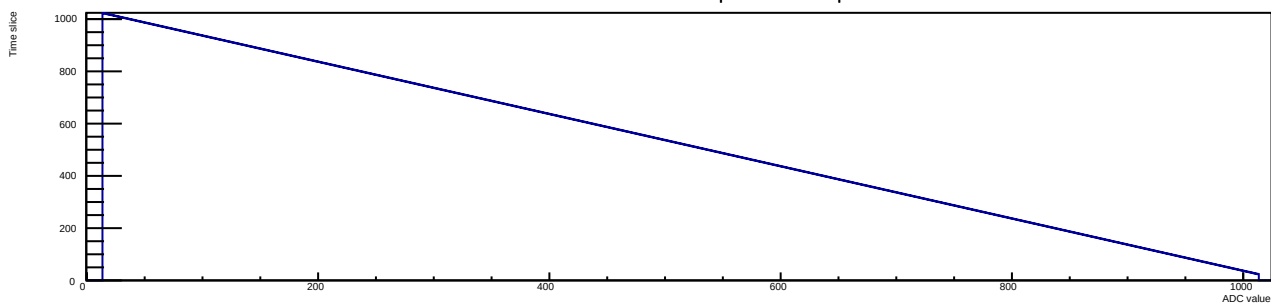
Run 18 Evt 4 Time mcm 0 chip 7 chan 0 ramps-1



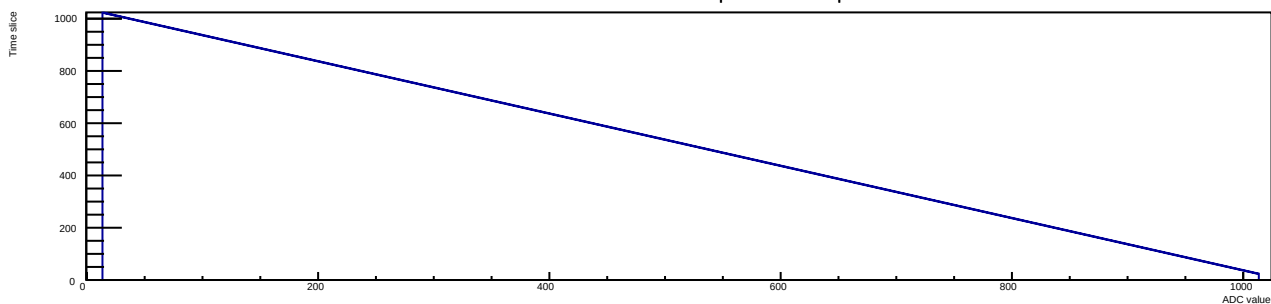
Run 18 Evt 4 Time mcm 0 chip 7 chan 1 ramps-1



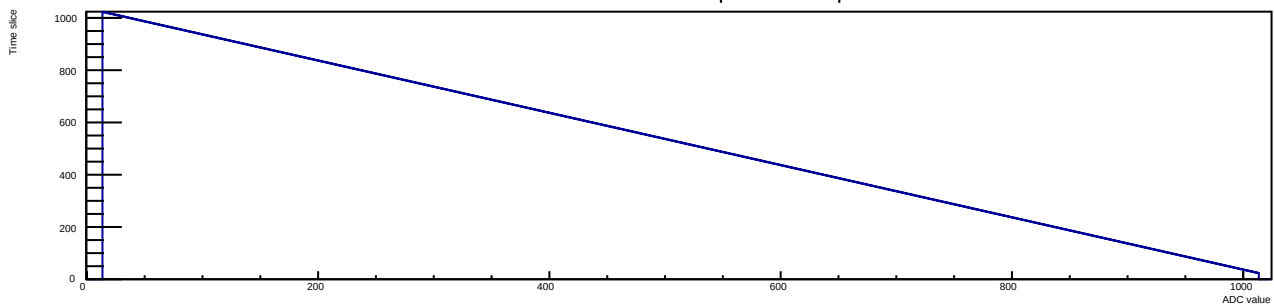
Run 18 Evt 4 Time mcm 0 chip 7 chan 2 ramps-1



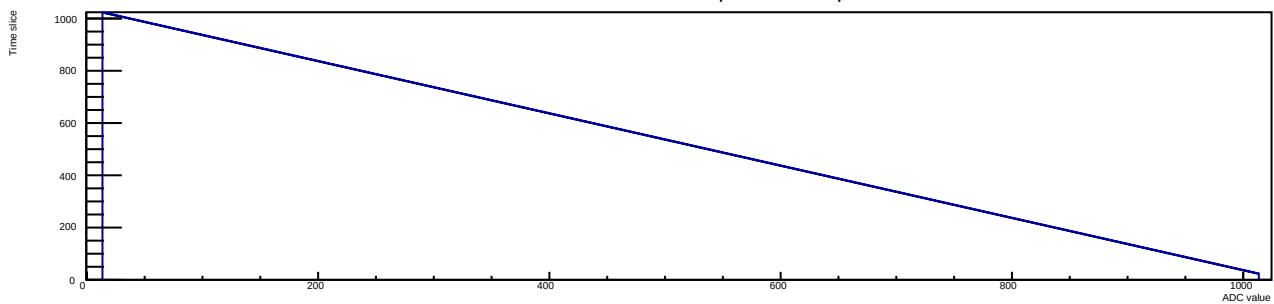
Run 18 Evt 4 Time mcm 0 chip 7 chan 3 ramps-1



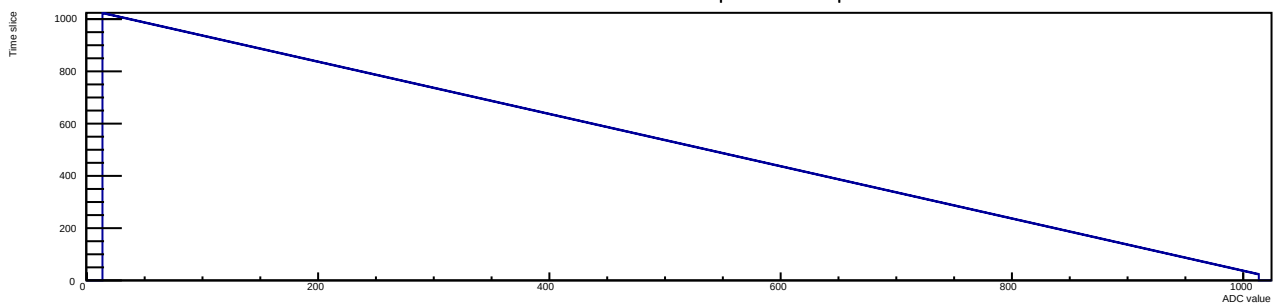
Run 18 Evt 4 Time mcm 0 chip 7 chan 4 ramps-1



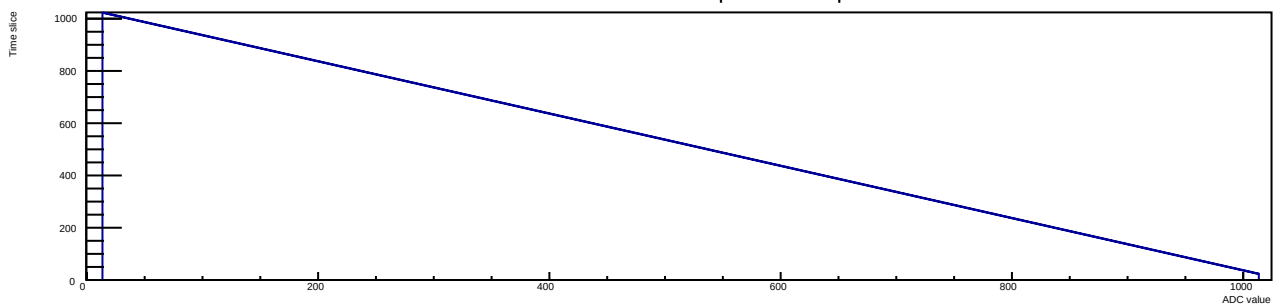
Run 18 Evt 4 Time mcm 0 chip 7 chan 5 ramps-1



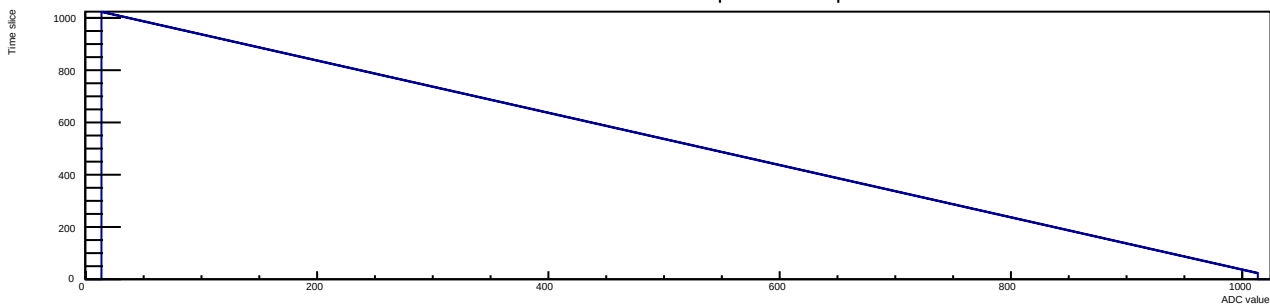
Run 18 Evt 4 Time mcm 0 chip 7 chan 6 ramps-1



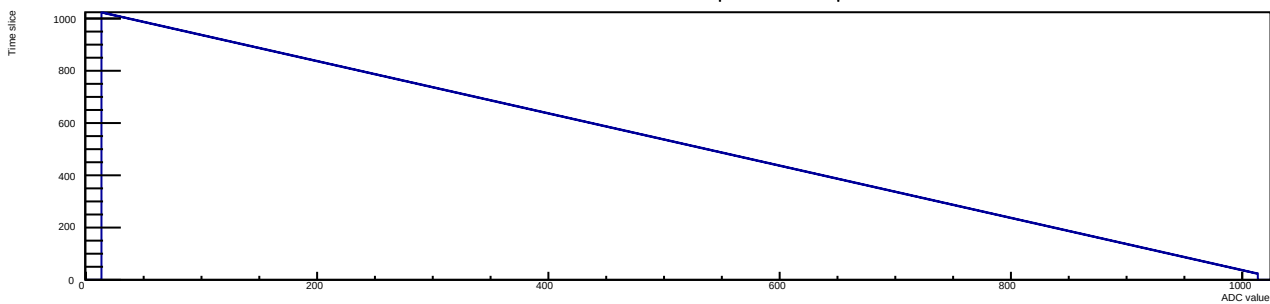
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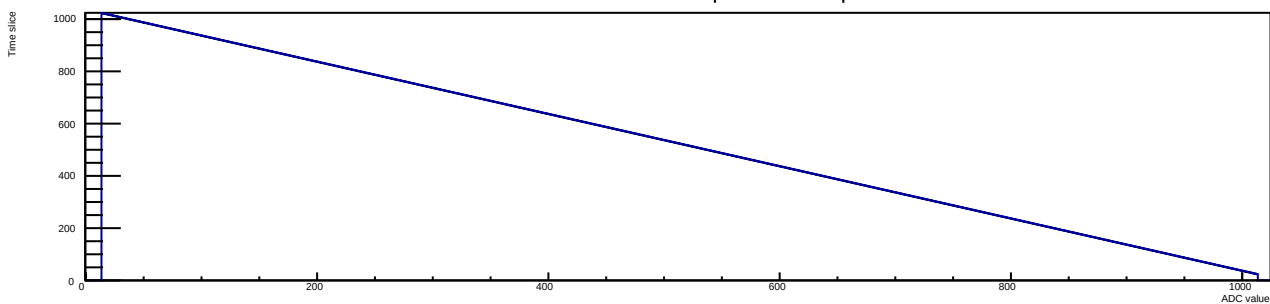
Run 18 Evt 4 Time mcm 0 chip 7 chan 8 ramps-1



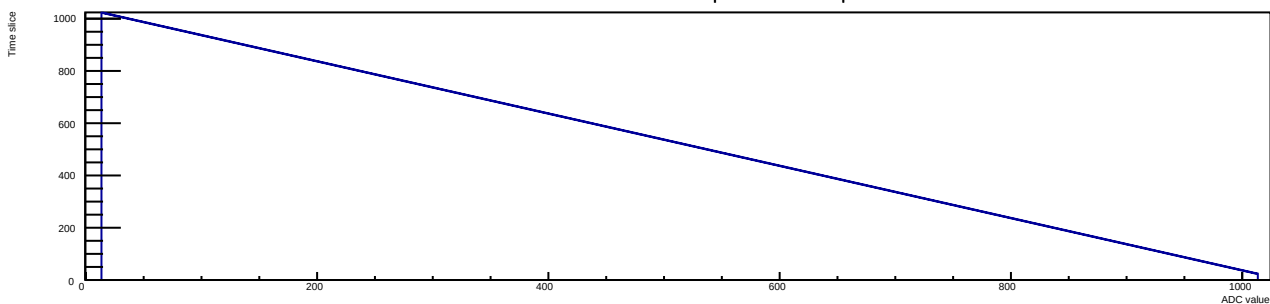
Run 18 Evt 4 Time mcm 0 chip 7 chan 9 ramps-1



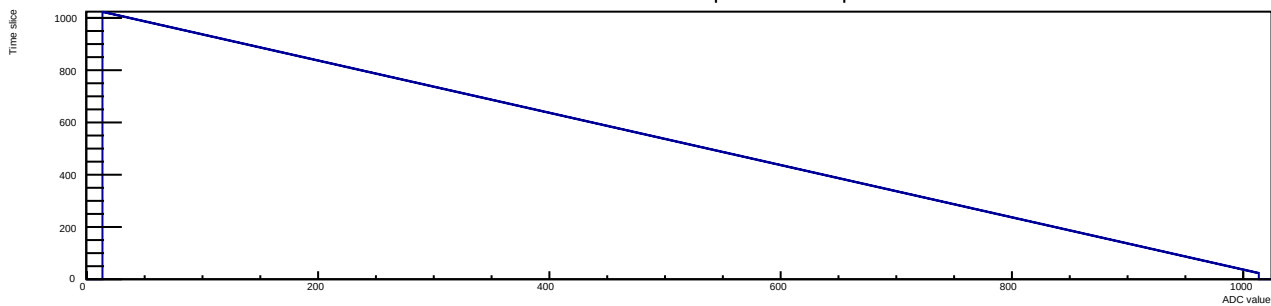
Run 18 Evt 4 Time mcm 0 chip 7 chan 10 ramps-1



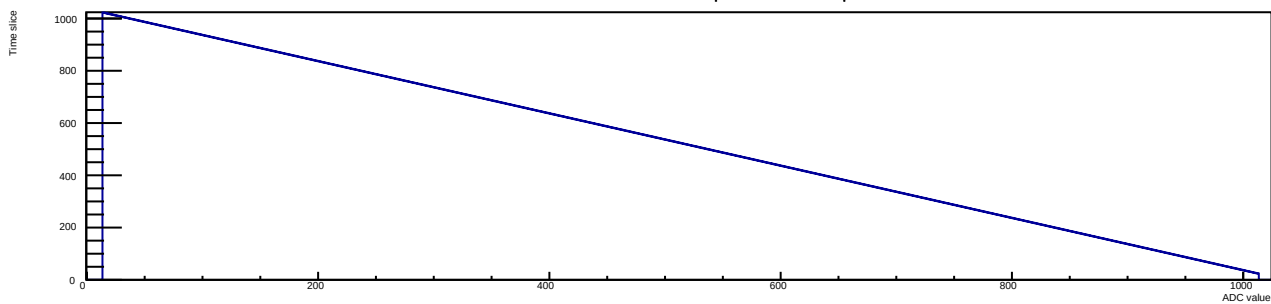
Run 18 Evt 4 Time mcm 0 chip 7 chan 11 ramps-1



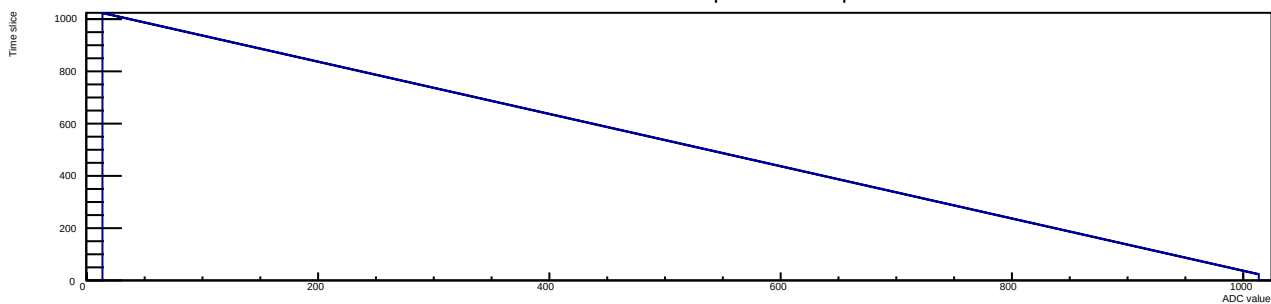
Run 18 Evt 4 Time mcm 0 chip 7 chan 12 ramps-1



Run 18 Evt 4 Time mcm 0 chip 7 chan 13 ramps-1



Run 18 Evt 4 Time mcm 0 chip 7 chan 14 ramps-1



Run 18 Evt 4 Time mcm 0 chip 7 chan 15 ramps-1

