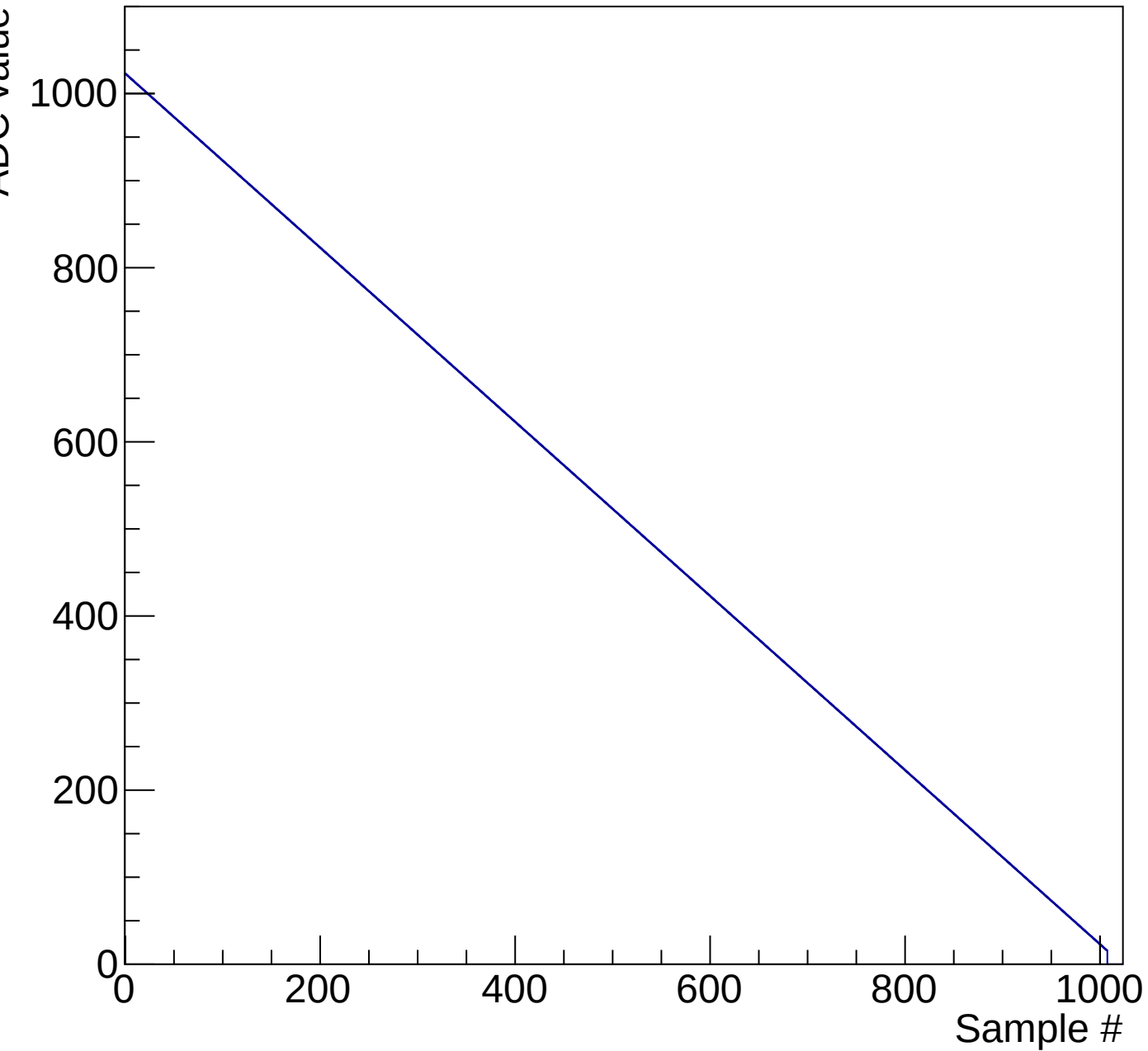
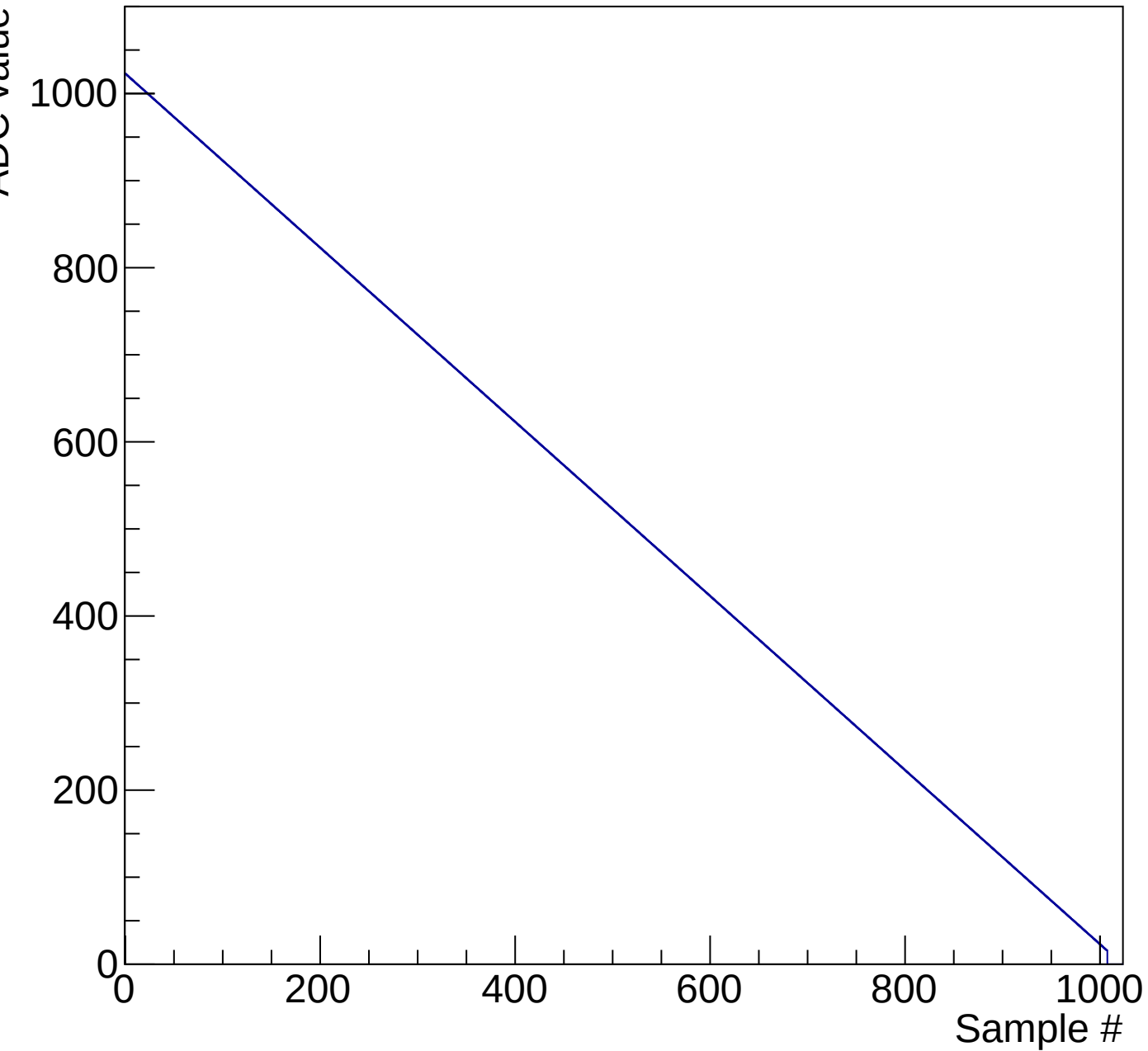


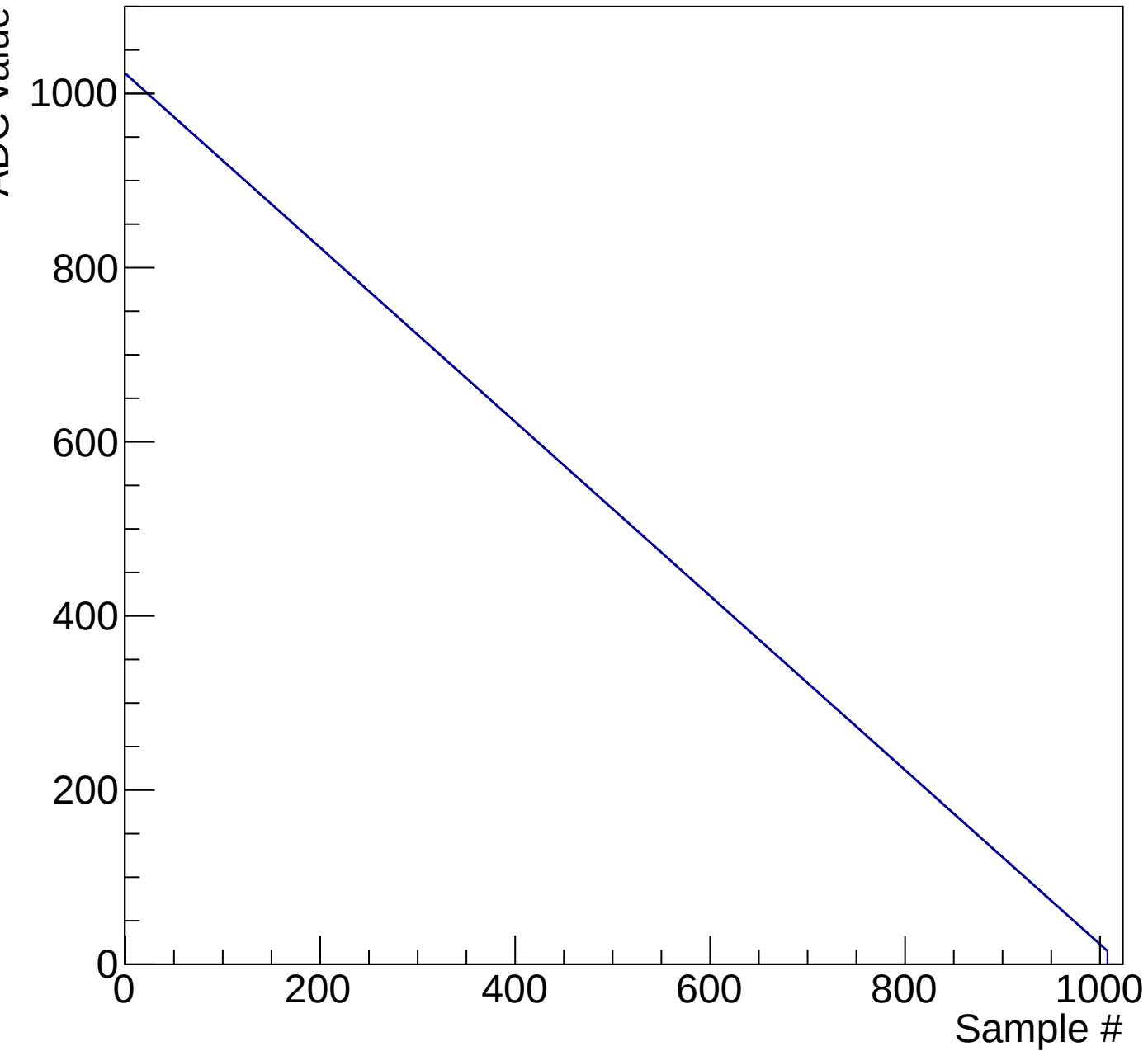
Channel 0 pattern 2



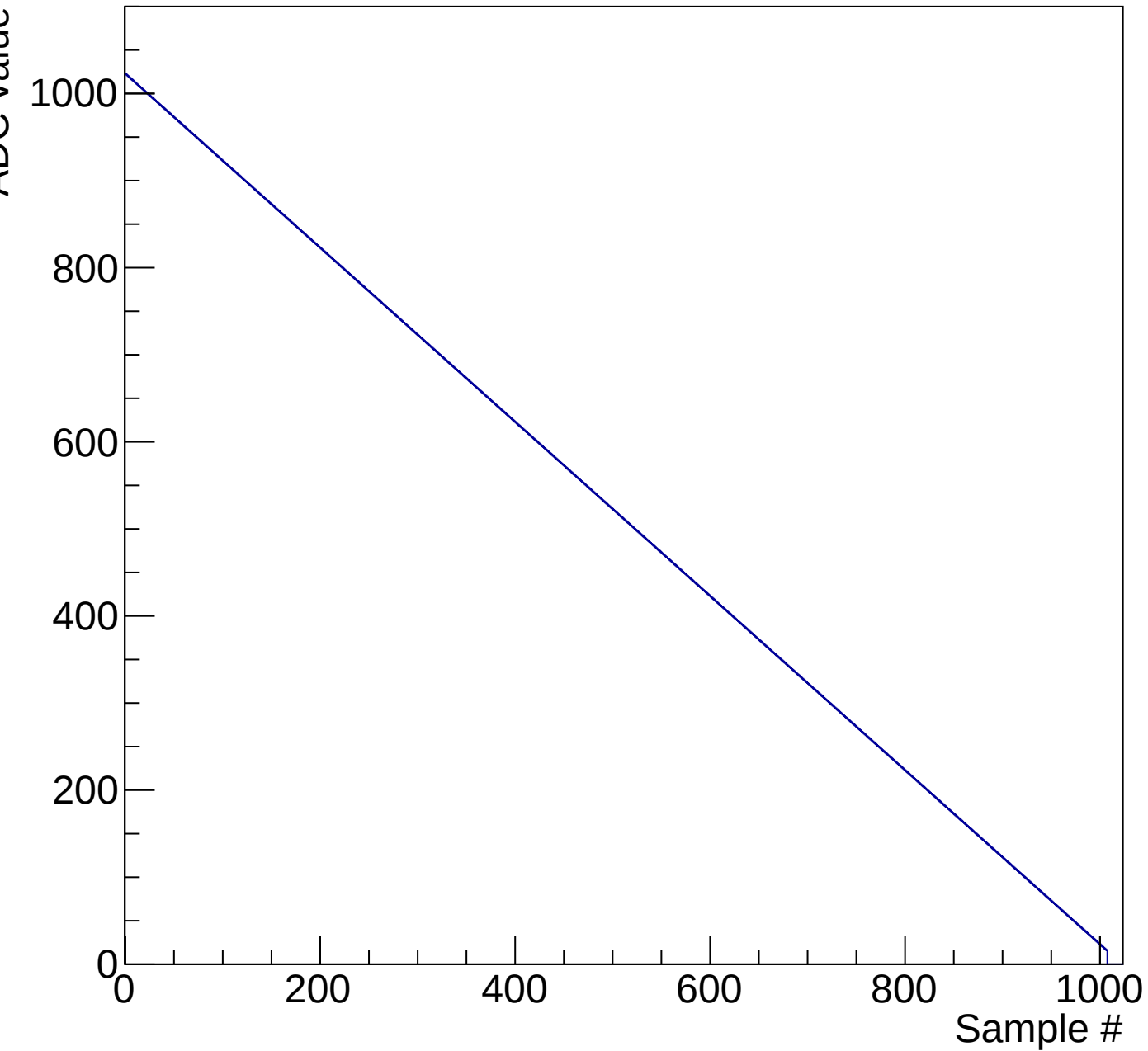
Channel 1 pattern 2



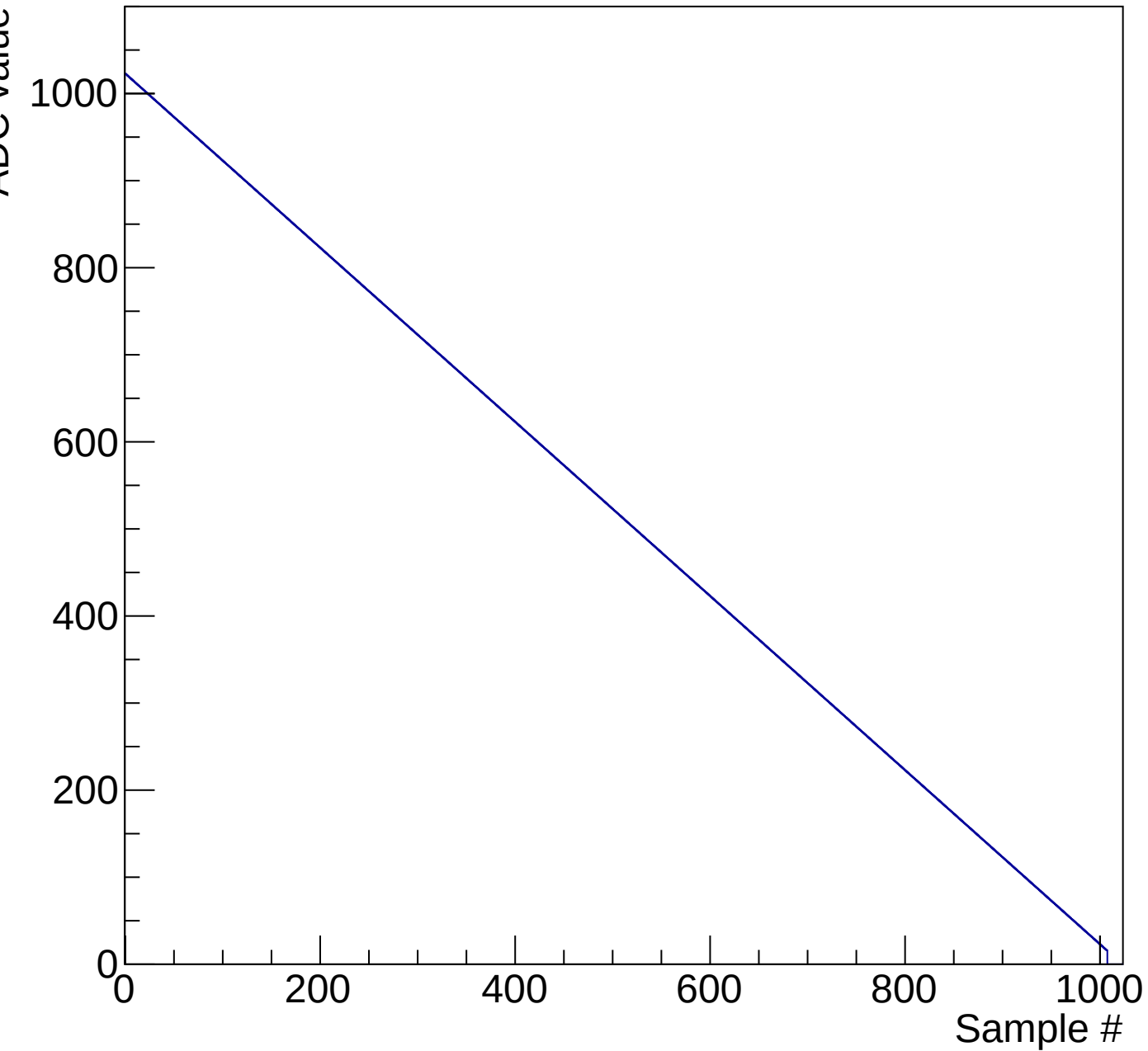
Channel 2 pattern 2



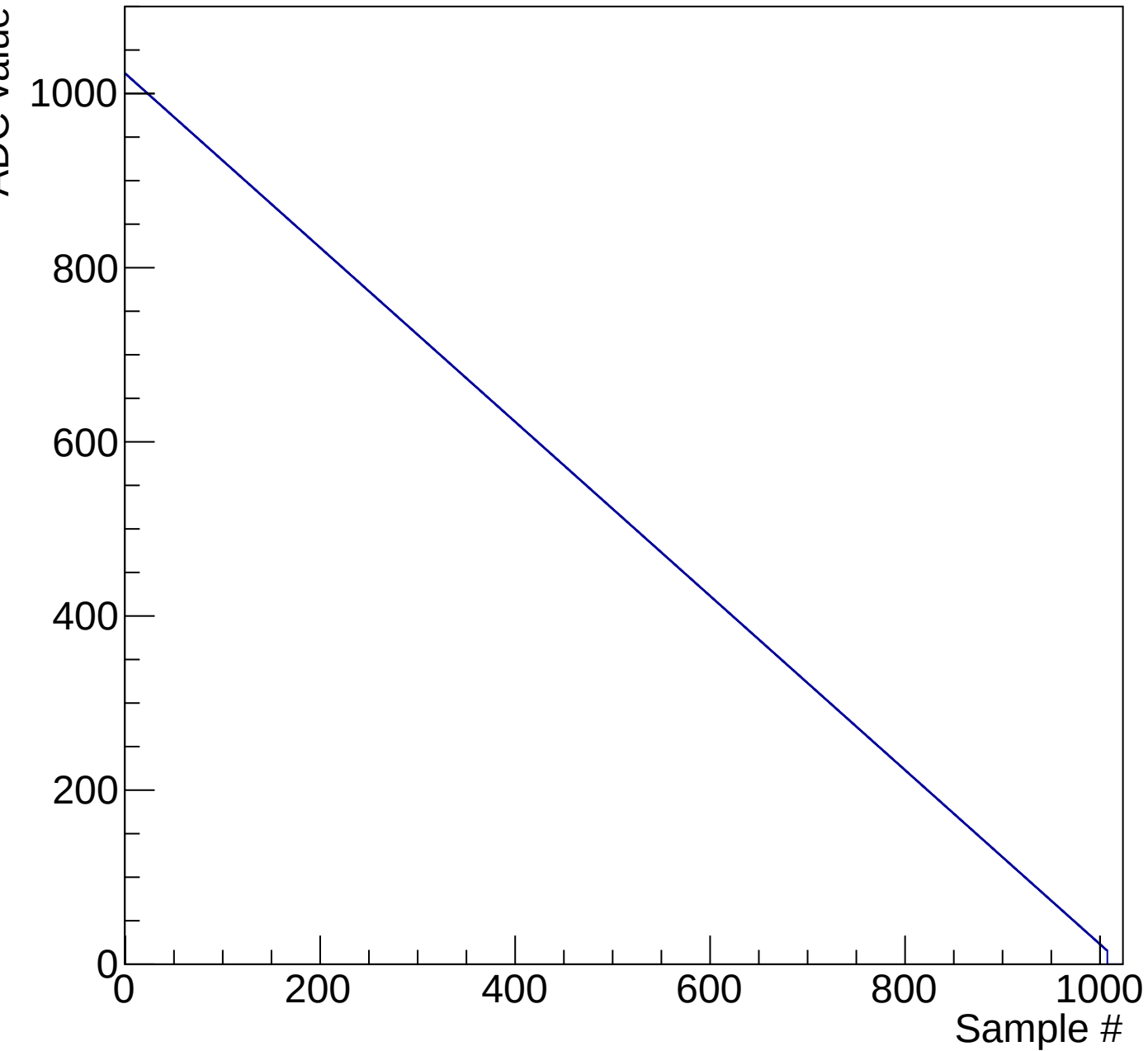
Channel 3 pattern 2



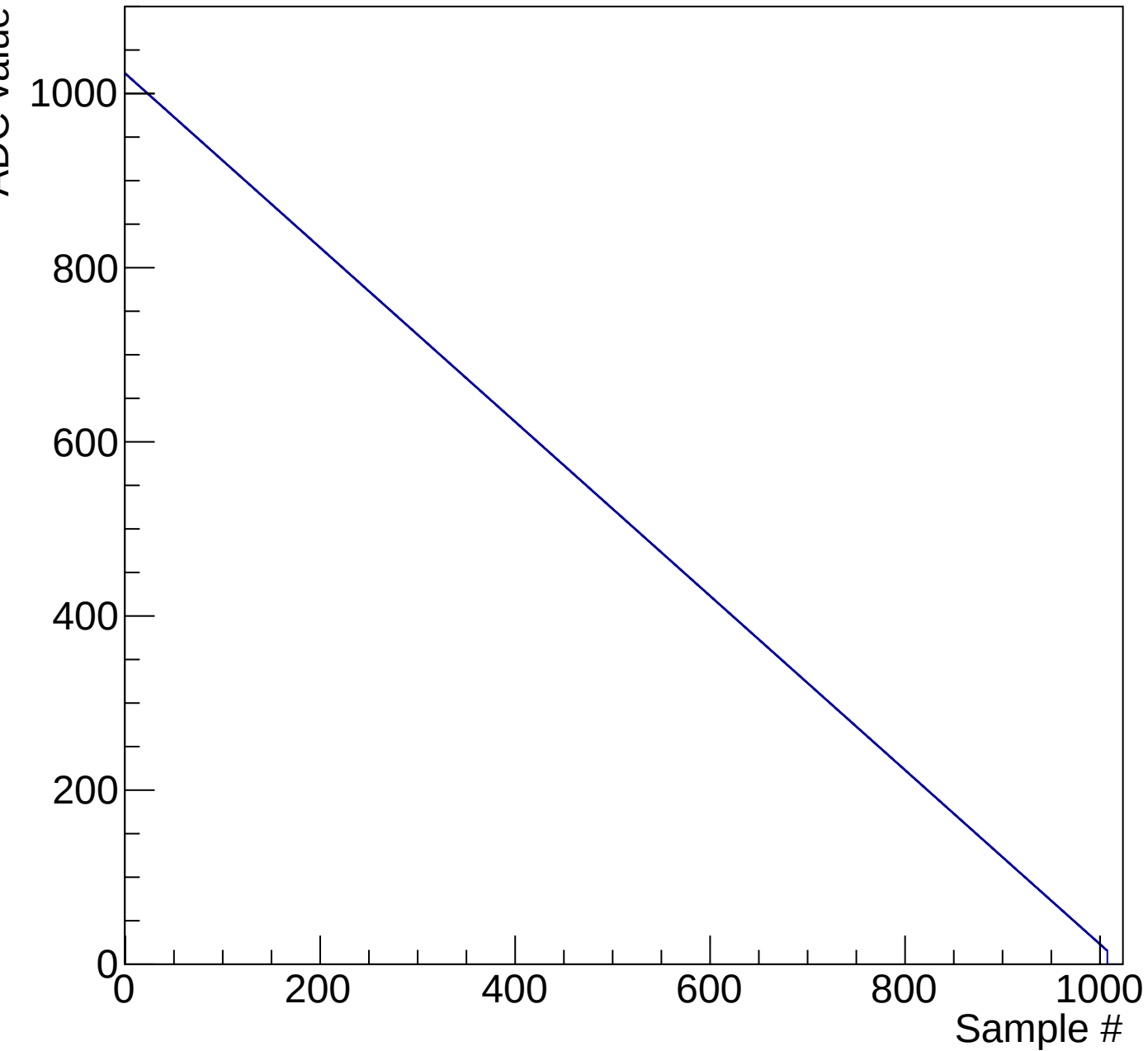
Channel 4 pattern 2



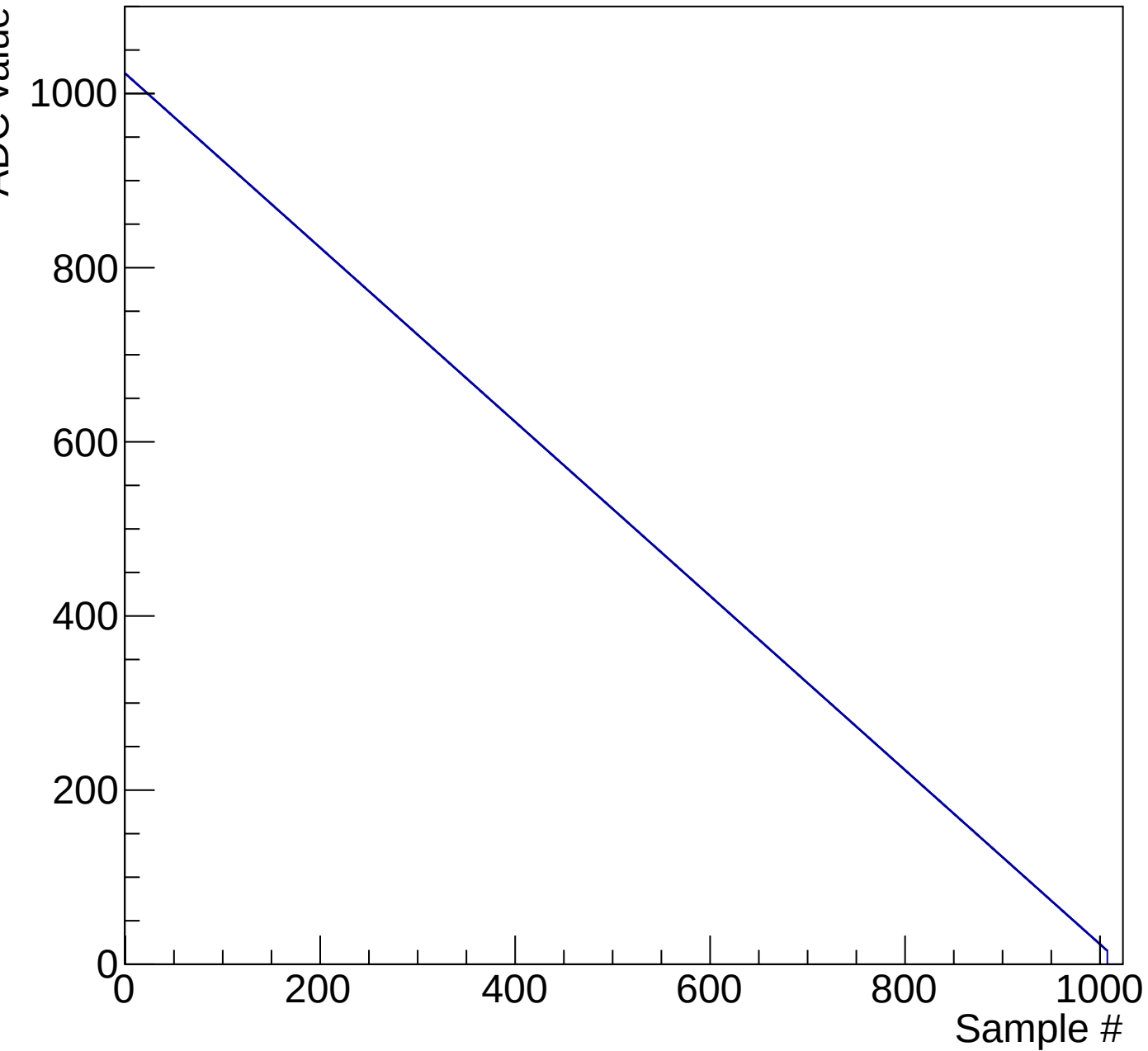
Channel 5 pattern 2



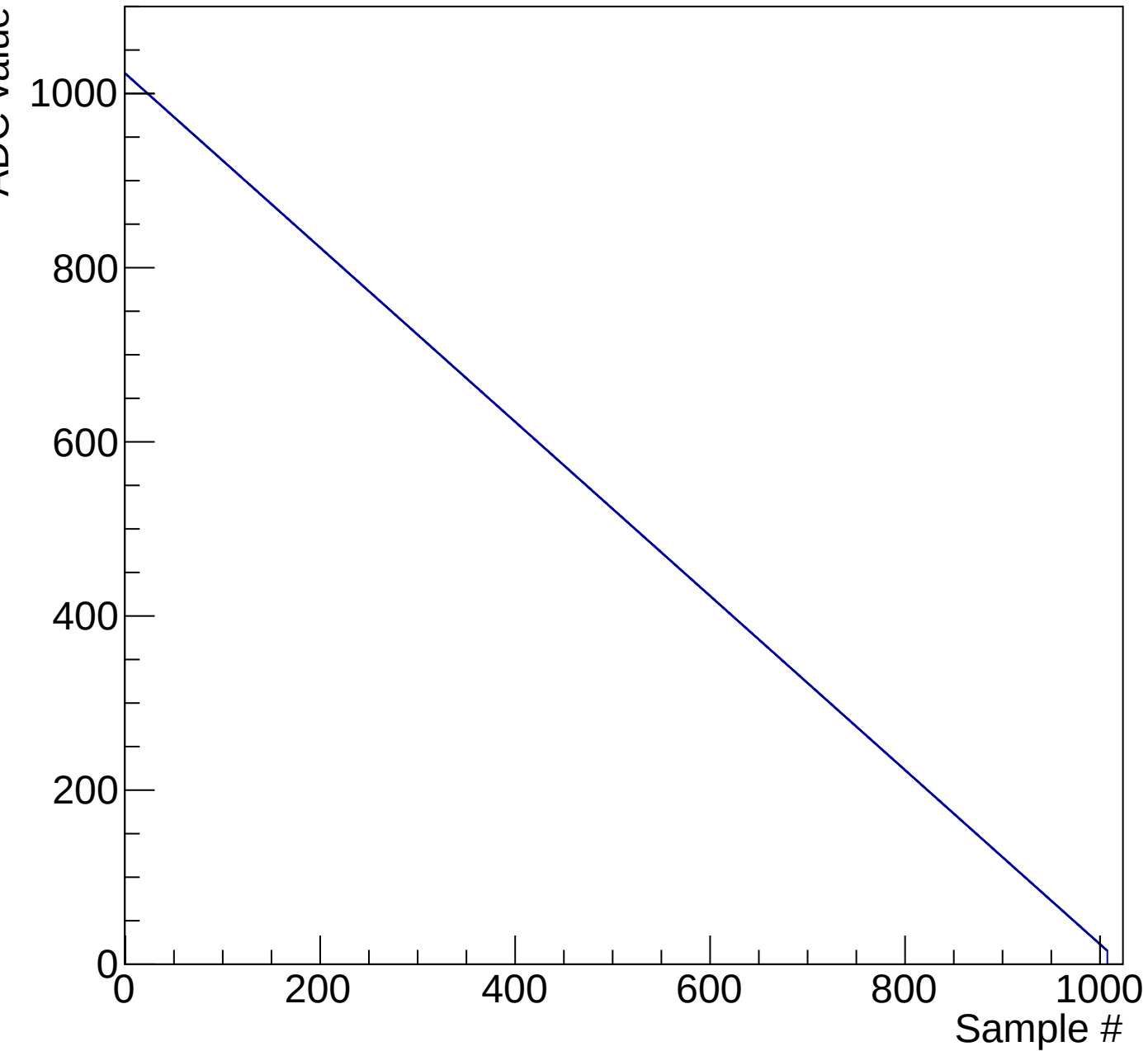
Channel 6 pattern 2



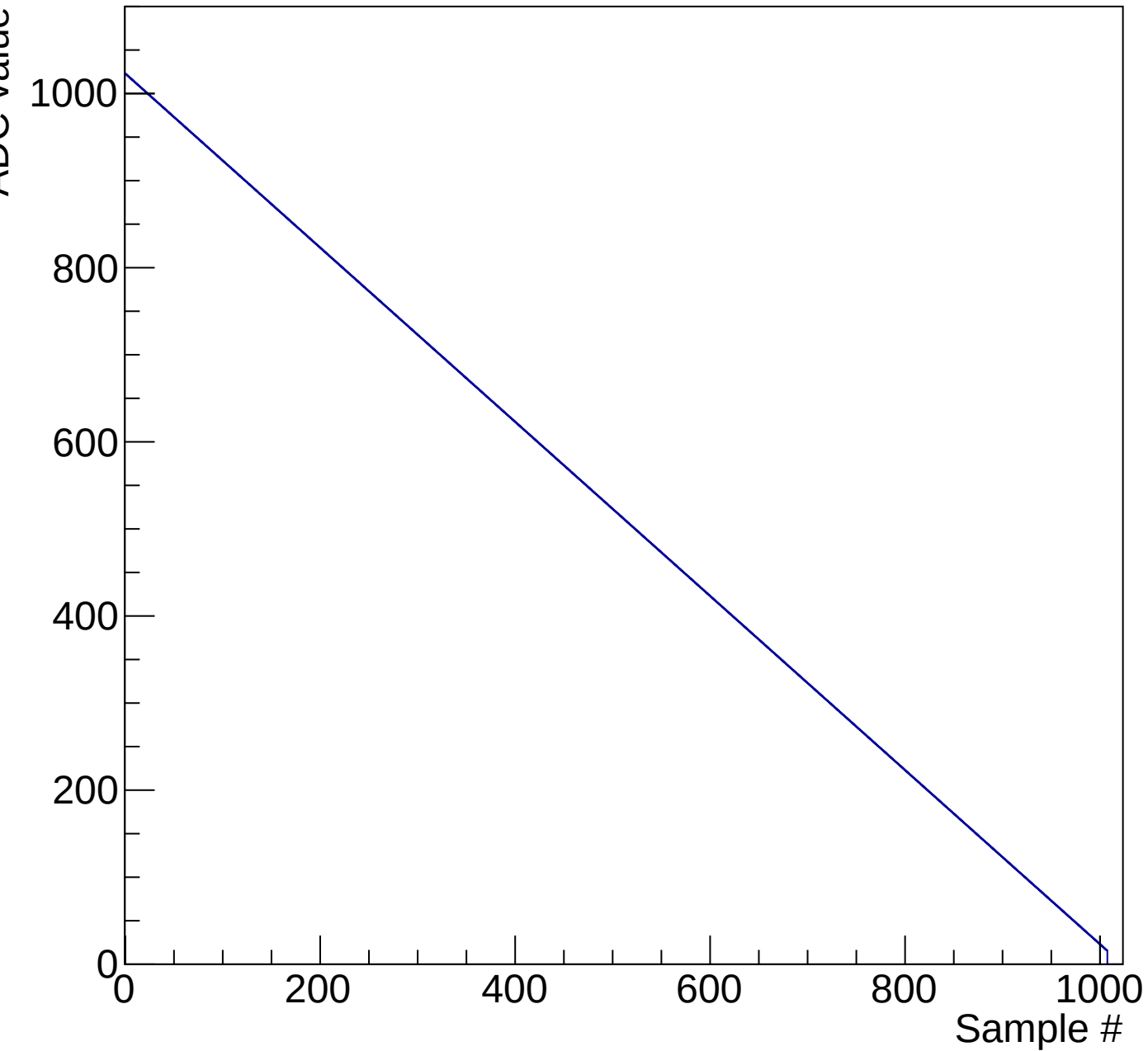
Channel 7 pattern 2



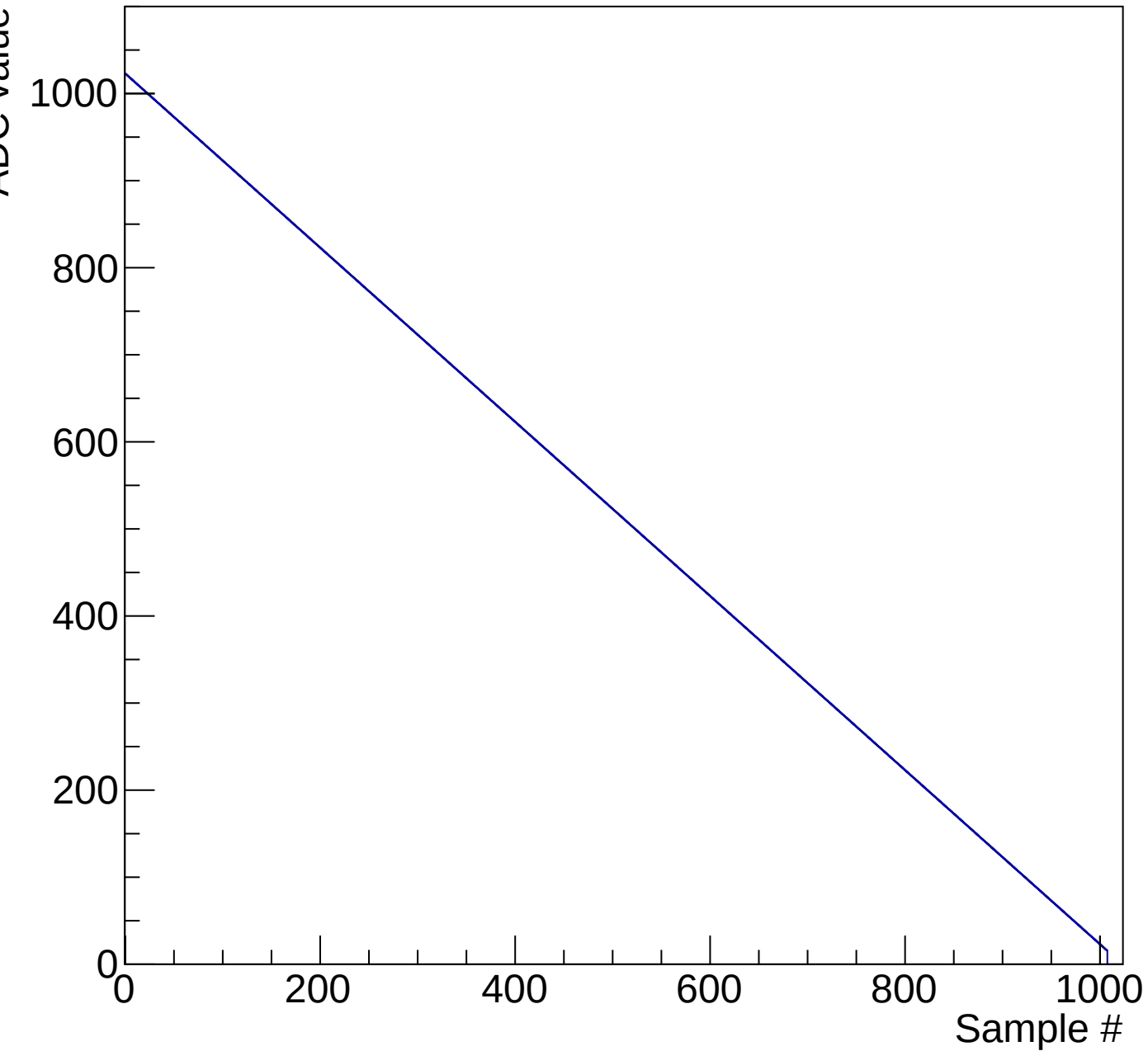
Channel 8 pattern 2



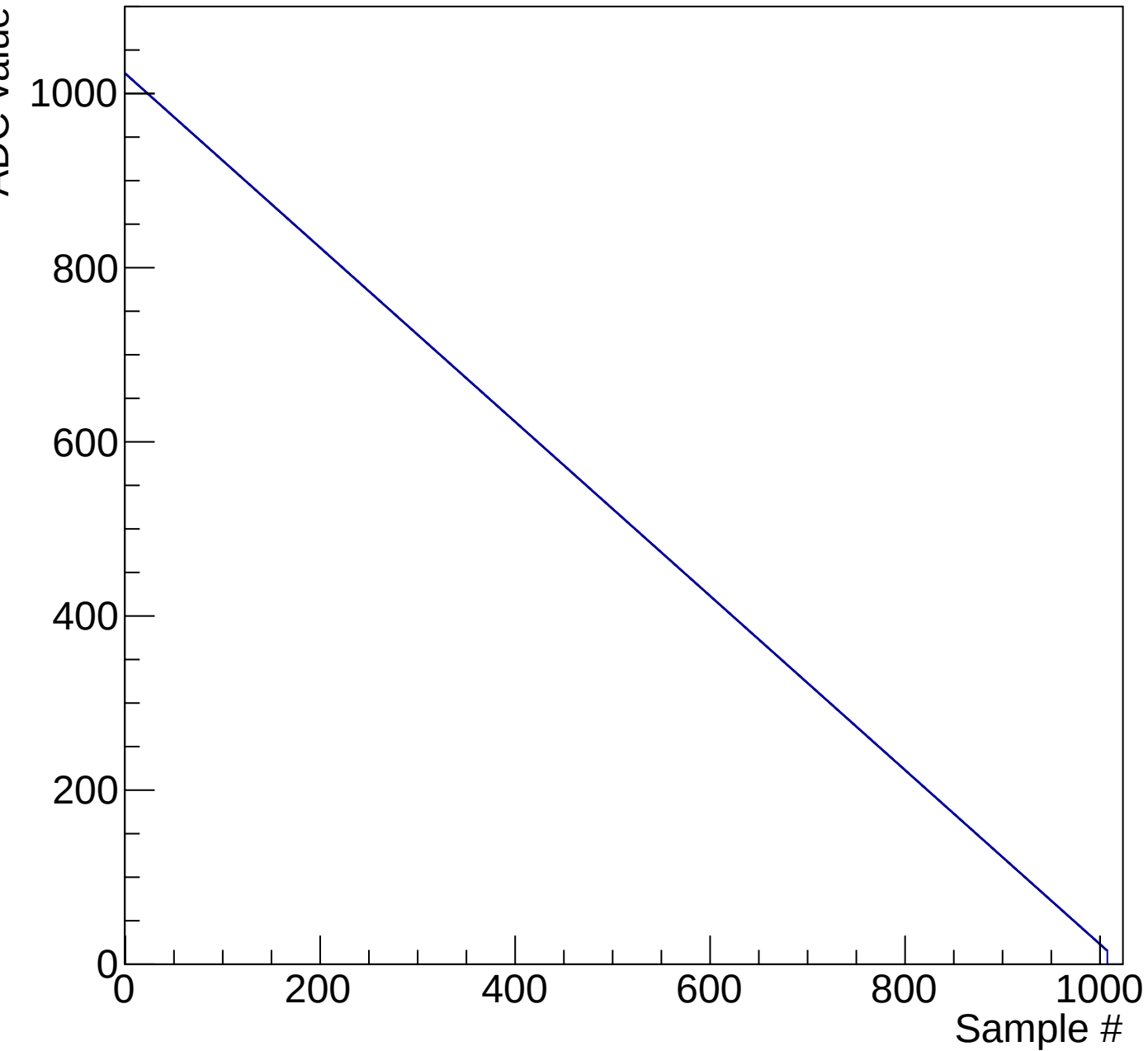
Channel 9 pattern 2



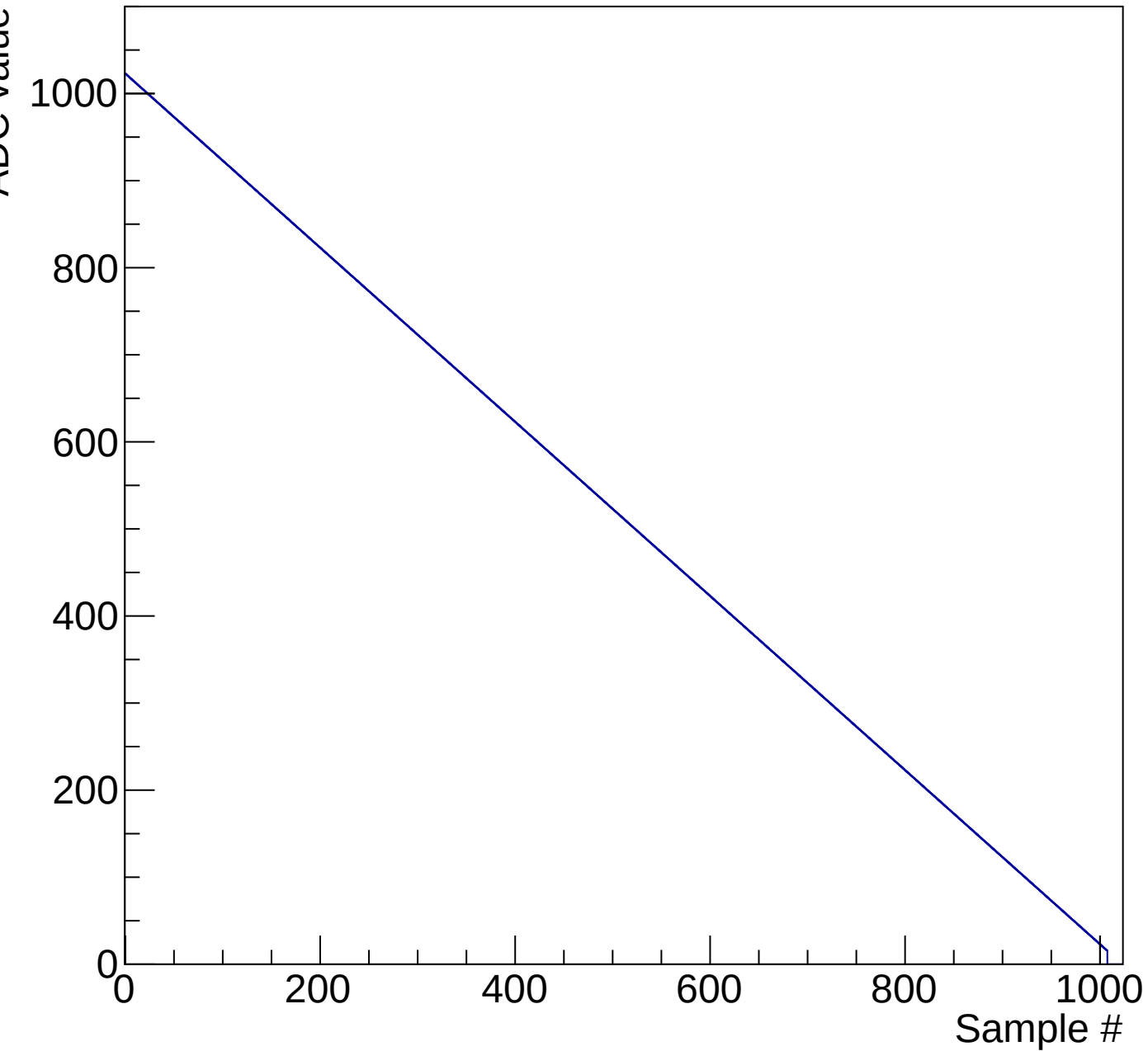
Channel 10 pattern 2



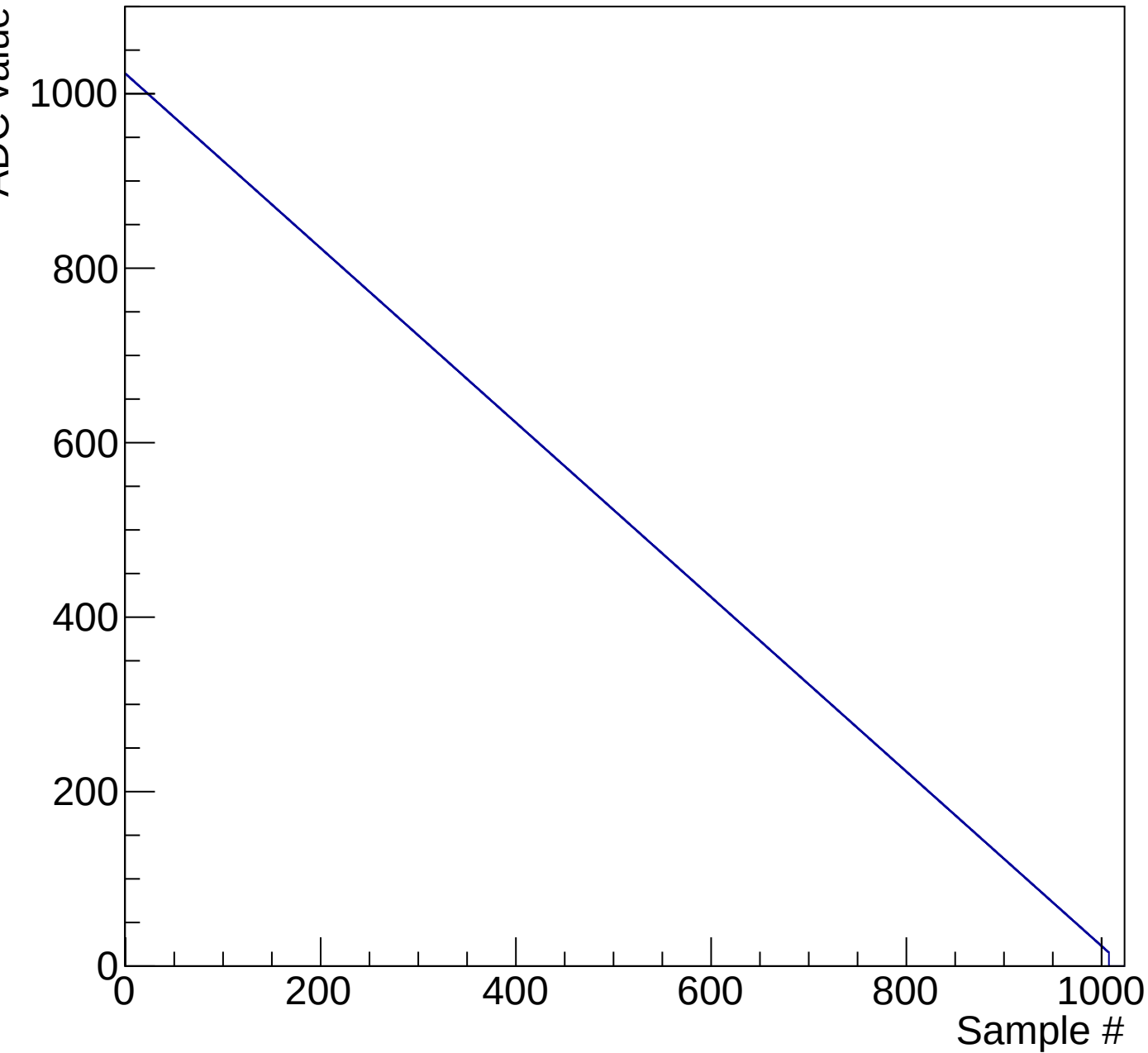
Channel 11 pattern 2



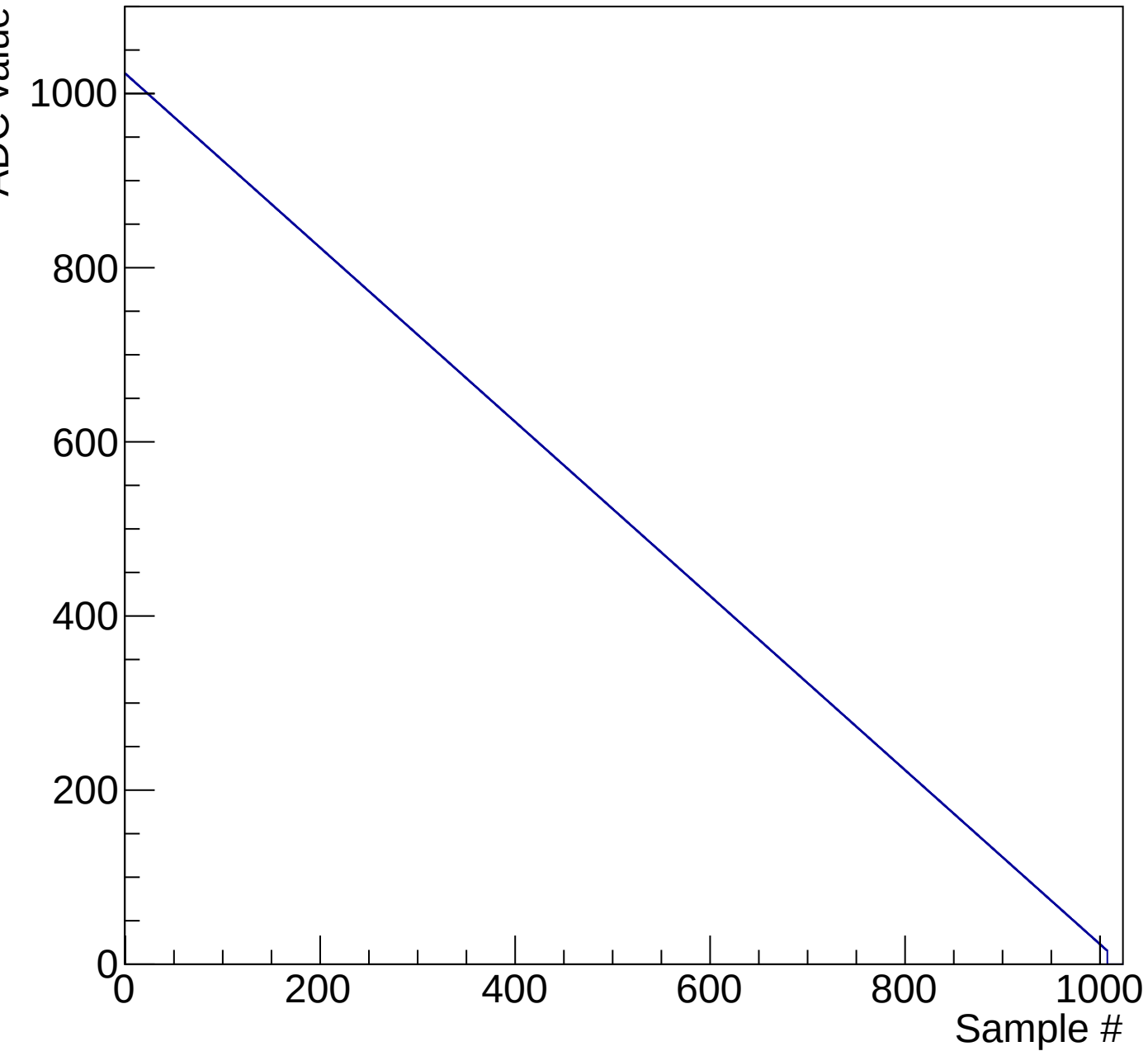
Channel 12 pattern 2



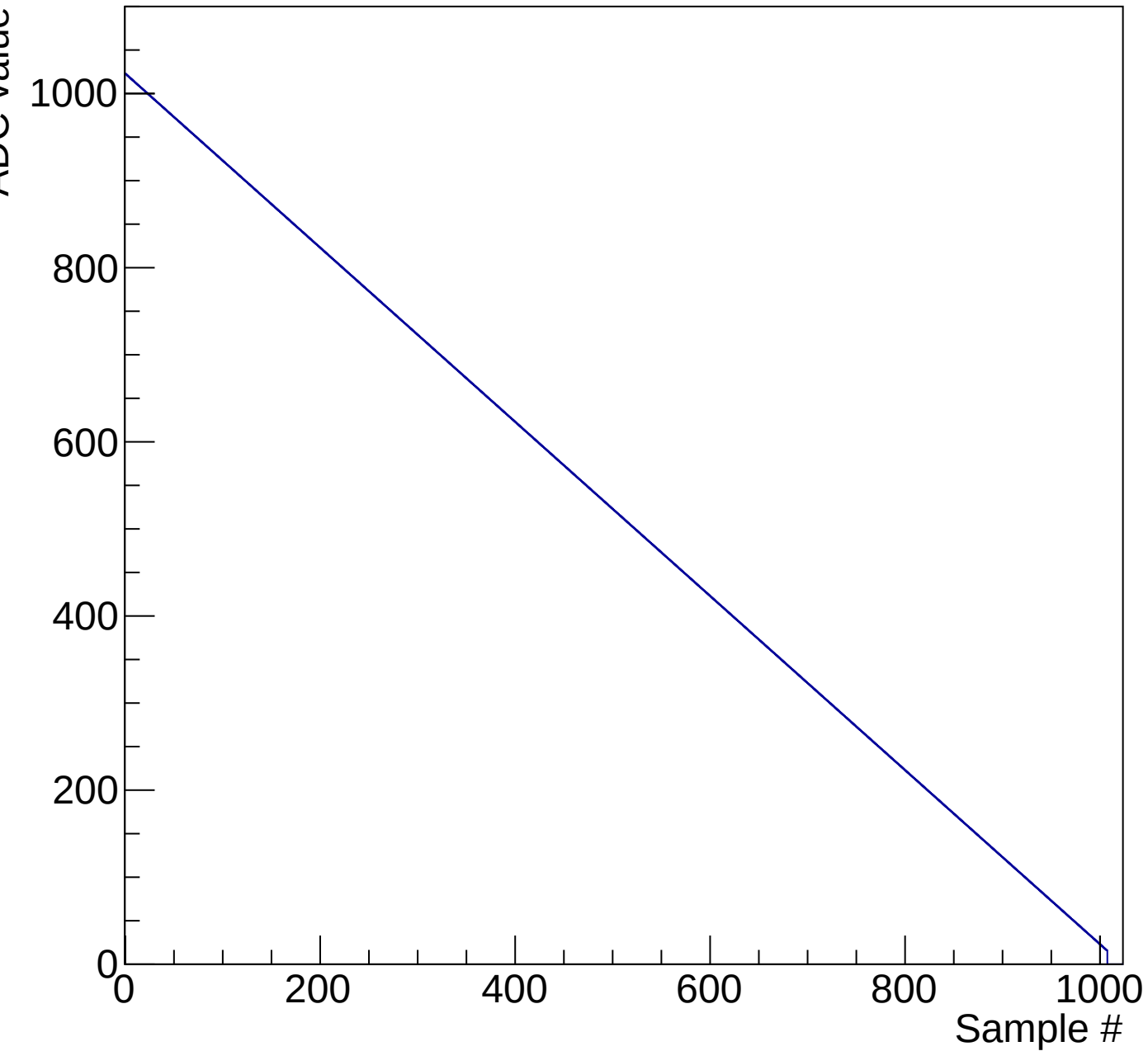
Channel 13 pattern 2



Channel 14 pattern 2



Channel 15 pattern 2



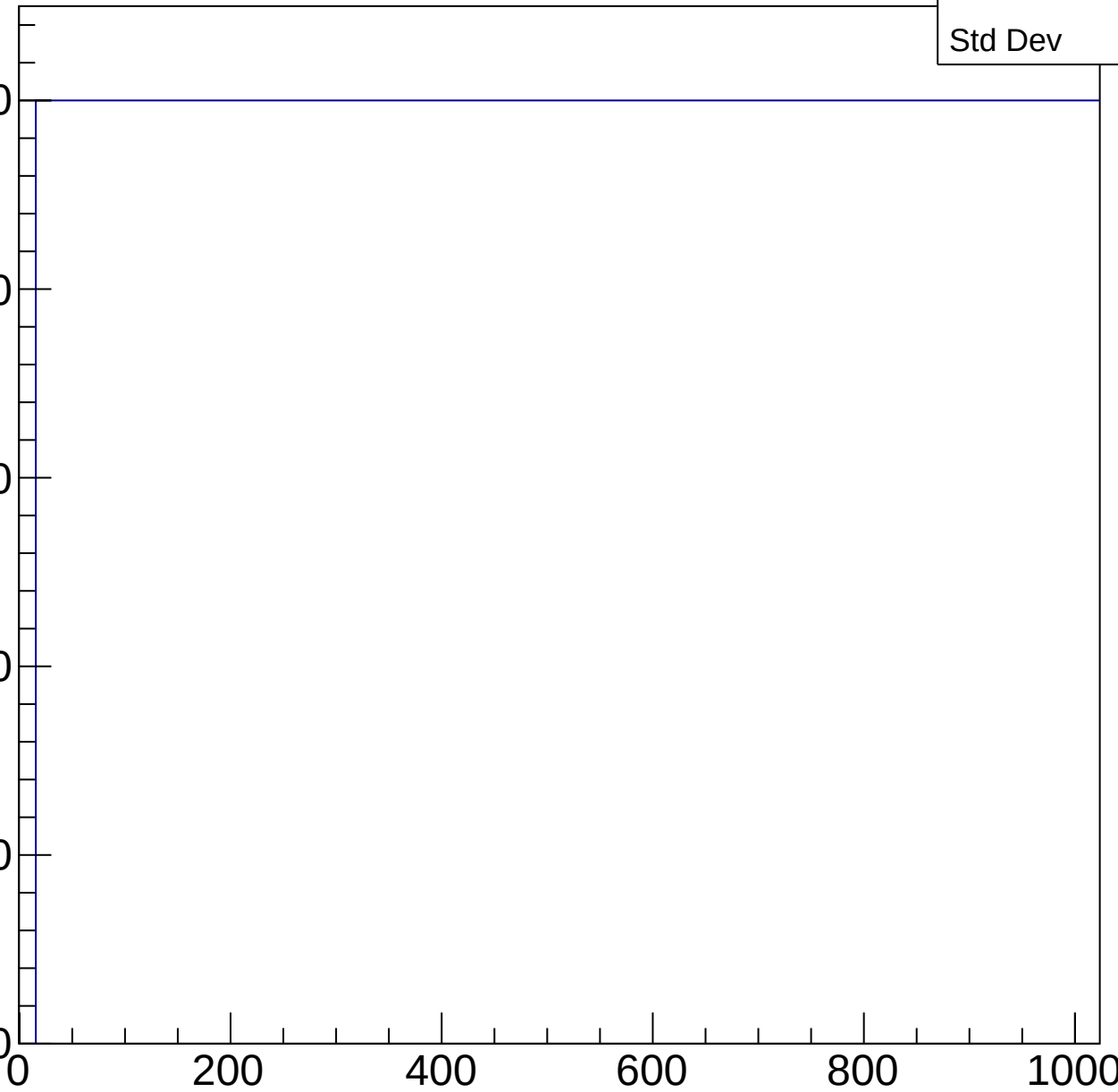
Ramp saltro:0 chip:0:7 channel 0 pattern2

Entries

500
400
300
200
100
0

Mean	519.5
Std Dev	291

ADC value



Ramp saltro:0 chip:0:7 channel 1 pattern2

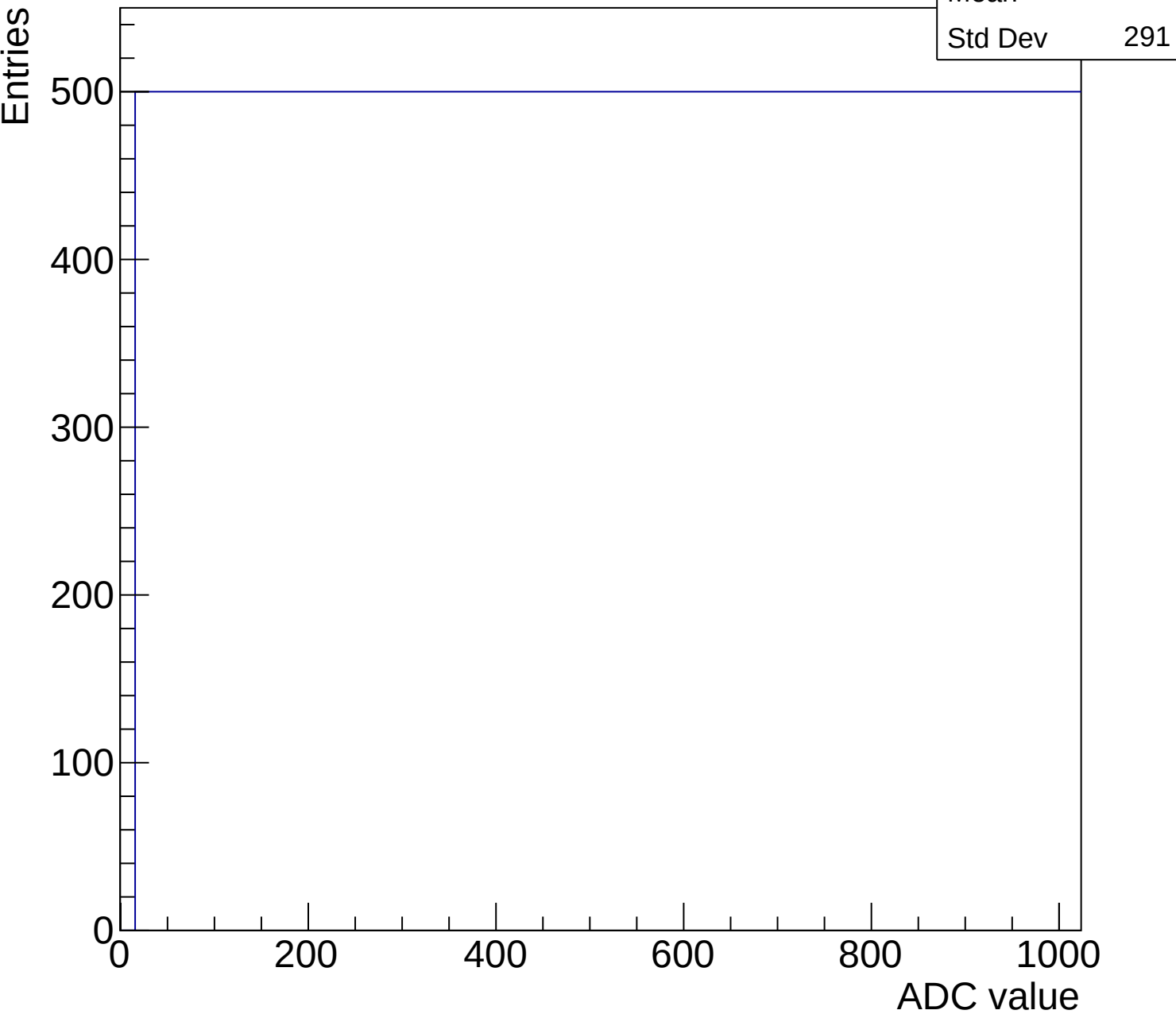
Entries

500
400
300
200
100
0

Mean	519.5
Std Dev	291

ADC value

0 200 400 600 800 1000



Ramp saltro:0 chip:0:7 channel 2 pattern2

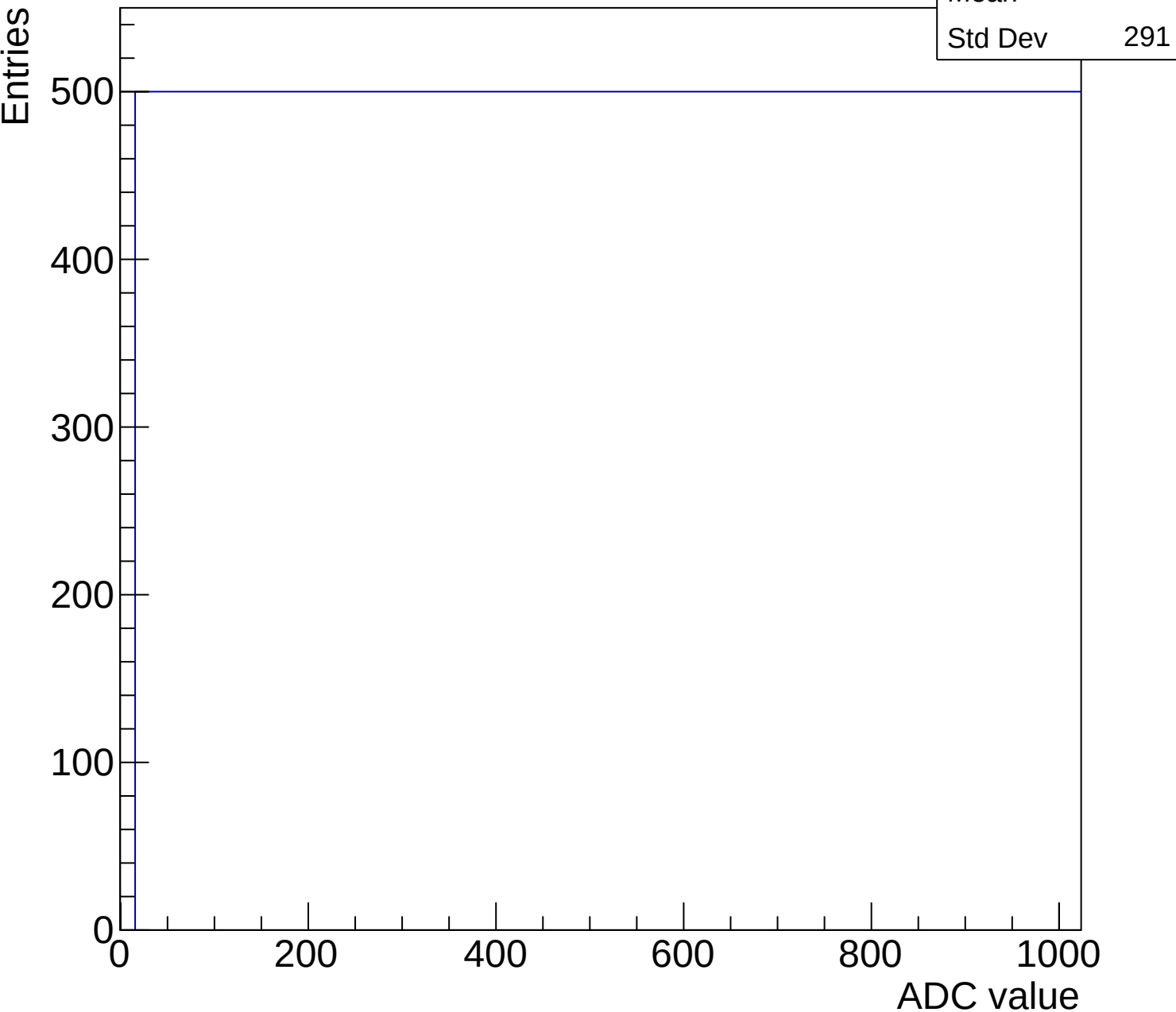
Entries

500
400
300
200
100
0

Mean	519.5
Std Dev	291

0 200 400 600 800 1000

ADC value



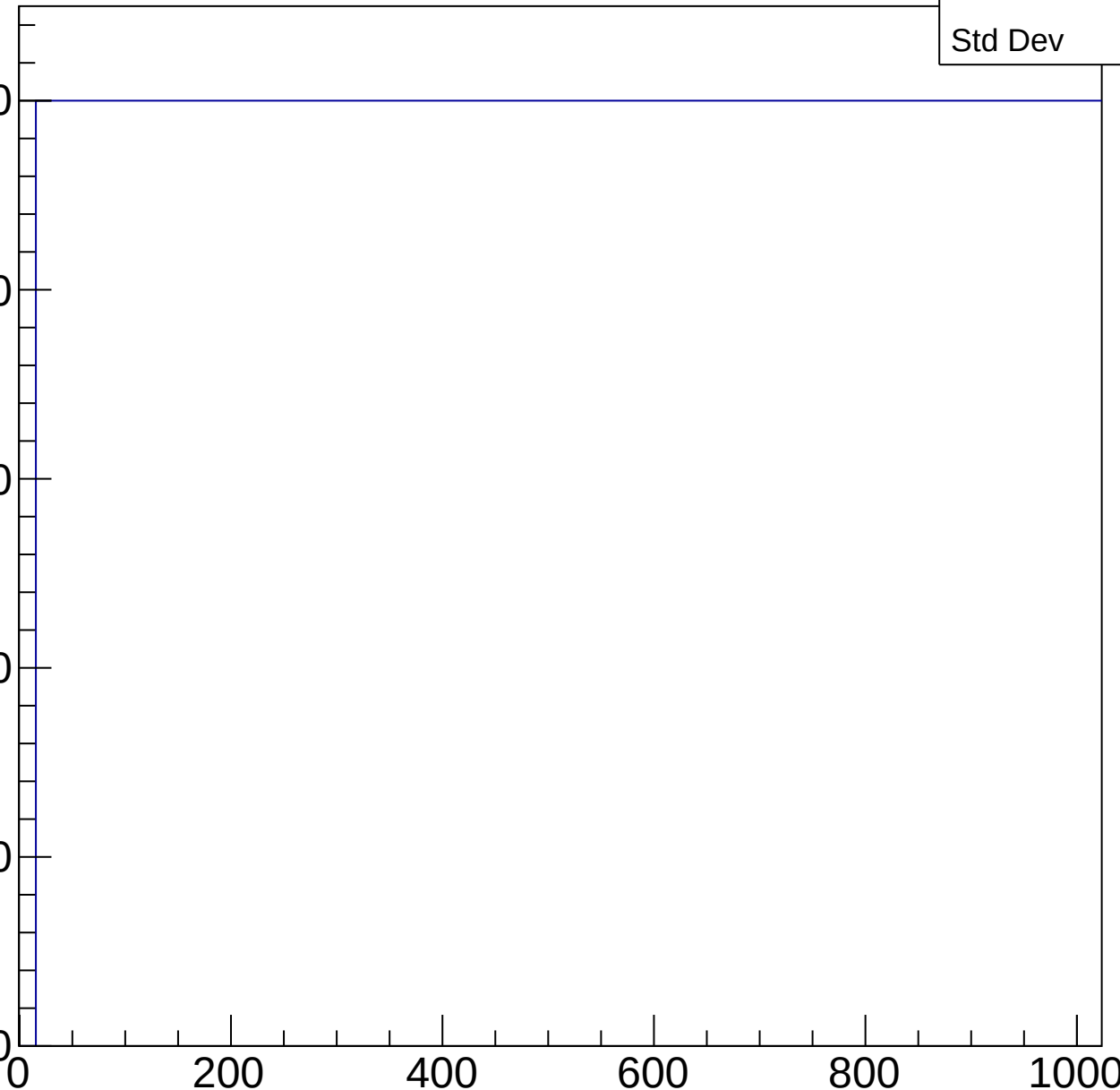
Ramp saltro:0 chip:0:7 channel 3 pattern2

Entries

500
400
300
200
100
0

Mean	519.5
Std Dev	291

ADC value



Ramp salto:0 chip:0:7 channel 4 pattern2

Entries

500

400

300

200

100

0

0

200

400

600

800

1000

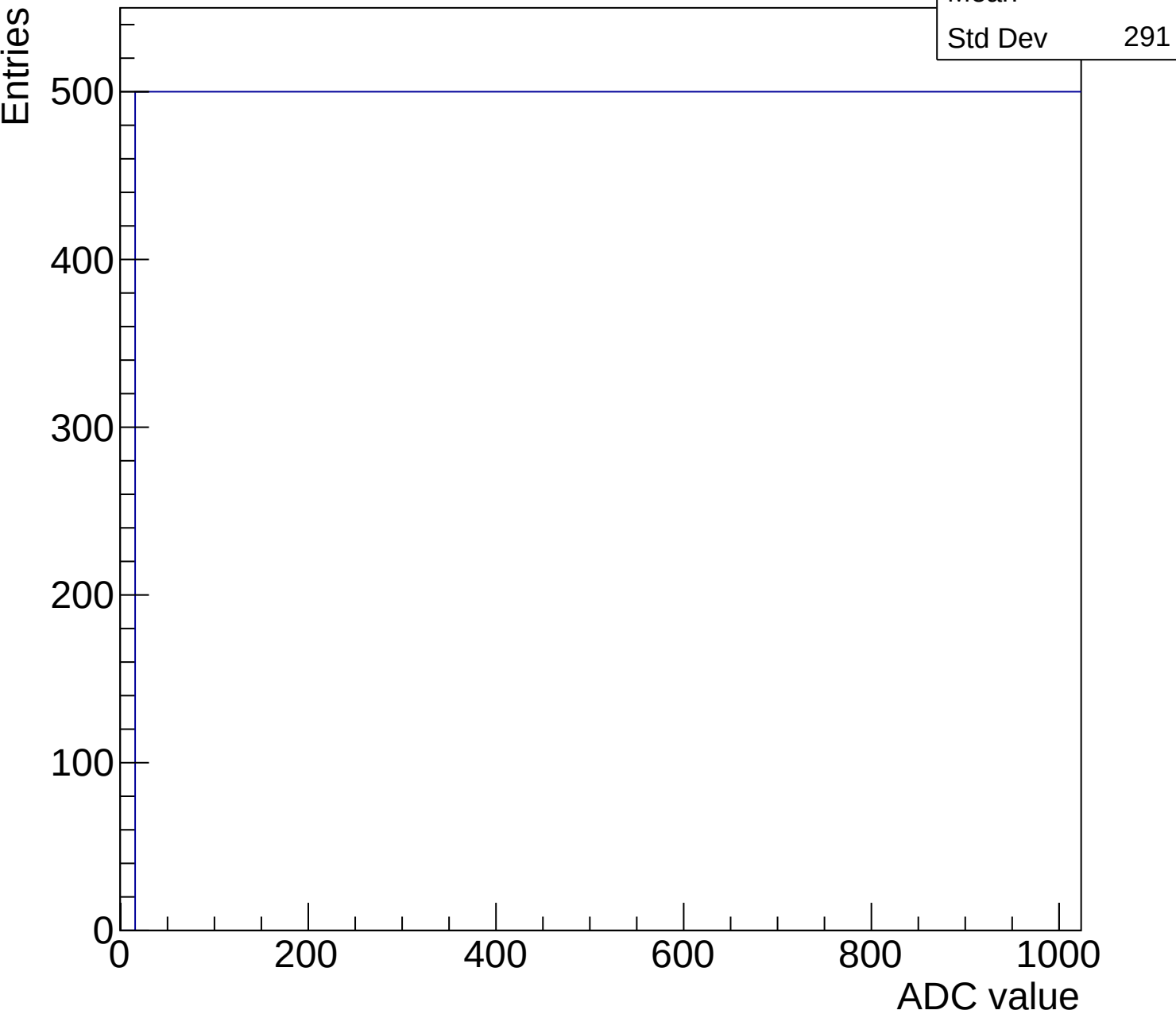
ADC value

Mean

519.5

Std Dev

291



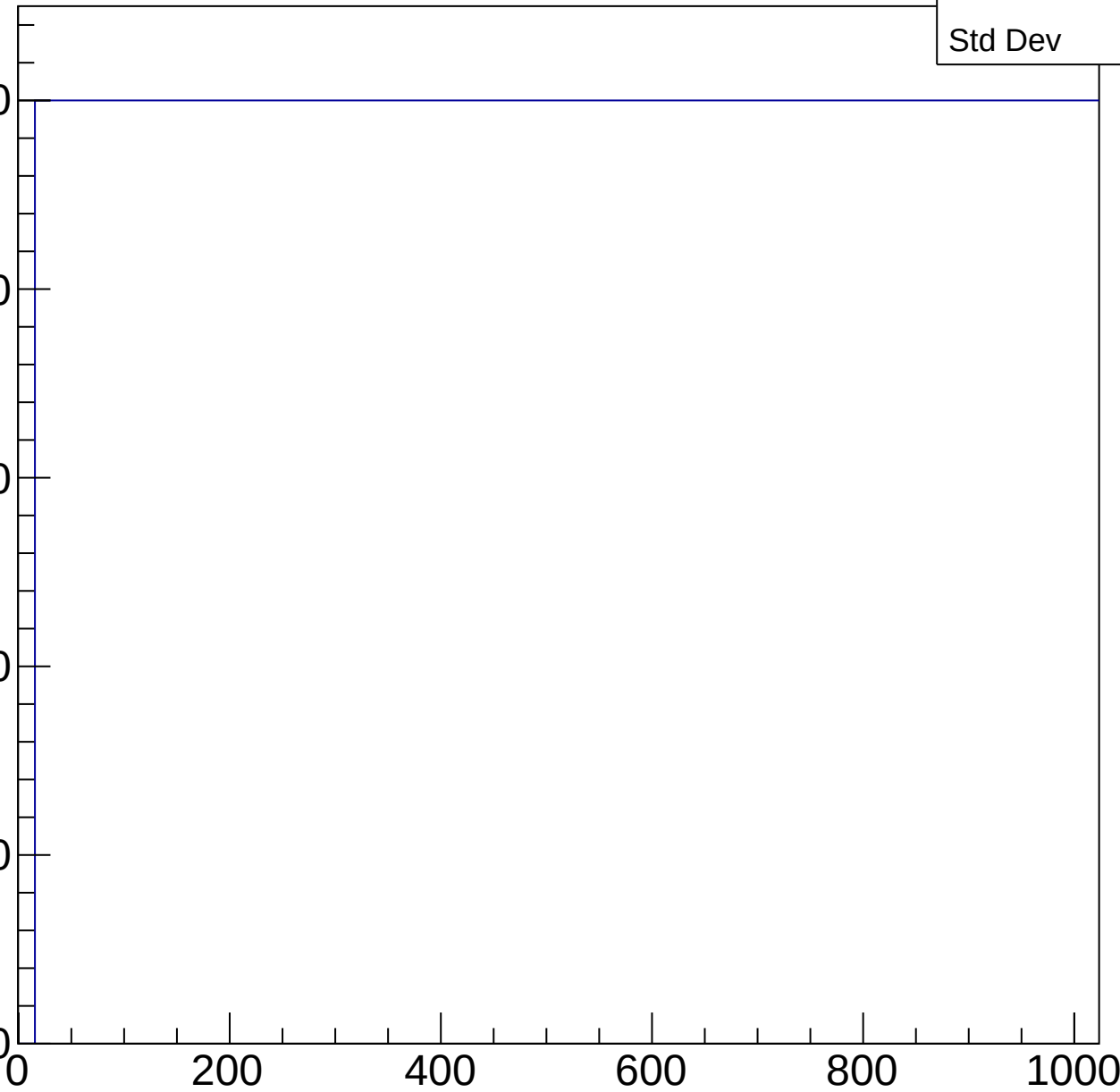
Ramp saltro:0 chip:0:7 channel 5 pattern2

Entries

500
400
300
200
100
0

Mean	519.5
Std Dev	291

ADC value



Ramp saltro:0 chip:0:7 channel 6 pattern2

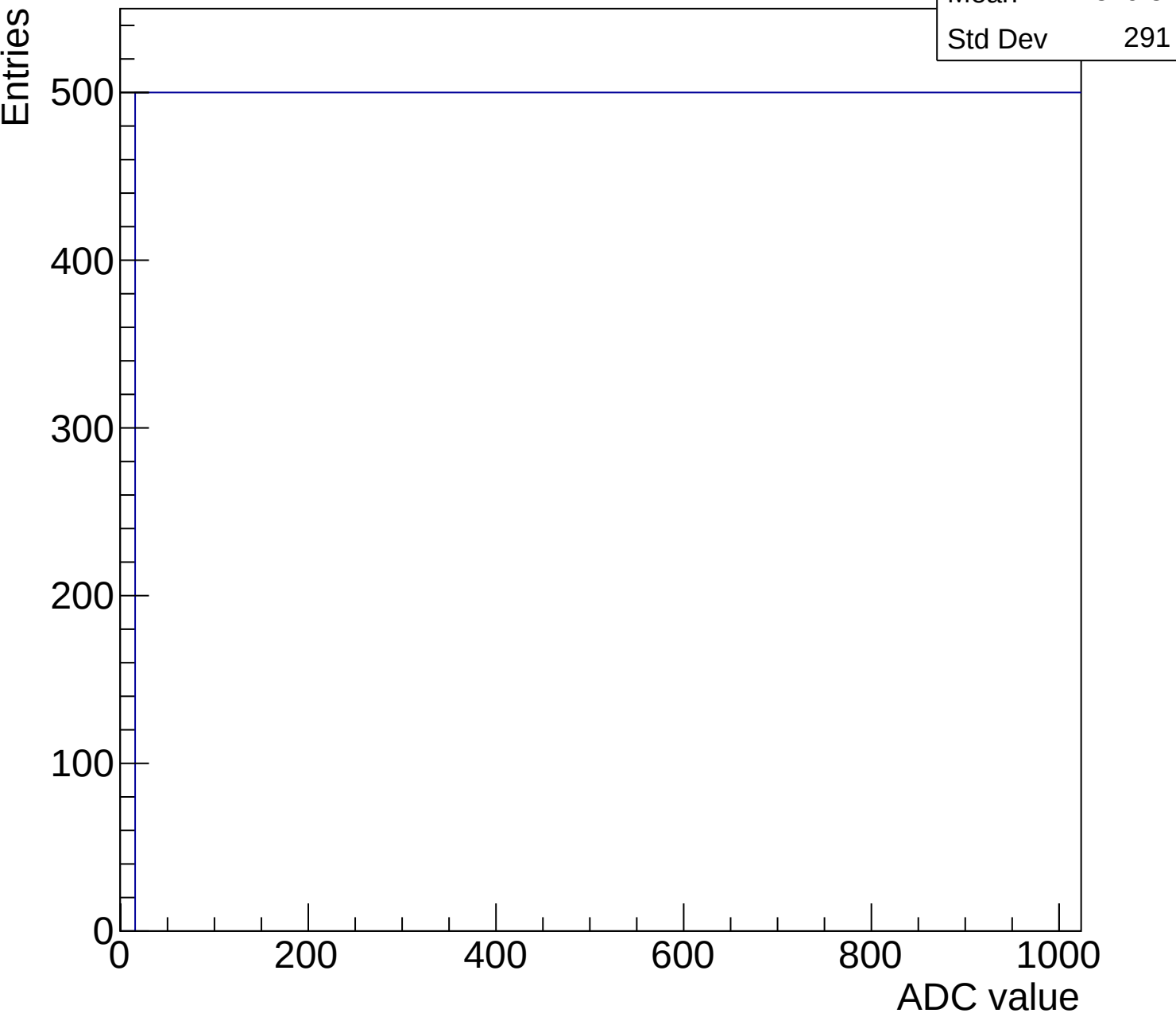
Entries

500
400
300
200
100
0

Mean	519.5
Std Dev	291

0 200 400 600 800 1000

ADC value



Ramp saltro:0 chip:0:7 channel 7 pattern2

Entries

500

400

300

200

100

0

0

200

400

600

800

1000

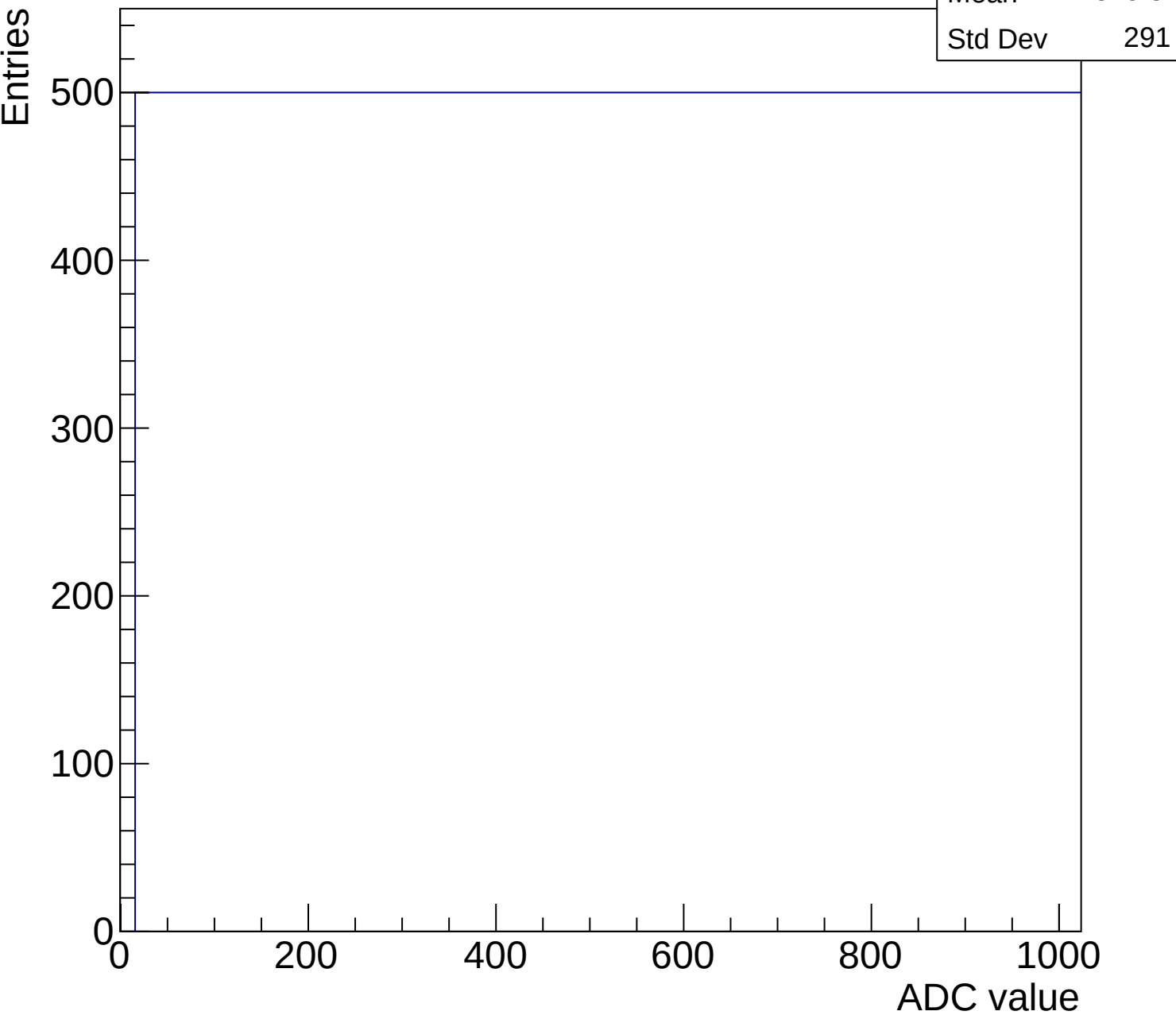
ADC value

Mean

519.5

Std Dev

291



Ramp saltro:0 chip:0:7 channel 8 pattern2

Entries

500

400

300

200

100

0

0

200

400

600

800

1000

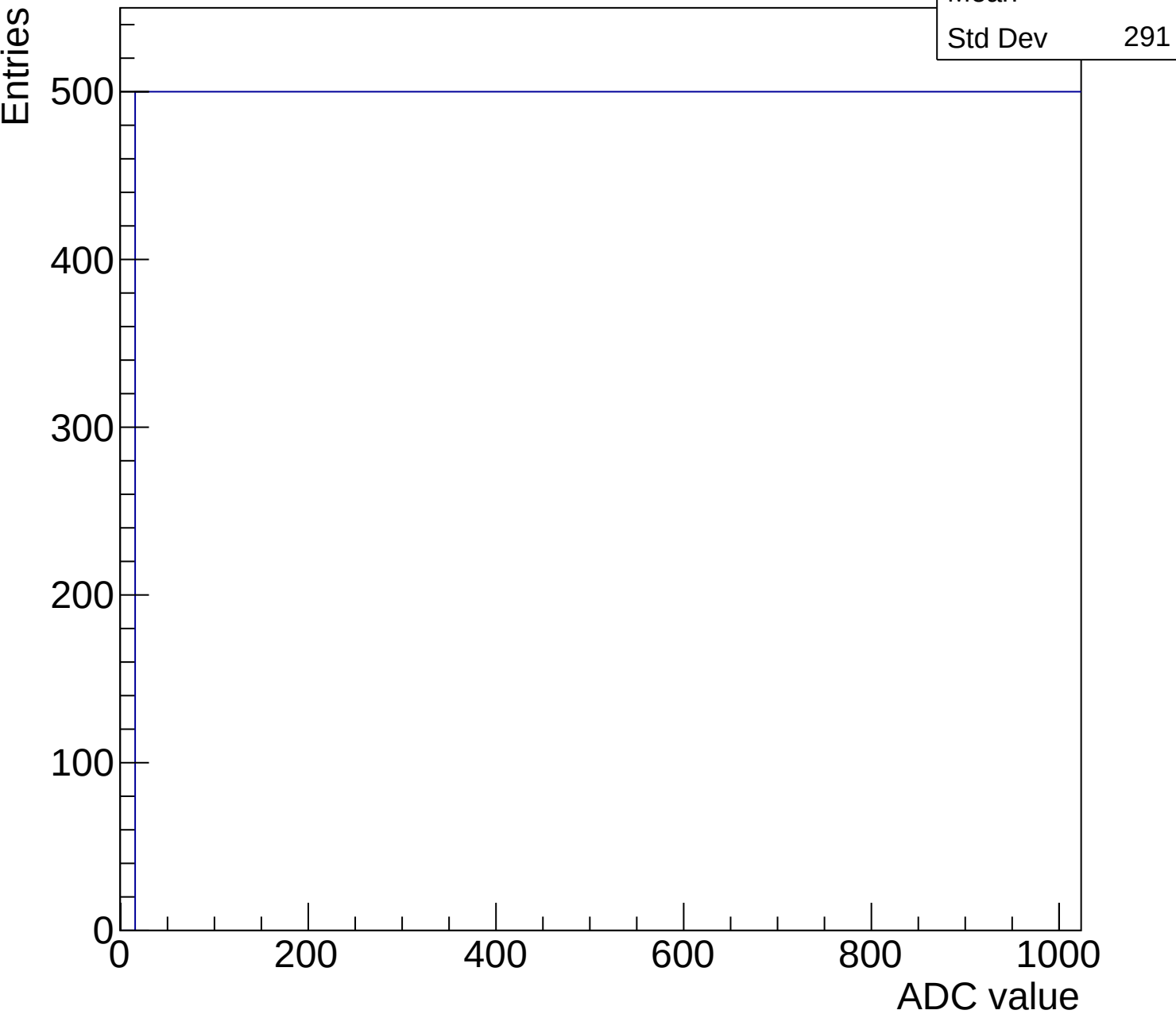
ADC value

Mean

519.5

Std Dev

291



Ramp saltro:0 chip:0:7 channel 9 pattern2

Entries

500

400

300

200

100

0

0

200

400

600

800

1000

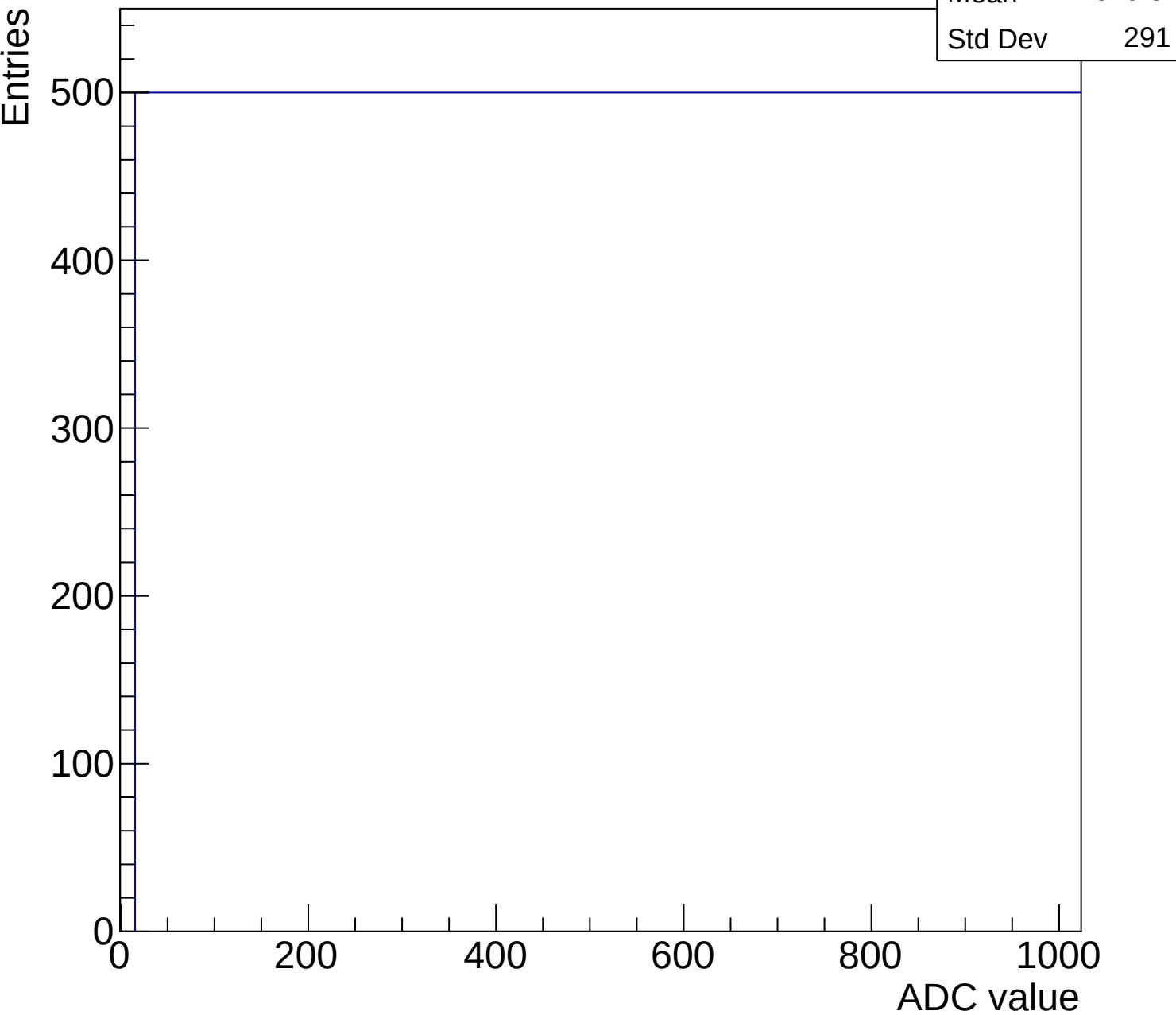
ADC value

Mean

519.5

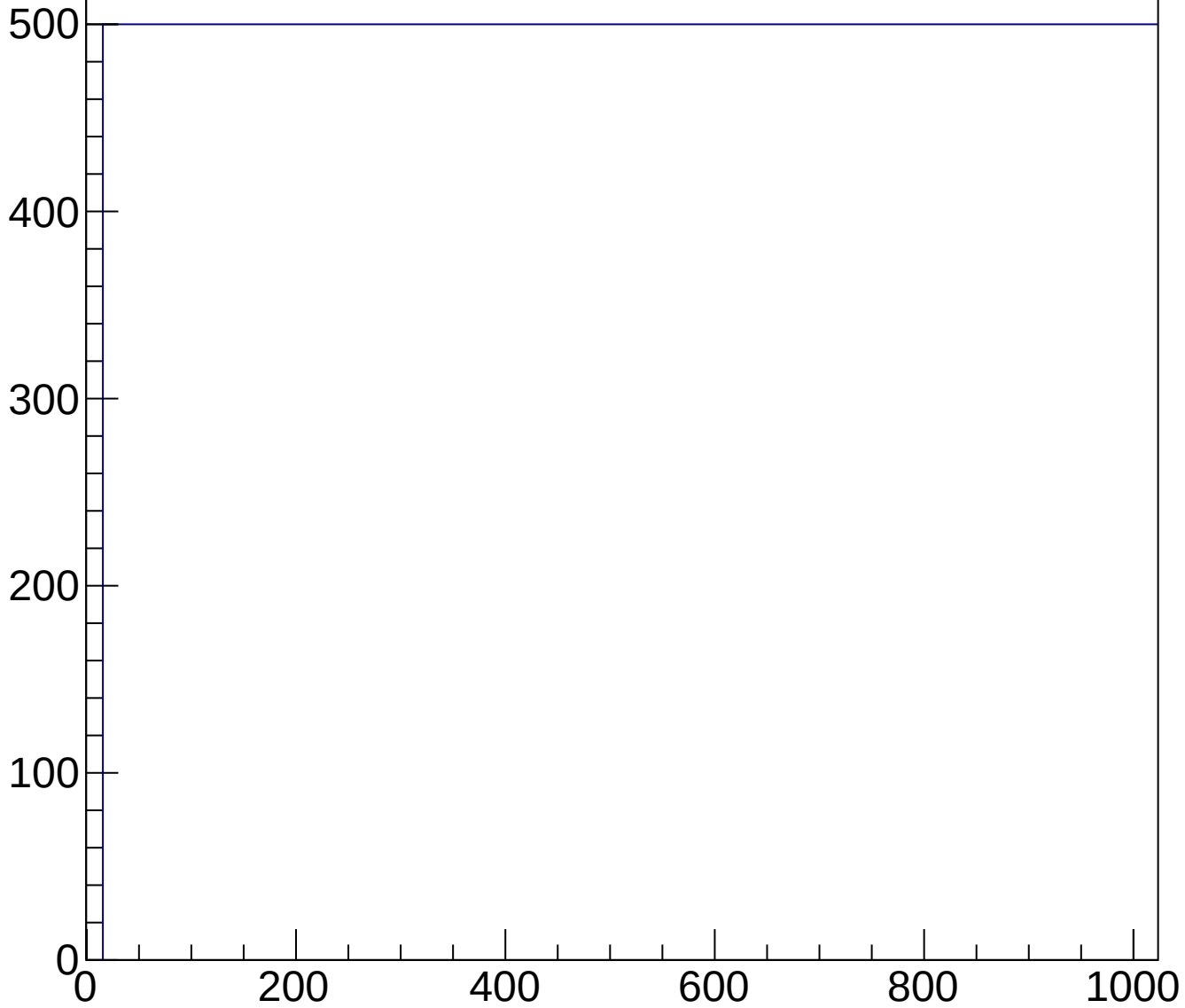
Std Dev

291



Ramp saltro:0 chip:0:7 channel 10 pattern2

Entries



Mean	519.5
Std Dev	291

ADC value

Ramp saltro:0 chip:0:7 channel 11 pattern2

Entries

500

400

300

200

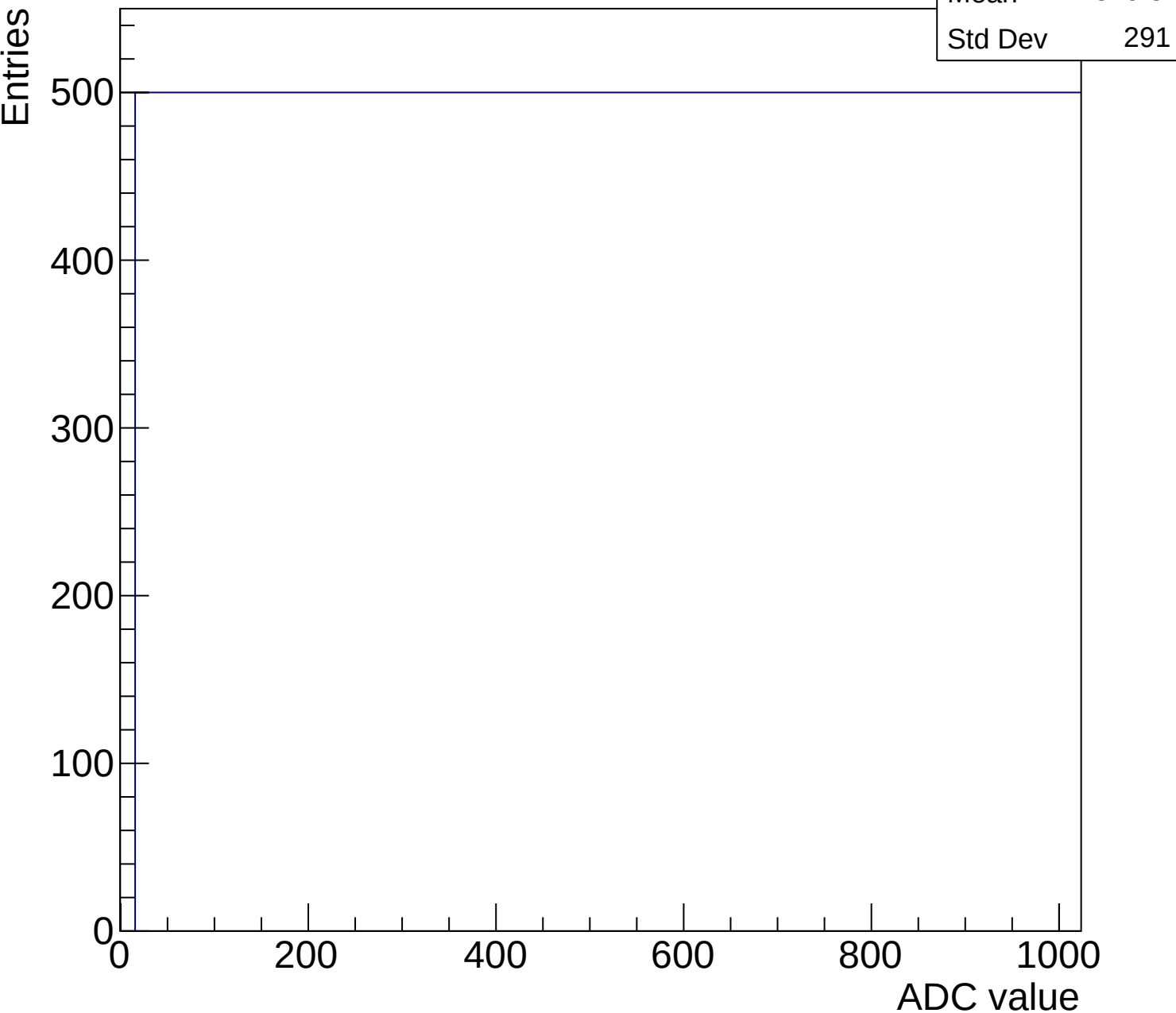
100

0

0 200 400 600 800 1000

ADC value

Mean	519.5
Std Dev	291



Ramp saltro:0 chip:0:7 channel 12 pattern2

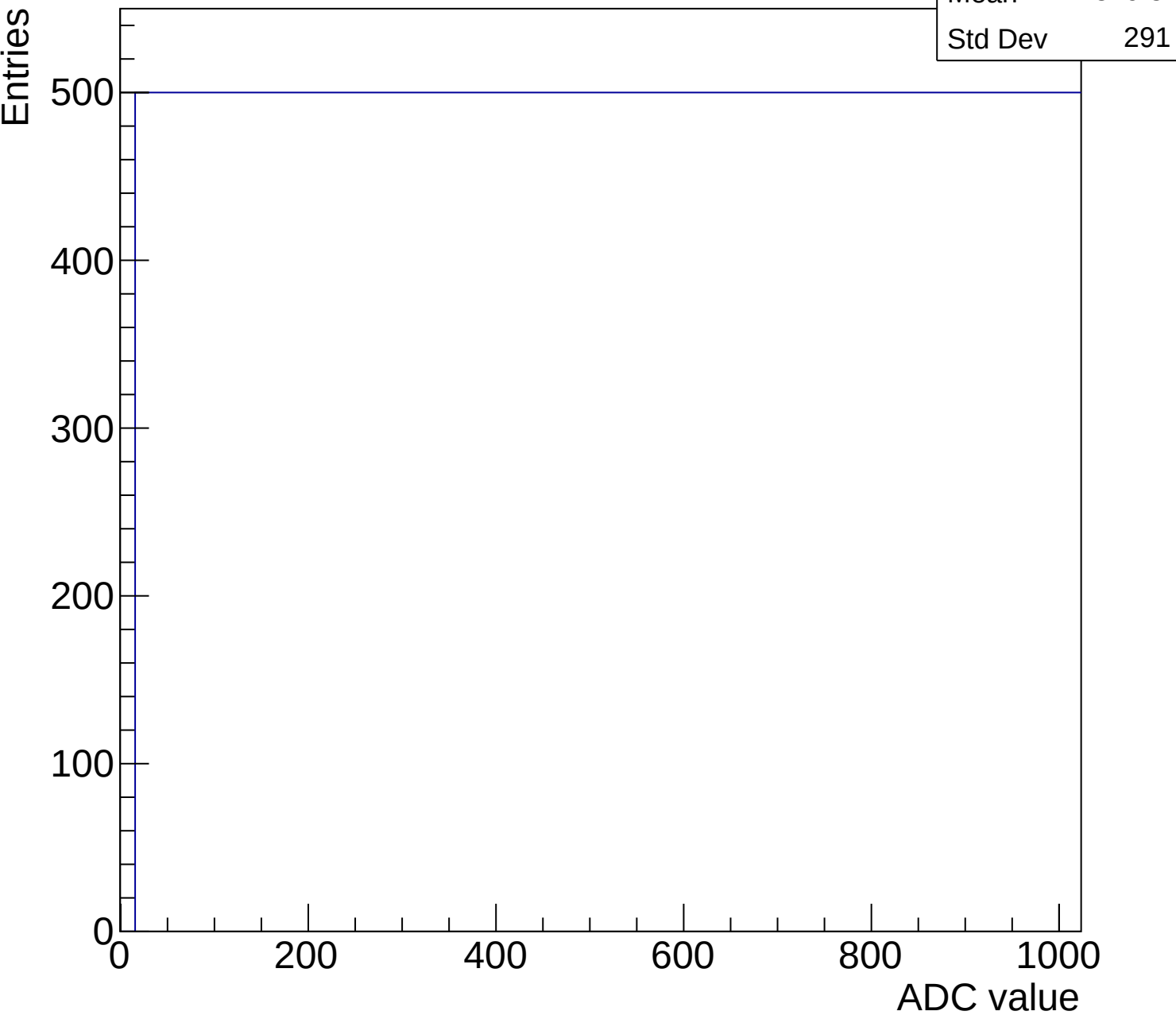
Entries

500
400
300
200
100
0

Mean	519.5
Std Dev	291

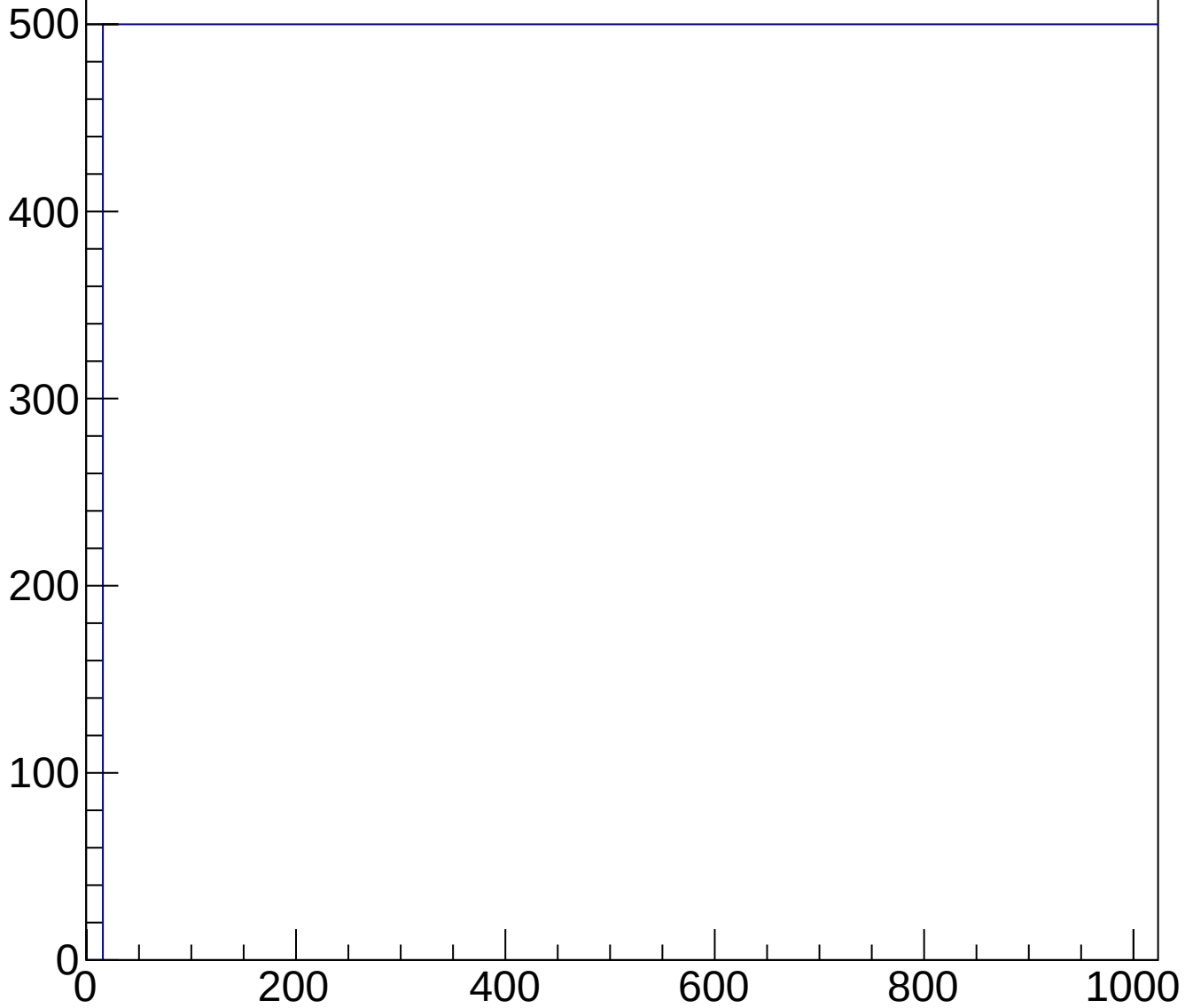
0 200 400 600 800 1000

ADC value



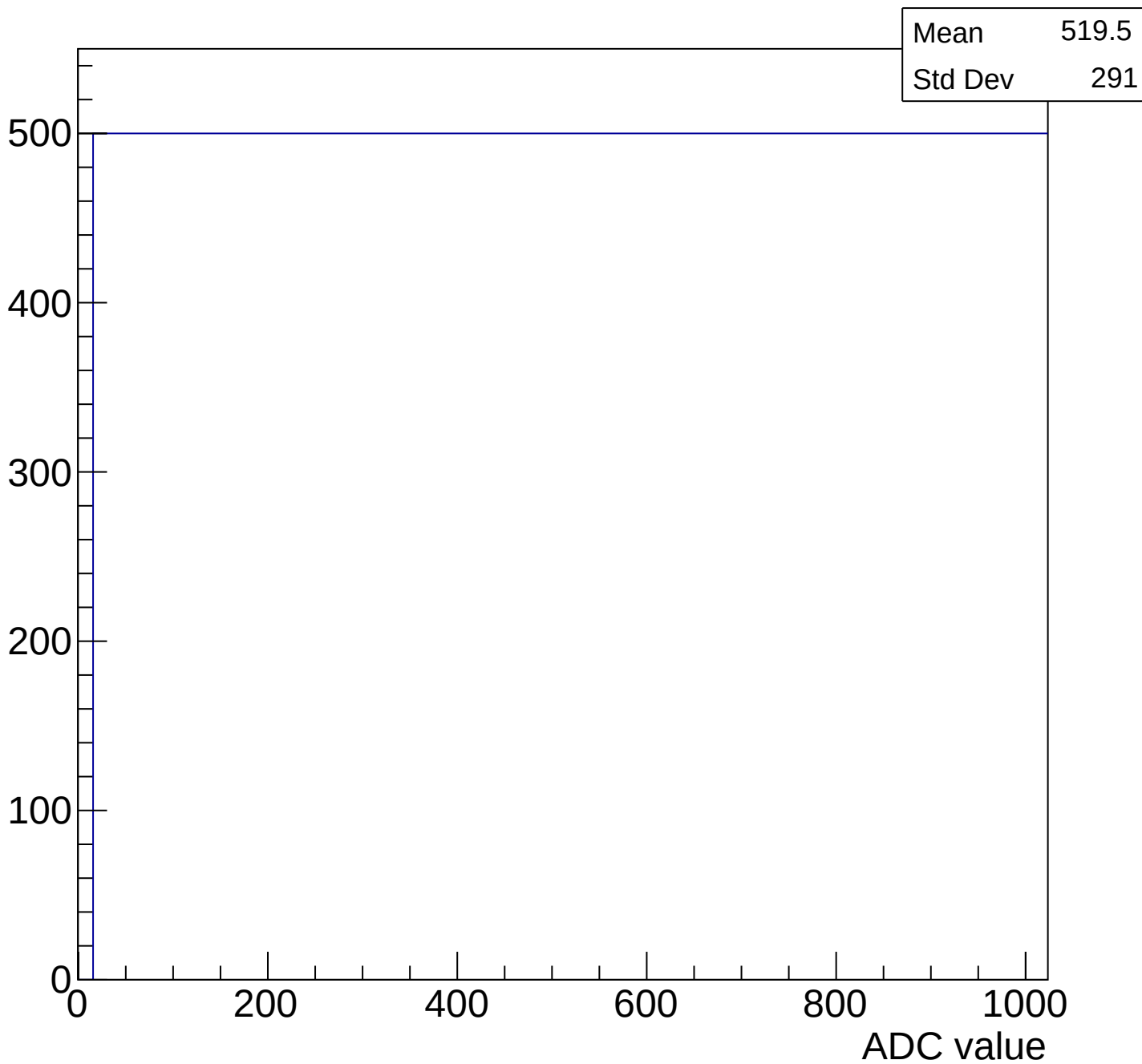
Ramp saltro:0 chip:0:7 channel 13 pattern2

Entries



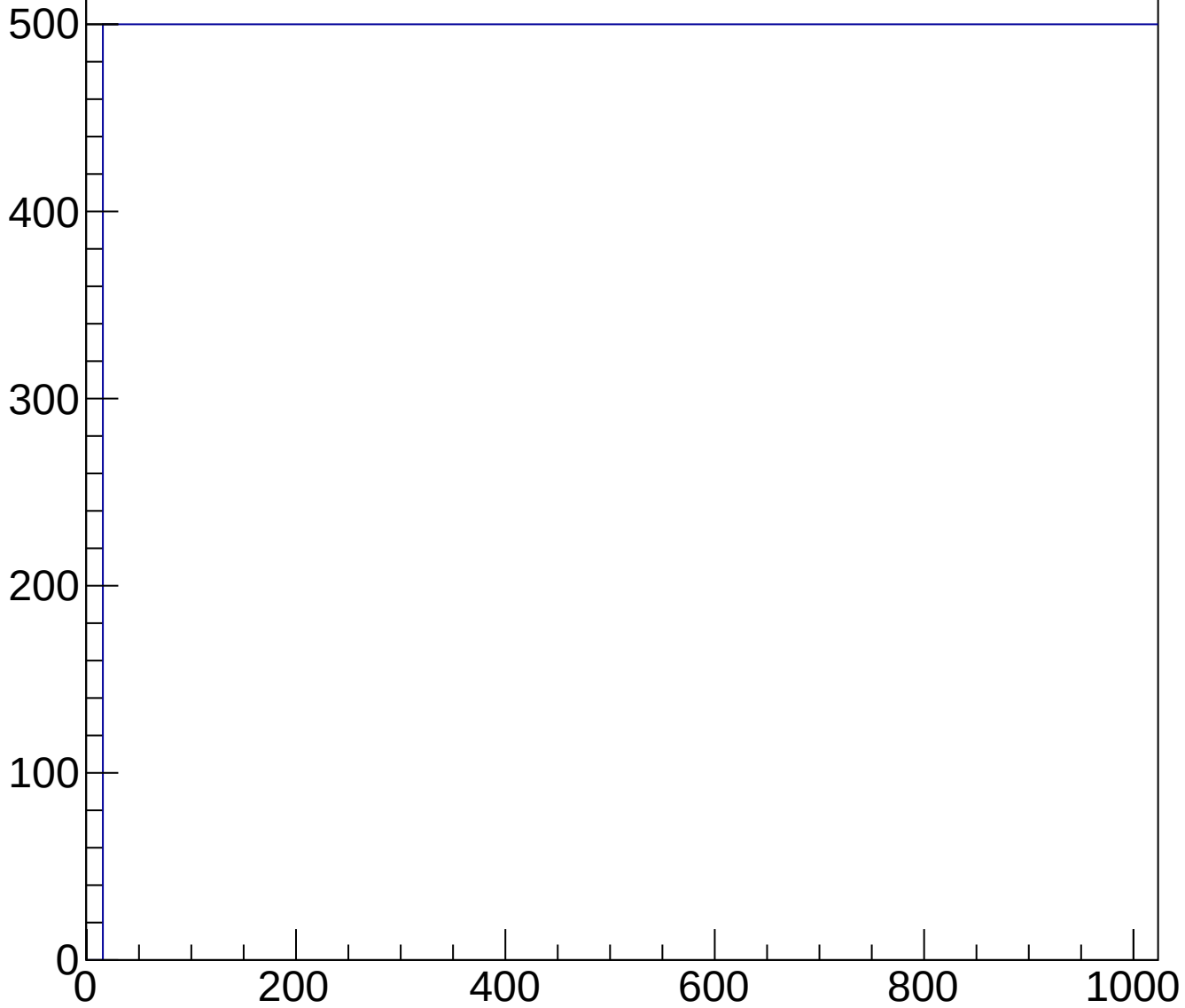
Ramp saltro:0 chip:0:7 channel 14 pattern2

Entries



Ramp saltro:0 chip:0:7 channel 15 pattern2

Entries



Mean	519.5
Std Dev	291

ADC value