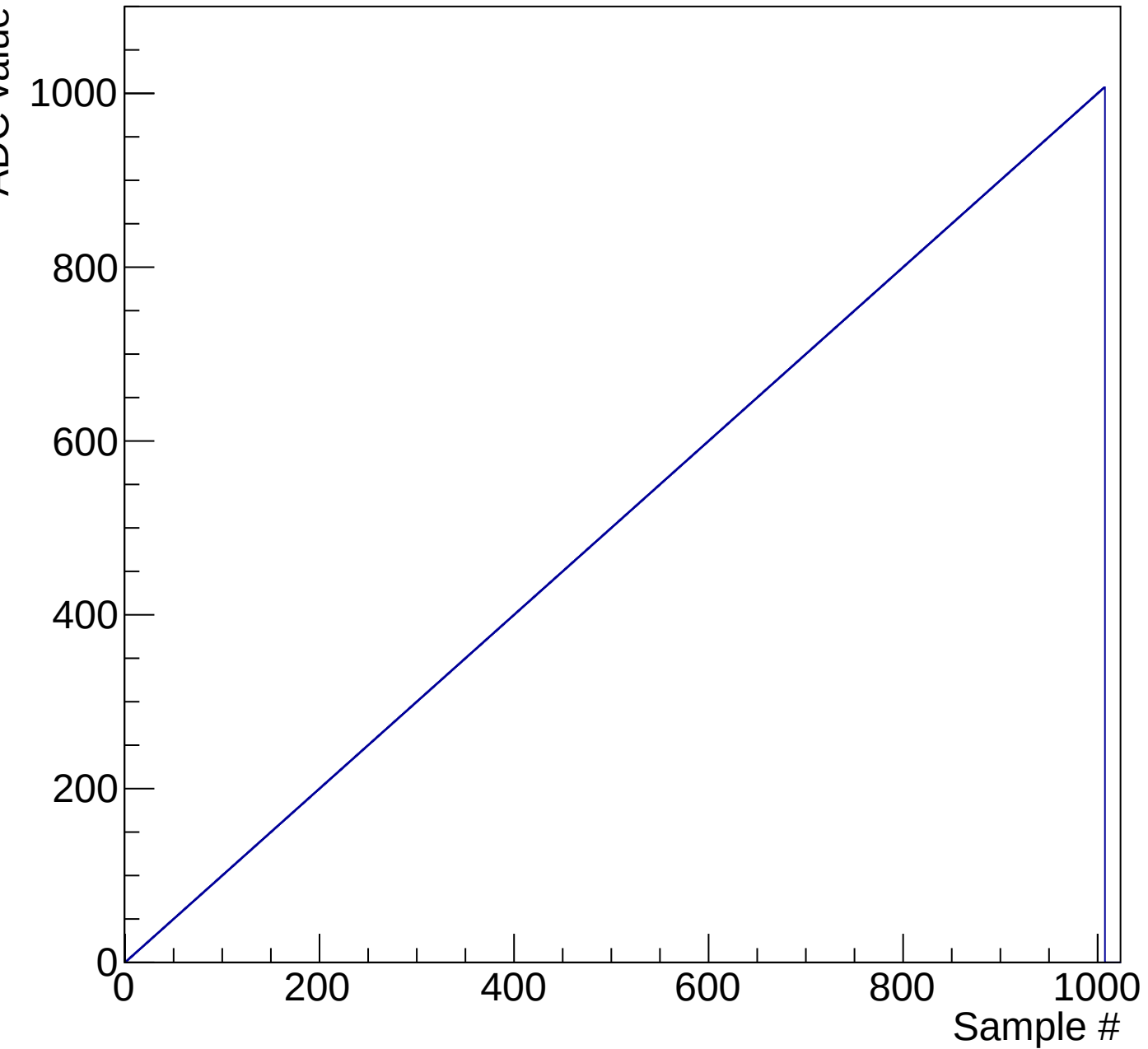
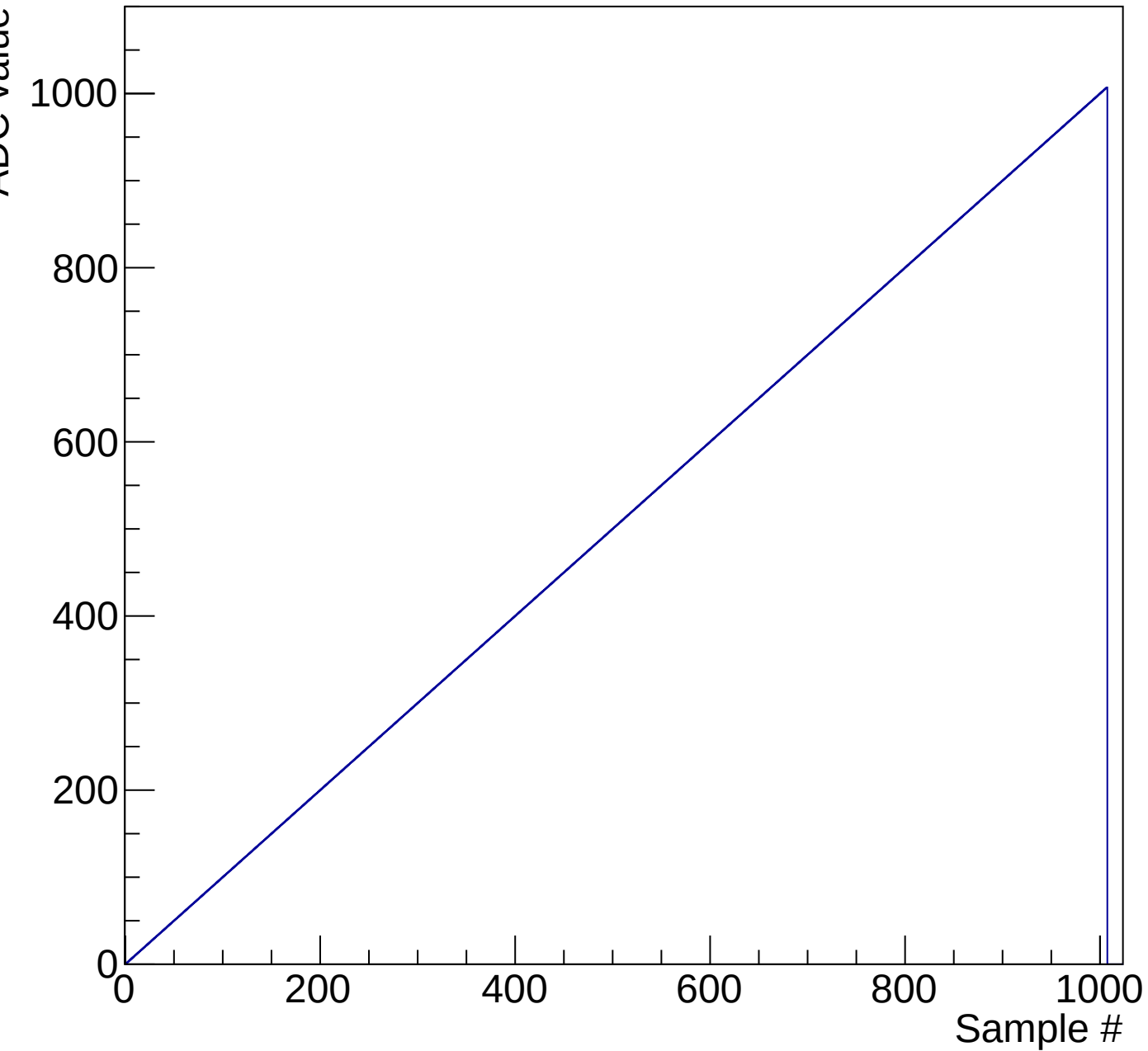


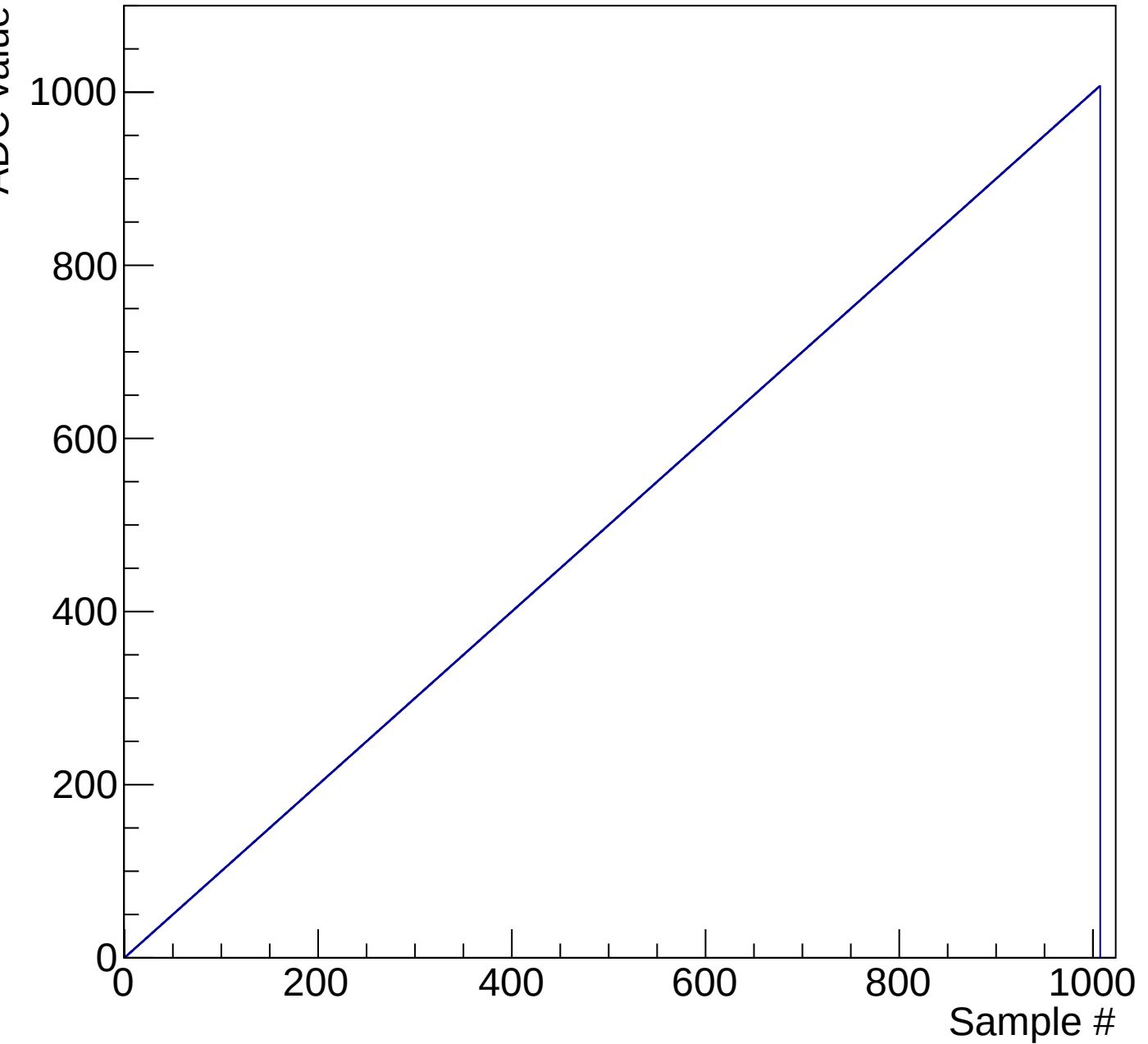
Channel 0 pattern 1



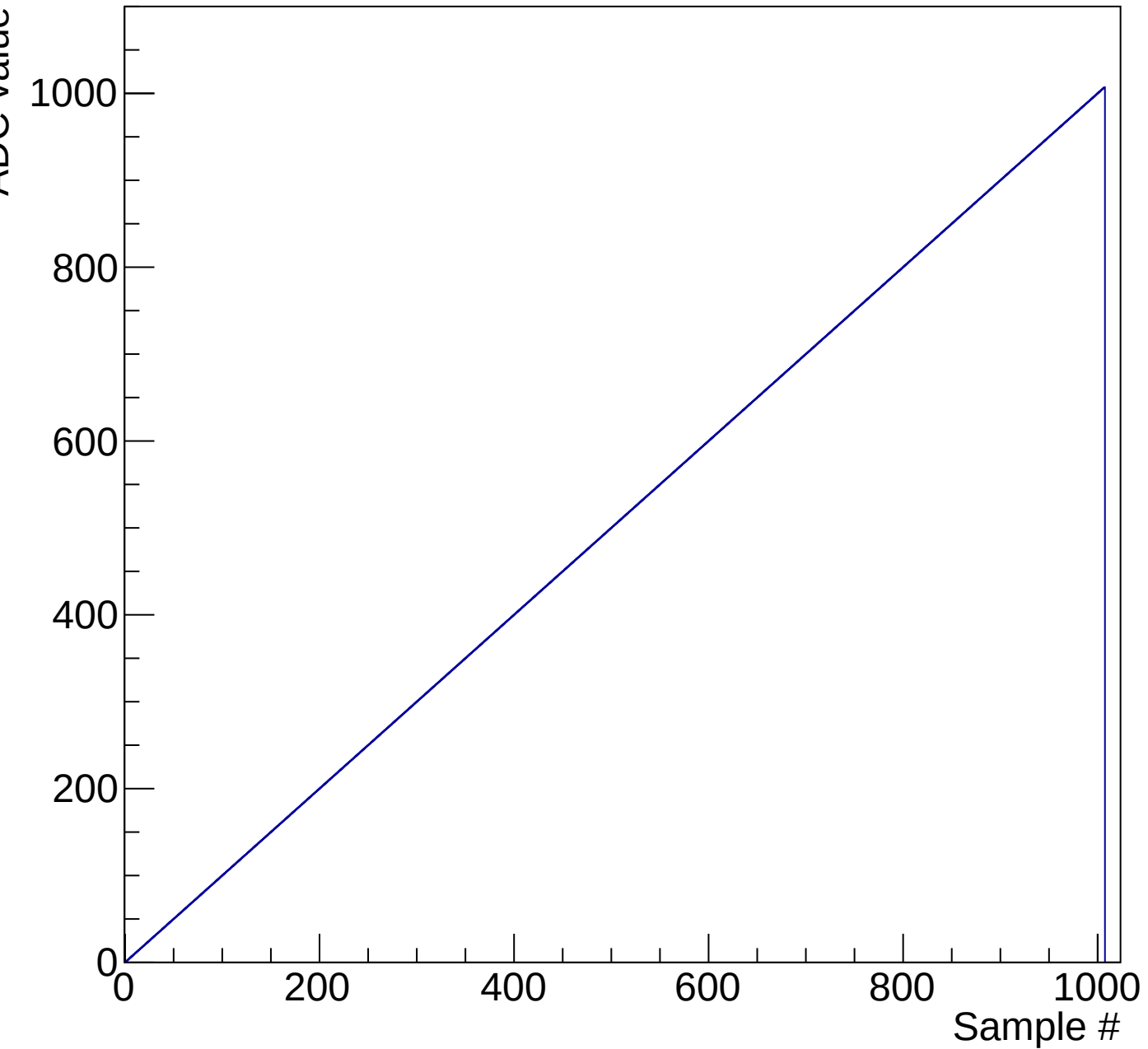
Channel 1 pattern 1



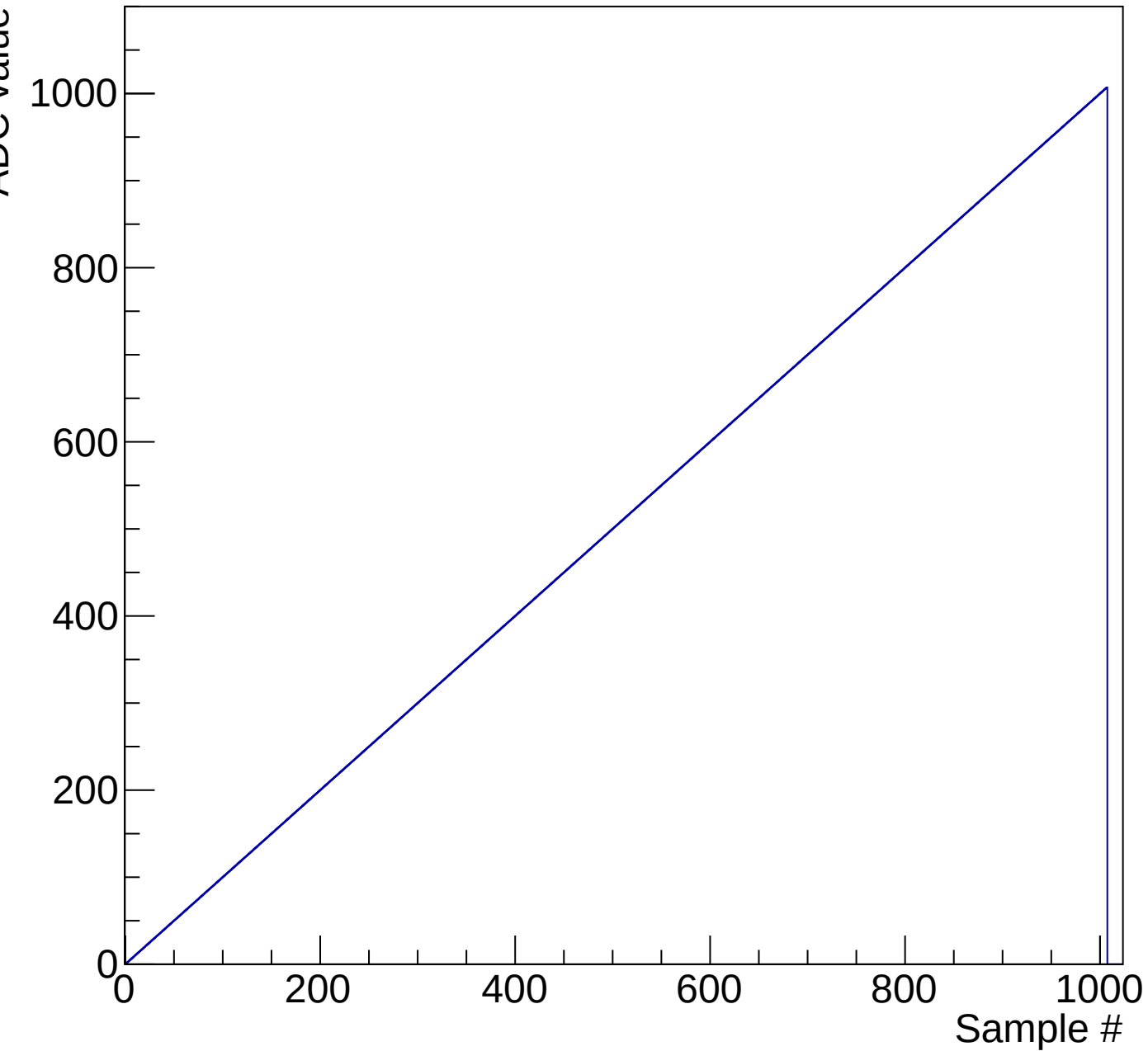
Channel 2 pattern 1



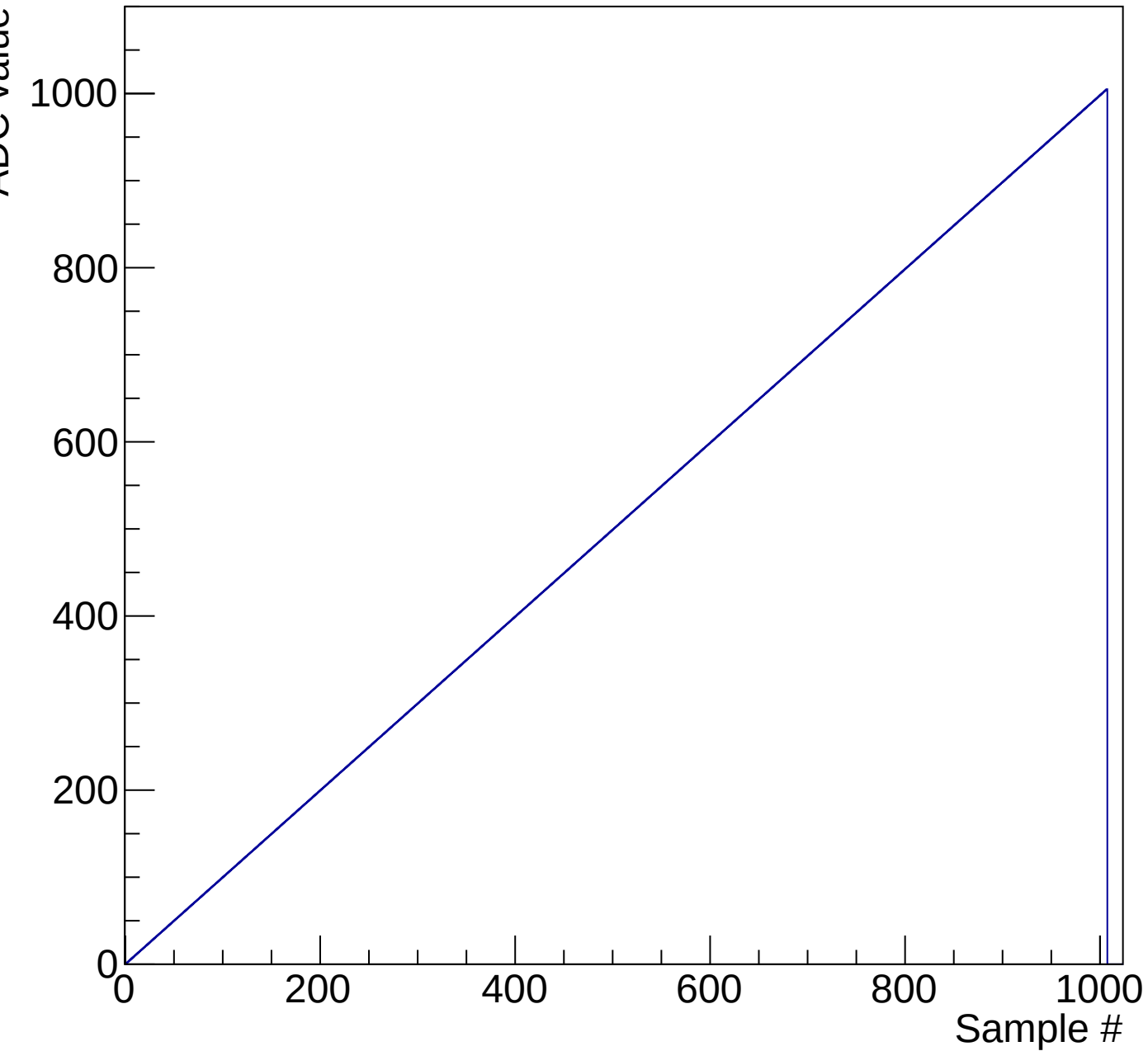
Channel 3 pattern 1



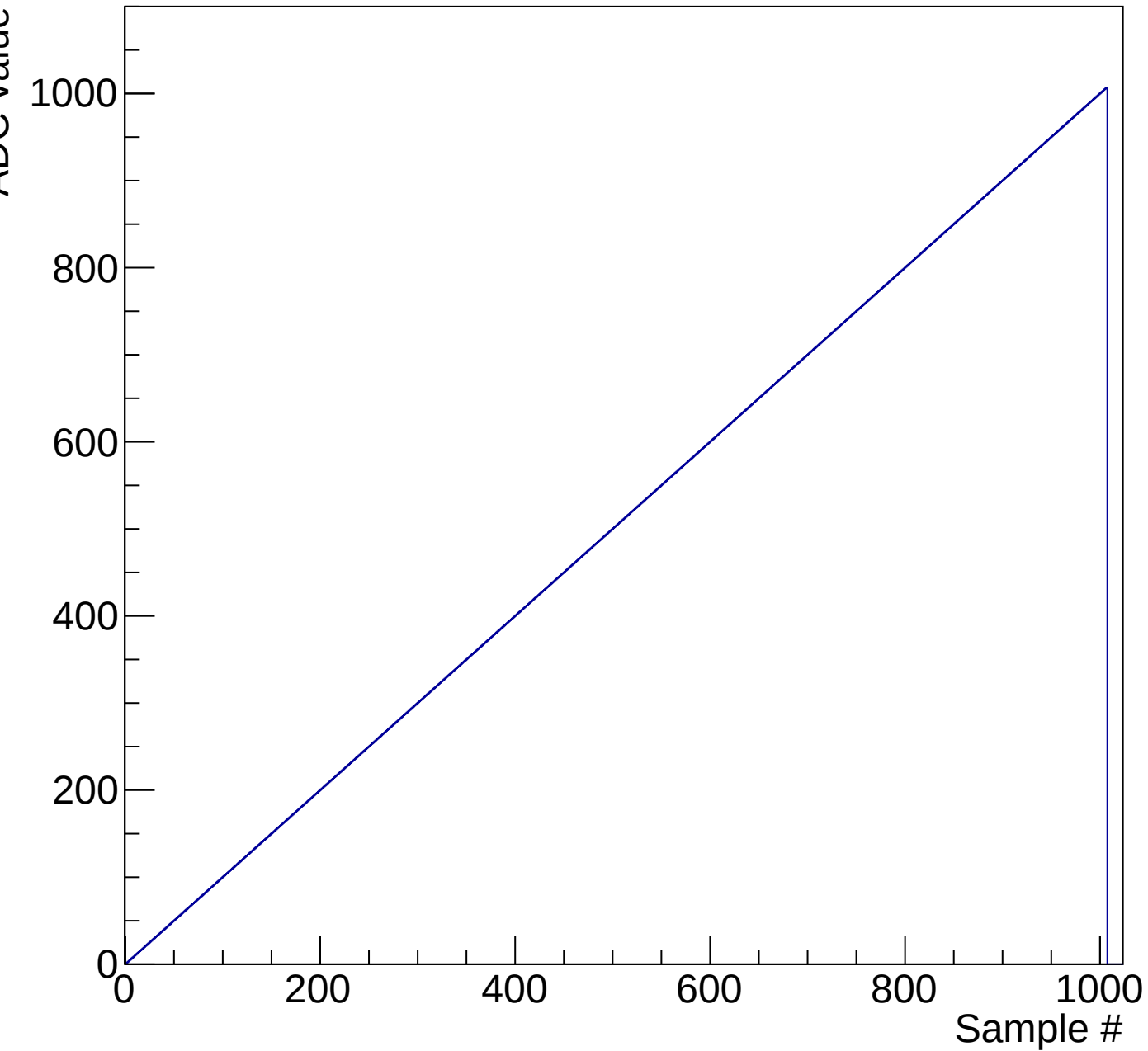
Channel 4 pattern 1



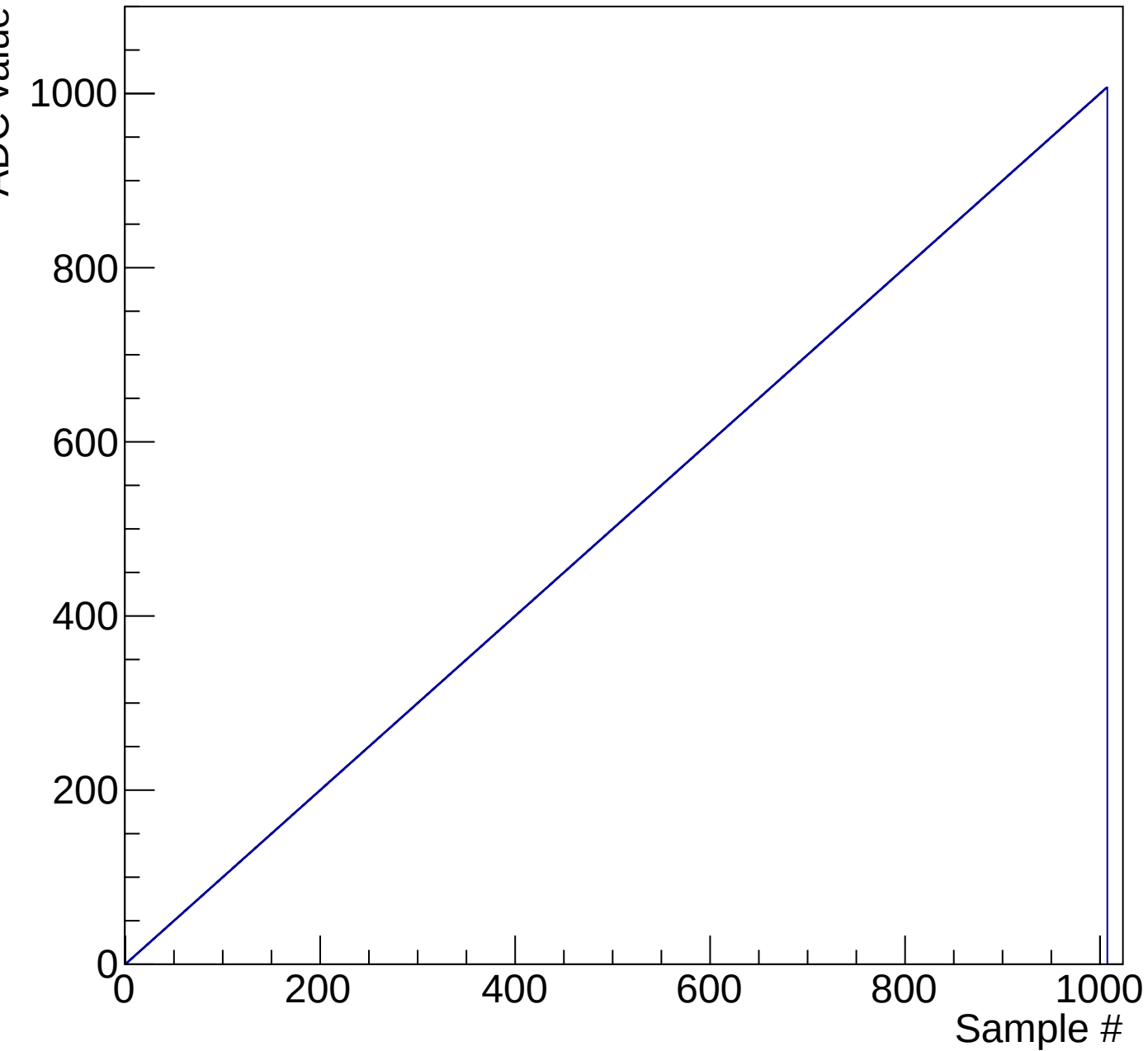
Channel 5 pattern 1



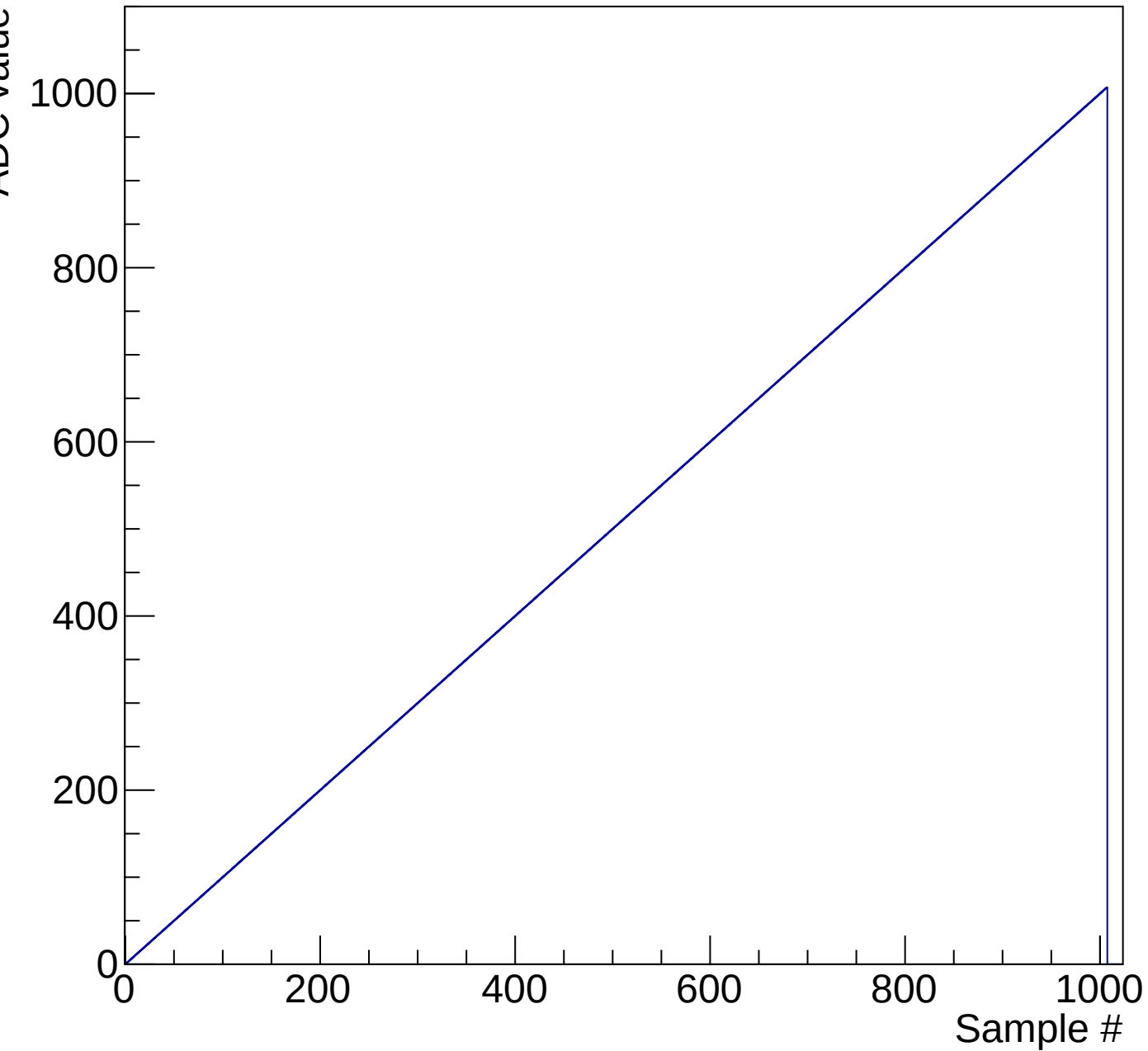
Channel 6 pattern 1



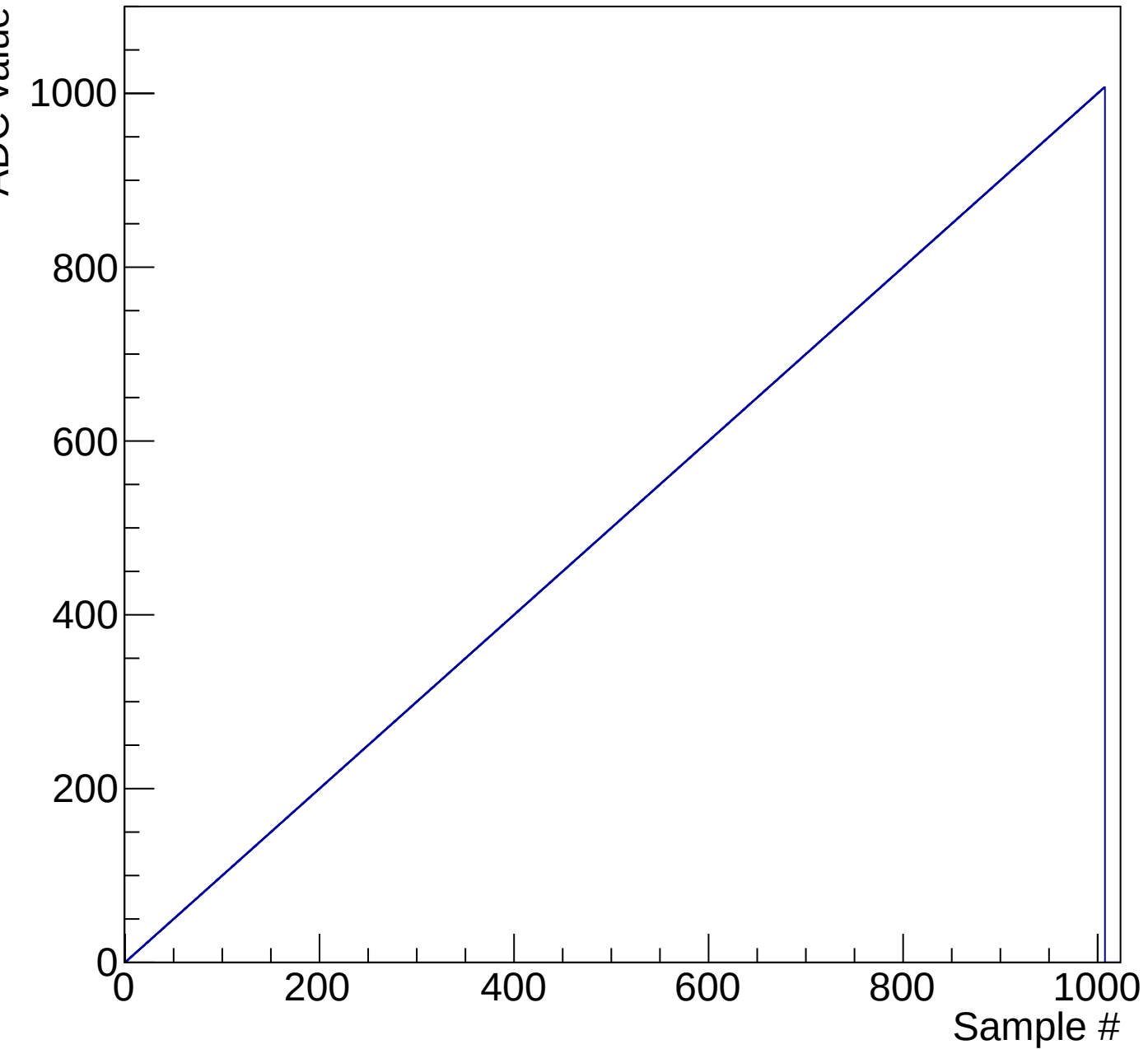
Channel 7 pattern 1



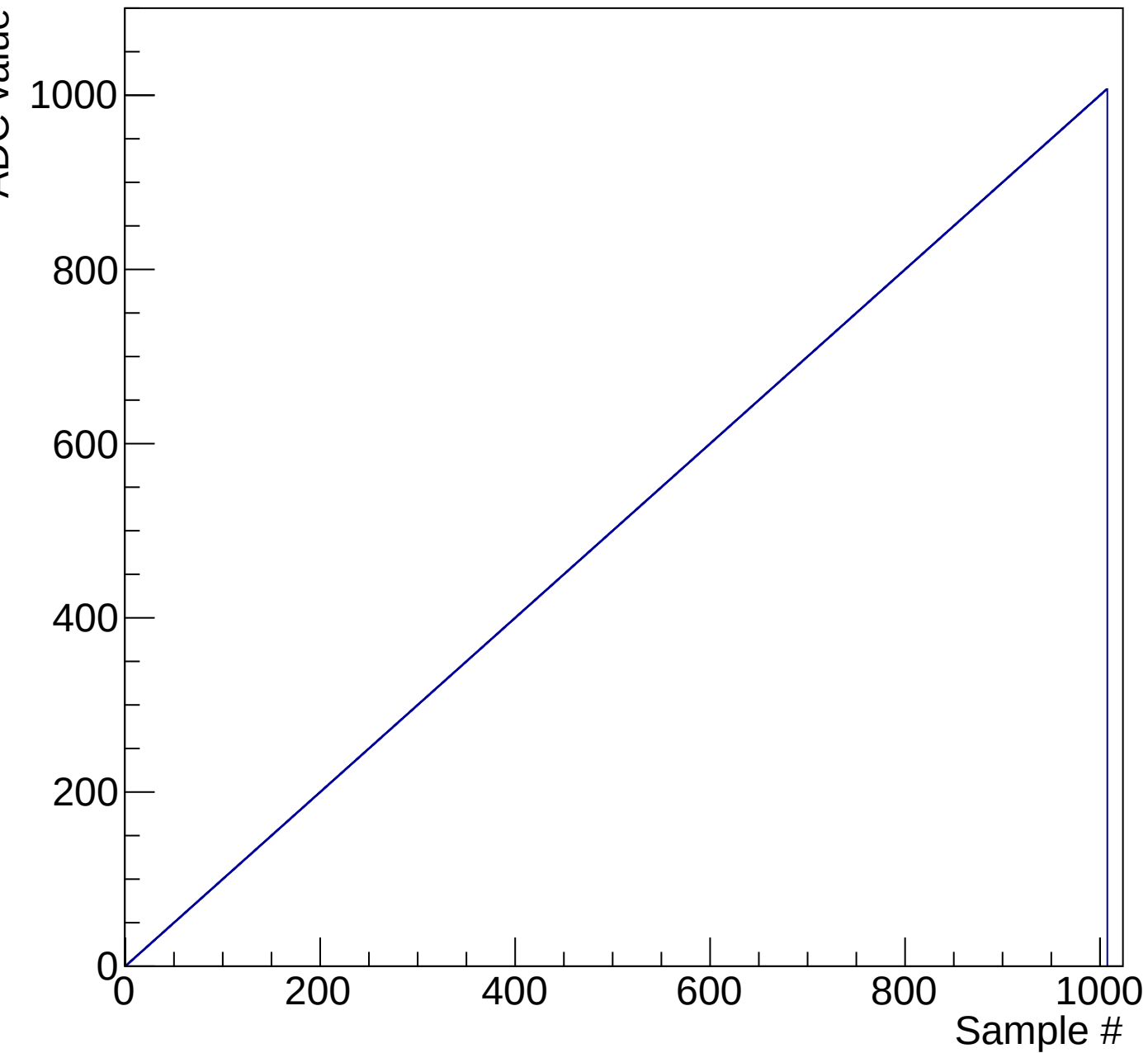
Channel 8 pattern 1



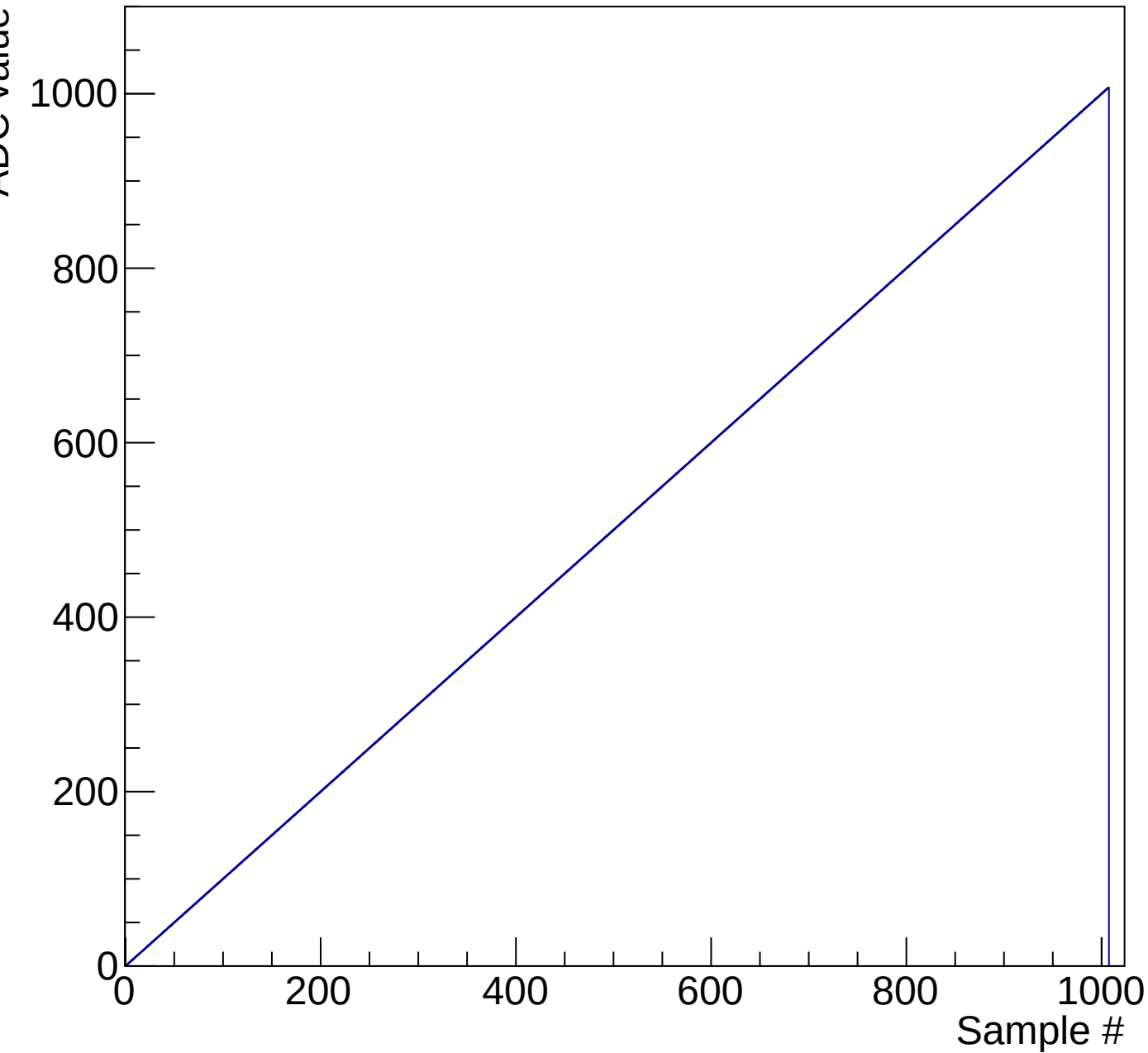
Channel 9 pattern 1



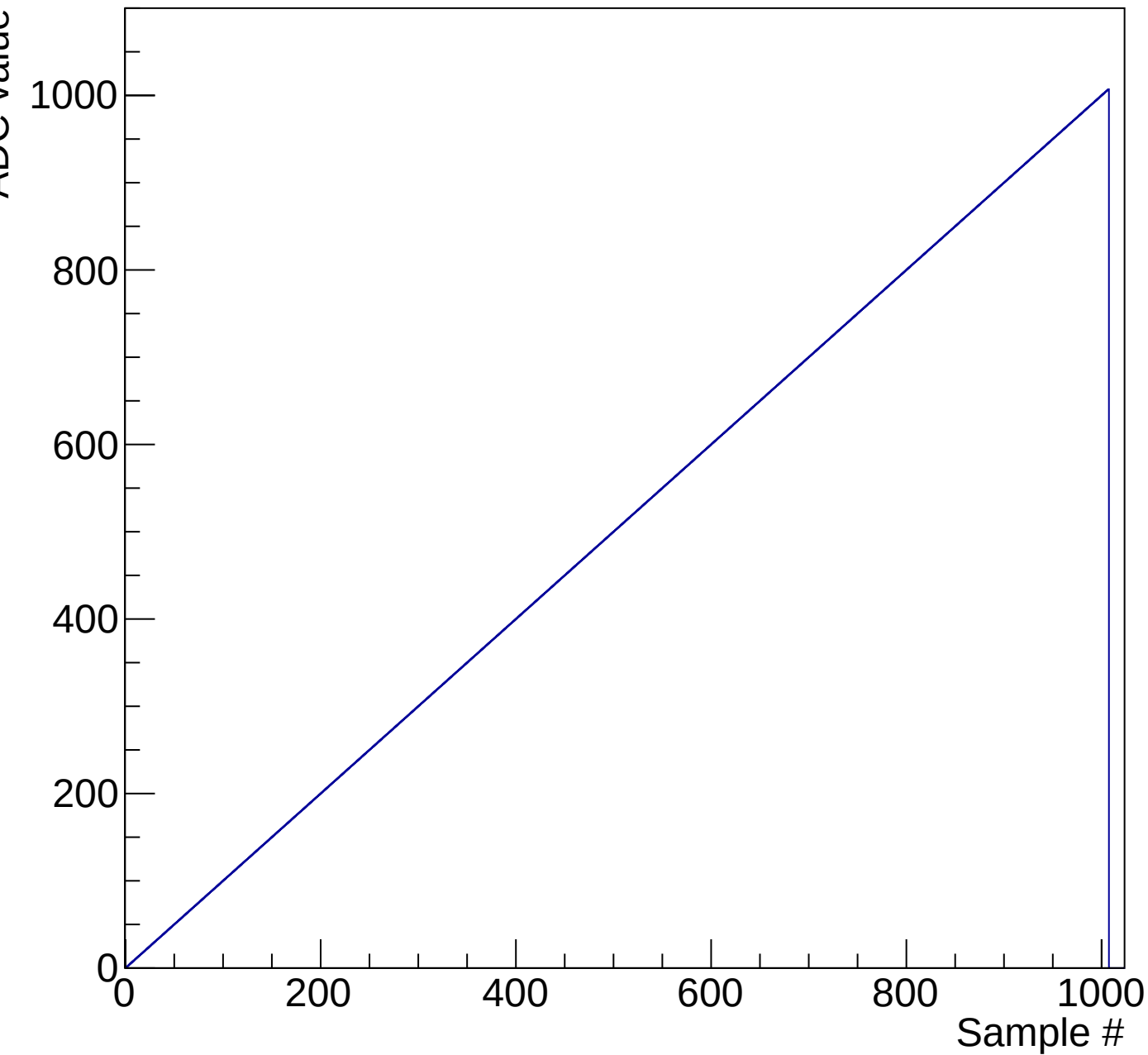
Channel 10 pattern 1



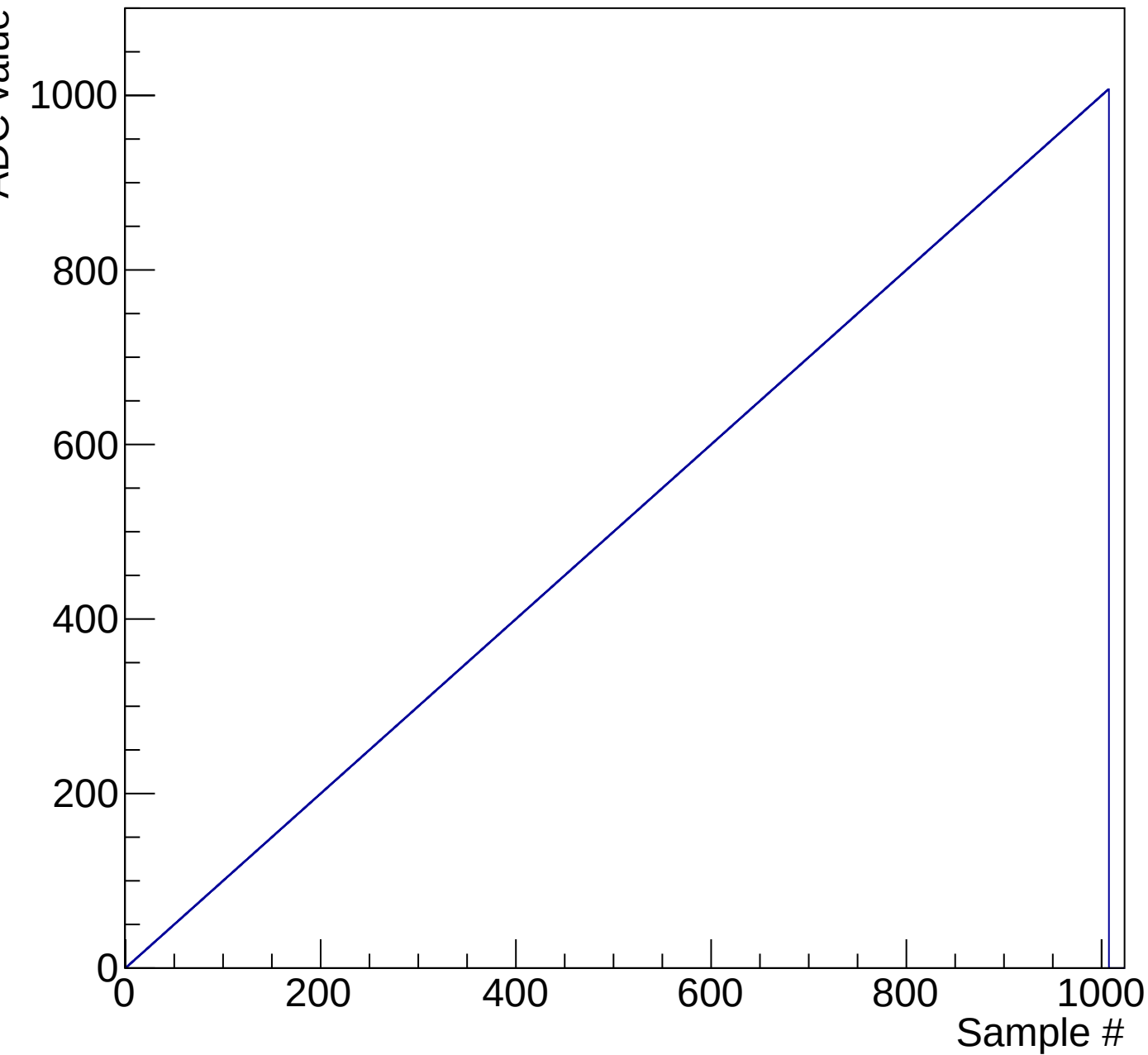
Channel 11 pattern 1



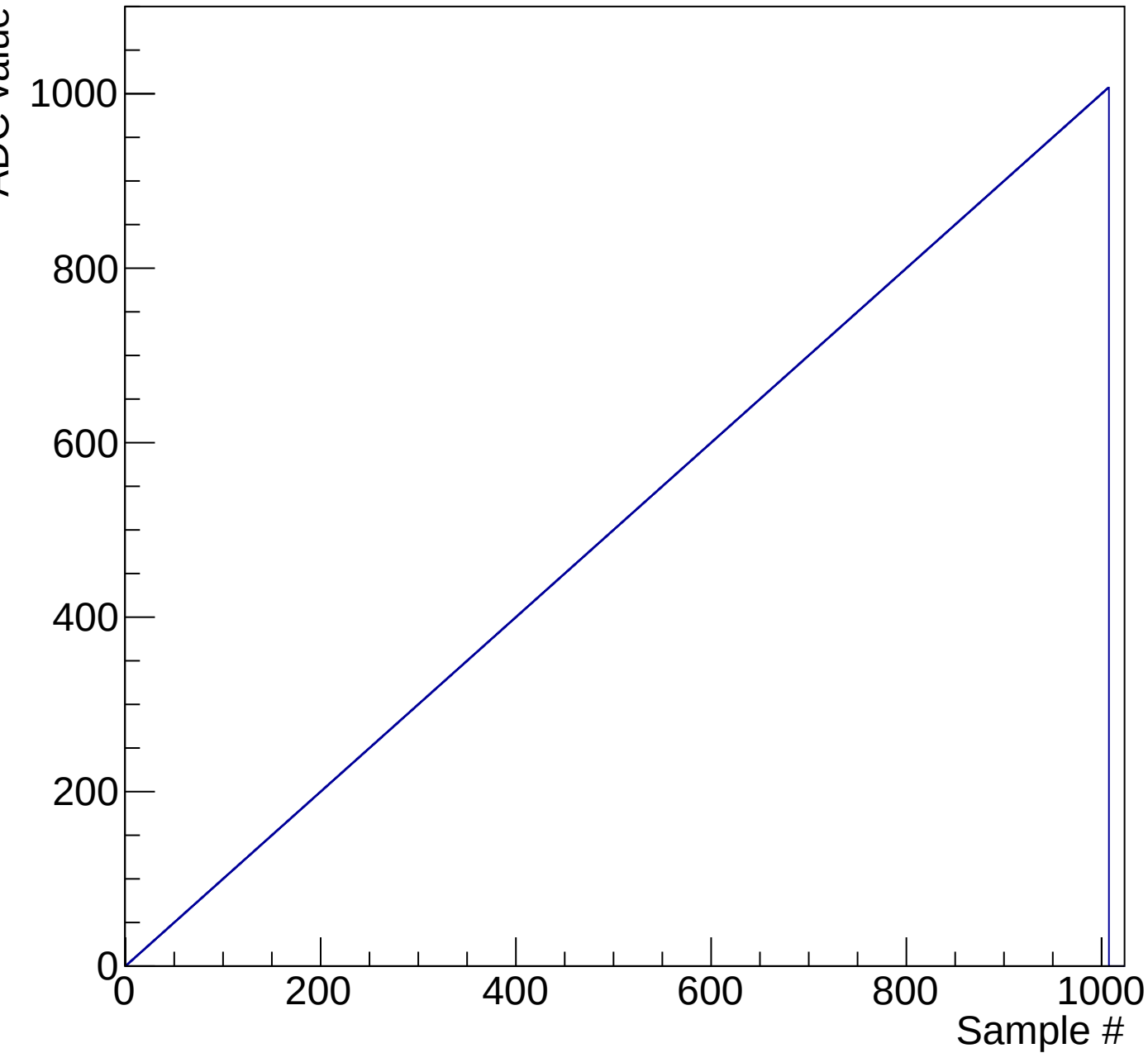
Channel 12 pattern 1



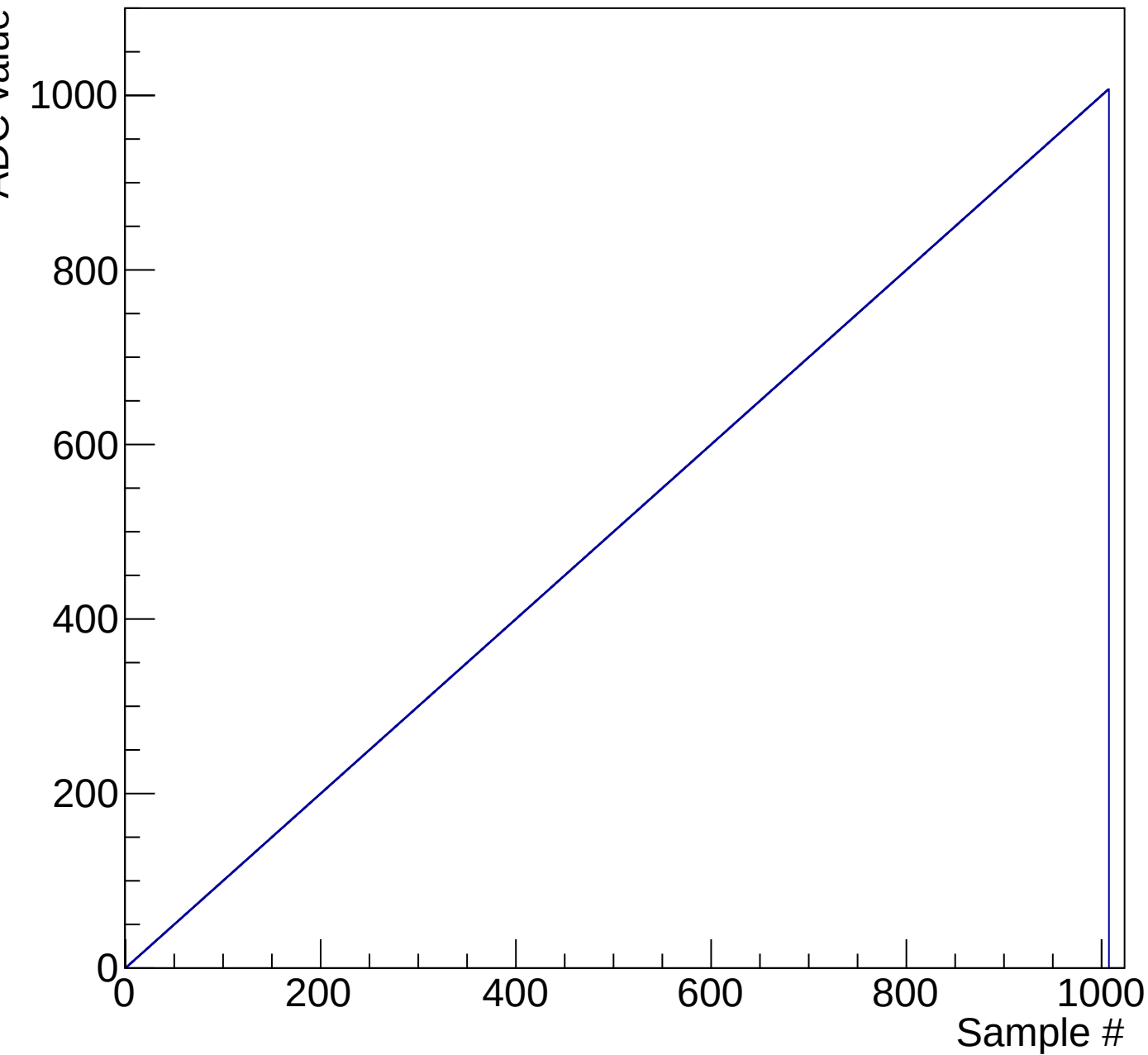
Channel 13 pattern 1



Channel 14 pattern 1



Channel 15 pattern 1



Ramp saltro:0 chip:0:7 channel 0 pattern1

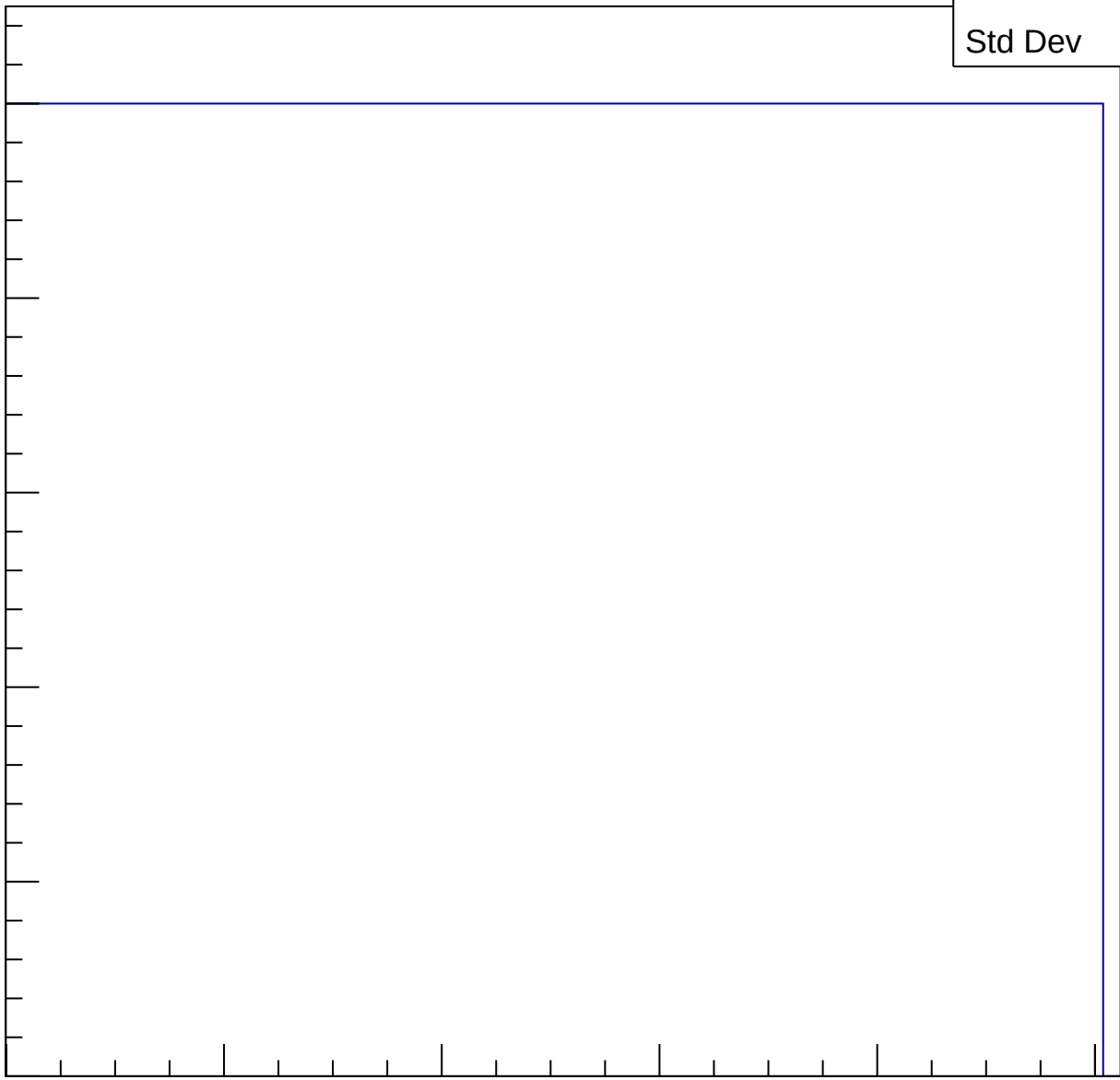
Entries

500
400
300
200
100
0

Mean	503.5
Std Dev	291

ADC value

0 200 400 600 800 1000



Ramp saltro:0 chip:0:7 channel 1 pattern1

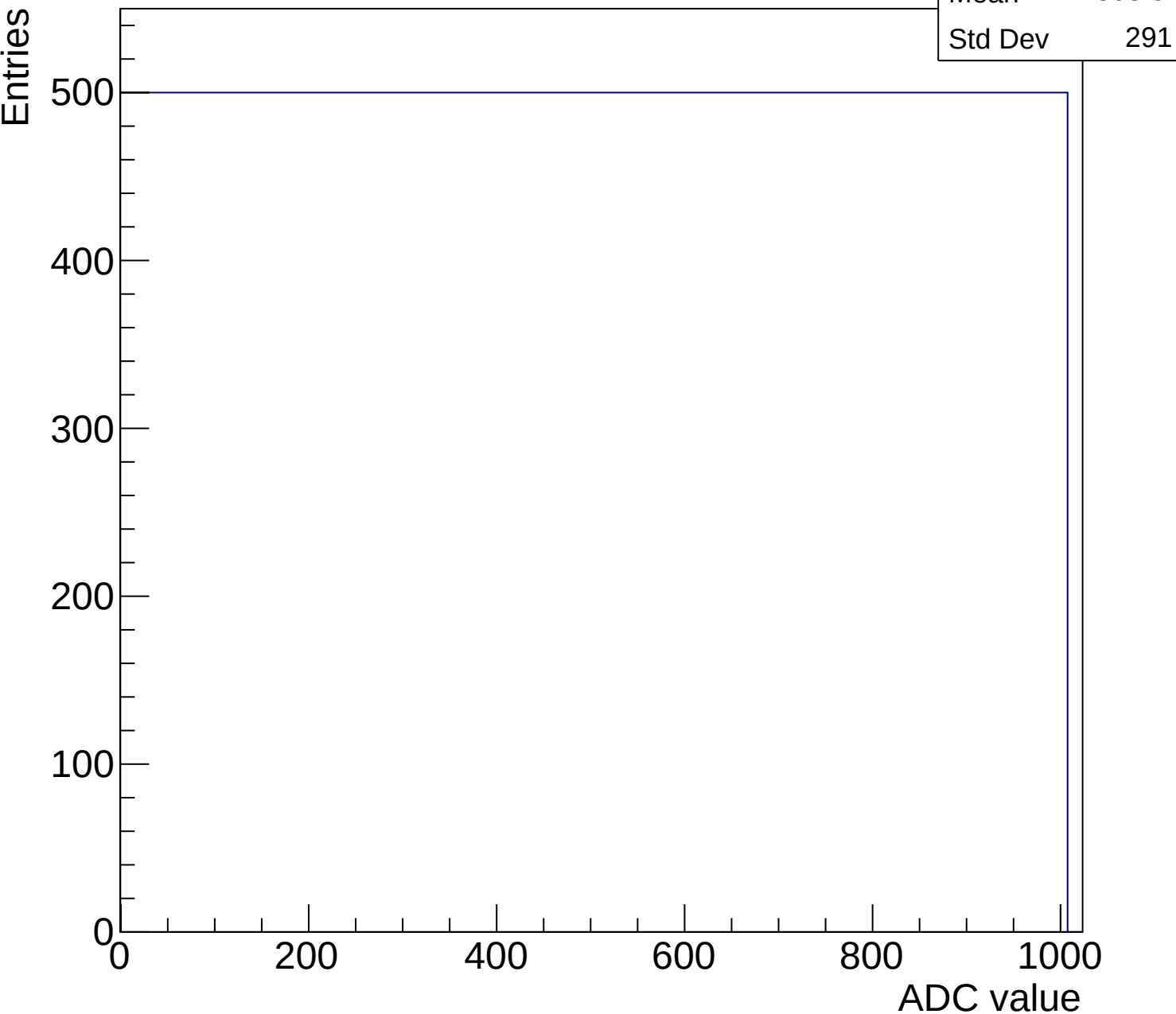
Entries

500
400
300
200
100
0

Mean	503.5
Std Dev	291

0 200 400 600 800 1000

ADC value



Ramp saltro:0 chip:0:7 channel 2 pattern1

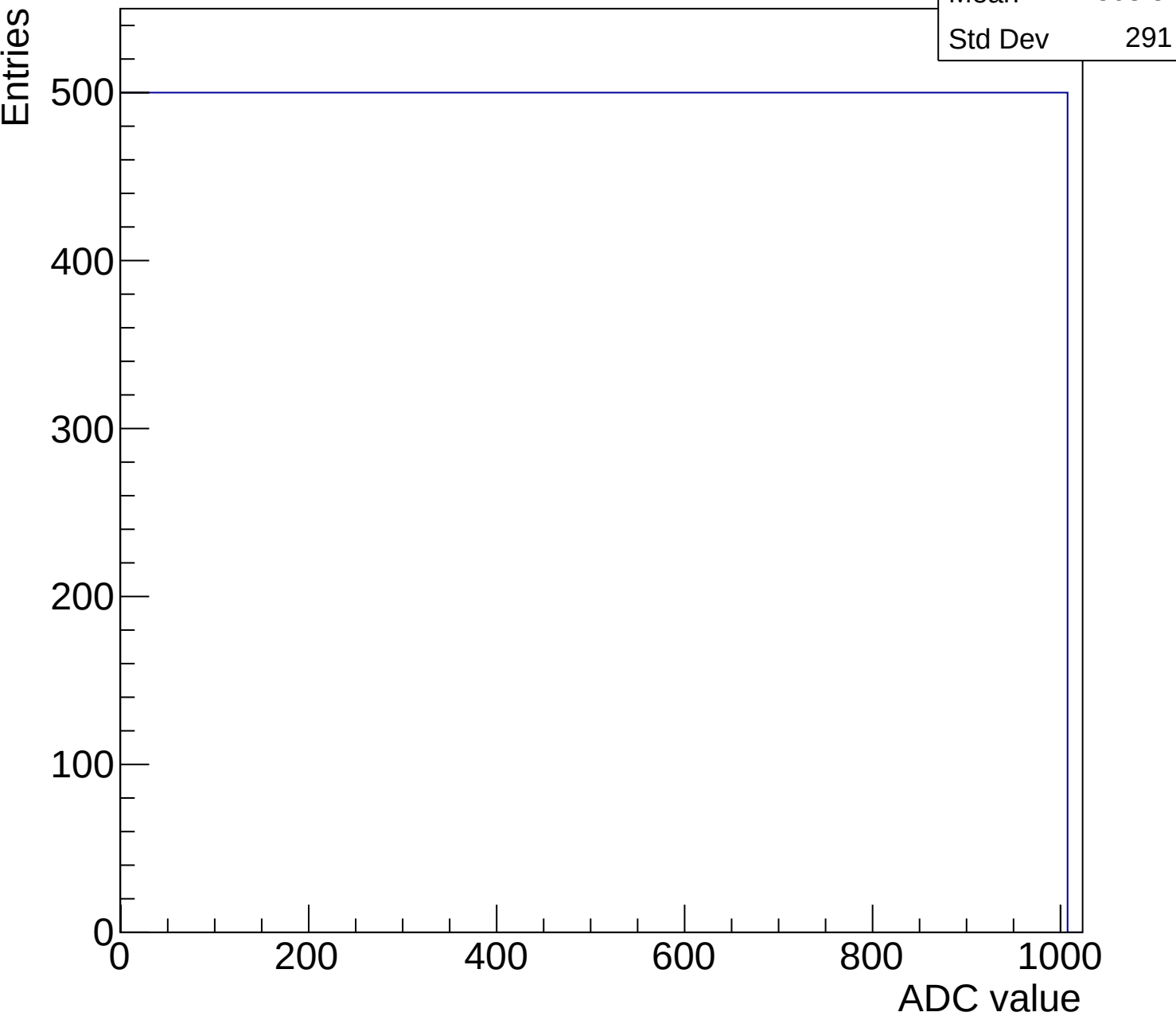
Entries

500
400
300
200
100
0

Mean	503.5
Std Dev	291

ADC value

0 200 400 600 800 1000



Ramp saltro:0 chip:0:7 channel 3 pattern1

Entries

500

400

300

200

100

0

0

200

400

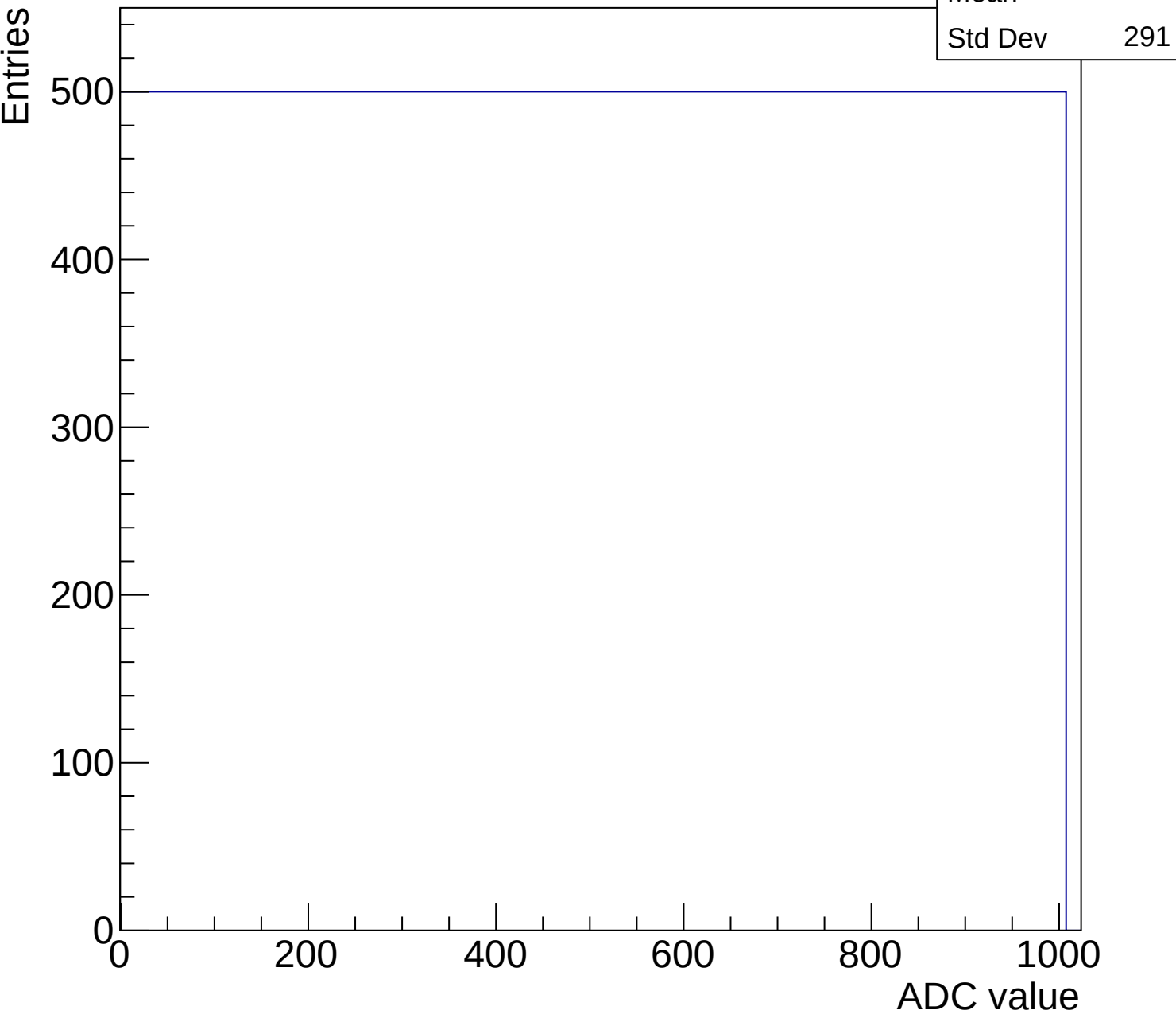
600

800

1000

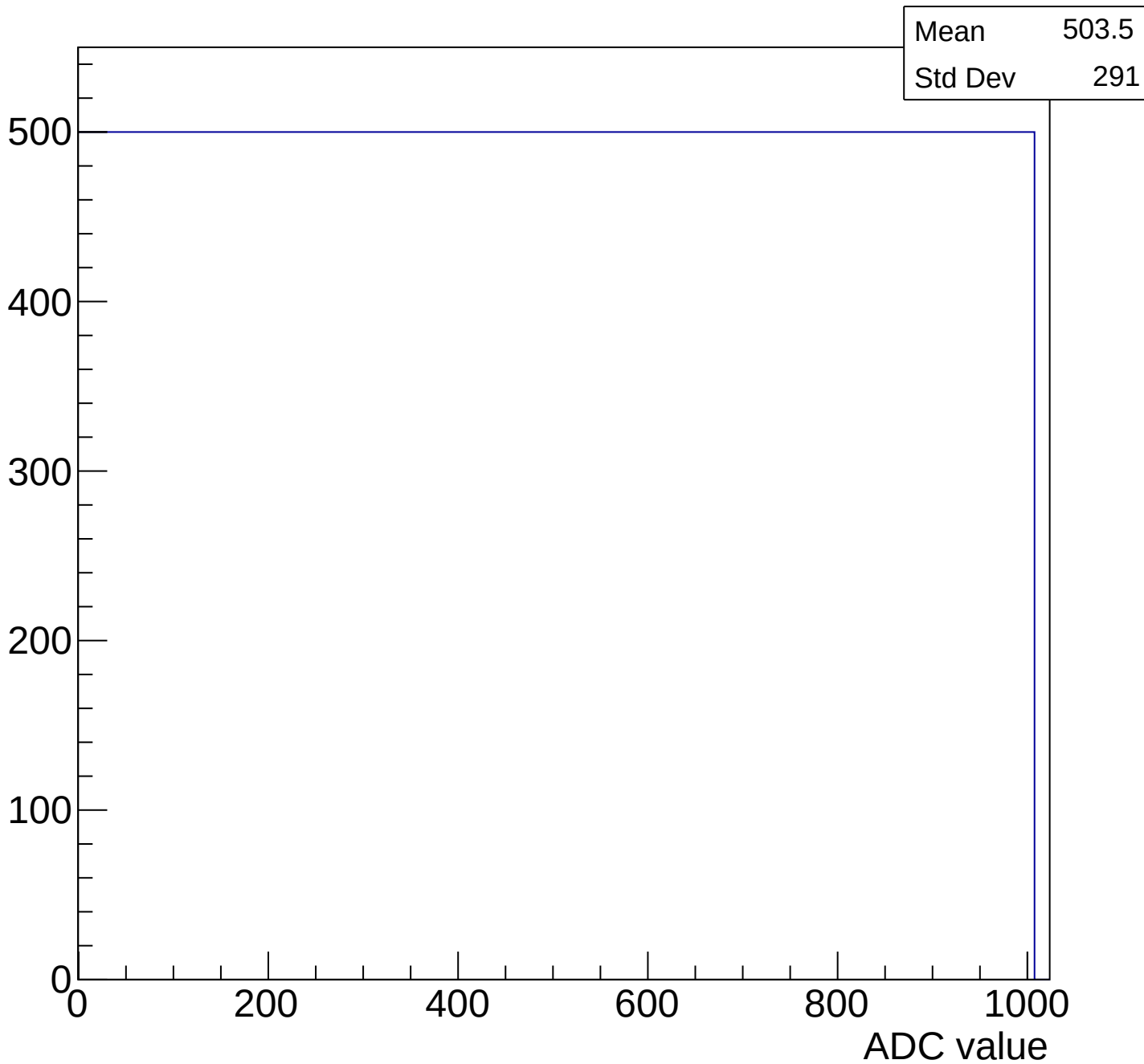
ADC value

Mean	503.5
Std Dev	291



Ramp saltro:0 chip:0:7 channel 4 pattern1

Entries



Ramp saltro:0 chip:0:7 channel 5 pattern1

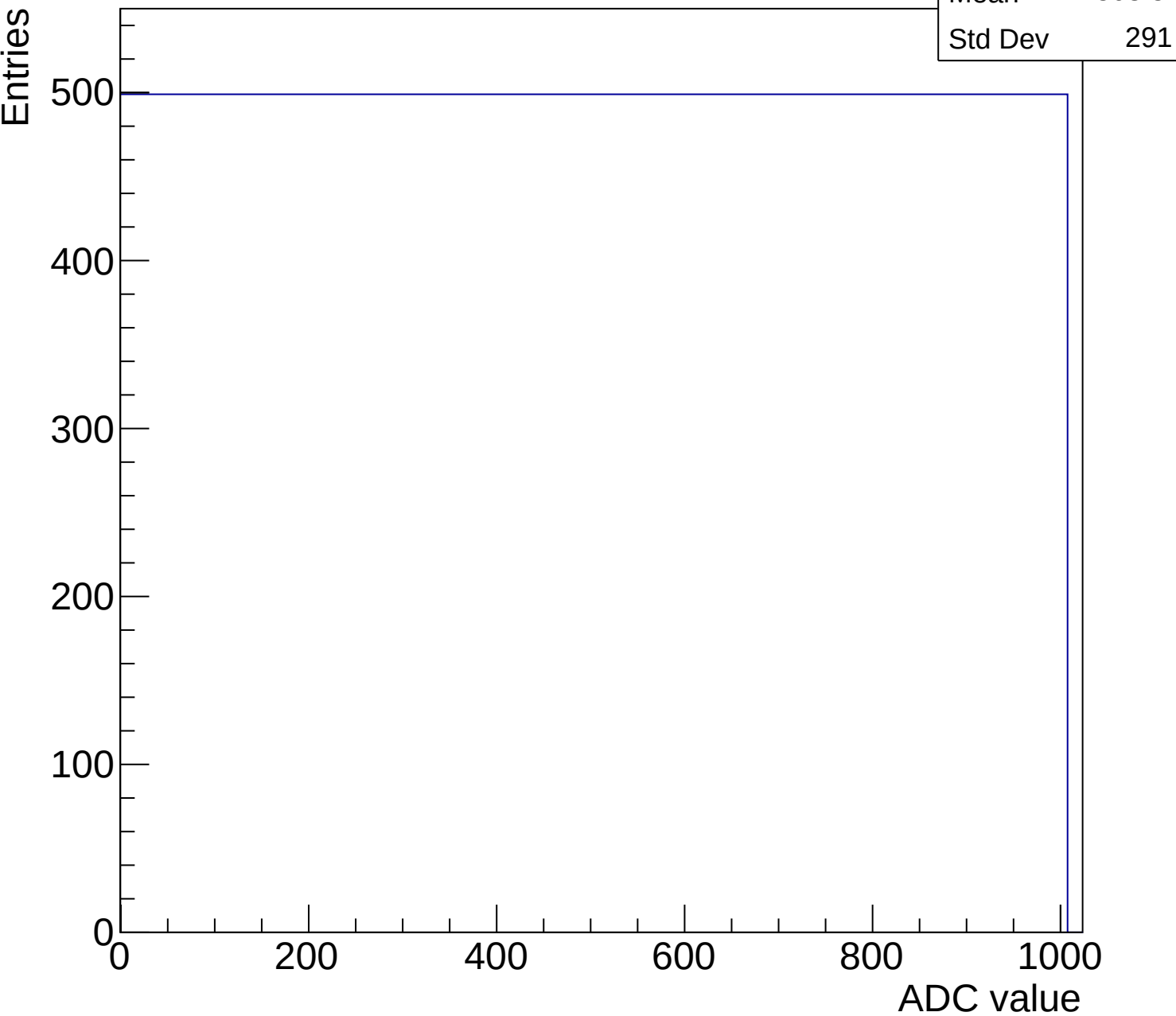
Entries

500
400
300
200
100
0

Mean	503.5
Std Dev	291

0 200 400 600 800 1000

ADC value



Ramp saltro:0 chip:0:7 channel 6 pattern1

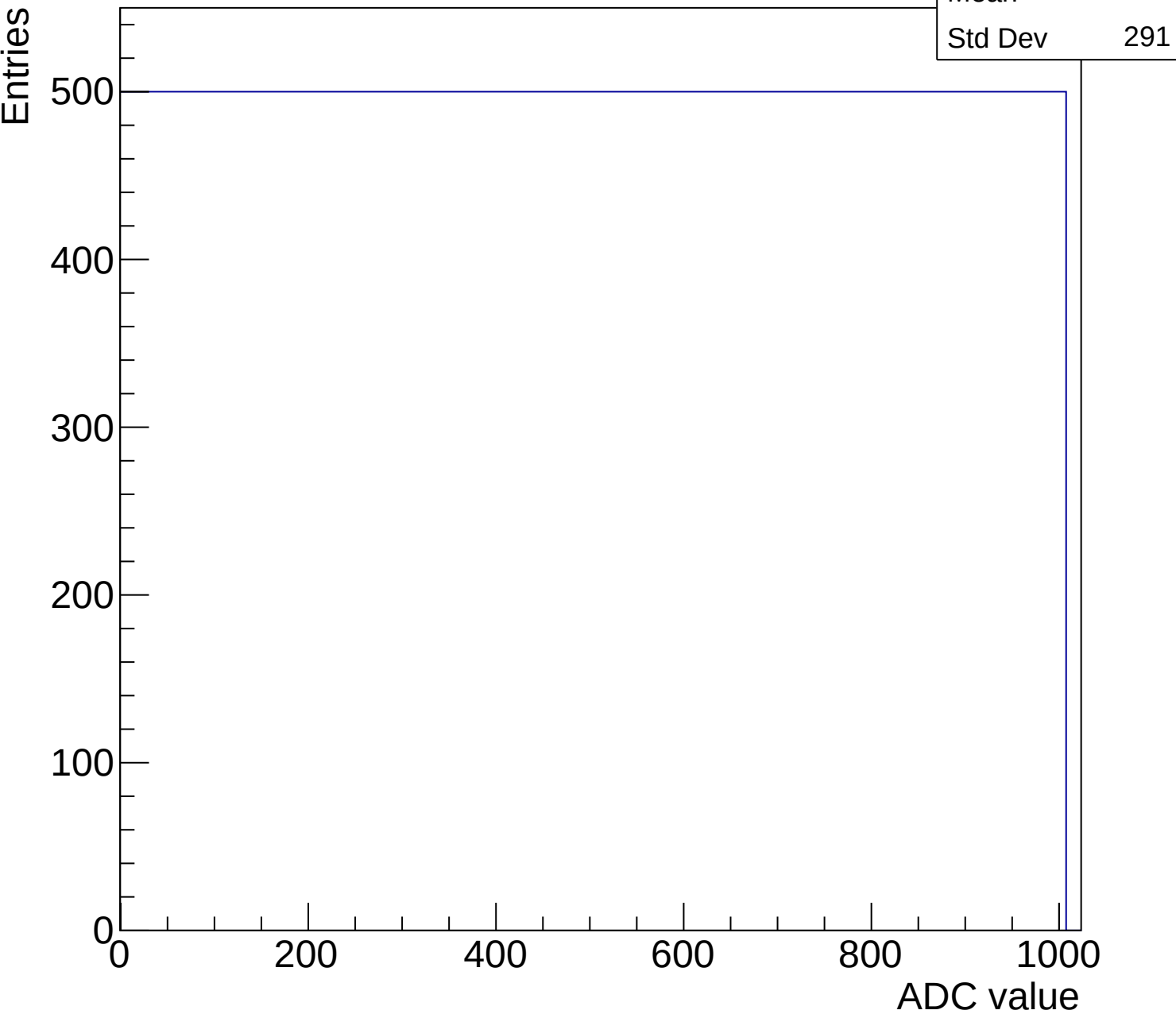
Entries

500
400
300
200
100
0

Mean	503.5
Std Dev	291

ADC value

0 200 400 600 800 1000



Ramp saltro:0 chip:0:7 channel 7 pattern1

Entries

500

400

300

200

100

0

0

200

400

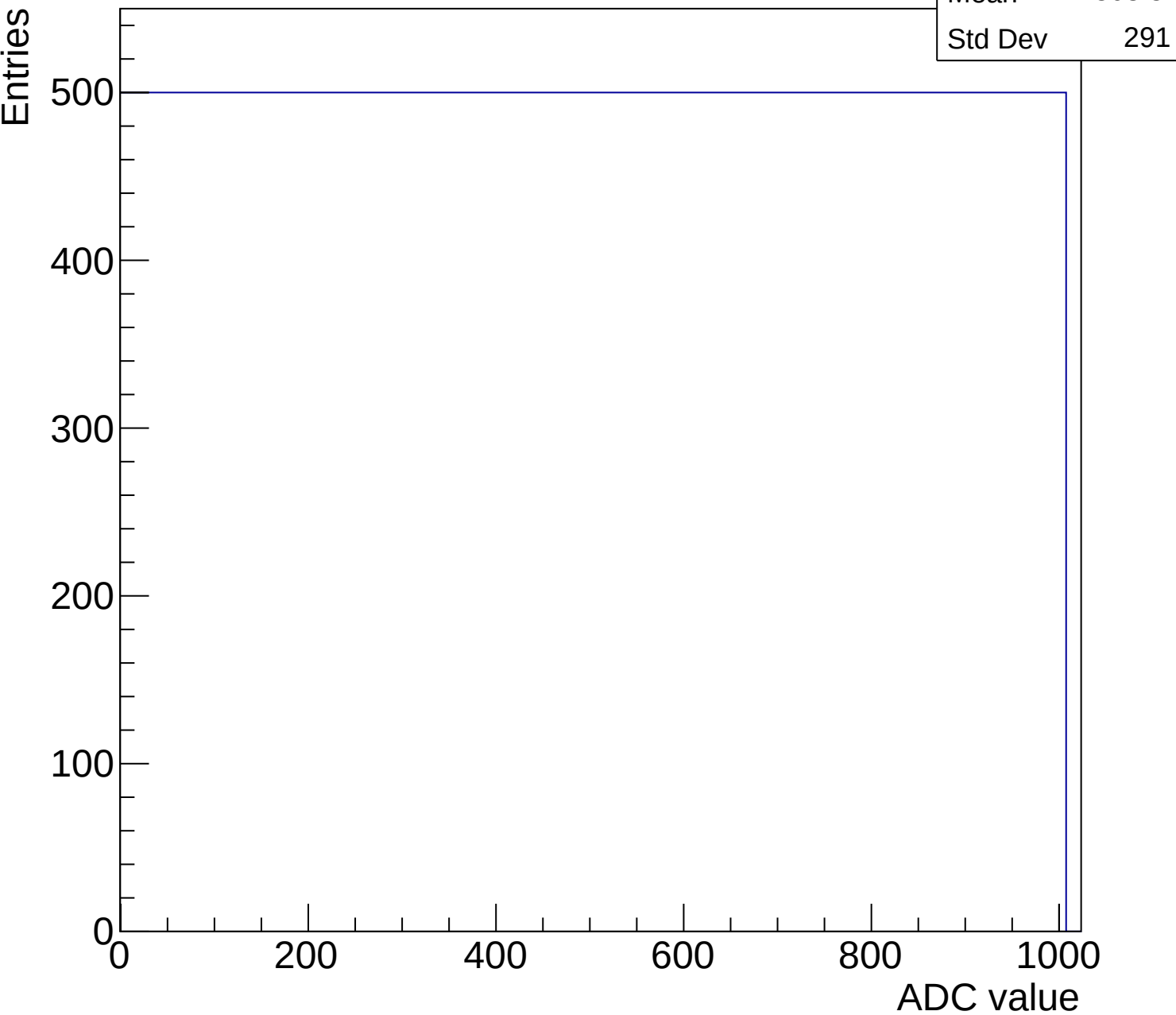
600

800

1000

ADC value

Mean	503.5
Std Dev	291



Ramp saltro:0 chip:0:7 channel 8 pattern1

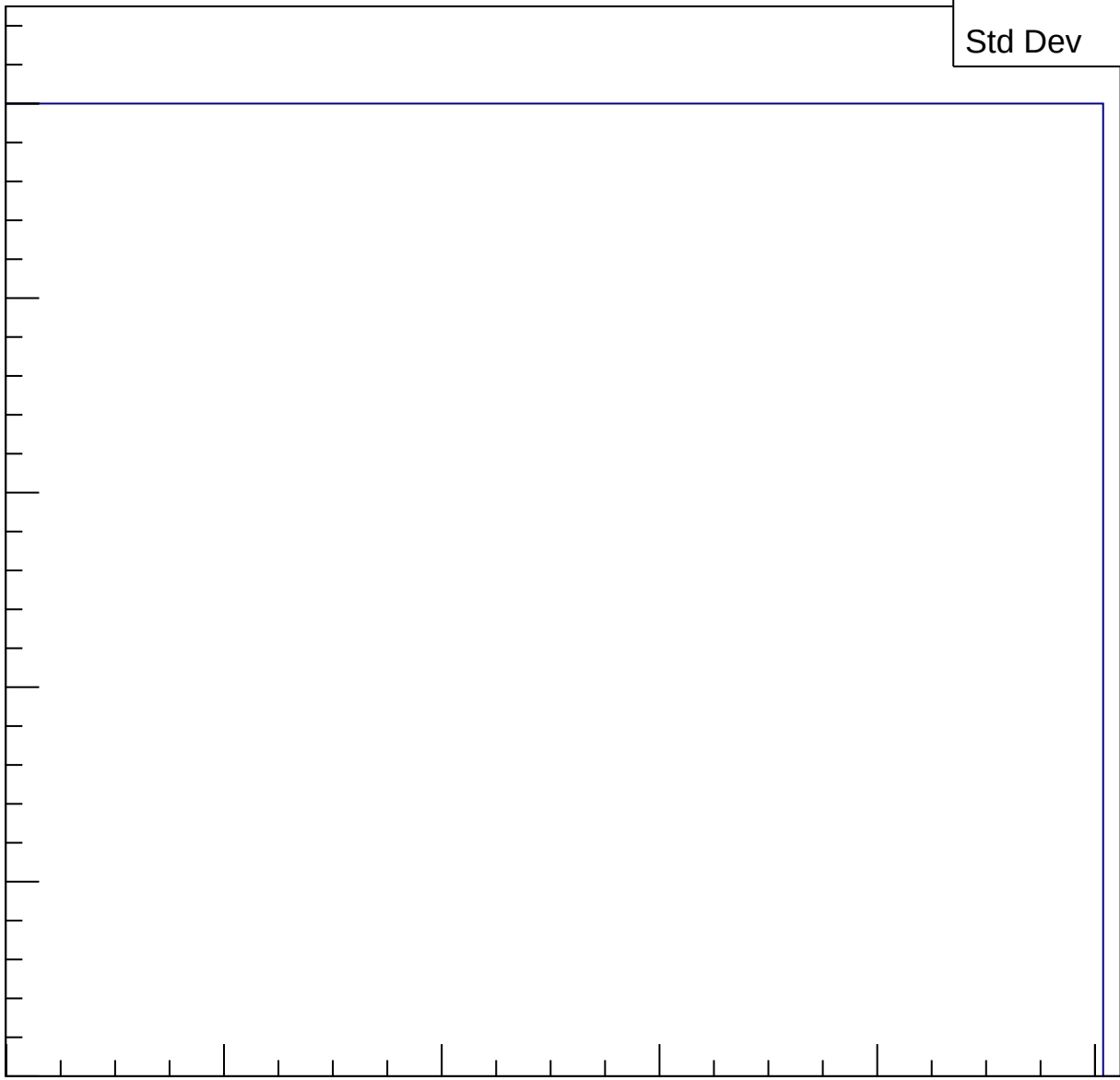
Entries

500
400
300
200
100
0

Mean	503.5
Std Dev	291

ADC value

0 200 400 600 800 1000



Ramp saltro:0 chip:0:7 channel 9 pattern1

Entries

500

400

300

200

100

0

0

200

400

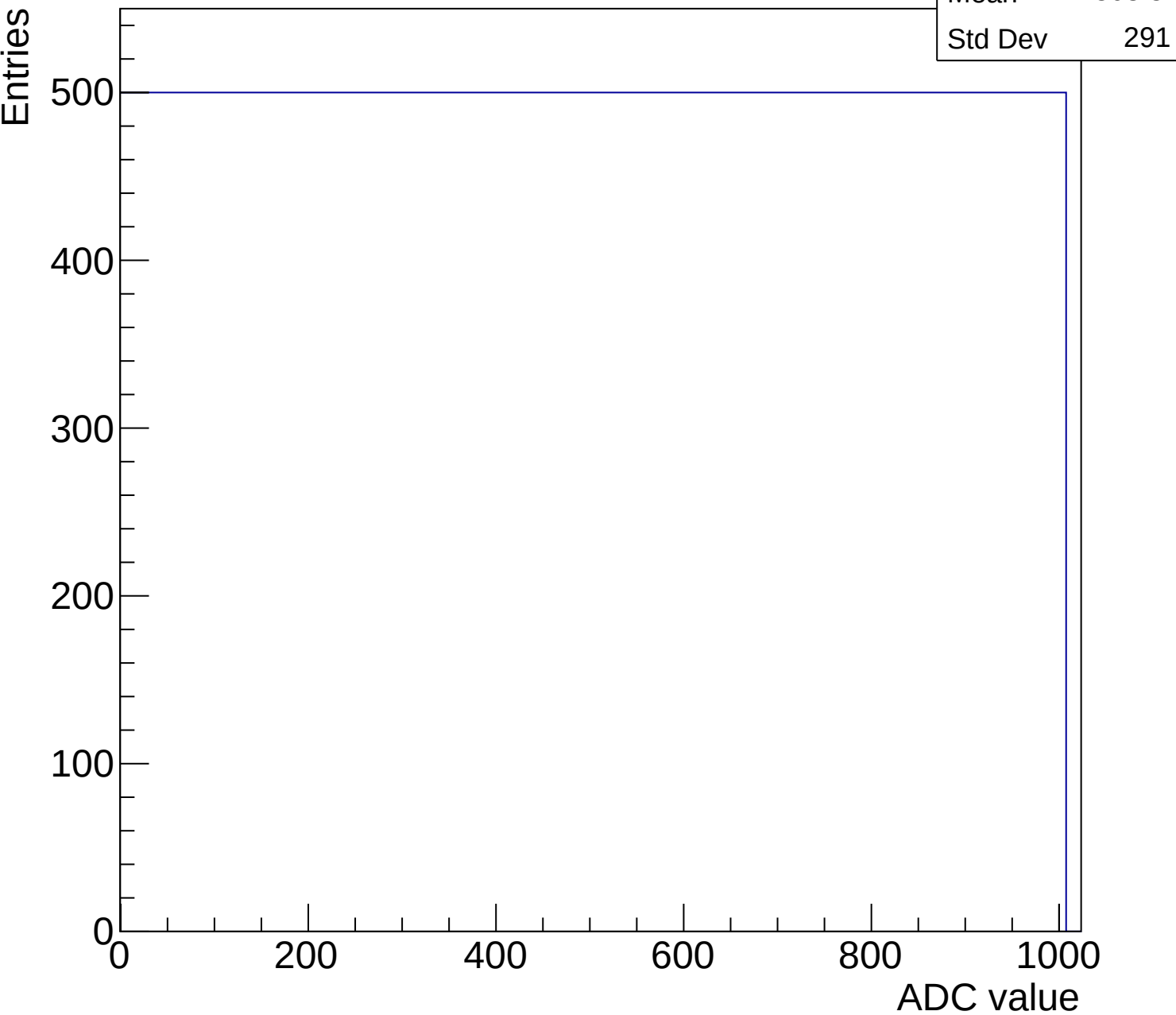
600

800

1000

ADC value

Mean	503.5
Std Dev	291



Ramp saltro:0 chip:0:7 channel 10 pattern1

Entries

500

400

300

200

100

0

0

200

400

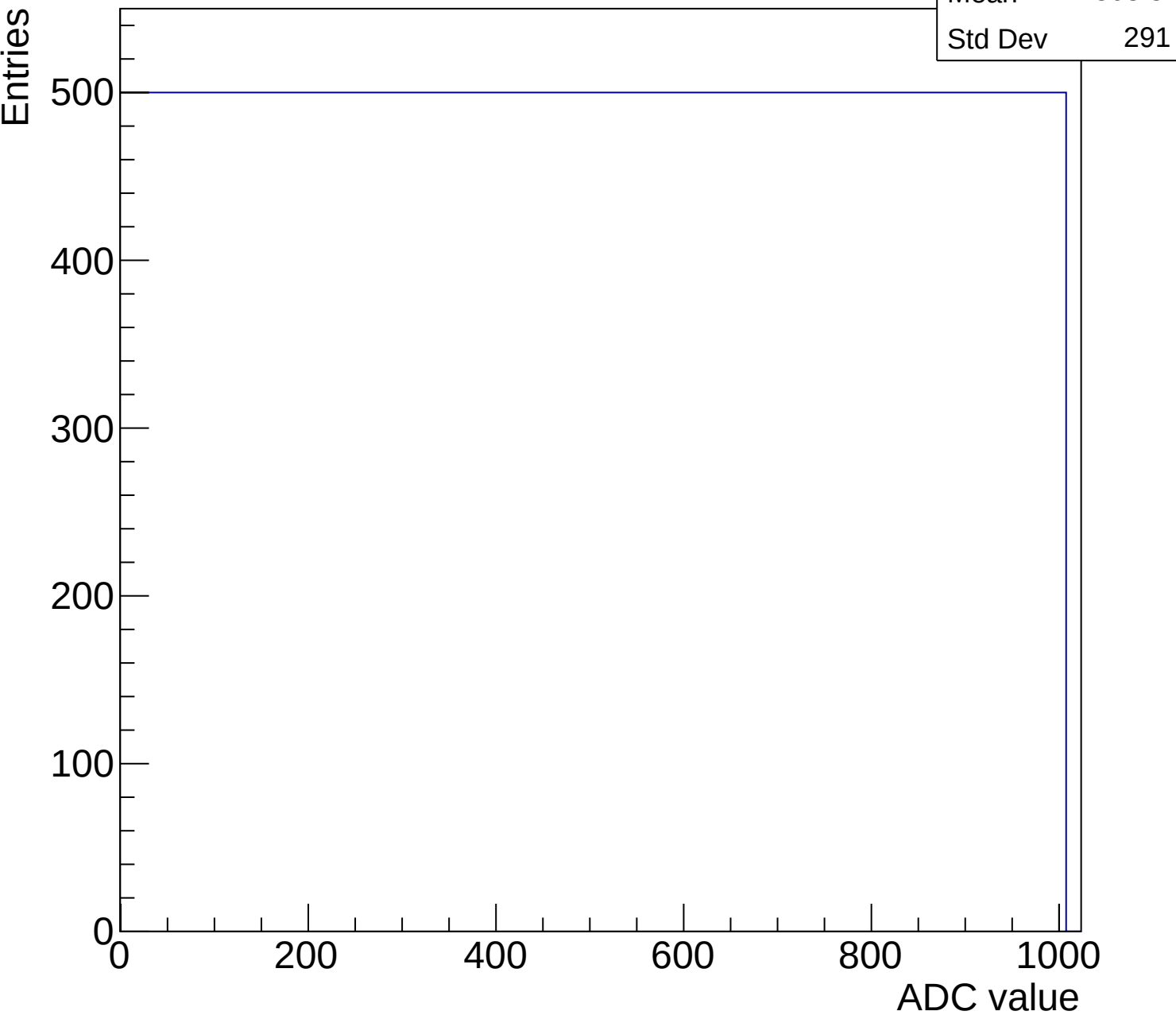
600

800

1000

ADC value

Mean	503.5
Std Dev	291



Ramp saltro:0 chip:0:7 channel 11 pattern1

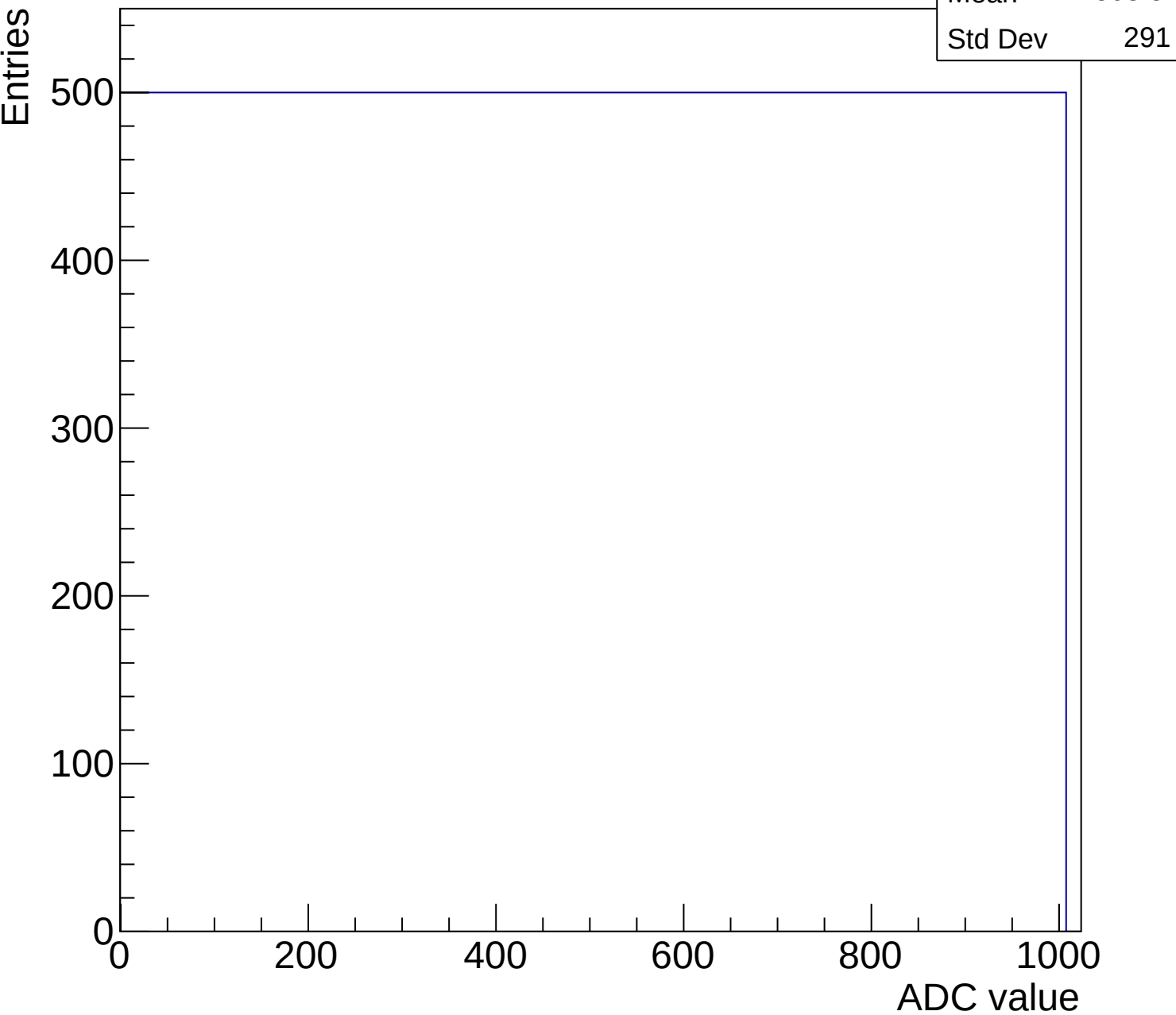
Entries

500
400
300
200
100
0

Mean	503.5
Std Dev	291

ADC value

0 200 400 600 800 1000



Ramp saltro:0 chip:0:7 channel 12 pattern1

Entries

500

400

300

200

100

0

0

200

400

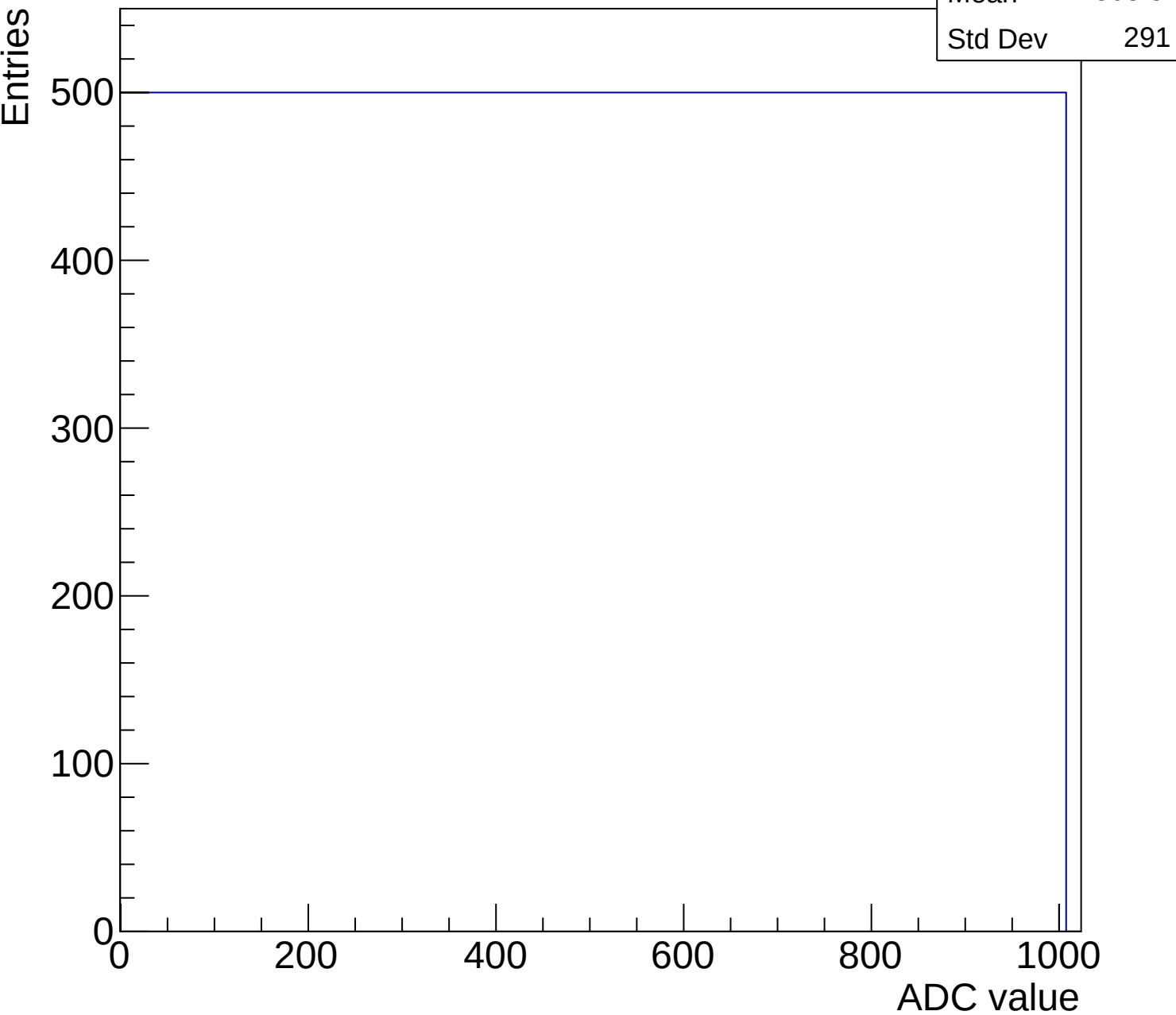
600

800

1000

ADC value

Mean	503.5
Std Dev	291



Ramp saltro:0 chip:0:7 channel 13 pattern1

Entries

500

400

300

200

100

0

0

200

400

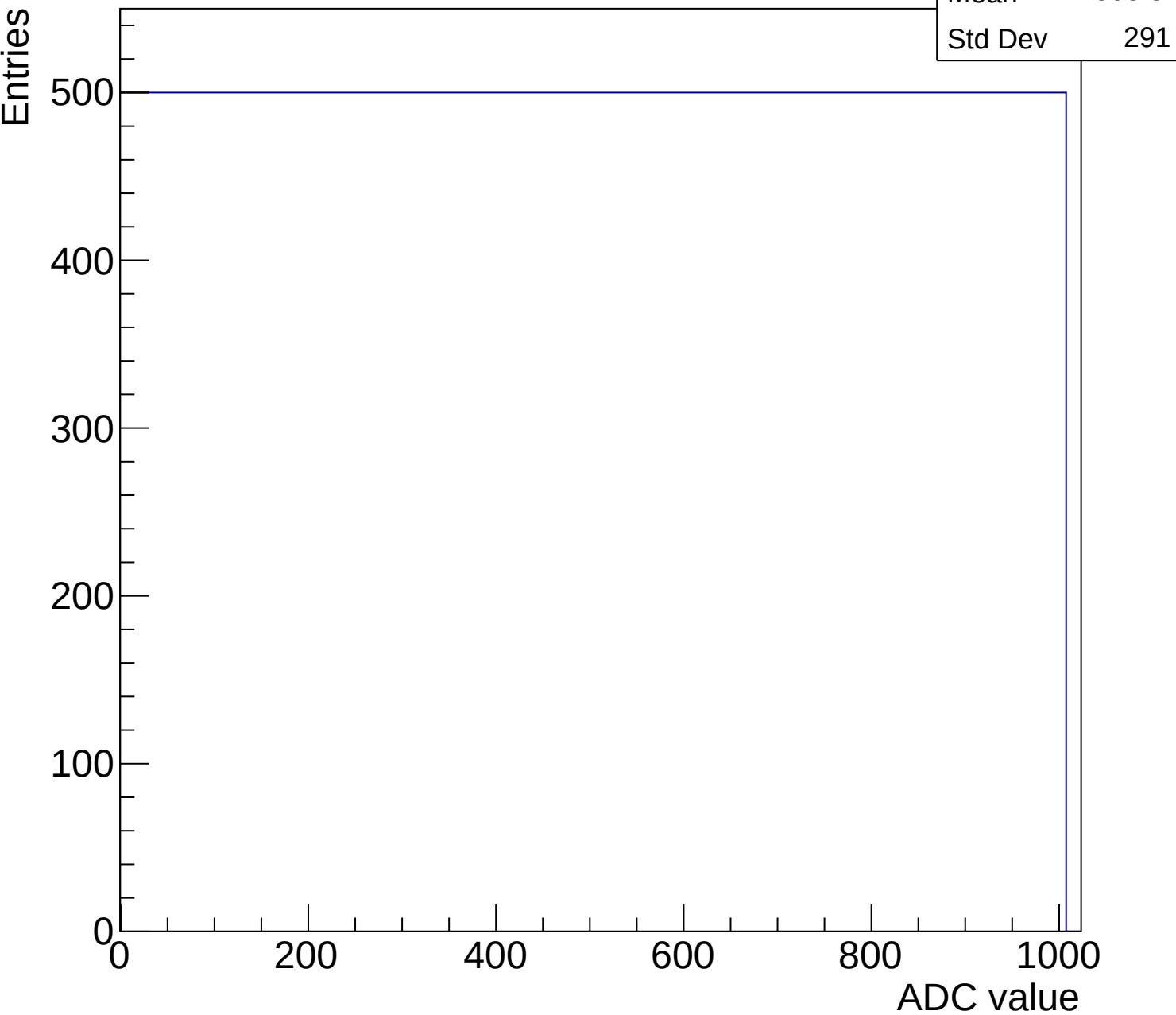
600

800

1000

ADC value

Mean	503.5
Std Dev	291



Ramp saltro:0 chip:0:7 channel 14 pattern1

Entries

500

400

300

200

100

0

0

200

400

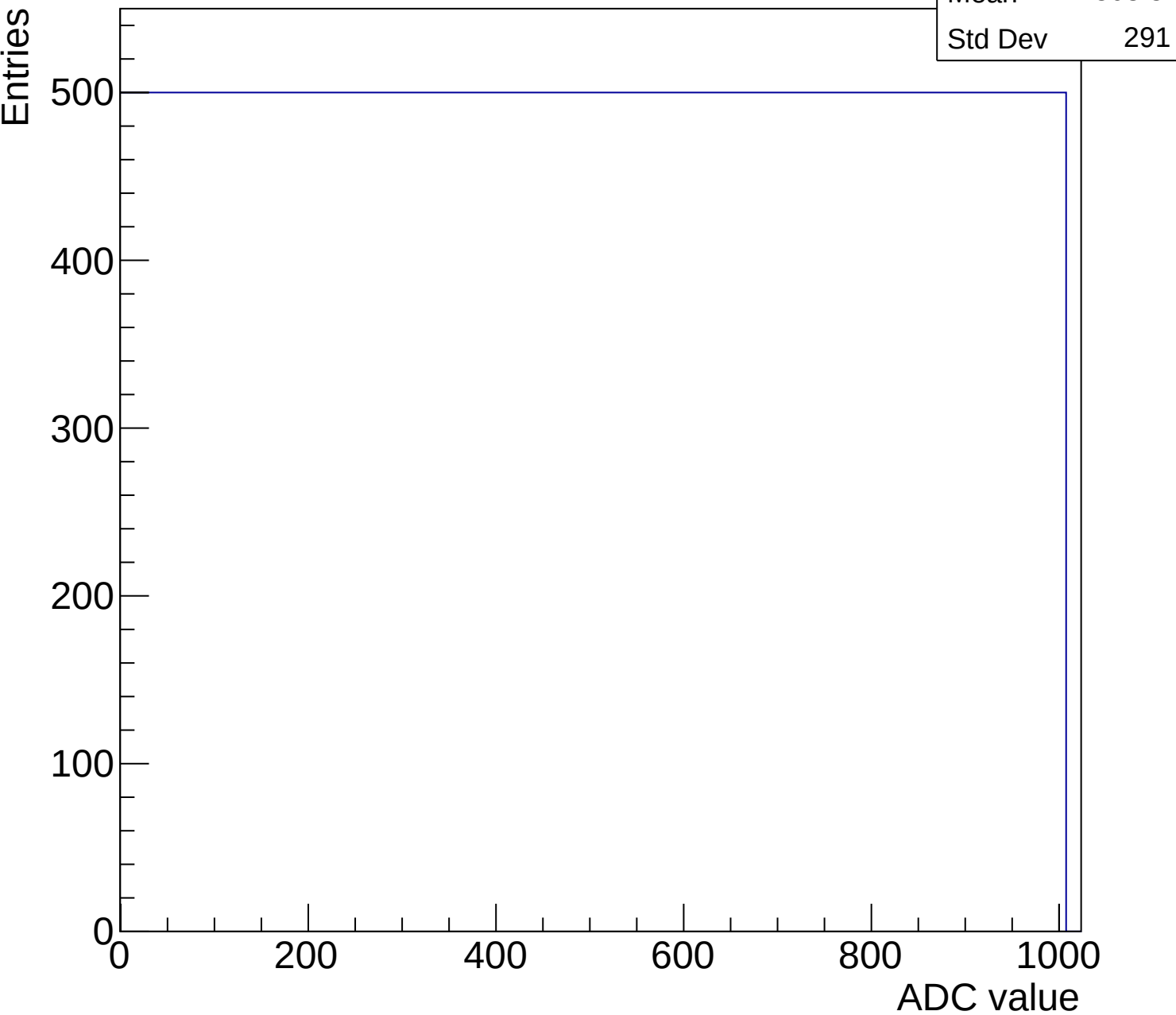
600

800

1000

ADC value

Mean	503.5
Std Dev	291



Ramp saltro:0 chip:0:7 channel 15 pattern1

Entries

500

400

300

200

100

0

0

200

400

600

800

1000

ADC value

Mean	503.5
Std Dev	291

