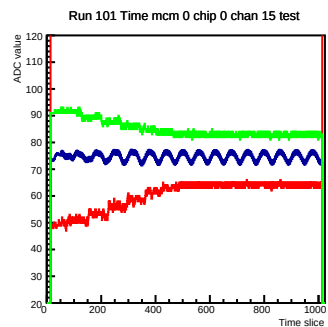
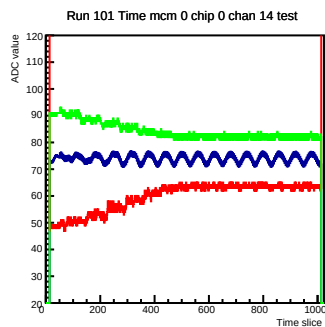
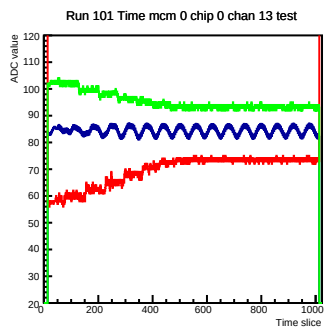
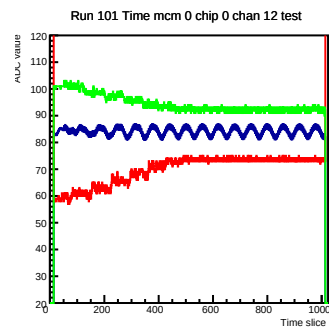
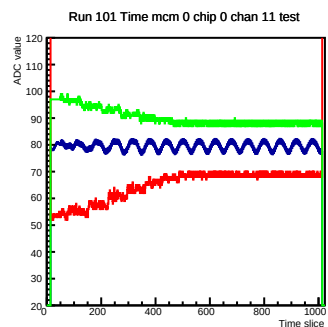
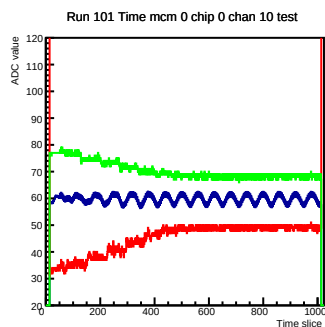
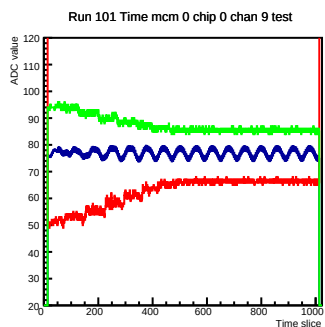
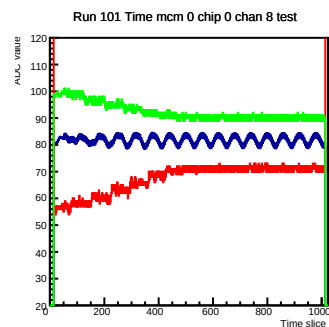
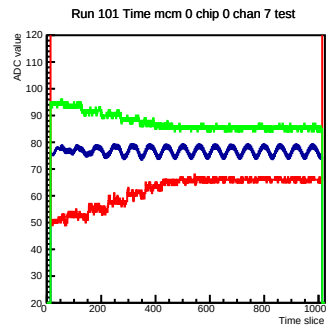
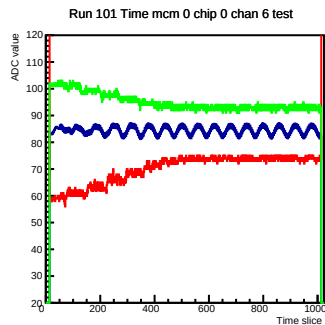
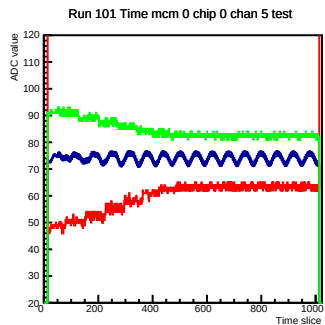
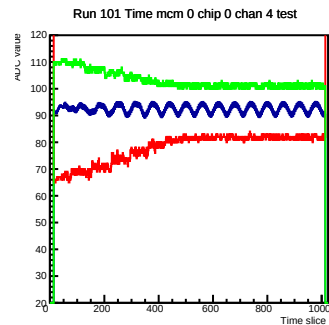
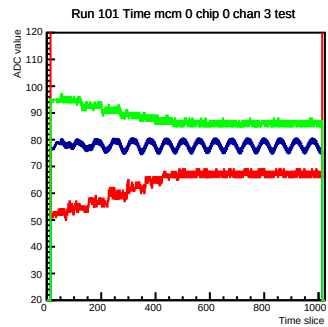
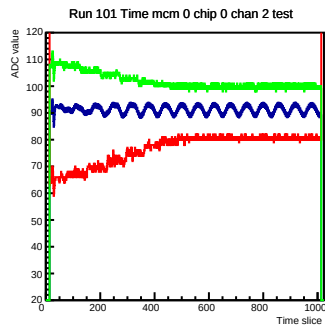
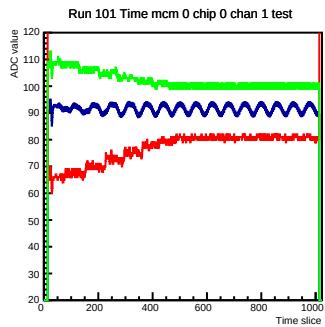
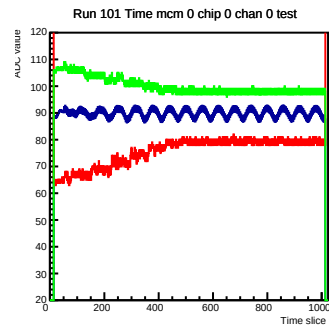
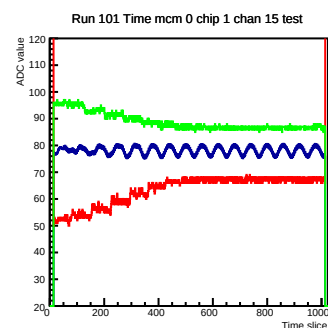
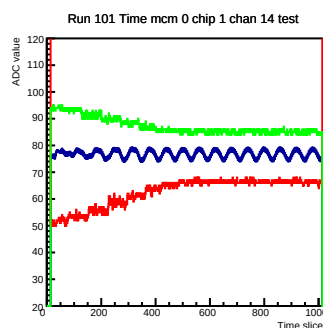
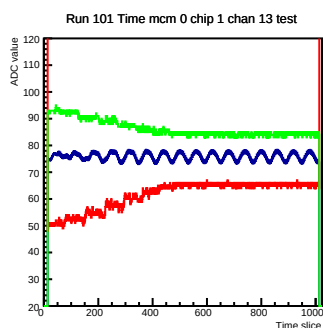
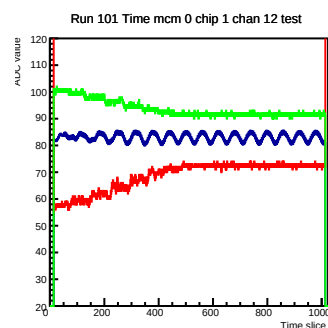
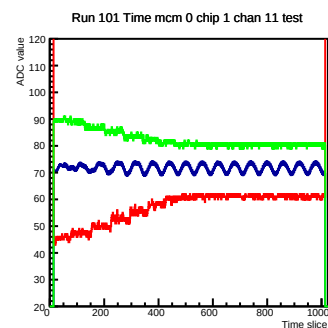
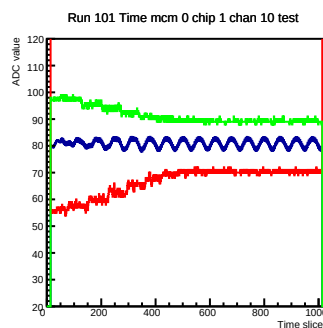
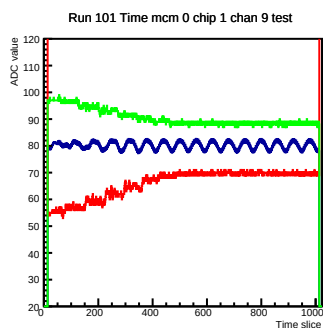
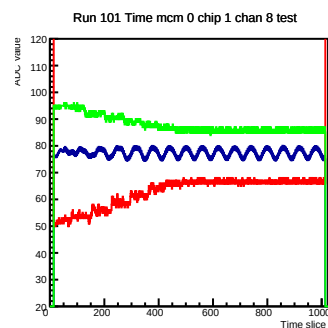
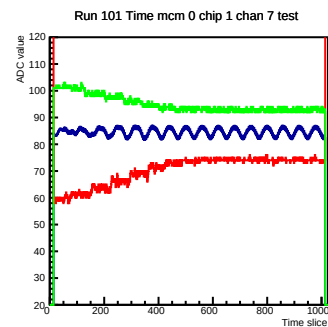
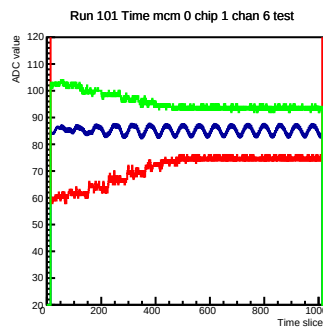
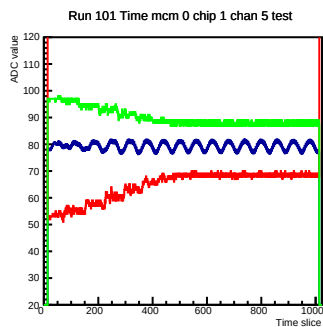
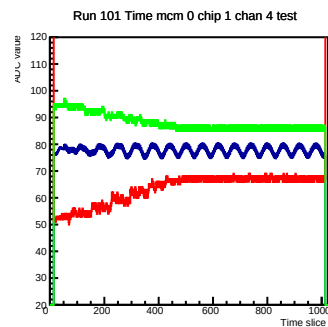
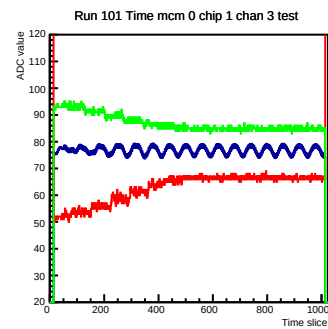
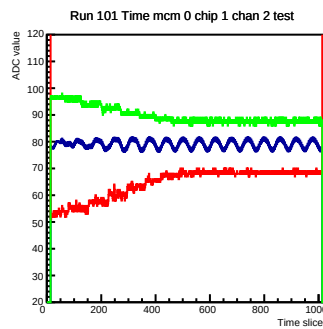
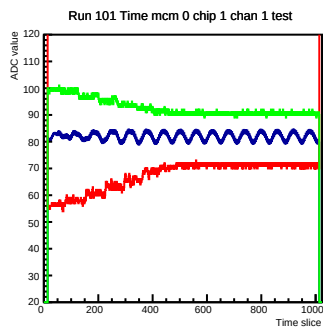
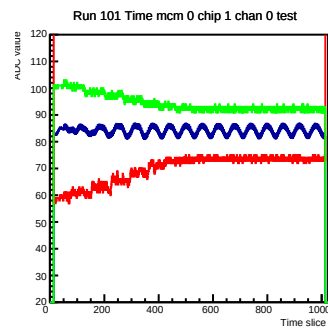
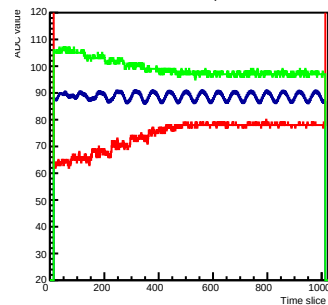


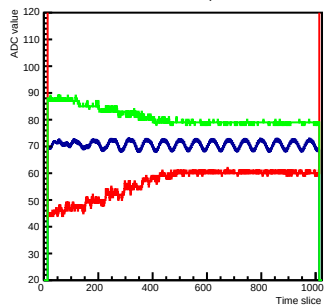




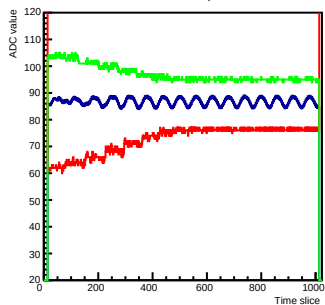
Run 101 Time mcm 0 chip 2 chan 0 test



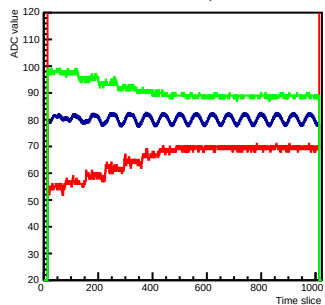
Run 101 Time mcm 0 chip 2 chan 1 test



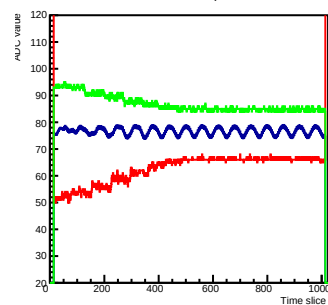
Run 101 Time mcm 0 chip 2 chan 2 test



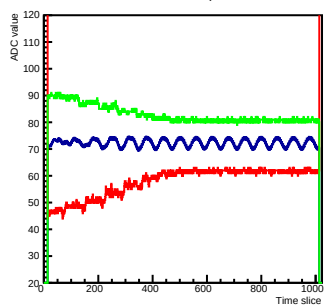
Run 101 Time mcm 0 chip 2 chan 3 test



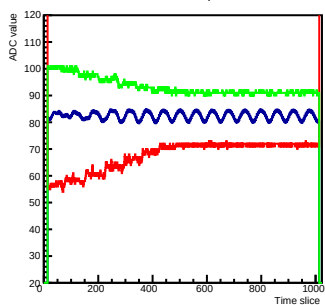
Run 101 Time mcm 0 chip 2 chan 4 test



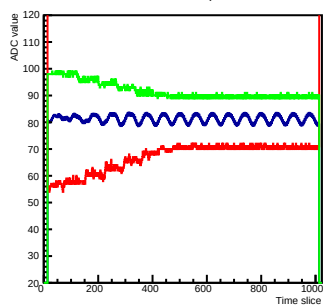
Run 101 Time mcm 0 chip 2 chan 5 test



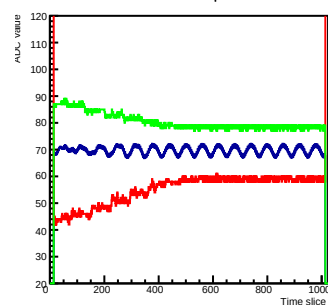
Run 101 Time mcm 0 chip 2 chan 6 test



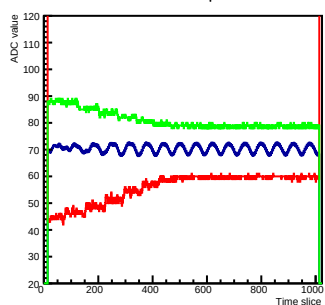
Run 101 Time mcm 0 chip 2 chan 7 test



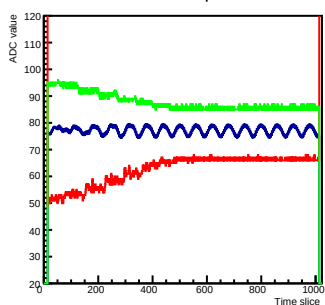
Run 101 Time mcm 0 chip 2 chan 8 test



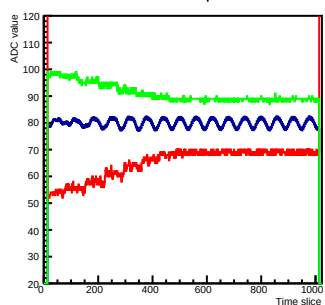
Run 101 Time mcm 0 chip 2 chan 9 test



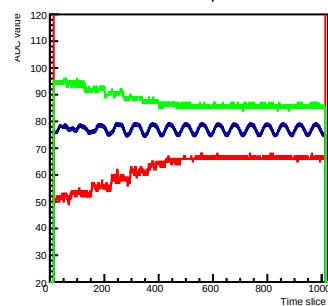
Run 101 Time mcm 0 chip 2 chan 10 tes



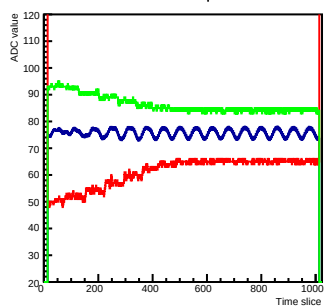
Run 101 Time mcm 0 chip 2 chan 11 tes



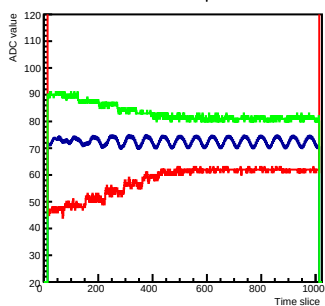
Run 101 Time mcm 0 chip 2 chan 12 tes



Run 101 Time mcm 0 chip 2 chan 13 tes



Run 101 Time mcm 0 chip 2 chan 14 tes



Run 101 Time mcm 0 chip 2 chan 15 tes

