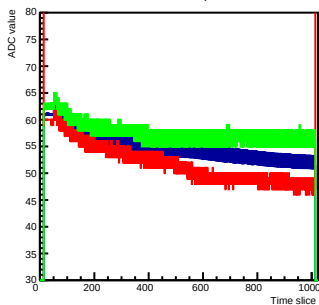
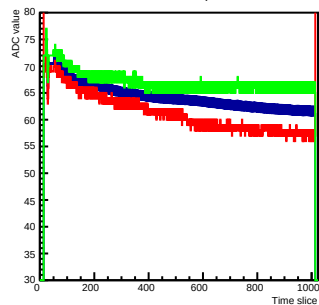


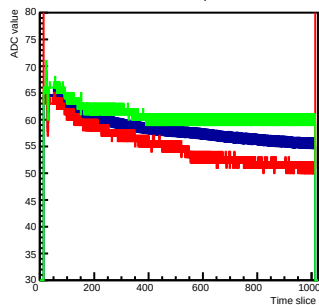
Run 110 Time mcm 0 chip 0 chan 0 test



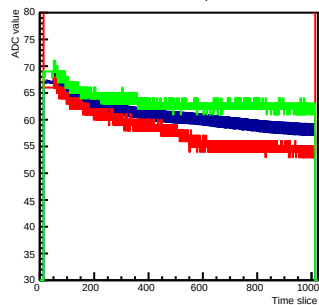
Run 110 Time mcm 0 chip 0 chan 1 test



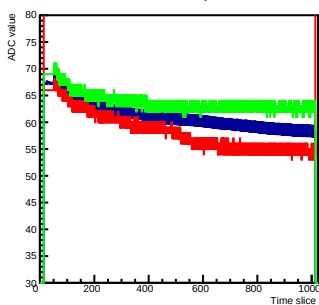
Run 110 Time mcm 0 chip 0 chan 2 test



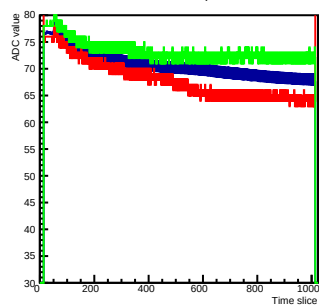
Run 110 Time mcm 0 chip 0 chan 3 test



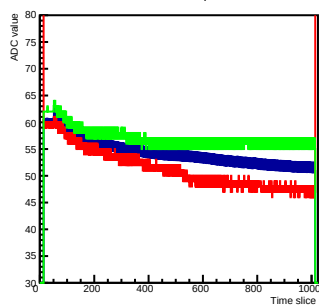
Run 110 Time mcm 0 chip 0 chan 4 test



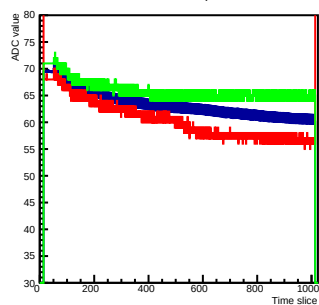
Run 110 Time mcm 0 chip 0 chan 5 test



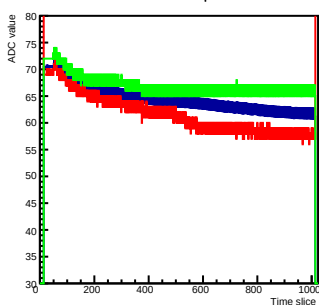
Run 110 Time mcm 0 chip 0 chan 6 test



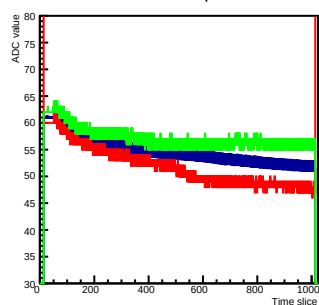
Run 110 Time mcm 0 chip 0 chan 7 test



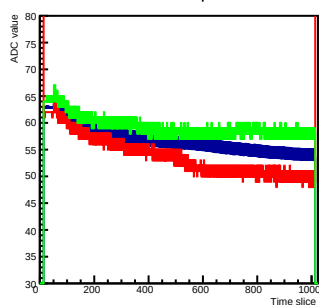
Run 110 Time mcm 0 chip 0 chan 8 test



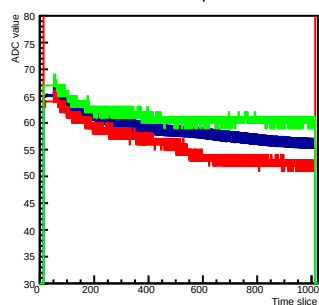
Run 110 Time mcm 0 chip 0 chan 9 test



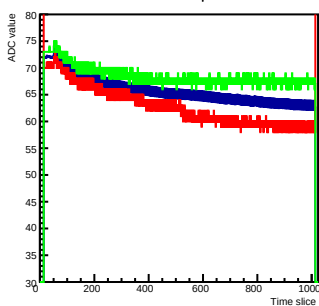
Run 110 Time mcm 0 chip 0 chan 10 tes



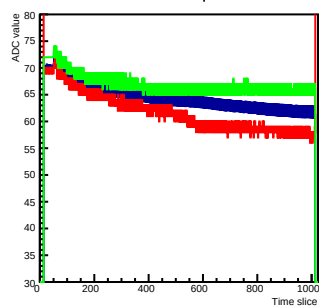
Run 110 Time mcm 0 chip 0 chan 11 tes



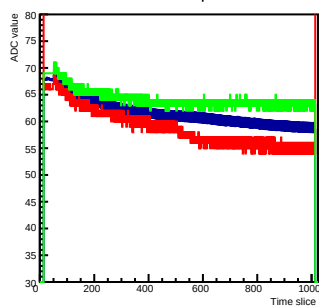
Run 110 Time mcm 0 chip 0 chan 12 test



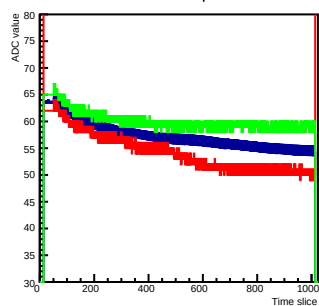
Run 110 Time mcm 0 chip 0 chan 13 test

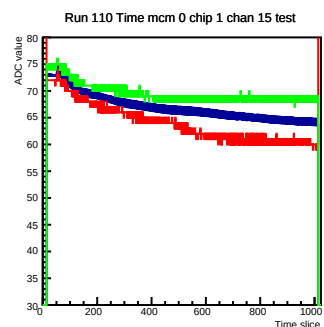
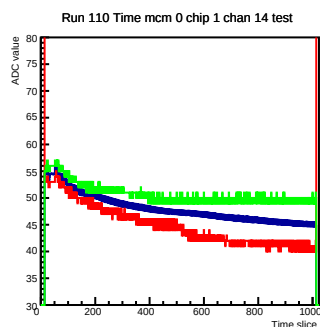
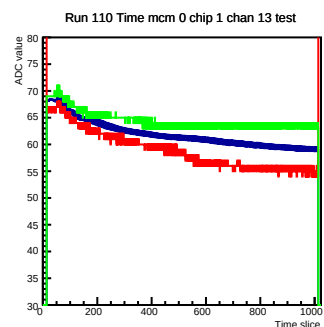
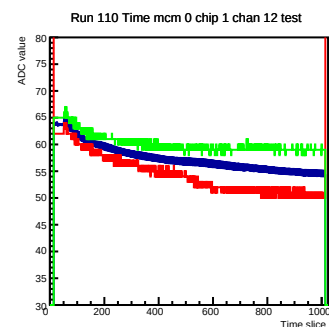
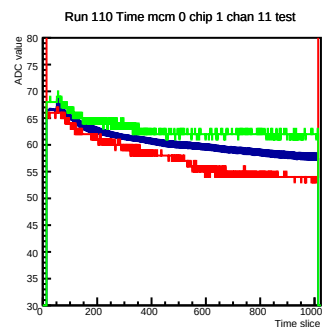
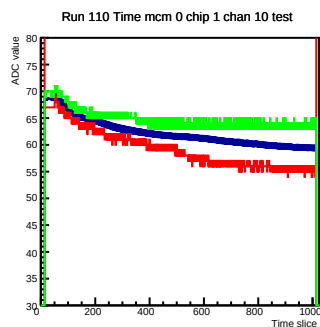
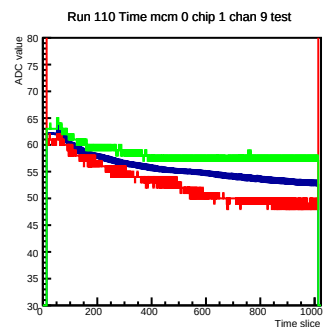
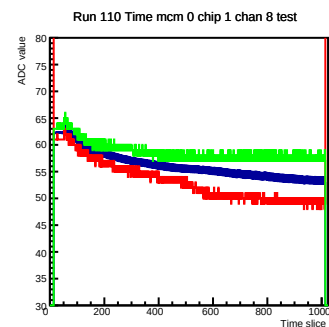
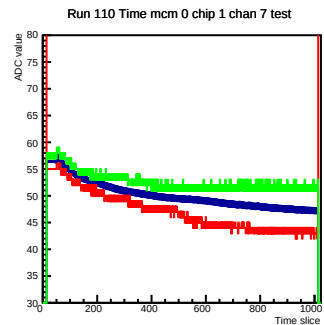
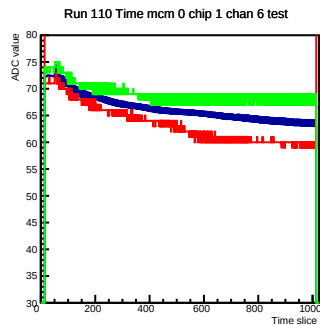
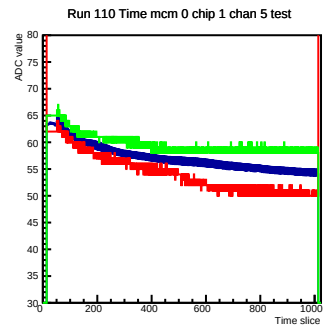
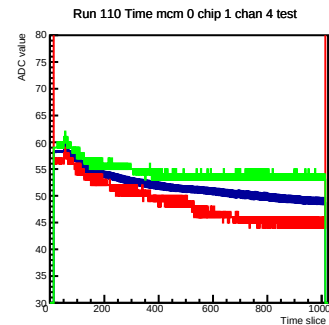
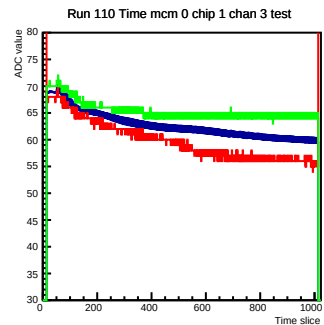
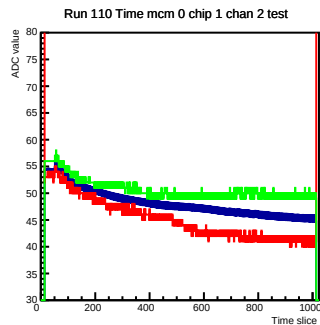
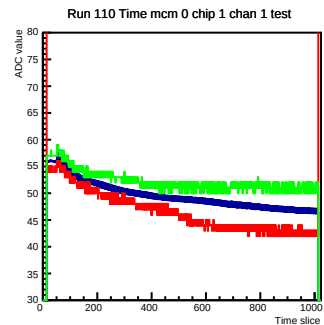
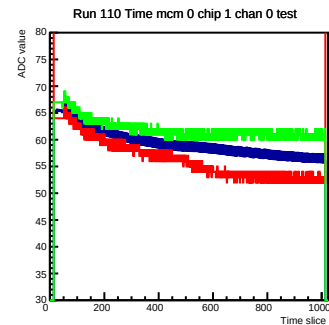


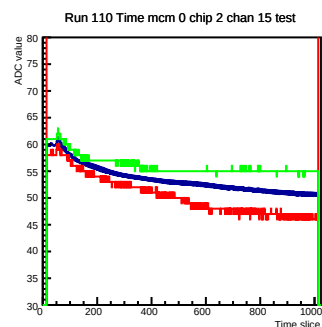
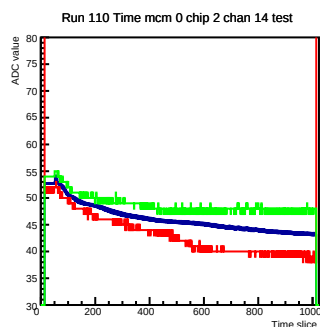
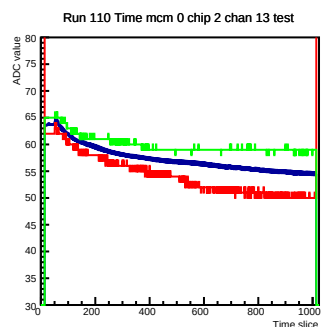
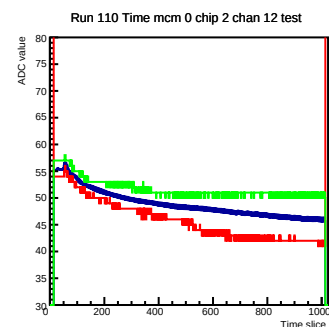
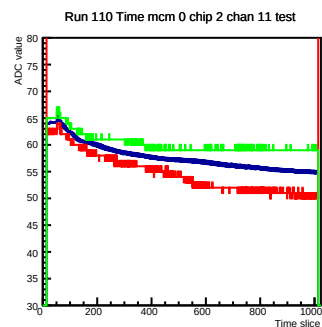
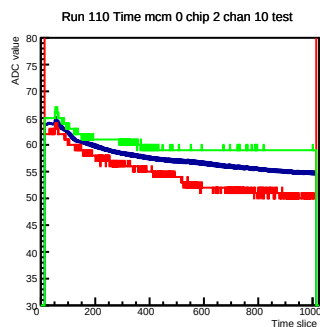
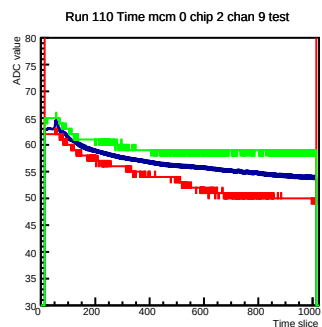
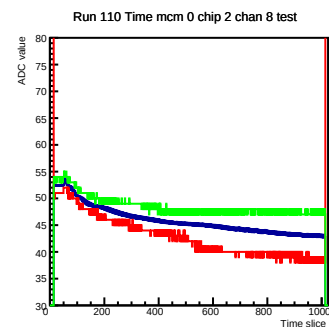
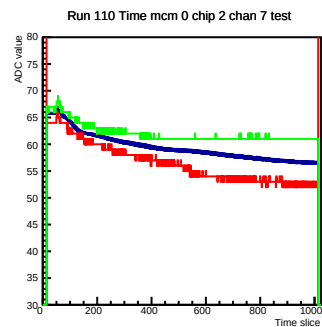
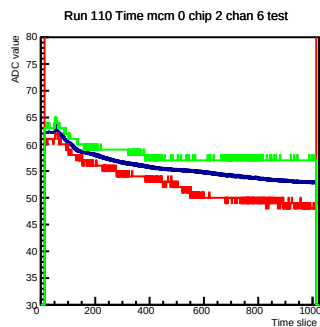
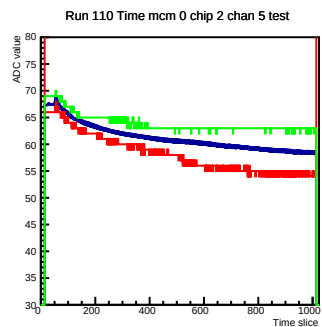
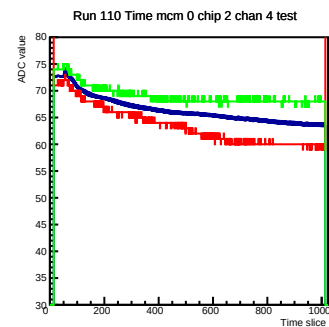
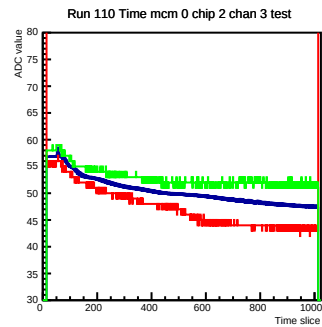
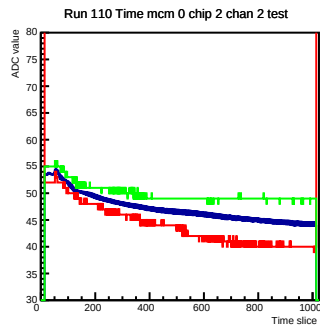
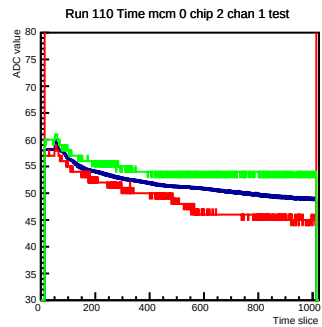
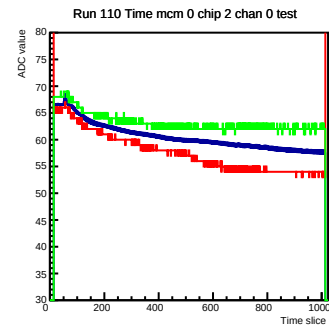
Run 110 Time mcm 0 chip 0 chan 14 tes

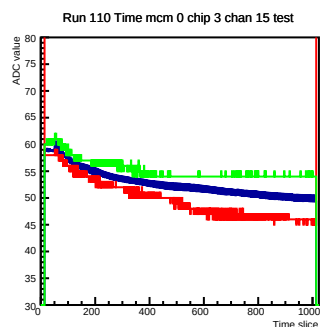
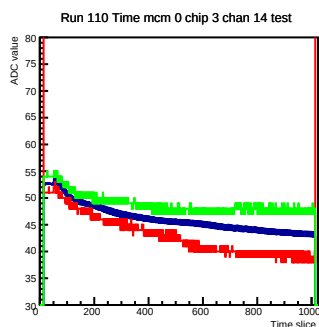
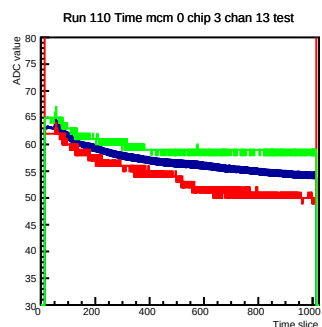
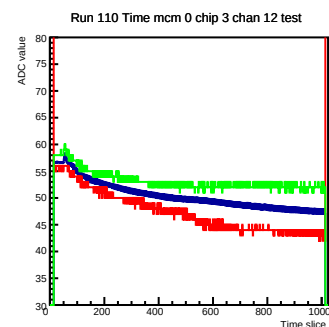
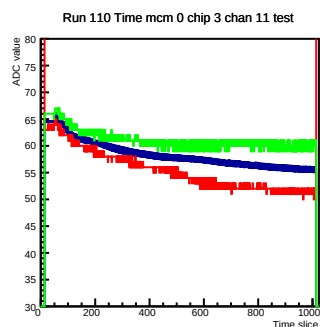
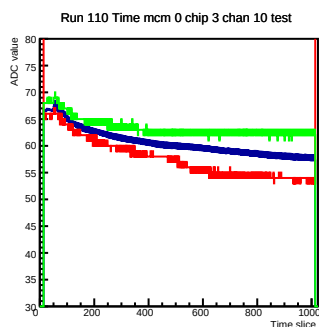
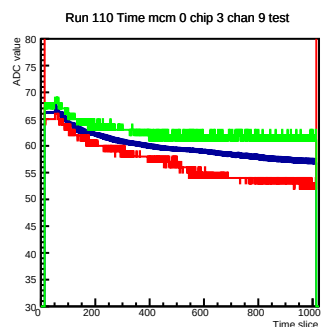
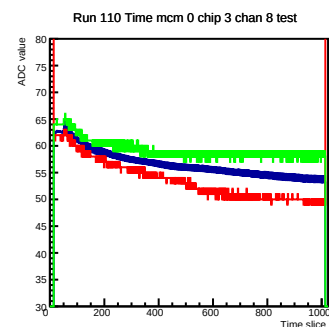
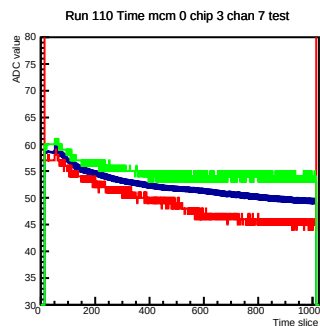
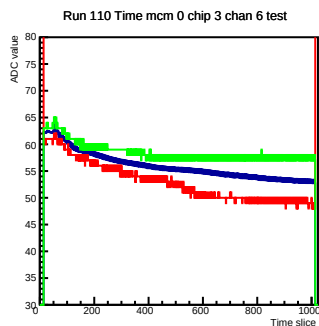
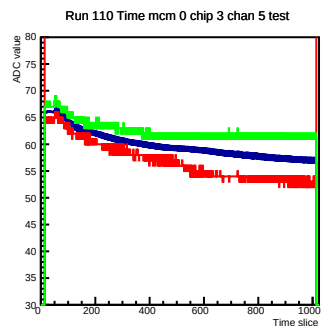
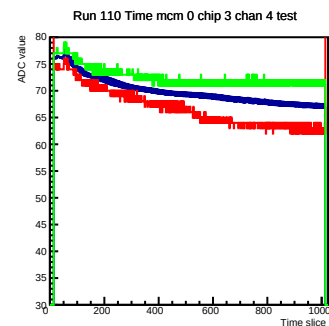
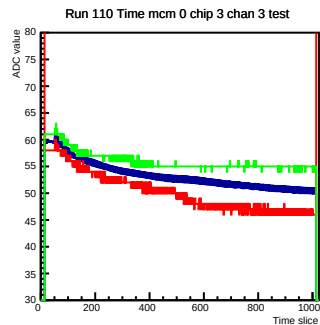
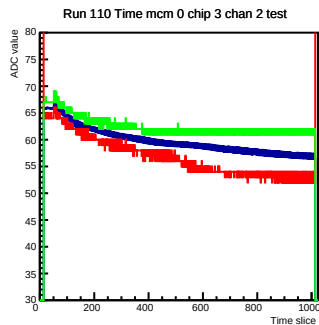
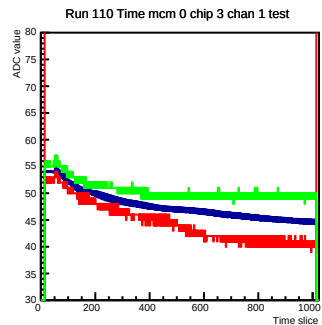
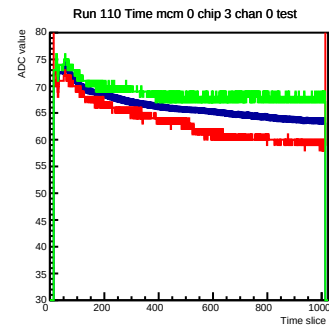


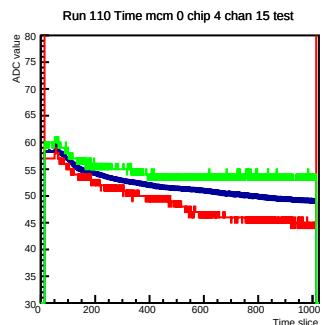
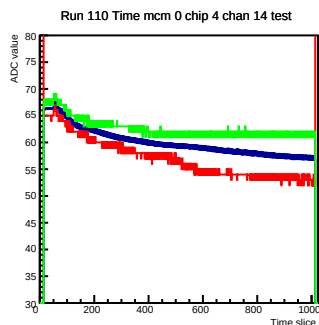
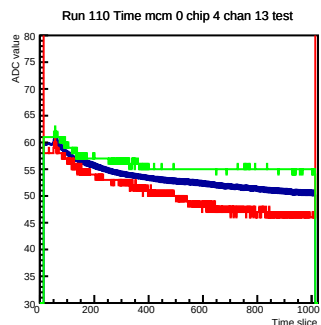
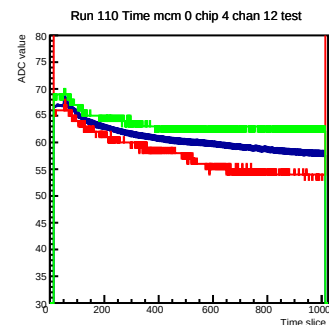
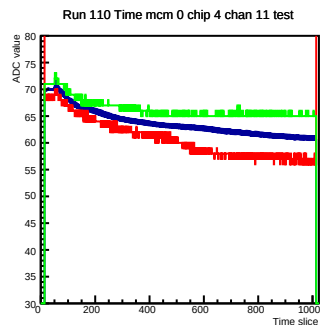
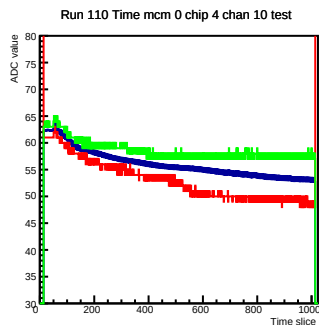
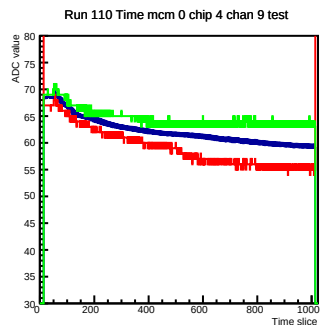
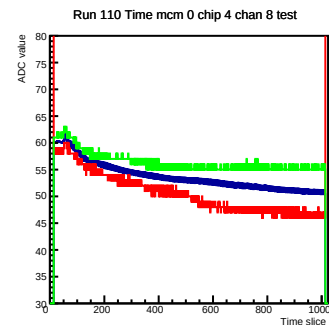
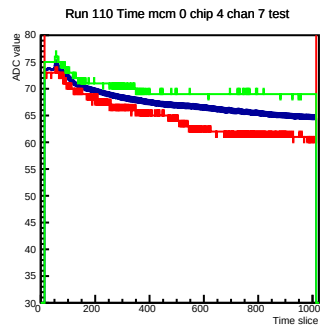
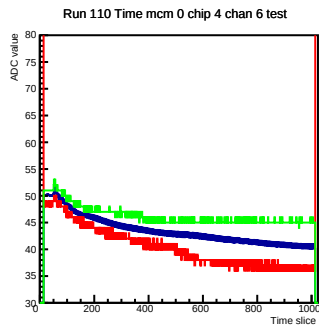
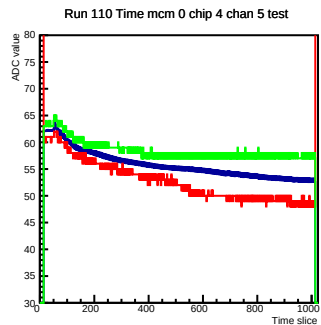
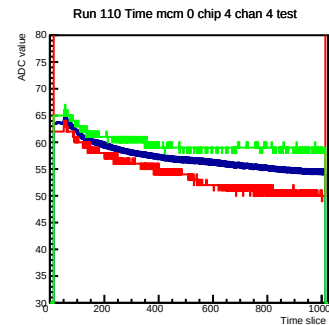
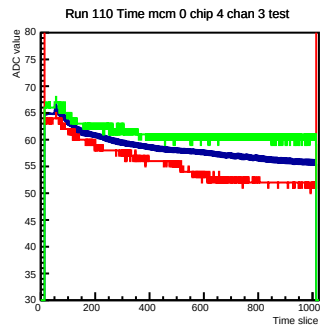
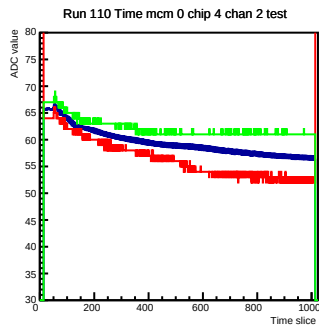
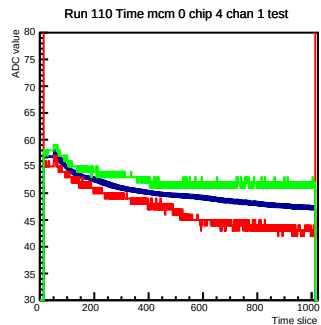
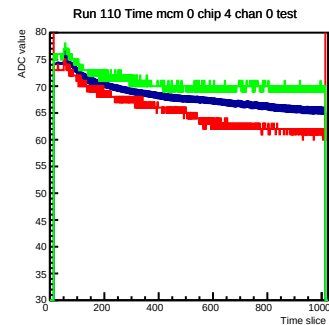
Run 110 Time mcm 0 chip 0 chan 15 tes

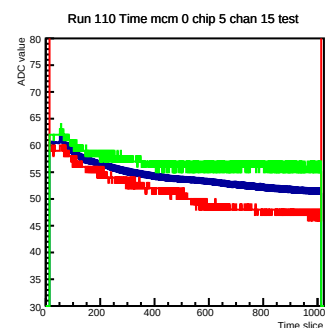
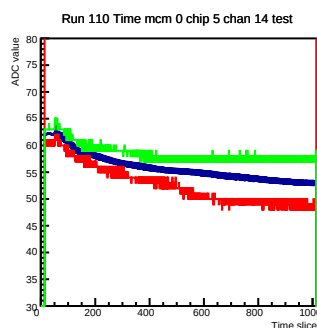
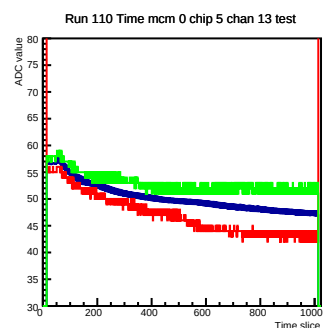
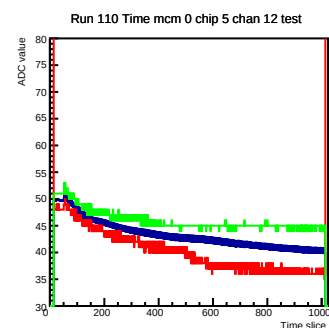
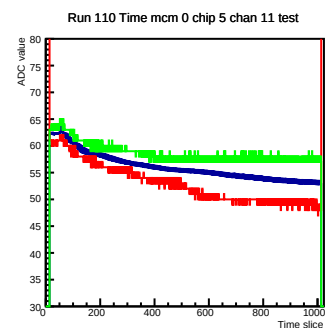
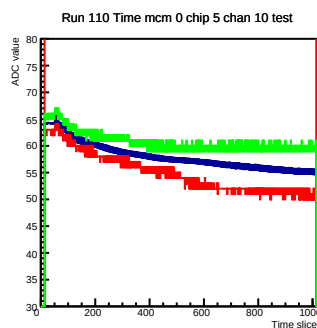
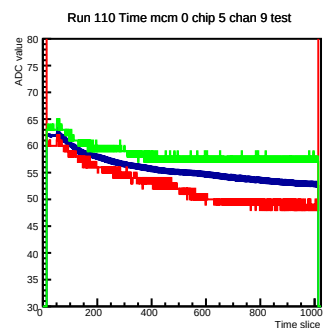
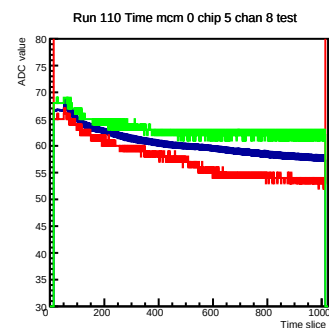
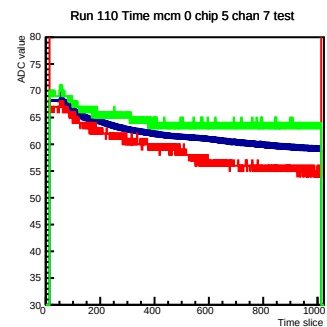
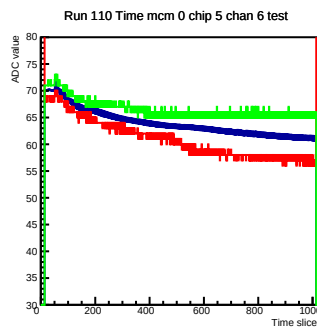
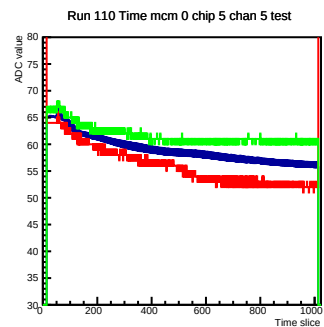
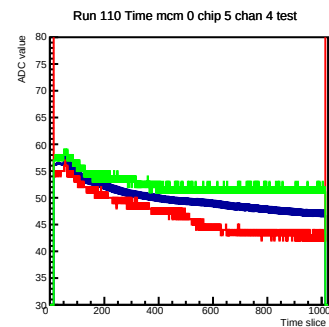
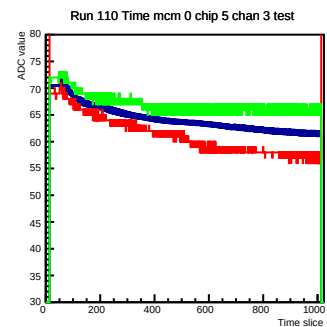
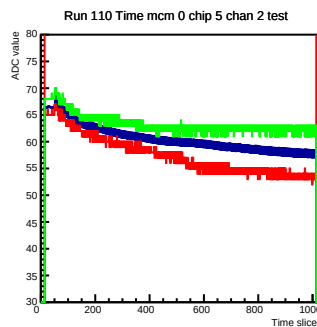
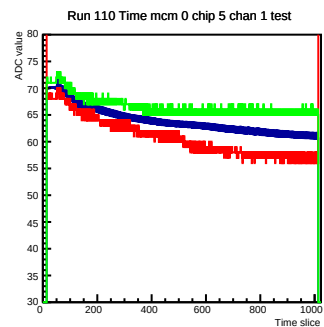
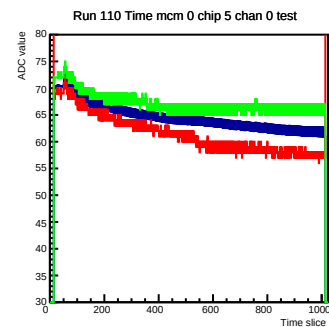


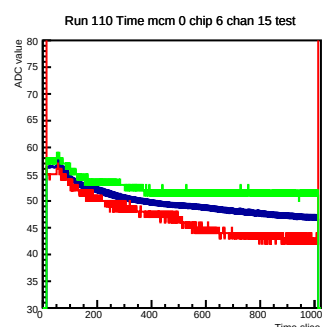
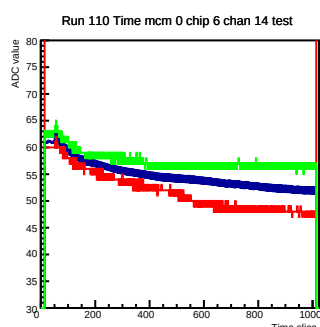
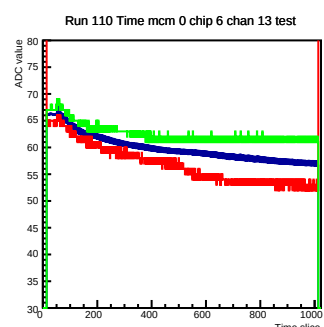
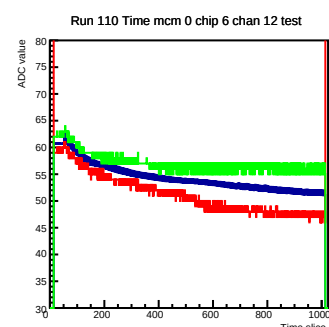
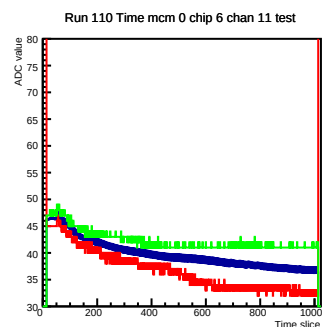
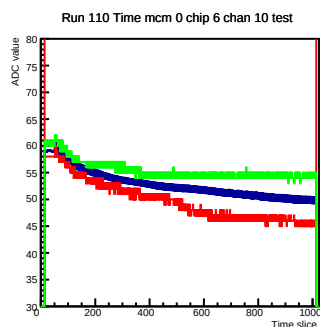
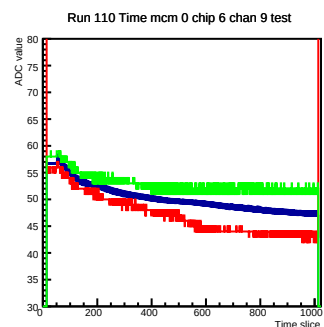
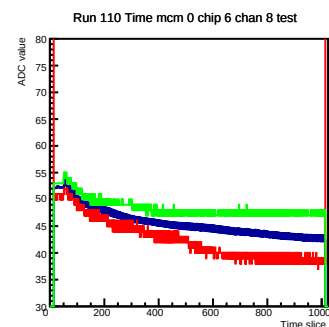
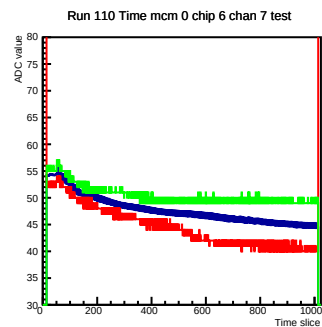
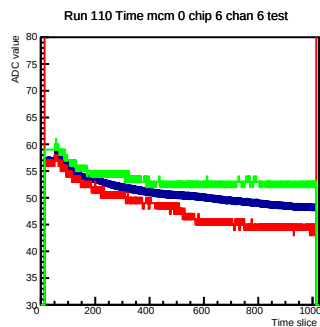
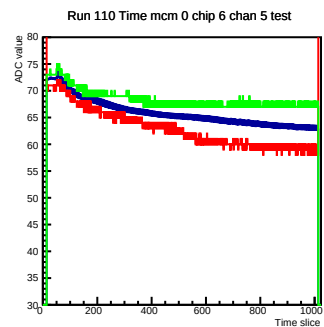
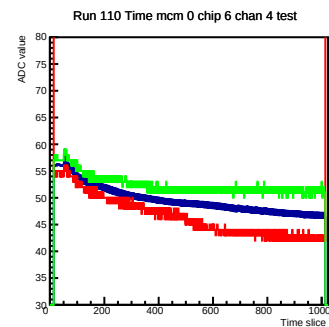
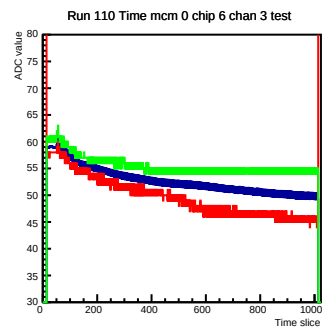
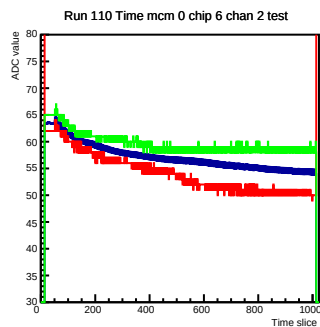
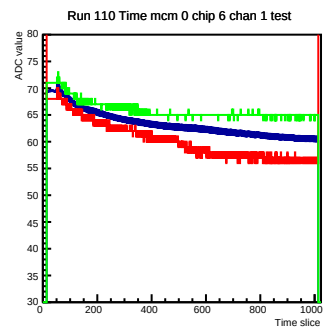
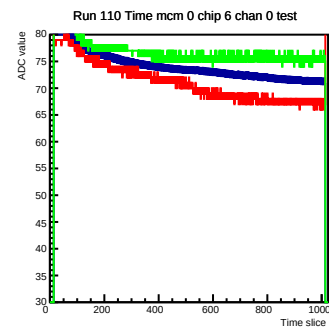




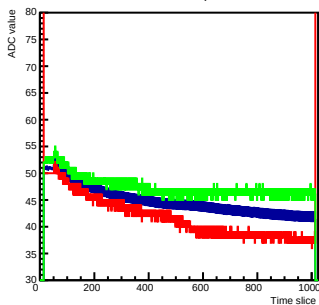




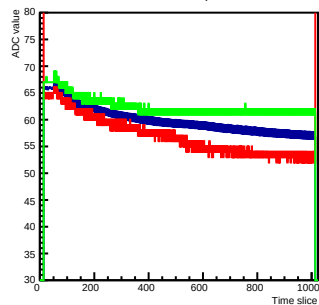




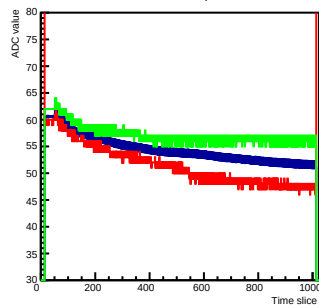
Run 110 Time mcm 0 chip 7 chan 0 test



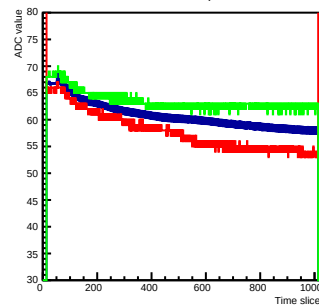
Run 110 Time mcm 0 chip 7 chan 1 test



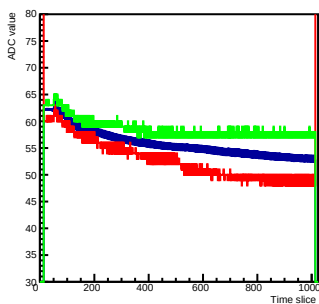
Run 110 Time mcm 0 chip 7 chan 2 test



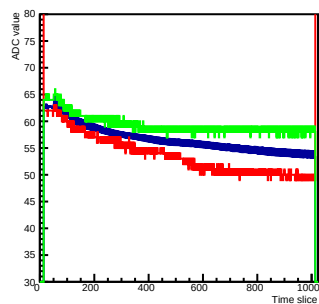
Run 110 Time mcm 0 chip 7 chan 3 test



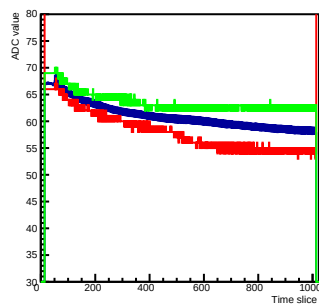
Run 110 Time mcm 0 chip 7 chan 4 test



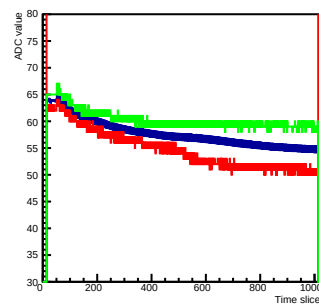
Run 110 Time mcm 0 chip 7 chan 5 test



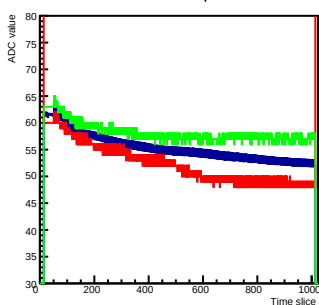
Run 110 Time mcm 0 chip 7 chan 6 test



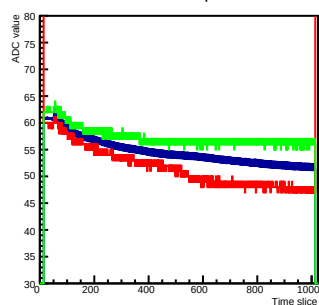
Run 110 Time mcm 0 chip 7 chan 7 test



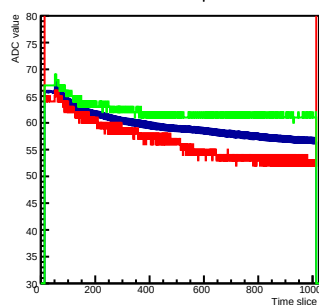
Run 110 Time mcm 0 chip 7 chan 8 test



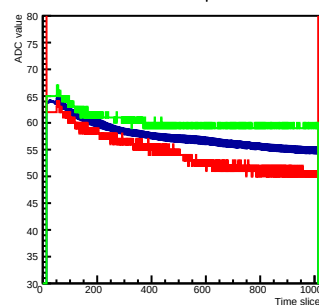
Run 110 Time mcm 0 chip 7 chan 9 test



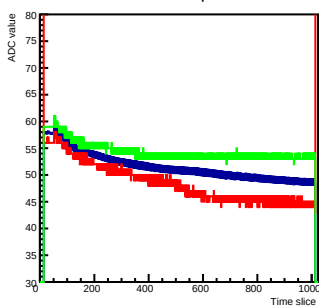
Run 110 Time mcm 0 chip 7 chan 10 tes



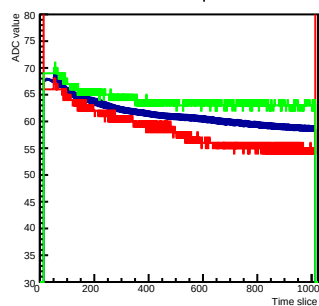
Run 110 Time mcm 0 chip 7 chan 11 tes



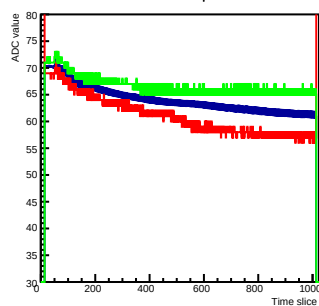
Run 110 Time mcm 0 chip 7 chan 12 test



Run 110 Time mcm 0 chip 7 chan 13 test



Run 110 Time mcm 0 chip 7 chan 14 tes



Run 110 Time mcm 0 chip 7 chan 15 tes

