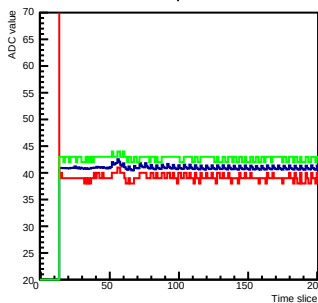
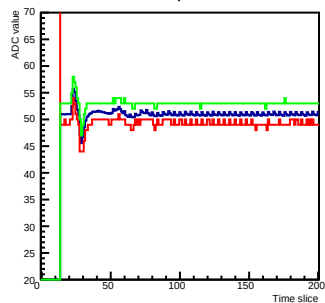


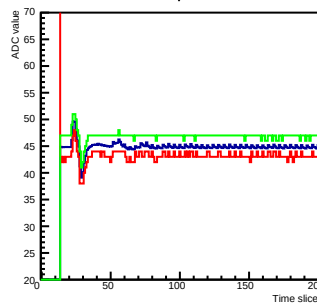
Time mcm 0 chip 0 chan 0 s200



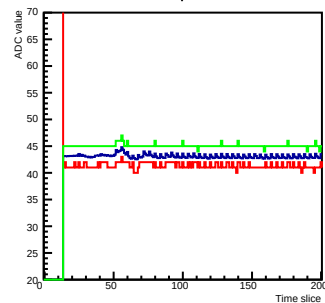
Time mcm 0 chip 0 chan 1 s200



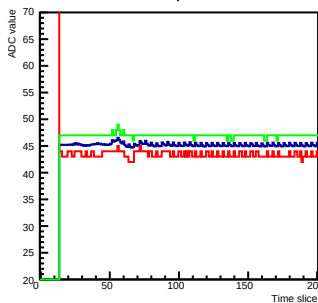
Time mcm 0 chip 0 chan 2 s200



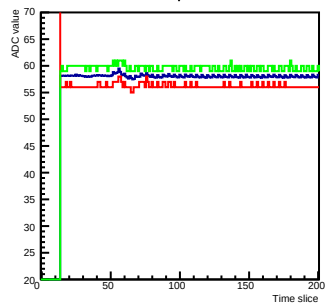
Time mcm 0 chip 0 chan 3 s200



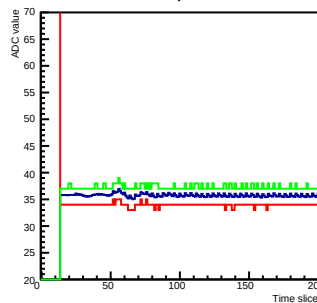
Time mcm 0 chip 0 chan 4 s200



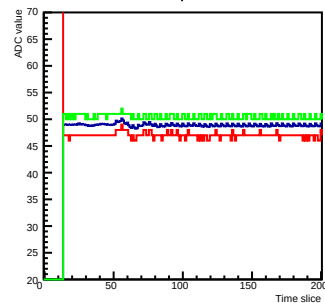
Time mcm 0 chip 0 chan 5 s200



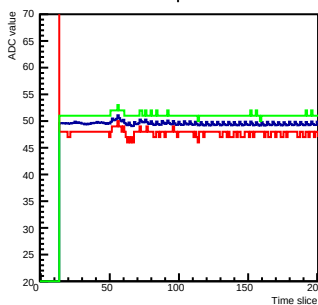
Time mcm 0 chip 0 chan 6 s200



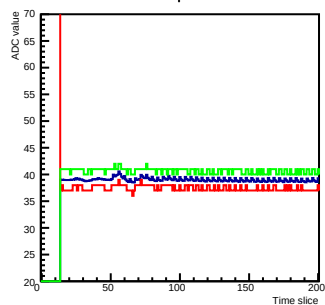
Time mcm 0 chip 0 chan 7 s200



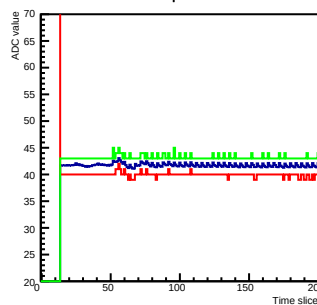
Time mcm 0 chip 0 chan 8 s200



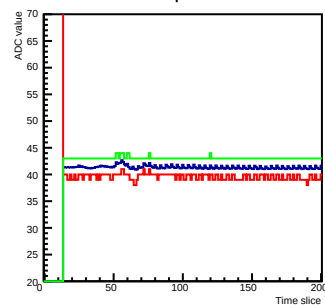
Time mcm 0 chip 0 chan 9 s200



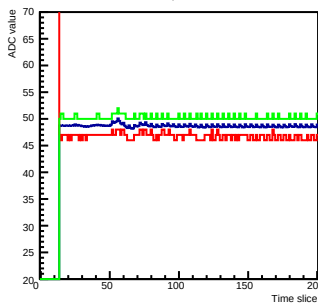
Time mcm 0 chip 0 chan 10 s200



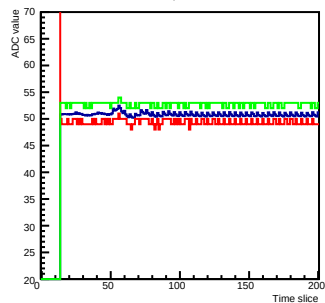
Time mcm 0 chip 0 chan 11 s200



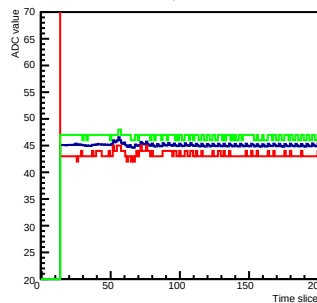
Time mcm 0 chip 0 chan 12 s200



Time mcm 0 chip 0 chan 13 s200



Time mcm 0 chip 0 chan 14 s200



Time mcm 0 chip 0 chan 15 s200

