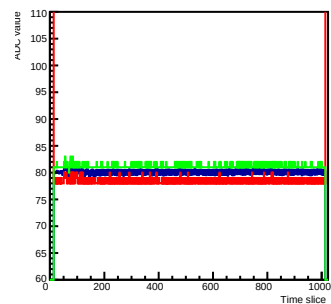
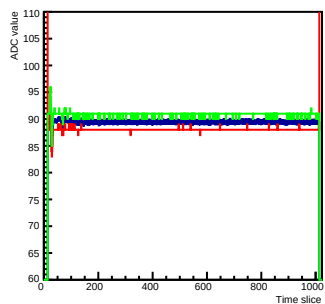


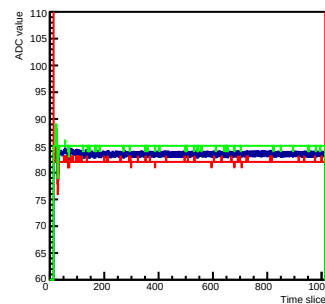
Run 0 Time mcm 0 chip 0 chan 0 test



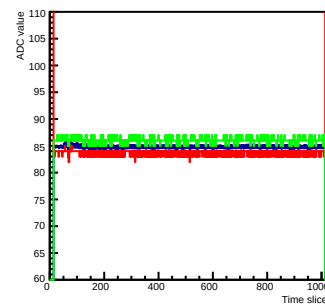
Run 0 Time mcm 0 chip 0 chan 1 test



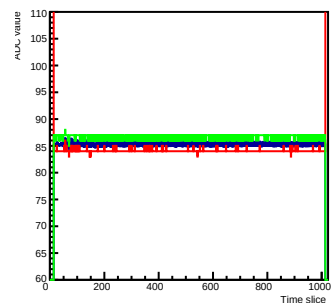
Run 0 Time mcm 0 chip 0 chan 2 test



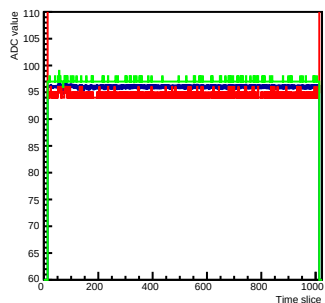
Run 0 Time mcm 0 chip 0 chan 3 test



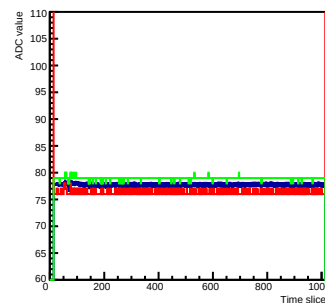
Run 0 Time mcm 0 chip 0 chan 4 test



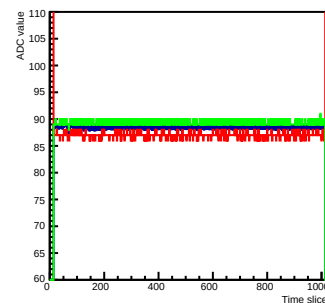
Run 0 Time mcm 0 chip 0 chan 5 test



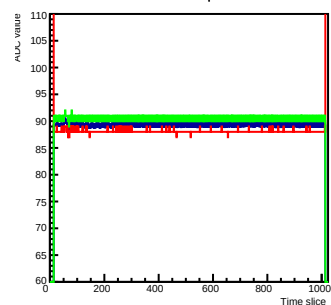
Run 0 Time mcm 0 chip 0 chan 6 test



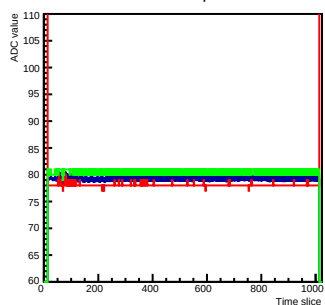
Run 0 Time mcm 0 chip 0 chan 7 test



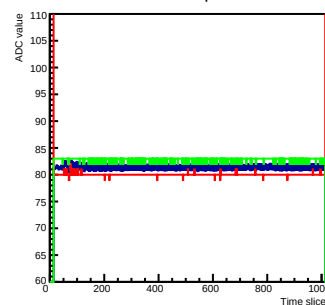
Run 0 Time mcm 0 chip 0 chan 8 test



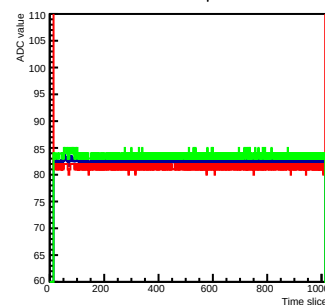
Run 0 Time mcm 0 chip 0 chan 9 test



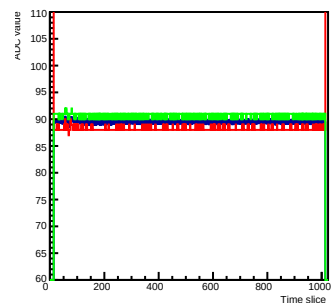
Run 0 Time mcm 0 chip 0 chan 10 test



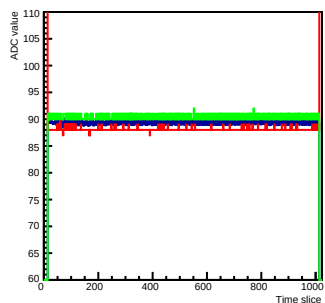
Run 0 Time mcm 0 chip 0 chan 11 test



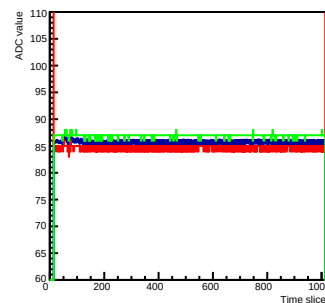
Run 0 Time mcm 0 chip 0 chan 12 test



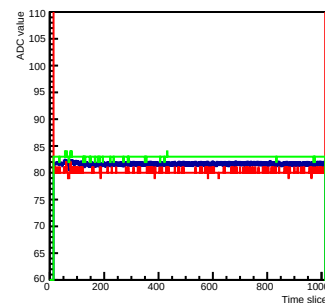
Run 0 Time mcm 0 chip 0 chan 13 test

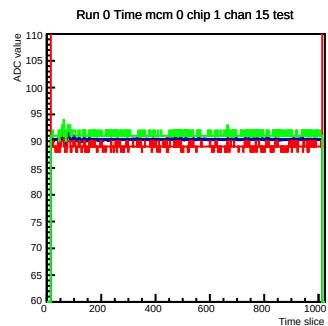
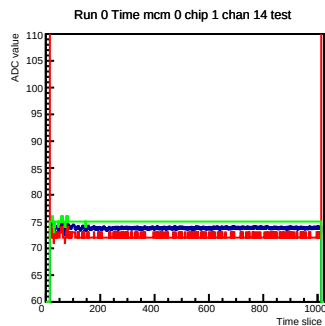
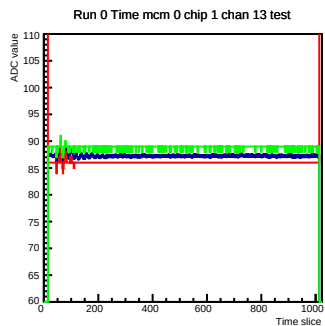
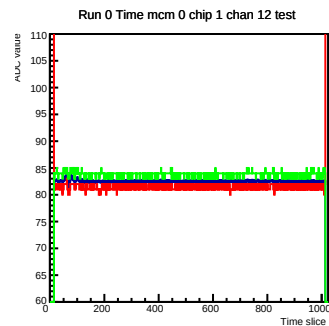
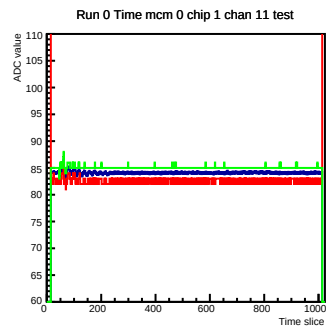
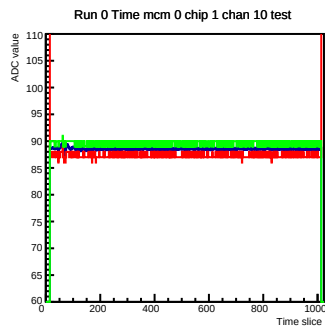
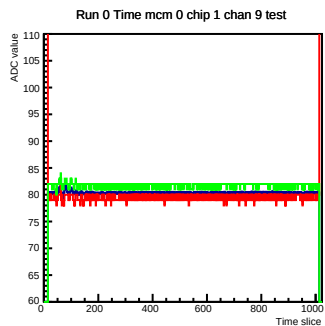
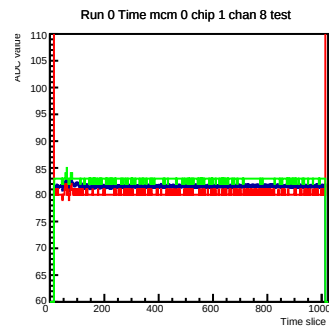
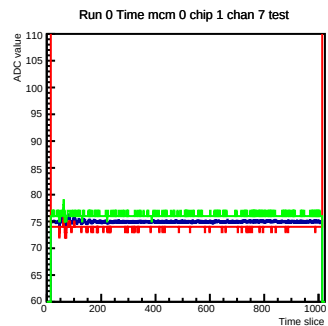
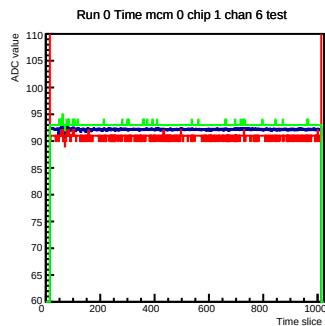
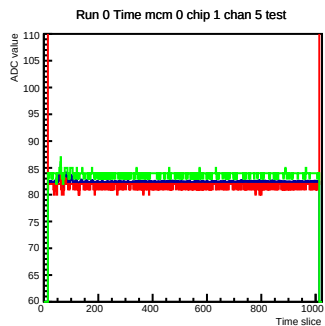
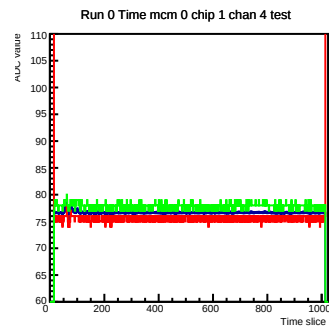
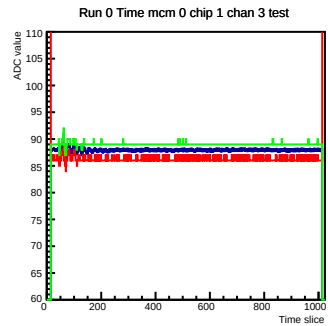
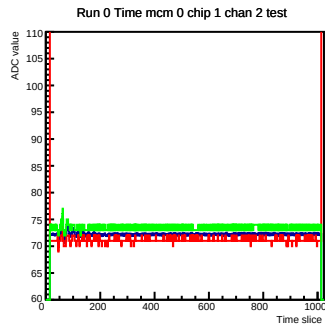
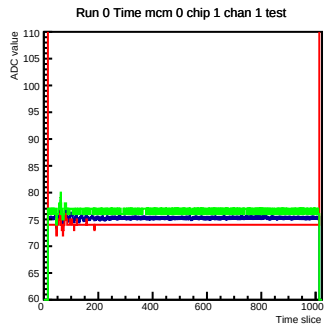
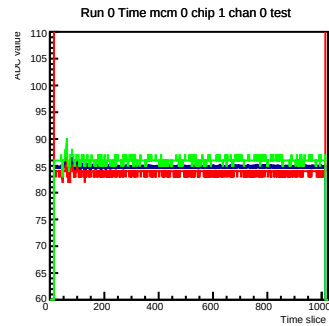


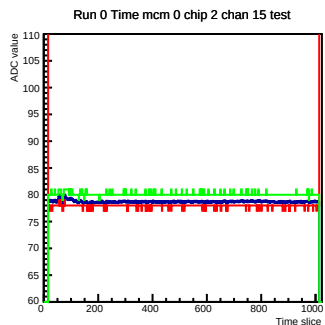
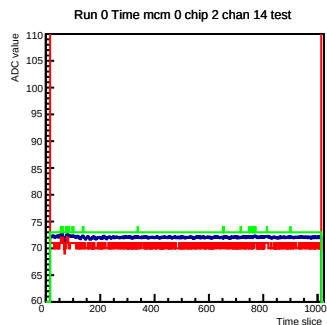
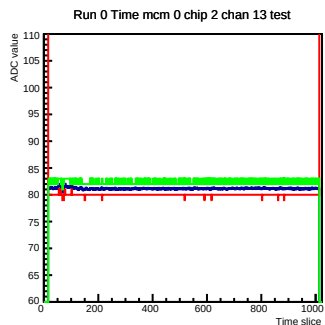
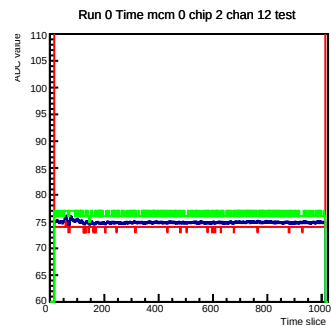
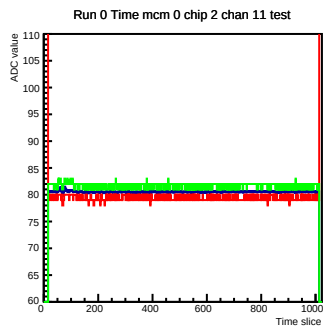
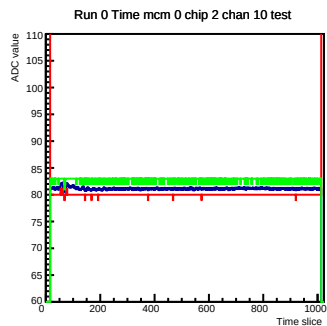
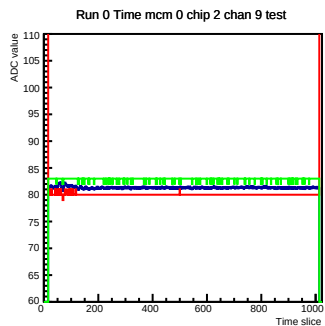
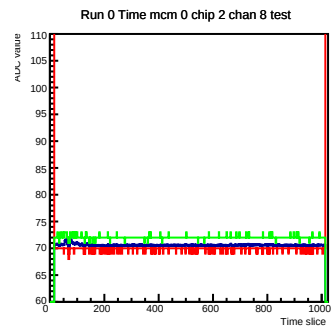
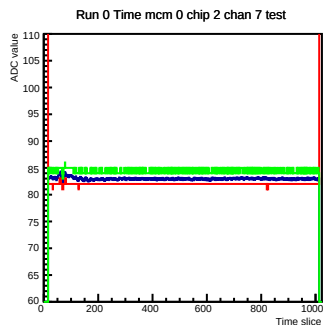
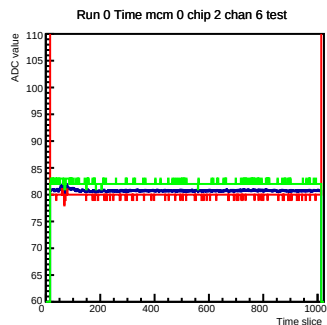
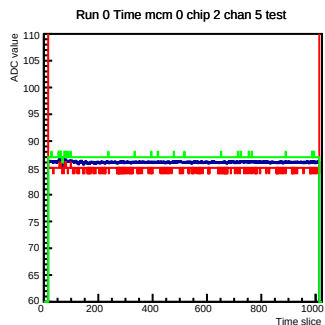
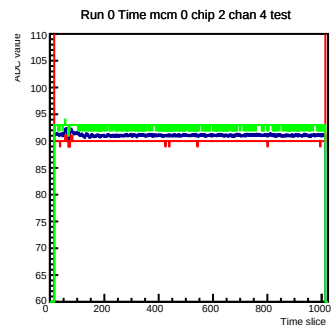
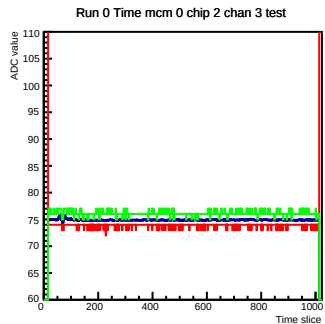
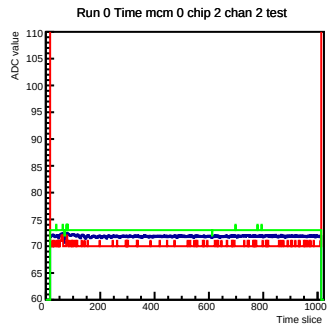
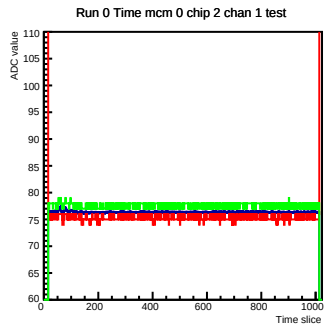
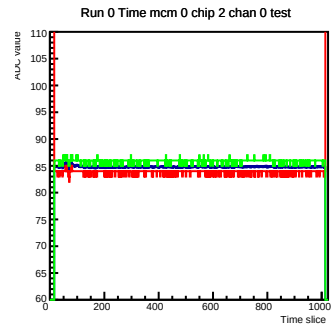
Run 0 Time mcm 0 chip 0 chan 14 test

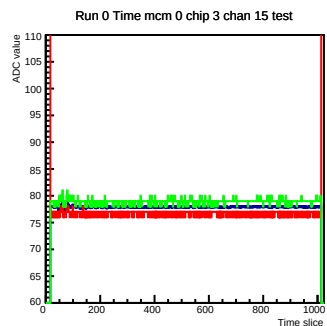
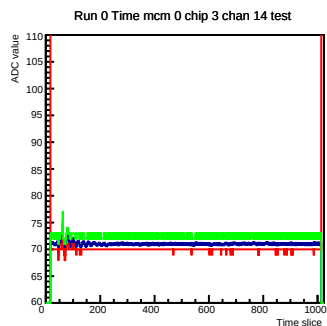
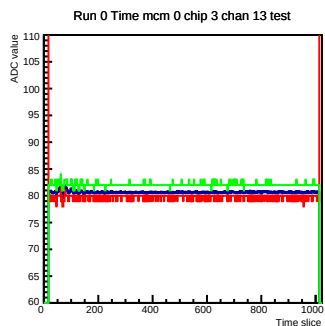
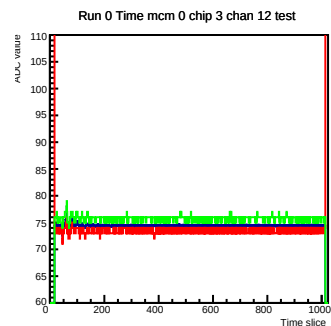
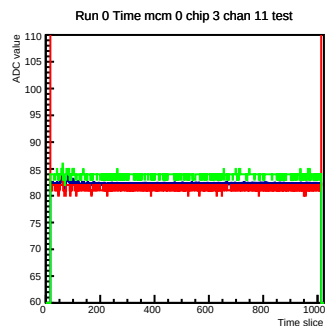
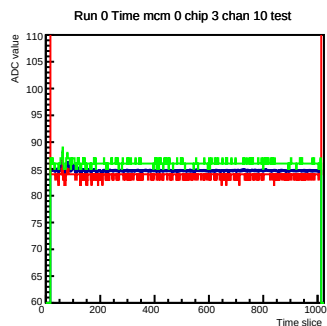
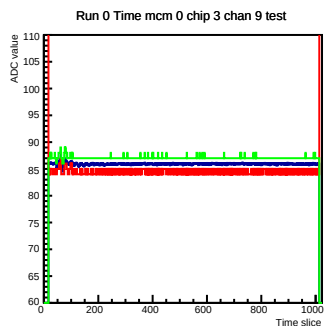
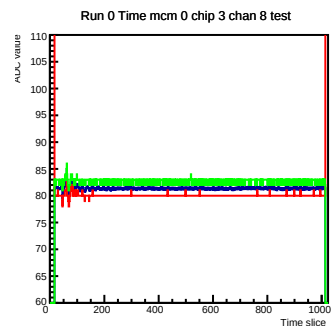
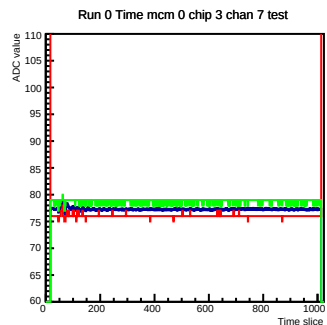
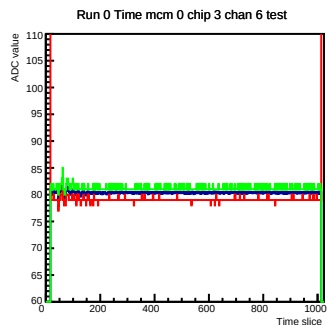
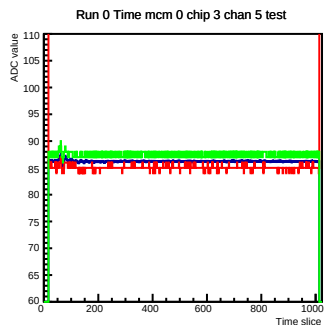
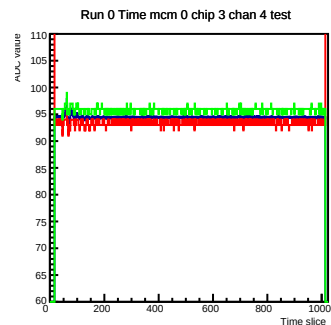
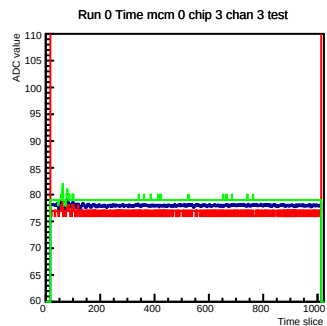
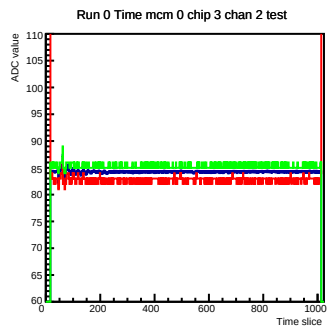
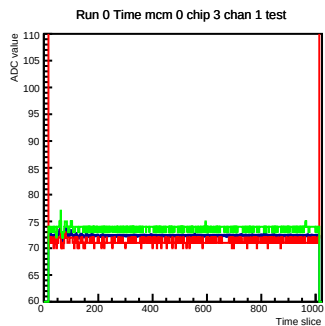
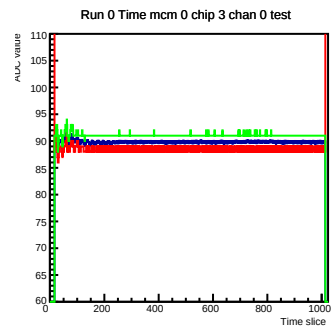


Run 0 Time mcm 0 chip 0 chan 15 test

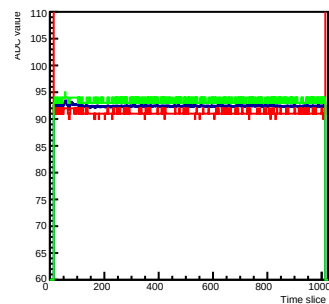




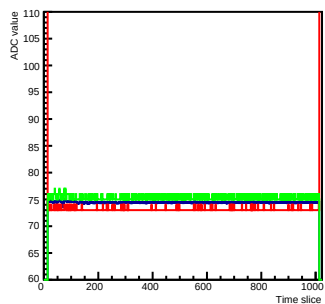




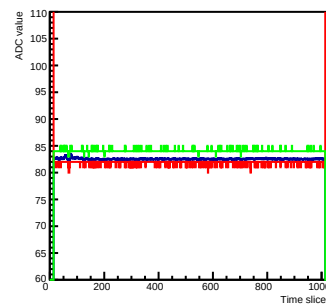
Run 0 Time mcm 0 chip 4 chan 0 test



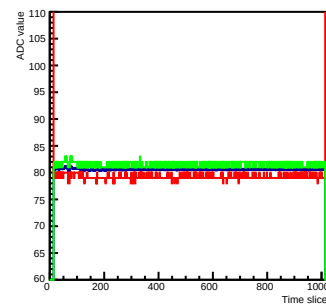
Run 0 Time mcm 0 chip 4 chan 1 test



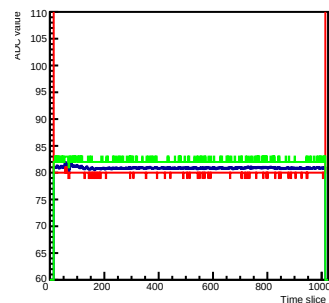
Run 0 Time mcm 0 chip 4 chan 2 test



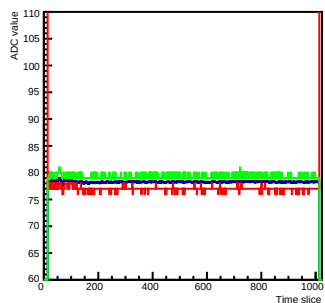
Run 0 Time mcm 0 chip 4 chan 3 test



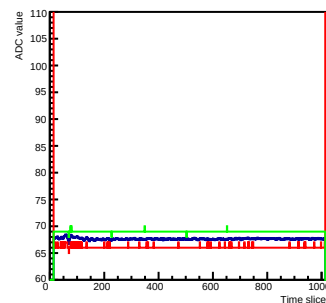
Run 0 Time mcm 0 chip 4 chan 4 test



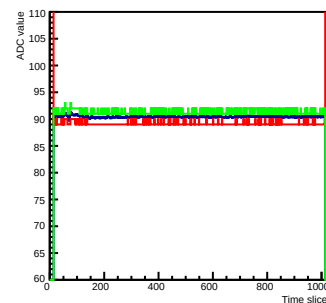
Run 0 Time mcm 0 chip 4 chan 5 test



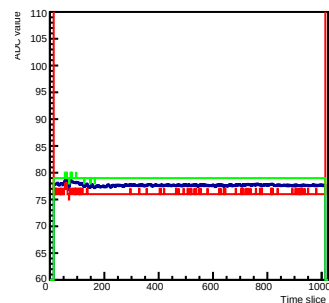
Run 0 Time mcm 0 chip 4 chan 6 test



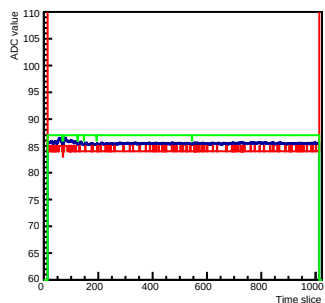
Run 0 Time mcm 0 chip 4 chan 7 test



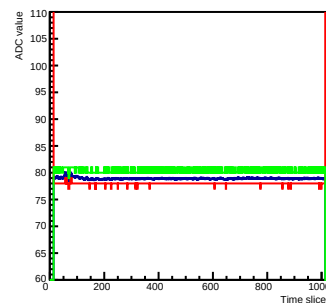
Run 0 Time mcm 0 chip 4 chan 8 test



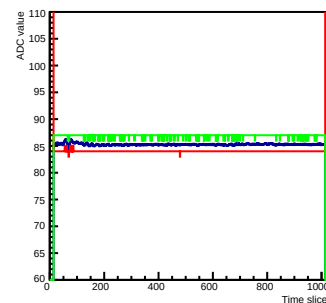
Run 0 Time mcm 0 chip 4 chan 9 test



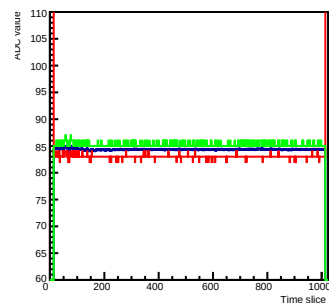
Run 0 Time mcm 0 chip 4 chan 10 test



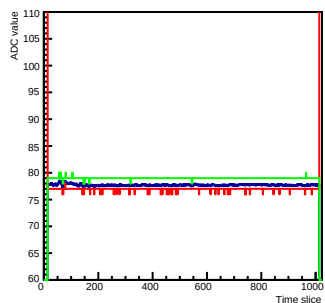
Run 0 Time mcm 0 chip 4 chan 11 test



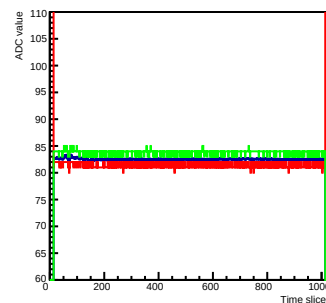
Run 0 Time mcm 0 chip 4 chan 12 test



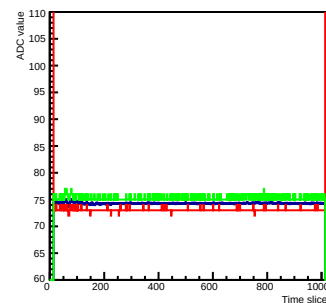
Run 0 Time mcm 0 chip 4 chan 13 test

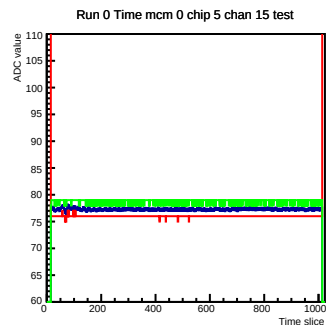
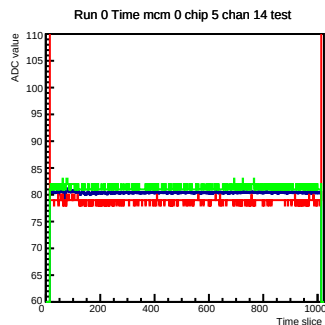
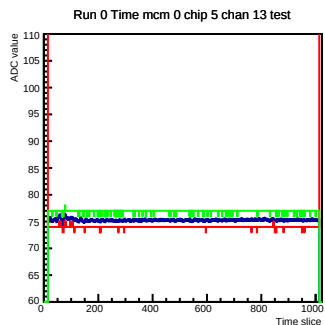
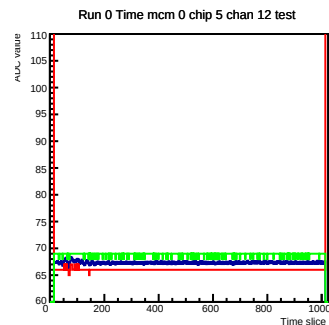
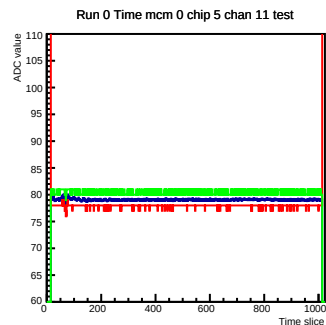
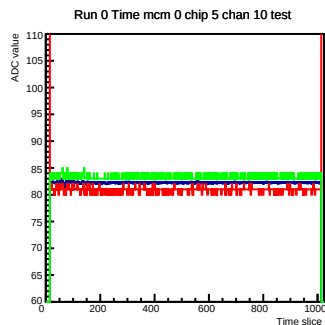
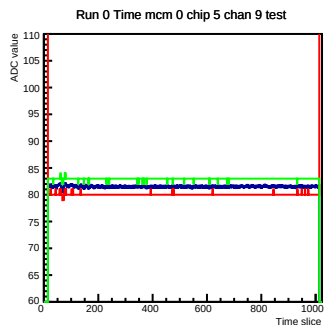
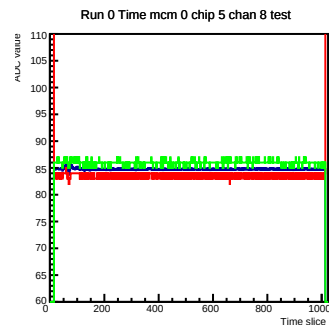
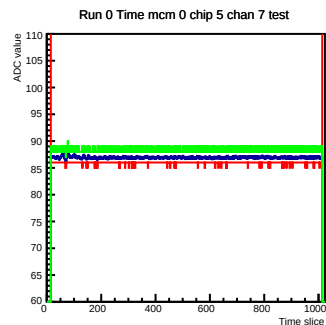
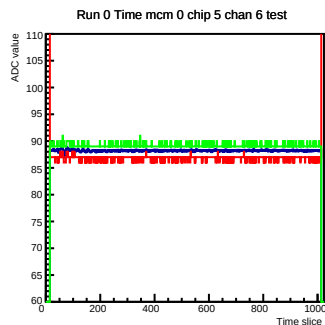
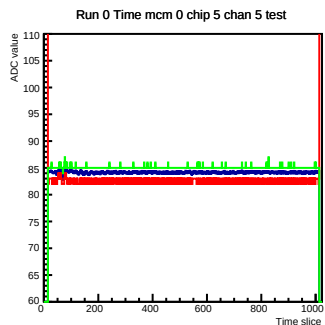
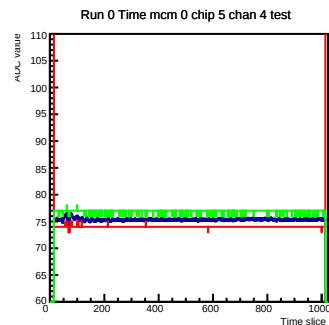
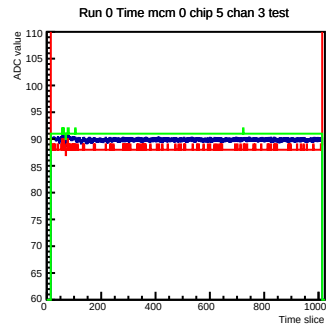
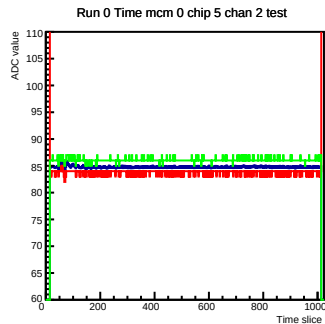
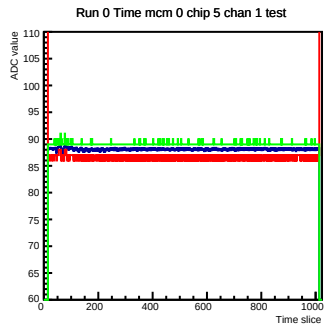
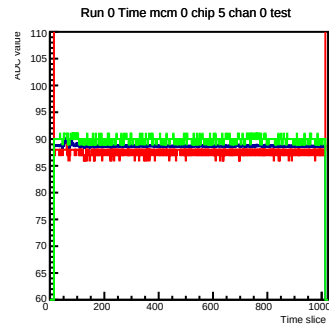


Run 0 Time mcm 0 chip 4 chan 14 test

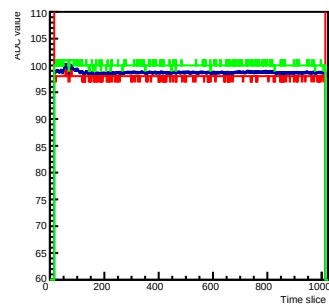


Run 0 Time mcm 0 chip 4 chan 15 test

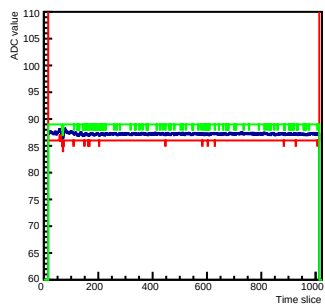




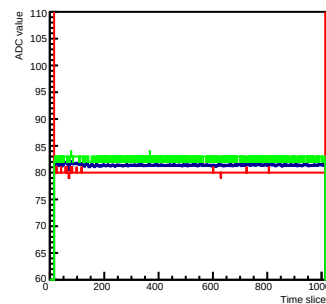
Run 0 Time mcm 0 chip 6 chan 0 test



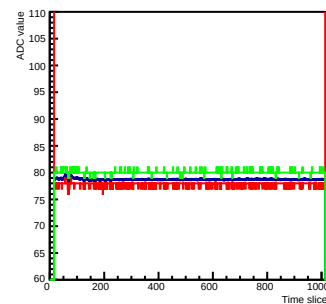
Run 0 Time mcm 0 chip 6 chan 1 test



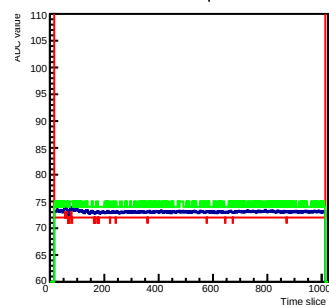
Run 0 Time mcm 0 chip 6 chan 2 test



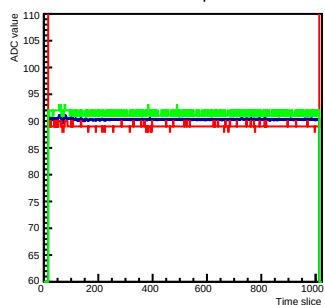
Run 0 Time mcm 0 chip 6 chan 3 test



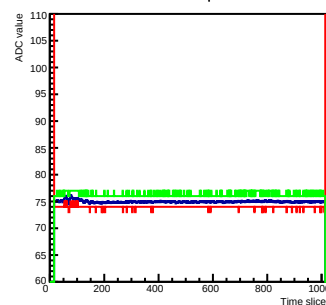
Run 0 Time mcm 0 chip 6 chan 4 test



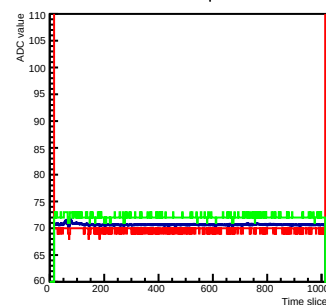
Run 0 Time mcm 0 chip 6 chan 5 test



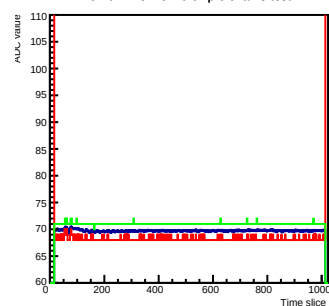
Run 0 Time mcm 0 chip 6 chan 6 test



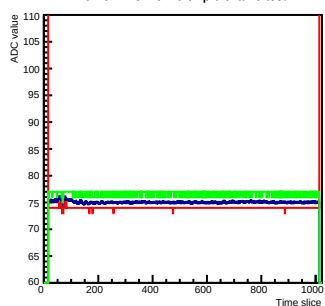
Run 0 Time mcm 0 chip 6 chan 7 test



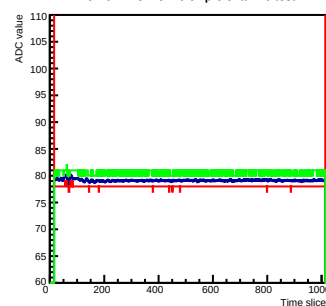
Run 0 Time mcm 0 chip 6 chan 8 test



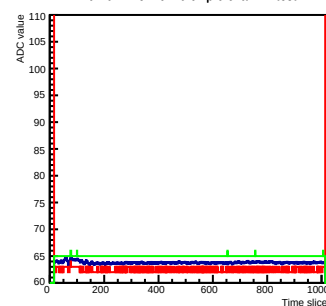
Run 0 Time mcm 0 chip 6 chan 9 test



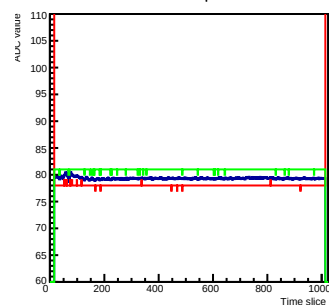
Run 0 Time mcm 0 chip 6 chan 10 test



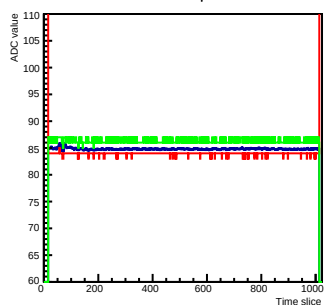
Run 0 Time mcm 0 chip 6 chan 11 test



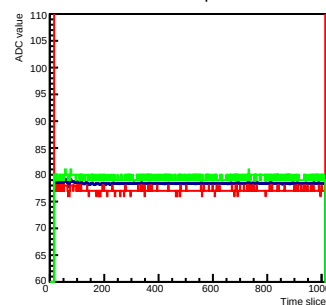
Run 0 Time mcm 0 chip 6 chan 12 test



Run 0 Time mcm 0 chip 6 chan 13 test



Run 0 Time mcm 0 chip 6 chan 14 test



Run 0 Time mcm 0 chip 6 chan 15 test

