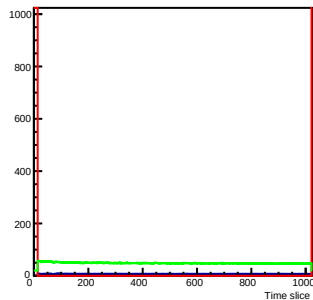
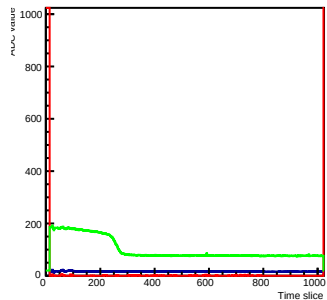


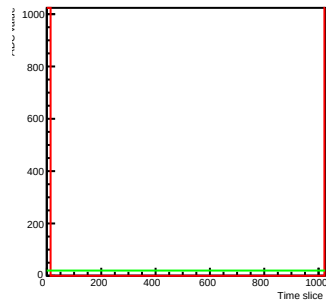
Run 0 Time mcm 0 chip 0 chan 0 s0-orig



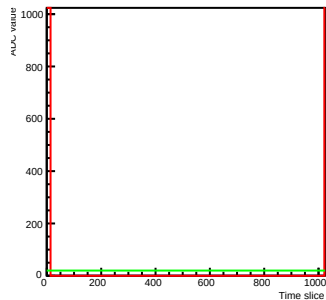
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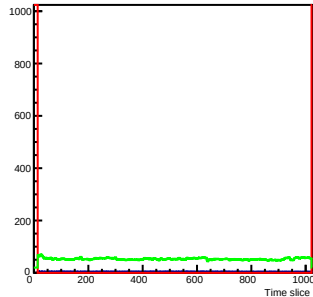
Run 0 Time mcm 0 chip 0 chan 2 s0-orig



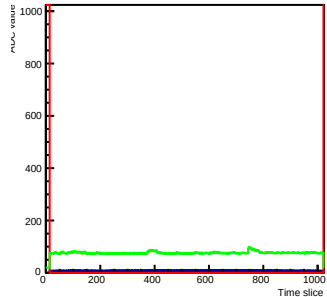
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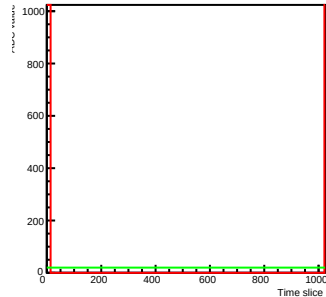
Run 0 Time mcm 0 chip 0 chan 4 s0-orig



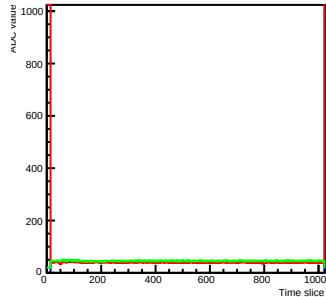
Run 0 Time mcm 0 chip 0 chan 5 s0-orig



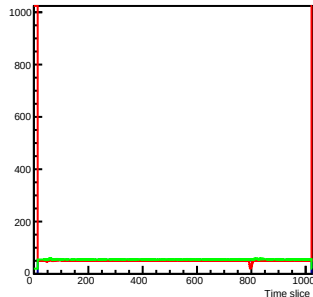
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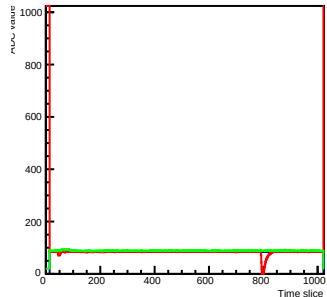
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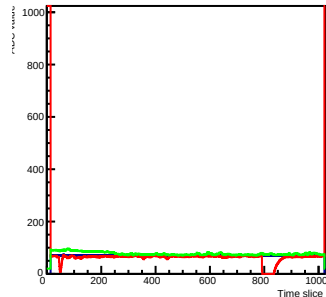
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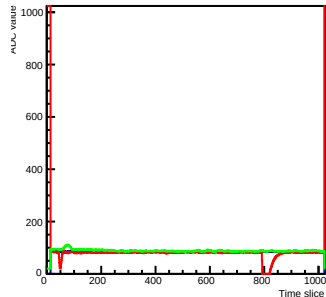
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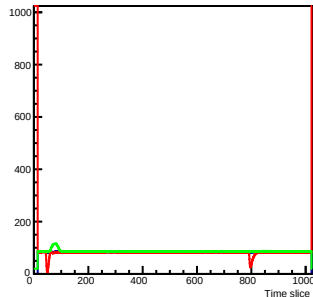
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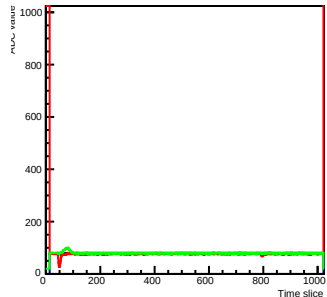
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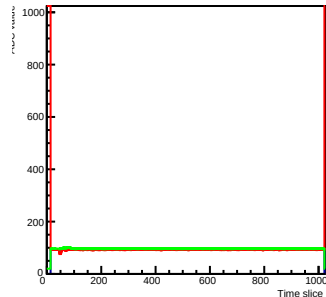
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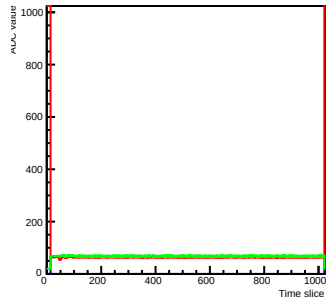
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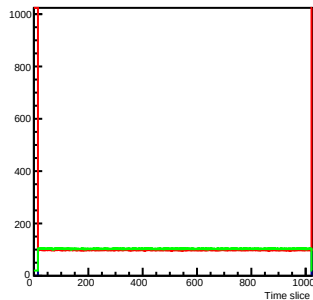
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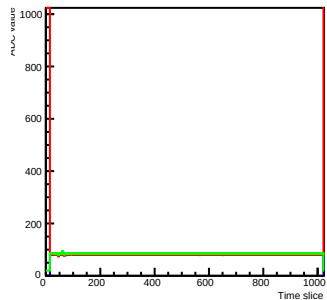
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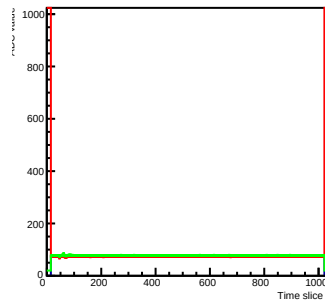
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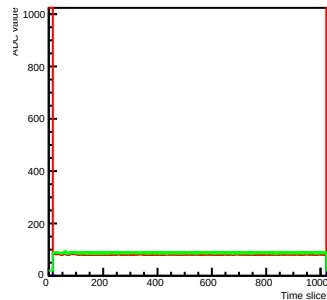
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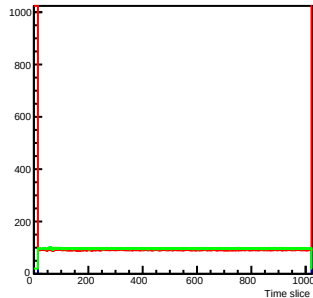
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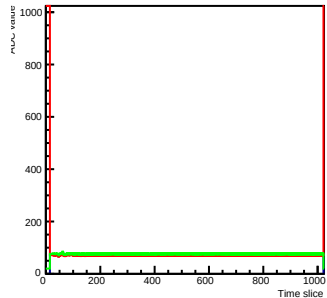
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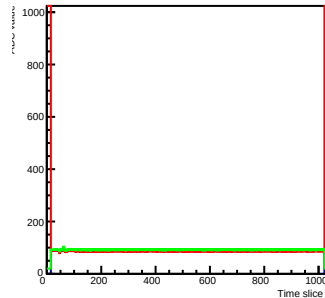
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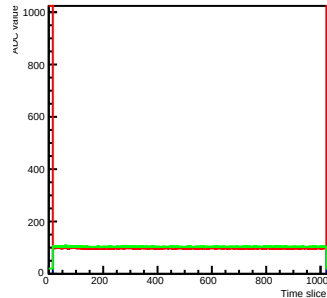
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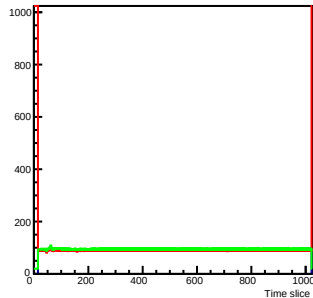
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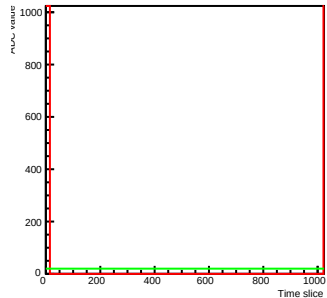
Run 0 Time mcm 0 chip 1 chan 7 s0-orig



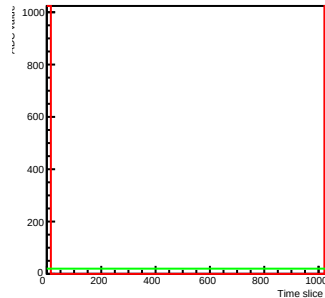
Run 0 Time mcm 0 chip 1 chan 8 s0-orig



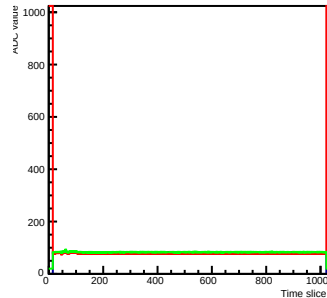
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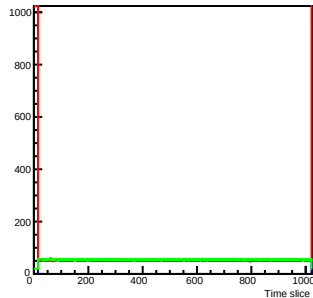
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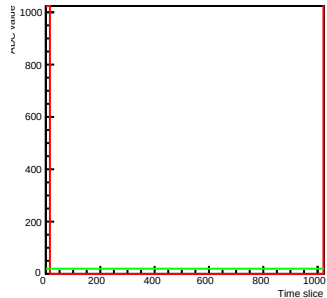
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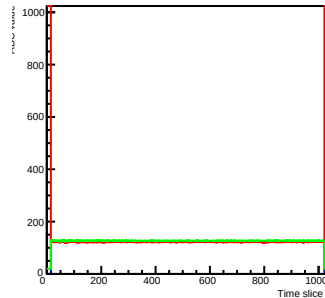
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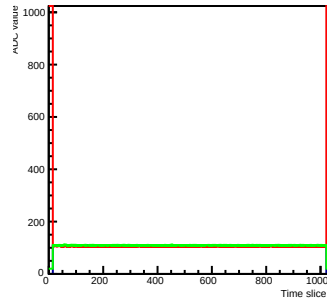
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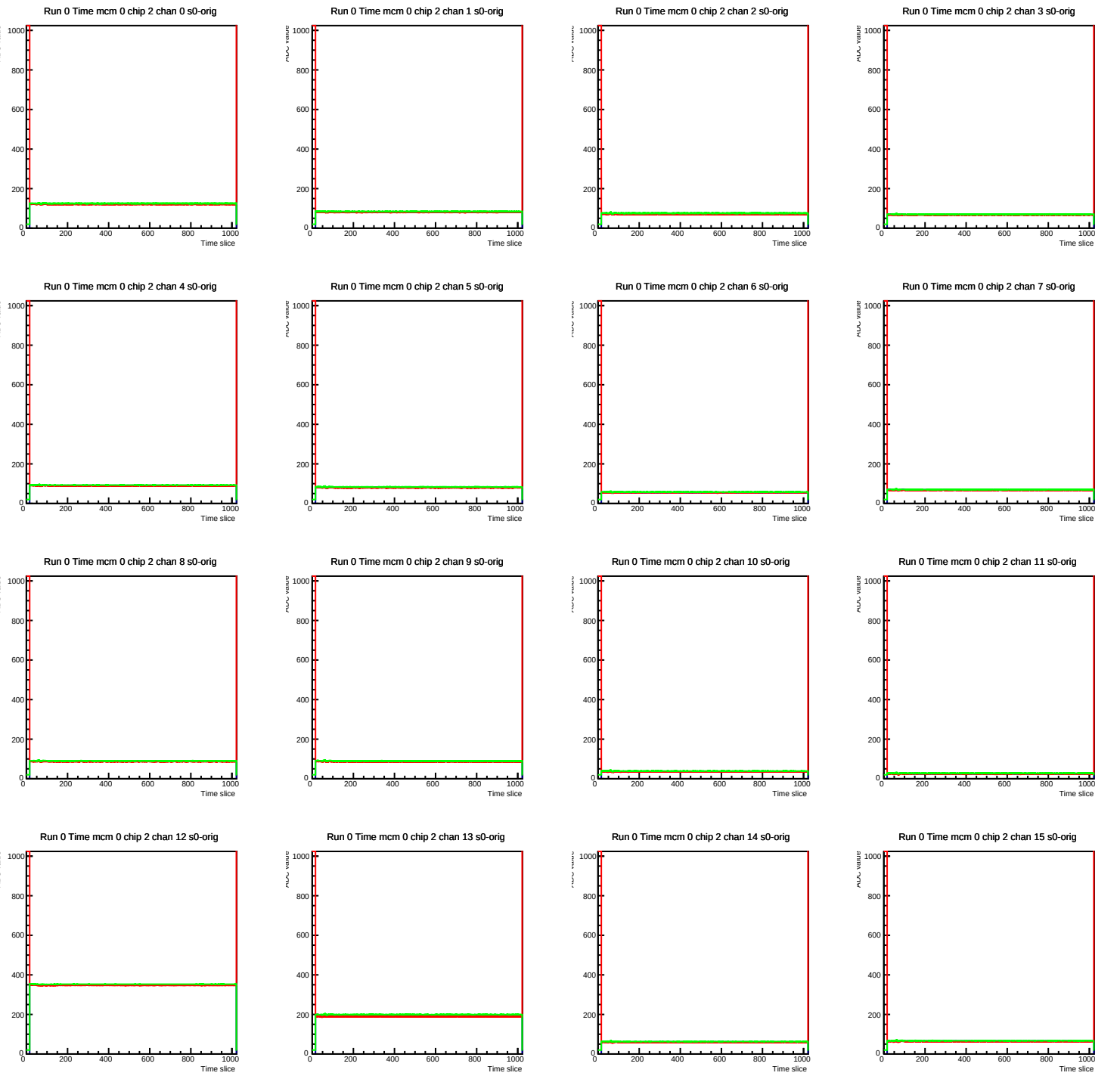


Run 0 Time mcm 0 chip 1 chan 14 s0-orig

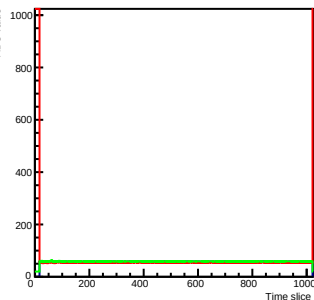


Run 0 Time mcm 0 chip 1 chan 15 s0-orig

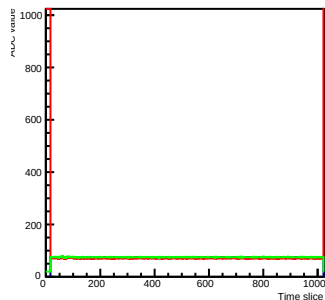




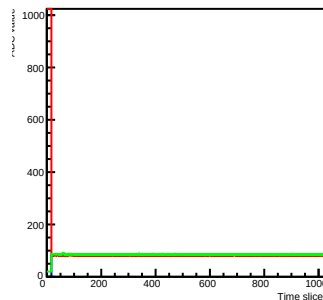
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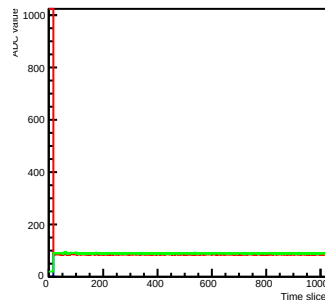
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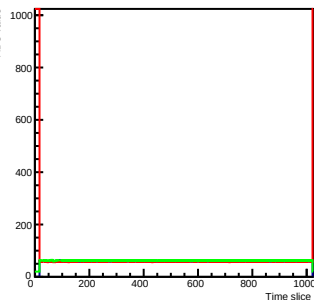
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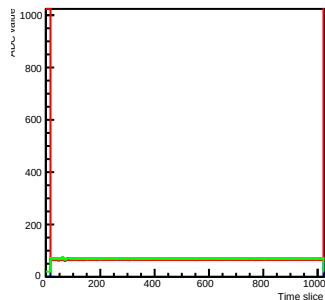
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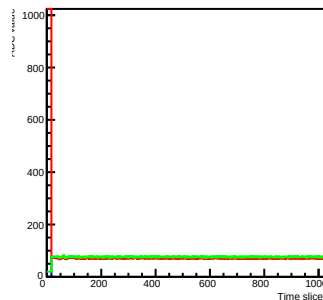
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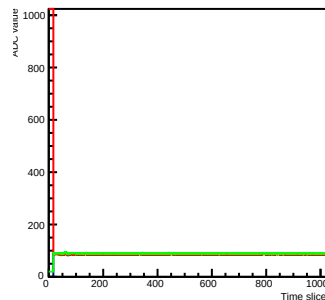
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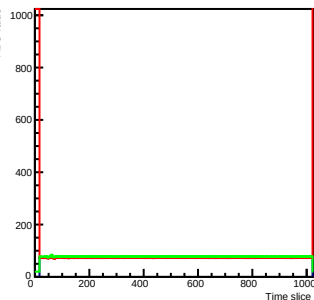
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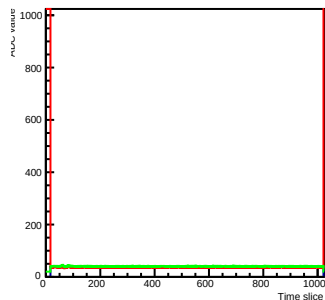
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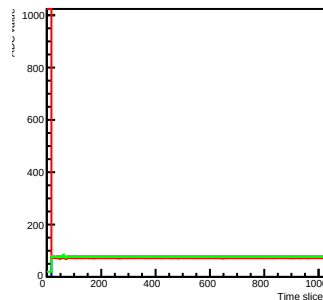
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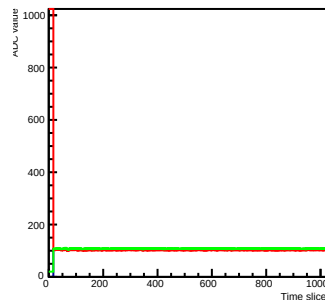
Run 0 Time mcm 0 chip 3 chan 9 s0-orig



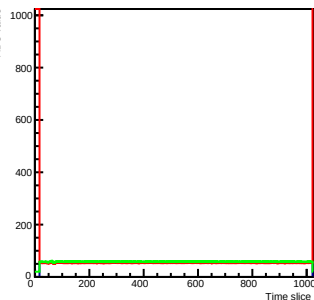
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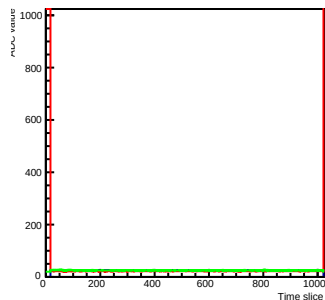
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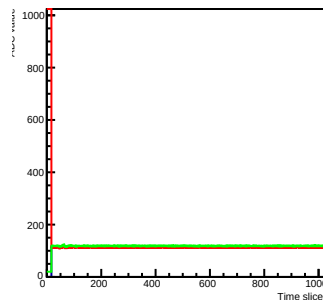
Run 0 Time mcm 0 chip 3 chan 12 s0-orig



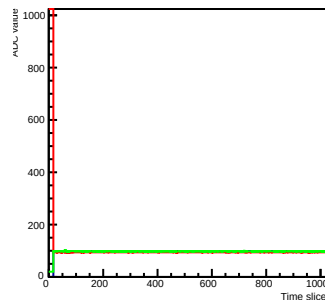
Run 0 Time mcm 0 chip 3 chan 13 s0-orig



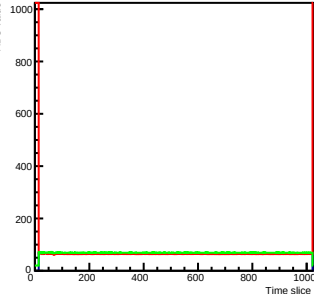
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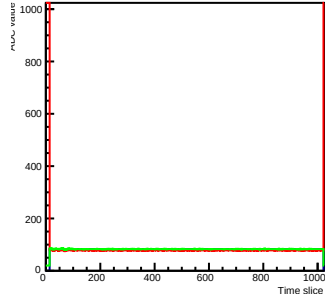
Run 0 Time mcm 0 chip 3 chan 15 s0-orig



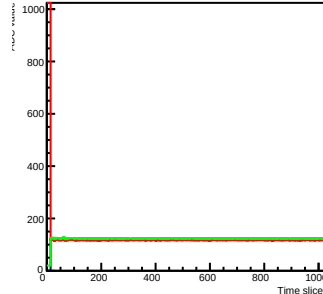
Run 0 Time mcm 0 chip 4 chan 0 s0-orig



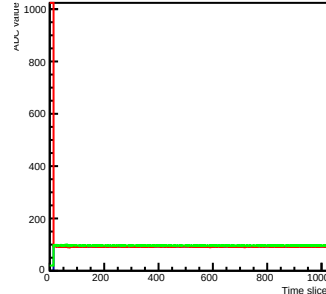
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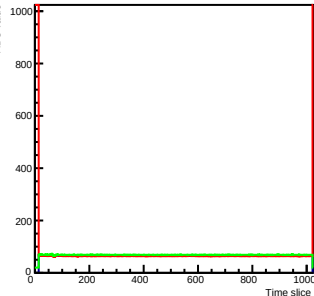
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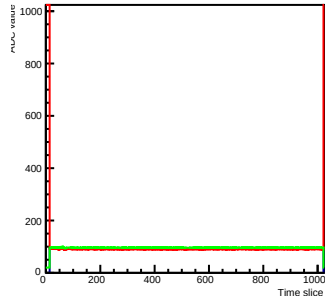
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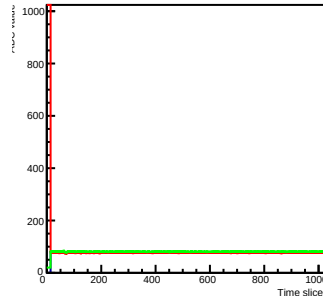
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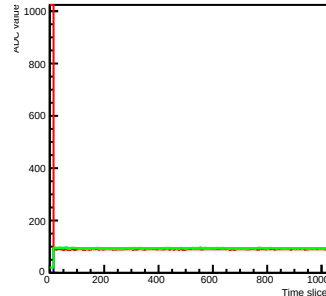
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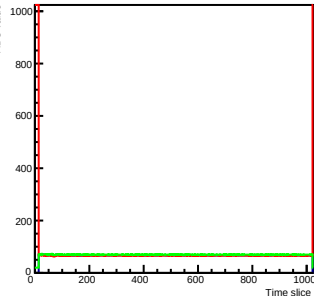
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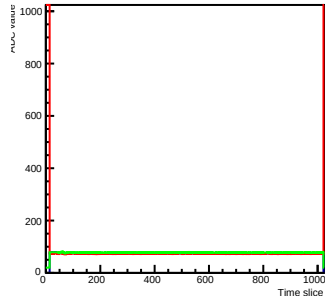
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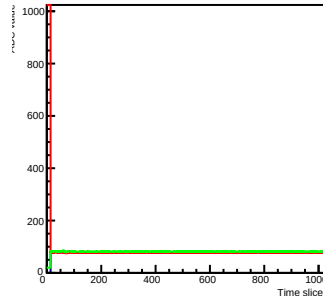
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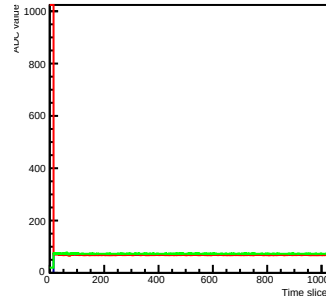
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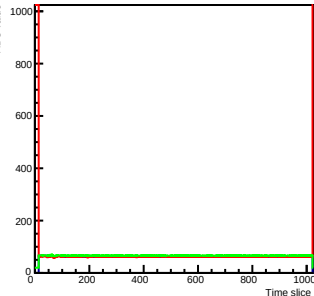
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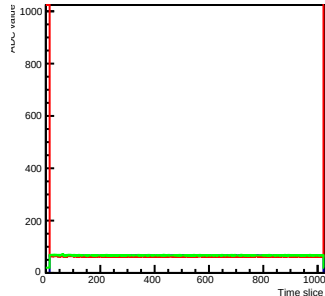
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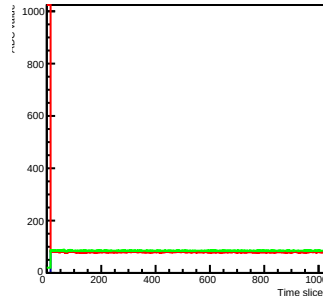
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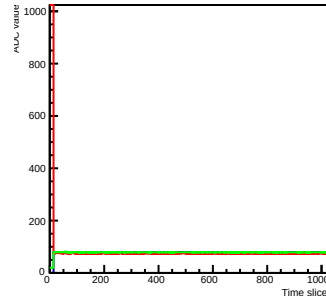
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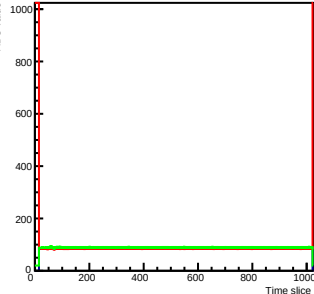
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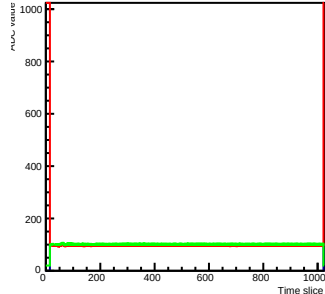
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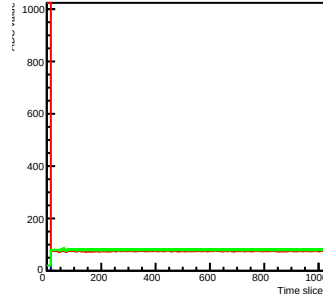
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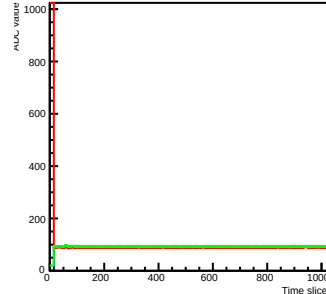
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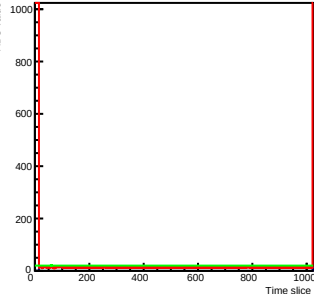
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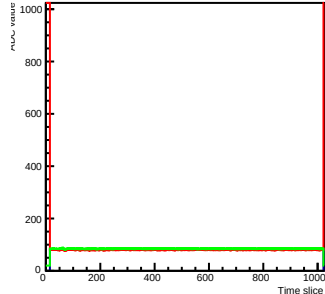
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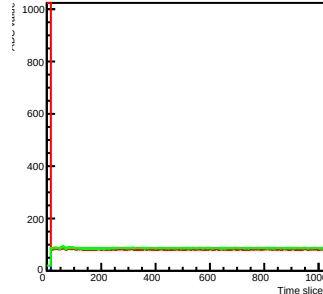
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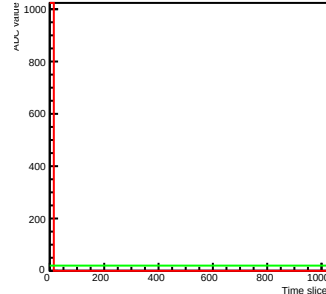
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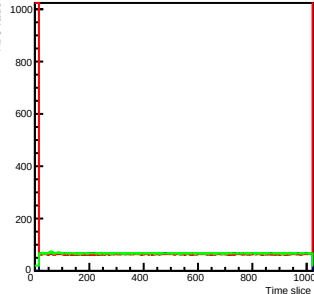
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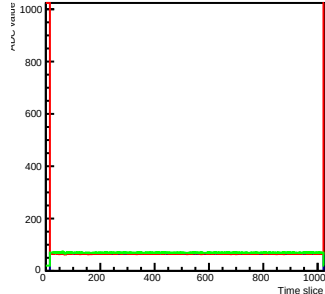
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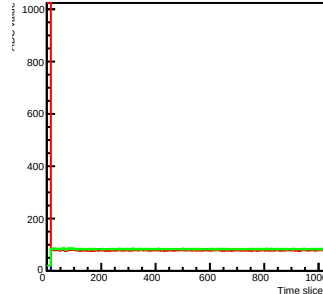
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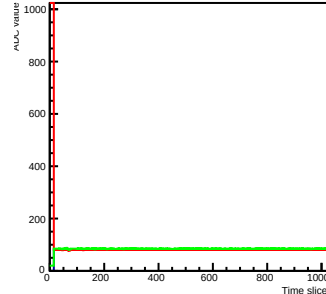
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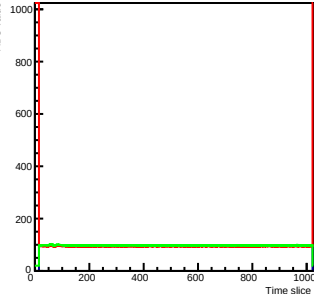
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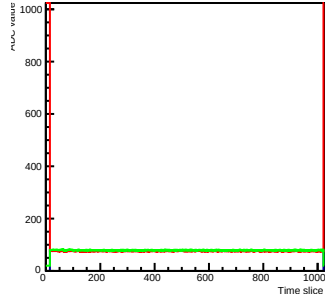
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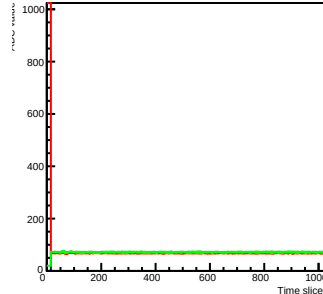
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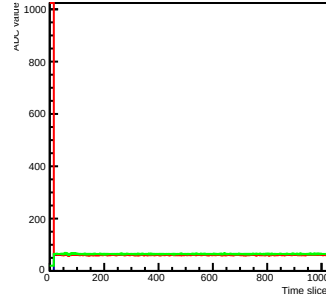
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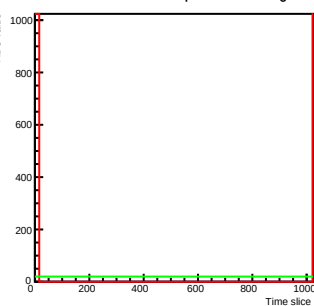
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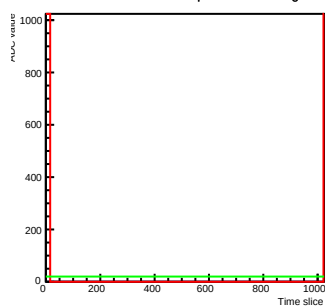
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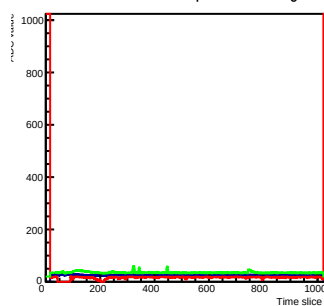
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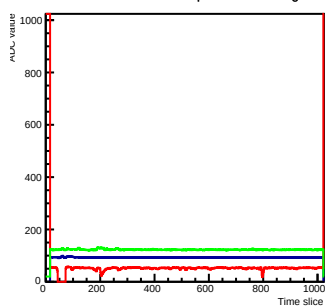
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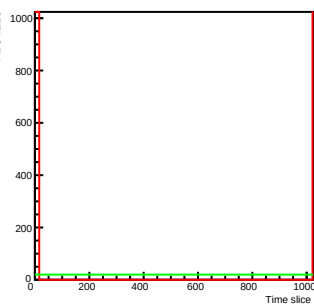
Run 0 Time mcm 0 chip 6 chan 2 s0-orig



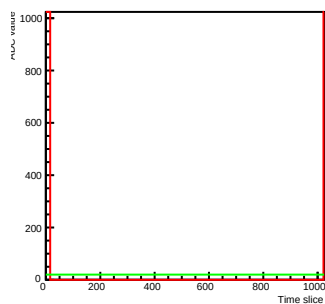
Run 0 Time mcm 0 chip 6 chan 3 s0-orig



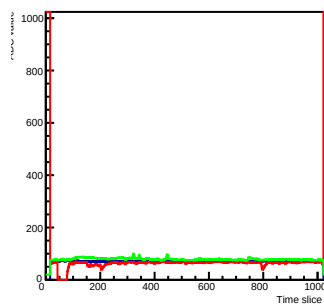
Run 0 Time mcm 0 chip 6 chan 4 s0-orig



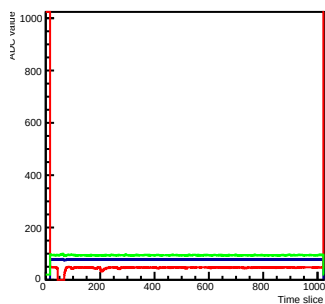
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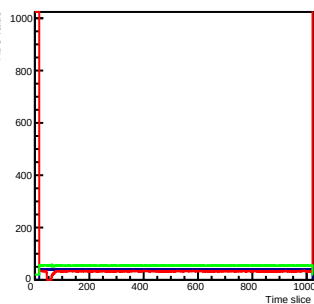
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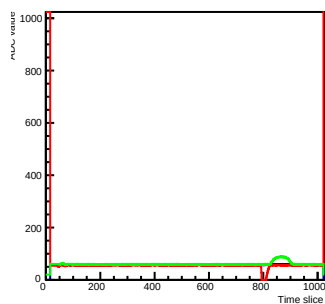
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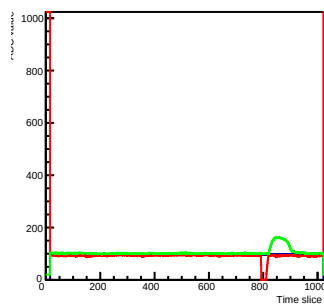
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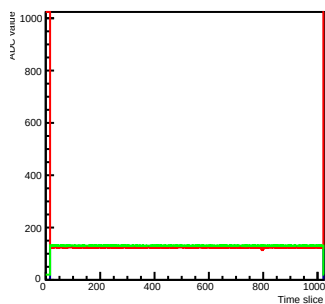
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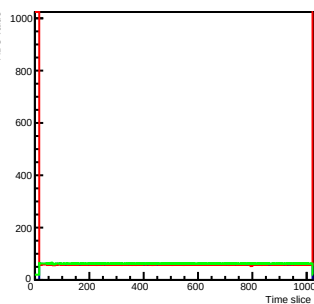
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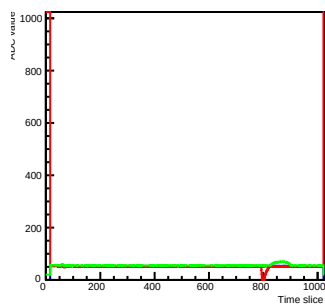
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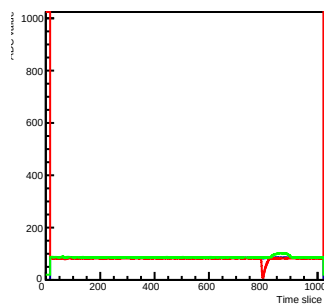
Run 0 Time mcm 0 chip 6 chan 12 s0-orig



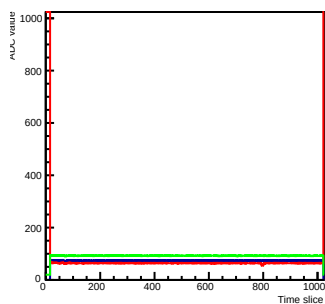
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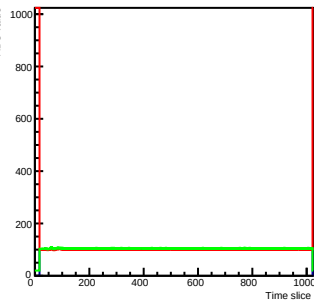
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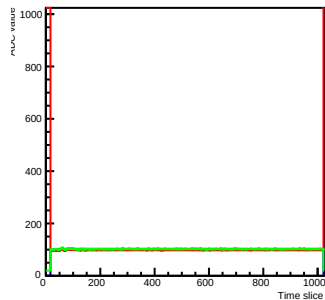
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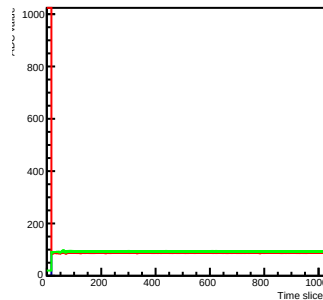
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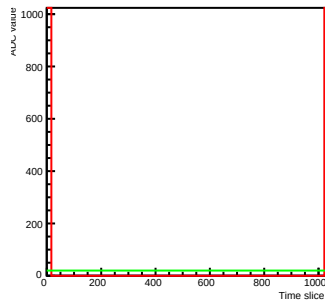
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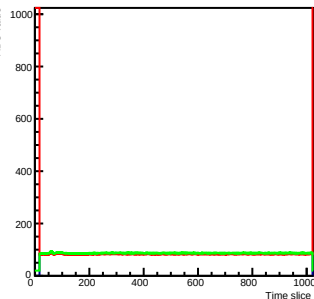
Run 0 Time mcm 0 chip 7 chan 2 s0-orig



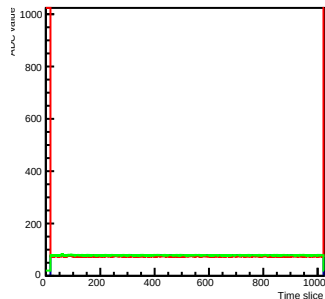
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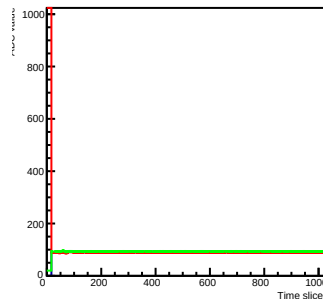
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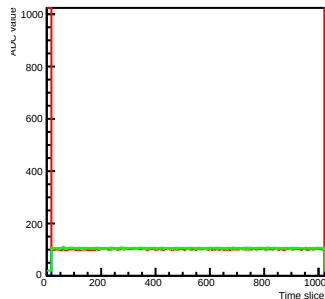
Run 0 Time mcm 0 chip 7 chan 5 s0-orig



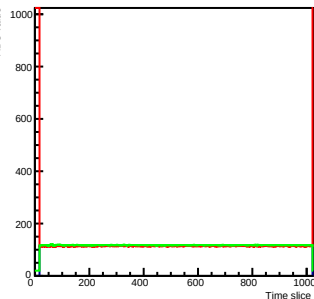
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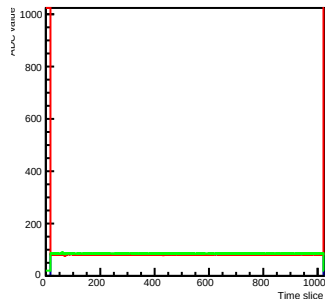
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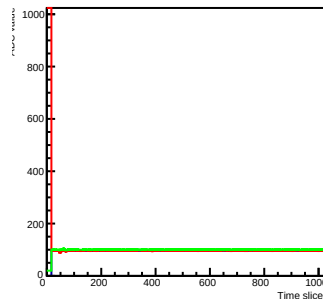
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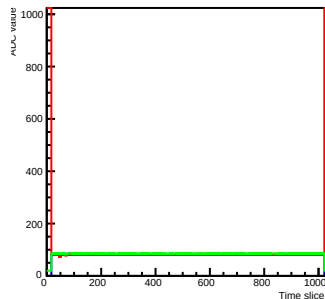
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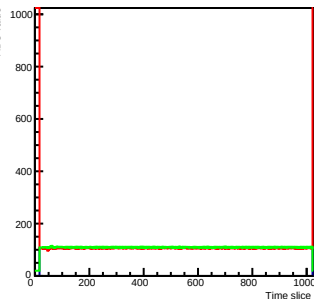
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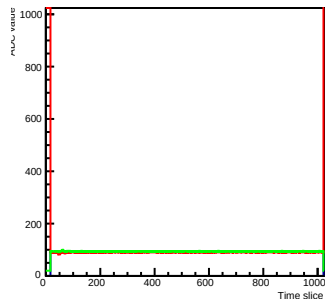
Run 0 Time mcm 0 chip 7 chan 11 s0-orig



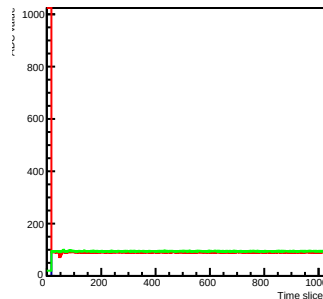
Run 0 Time mcm 0 chip 7 chan 12 s0-orig



Run 0 Time mcm 0 chip 7 chan 13 s0-orig



Run 0 Time mcm 0 chip 7 chan 14 s0-orig



Run 0 Time mcm 0 chip 7 chan 15 s0-orig

