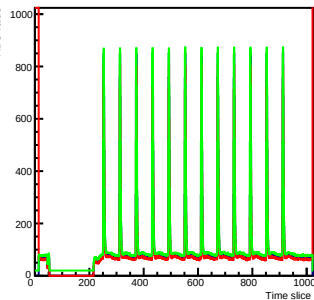
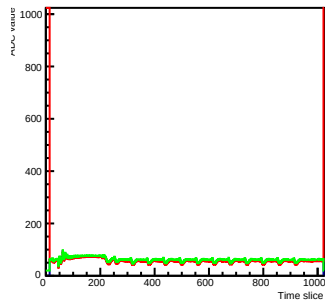


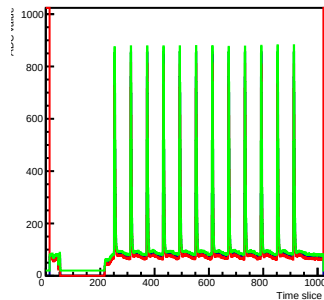
Run 1 Time mcm 0 chip 0 chan 0 s1-test3



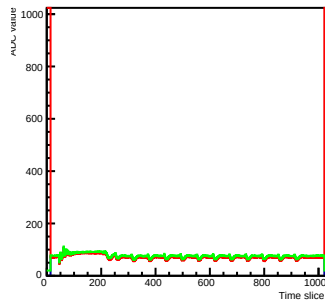
Run 1 Time mcm 0 chip 0 chan 1 s1-test3



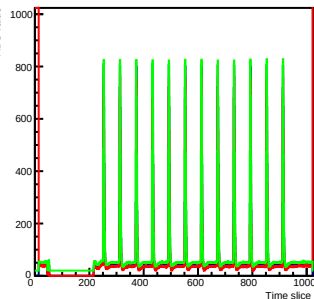
Run 1 Time mcm 0 chip 0 chan 2 s1-test3



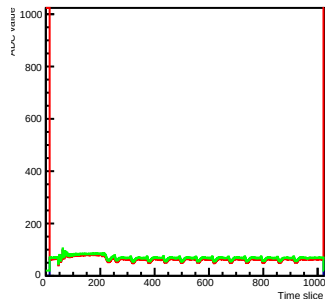
Run 1 Time mcm 0 chip 0 chan 3 s1-test3



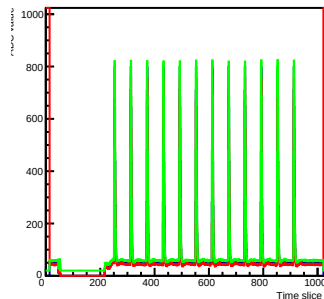
Run 1 Time mcm 0 chip 0 chan 4 s1-test3



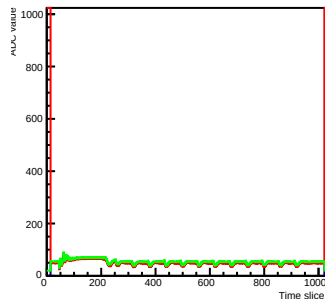
Run 1 Time mcm 0 chip 0 chan 5 s1-test3



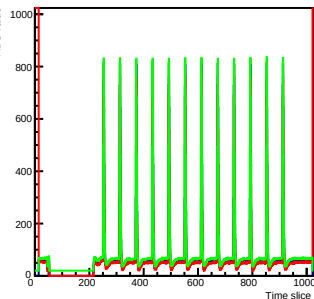
Run 1 Time mcm 0 chip 0 chan 6 s1-test3



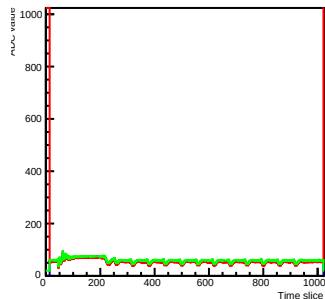
Run 1 Time mcm 0 chip 0 chan 7 s1-test3



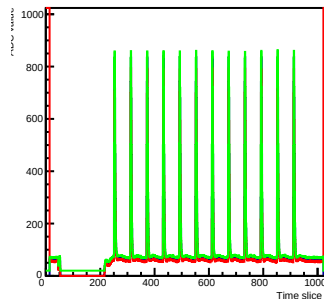
Run 1 Time mcm 0 chip 0 chan 8 s1-test3



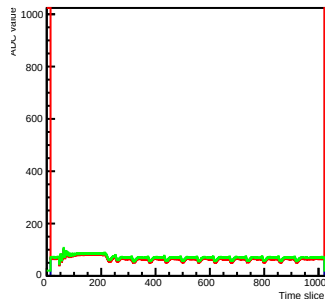
Run 1 Time mcm 0 chip 0 chan 9 s1-test3



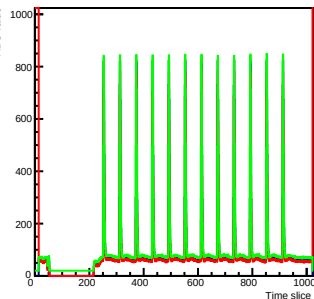
Run 1 Time mcm 0 chip 0 chan 10 s1-test3



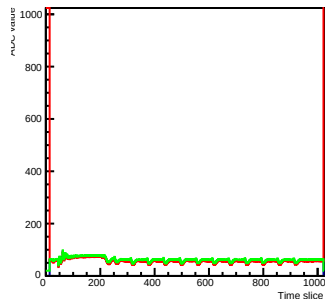
Run 1 Time mcm 0 chip 0 chan 11 s1-test3



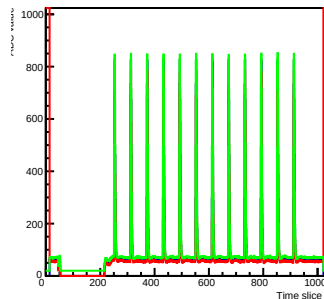
Run 1 Time mcm 0 chip 0 chan 12 s1-test3



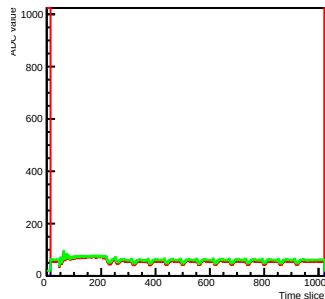
Run 1 Time mcm 0 chip 0 chan 13 s1-test3



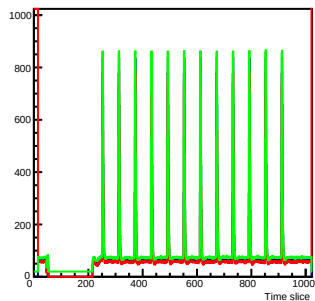
Run 1 Time mcm 0 chip 0 chan 14 s1-test3



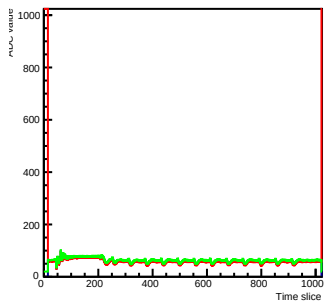
Run 1 Time mcm 0 chip 0 chan 15 s1-test3



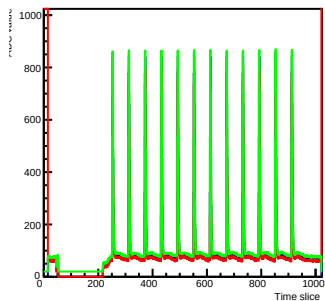
Run 1 Time mcm 0 chip 1 chan 0 s1-test3



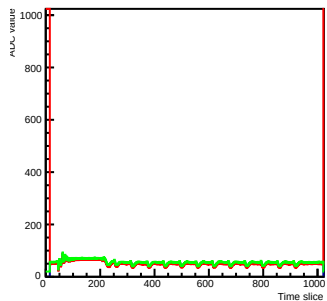
Run 1 Time mcm 0 chip 1 chan 1 s1-test3



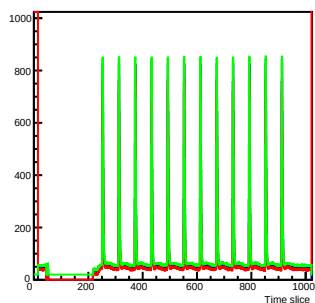
Run 1 Time mcm 0 chip 1 chan 2 s1-test3



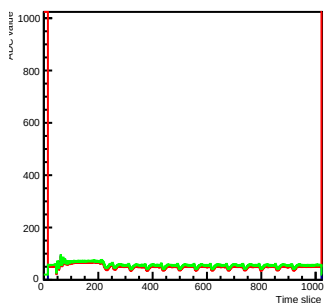
Run 1 Time mcm 0 chip 1 chan 3 s1-test3



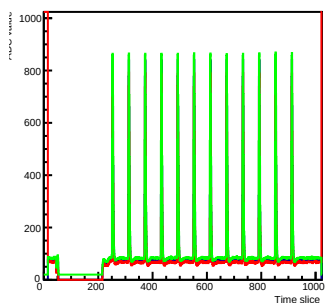
Run 1 Time mcm 0 chip 1 chan 4 s1-test3



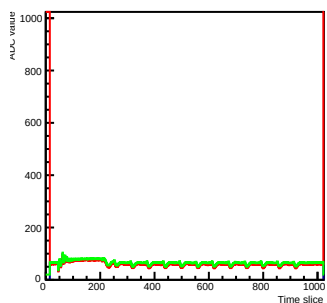
Run 1 Time mcm 0 chip 1 chan 5 s1-test3



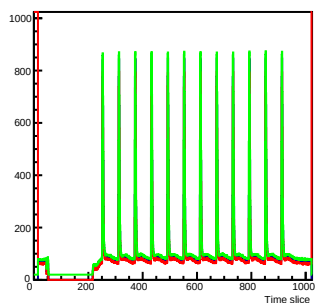
Run 1 Time mcm 0 chip 1 chan 6 s1-test3



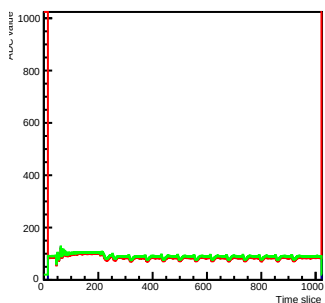
Run 1 Time mcm 0 chip 1 chan 7 s1-test3



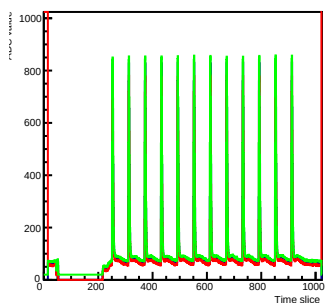
Run 1 Time mcm 0 chip 1 chan 8 s1-test3



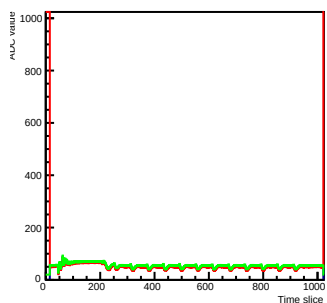
Run 1 Time mcm 0 chip 1 chan 9 s1-test3



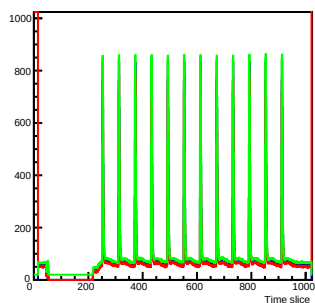
Run 1 Time mcm 0 chip 1 chan 10 s1-test3



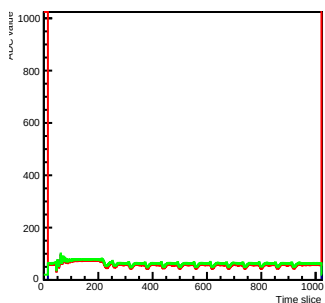
Run 1 Time mcm 0 chip 1 chan 11 s1-test3



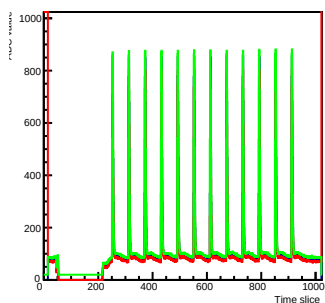
Run 1 Time mcm 0 chip 1 chan 12 s1-test3



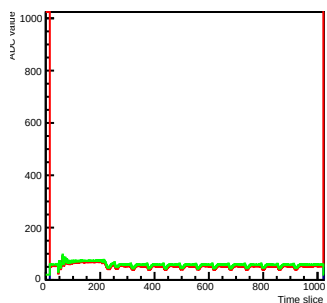
Run 1 Time mcm 0 chip 1 chan 13 s1-test3



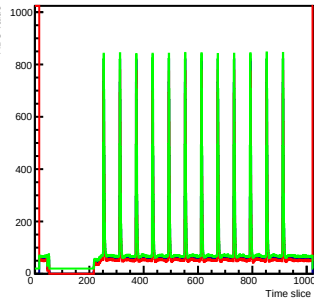
Run 1 Time mcm 0 chip 1 chan 14 s1-test3



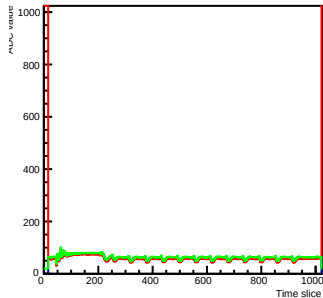
Run 1 Time mcm 0 chip 1 chan 15 s1-test3



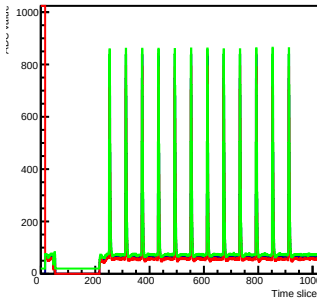
Run 1 Time mcm 0 chip 2 chan 0 s1-test3



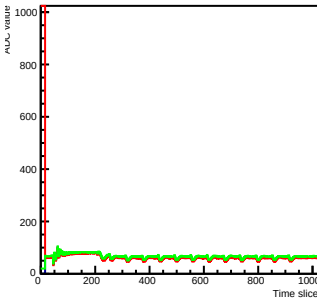
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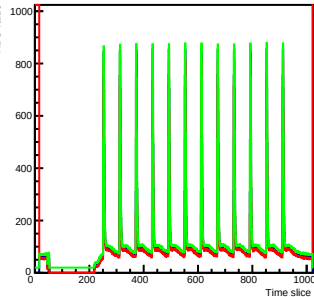
Run 1 Time mcm 0 chip 2 chan 2 s1-test3



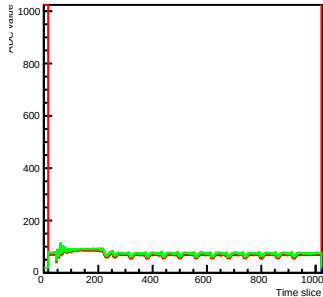
Run 1 Time mcm 0 chip 2 chan 3 s1-test3



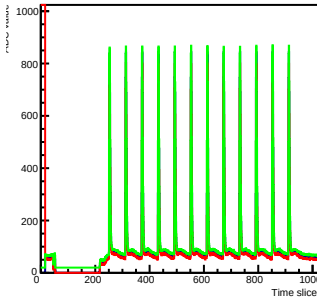
Run 1 Time mcm 0 chip 2 chan 4 s1-test3



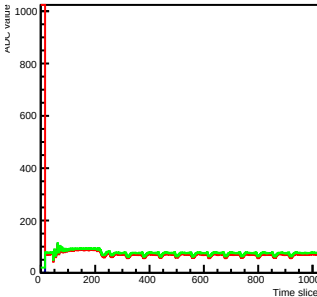
Run 1 Time mcm 0 chip 2 chan 5 s1-test3



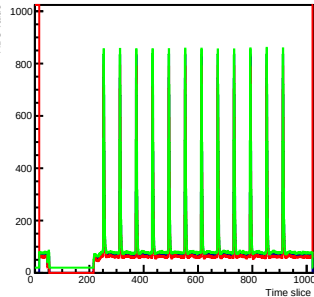
Run 1 Time mcm 0 chip 2 chan 6 s1-test3



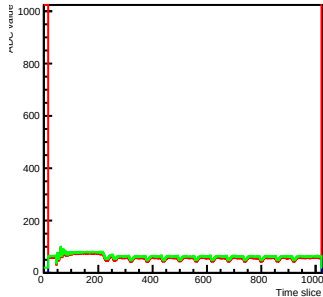
Run 1 Time mcm 0 chip 2 chan 7 s1-test3



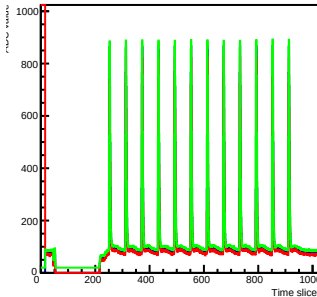
Run 1 Time mcm 0 chip 2 chan 8 s1-test3



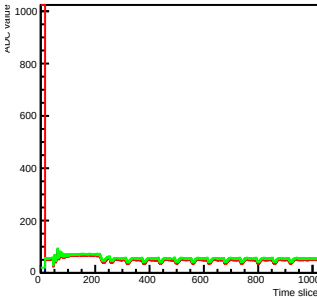
Run 1 Time mcm 0 chip 2 chan 9 s1-test3



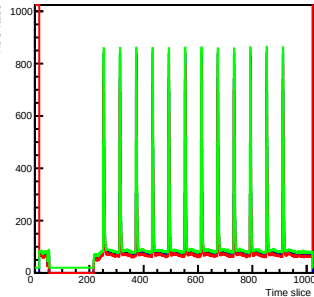
Run 1 Time mcm 0 chip 2 chan 10 s1-test3



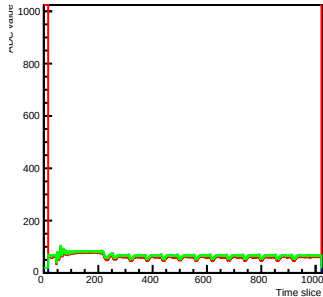
Run 1 Time mcm 0 chip 2 chan 11 s1-test3



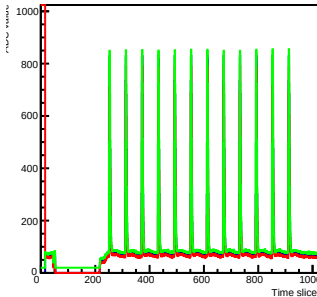
Run 1 Time mcm 0 chip 2 chan 12 s1-test3



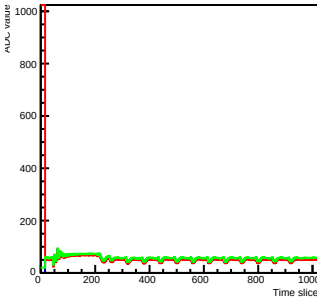
Run 1 Time mcm 0 chip 2 chan 13 s1-test3



Run 1 Time mcm 0 chip 2 chan 14 s1-test3

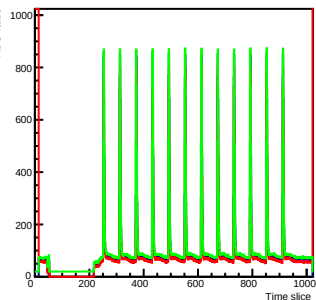


Run 1 Time mcm 0 chip 2 chan 15 s1-test3

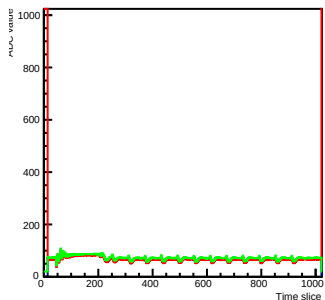




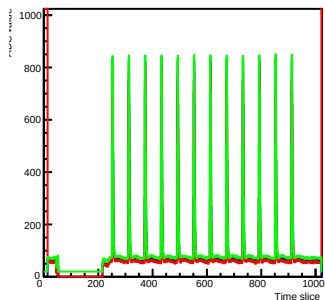
Run 1 Time mcm 0 chip 4 chan 0 s1-test3



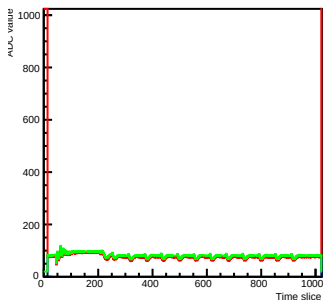
Run 1 Time mcm 0 chip 4 chan 1 s1-test3



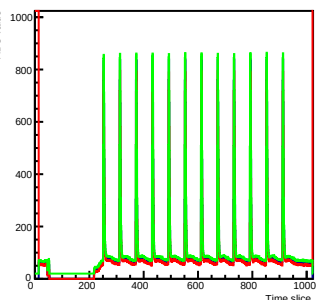
Run 1 Time mcm 0 chip 4 chan 2 s1-test3



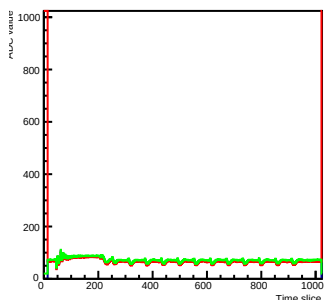
Run 1 Time mcm 0 chip 4 chan 3 s1-test3



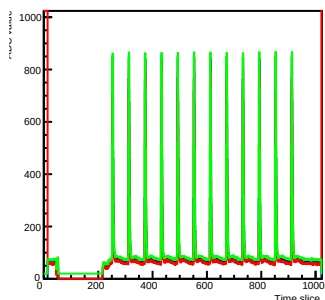
Run 1 Time mcm 0 chip 4 chan 4 s1-test3



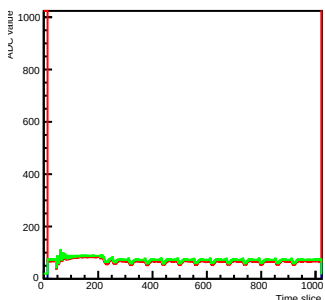
Run 1 Time mcm 0 chip 4 chan 5 s1-test3



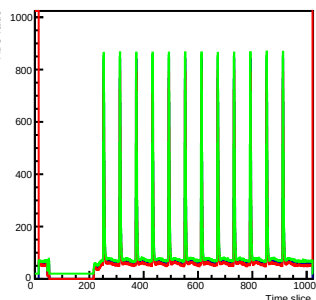
Run 1 Time mcm 0 chip 4 chan 6 s1-test3



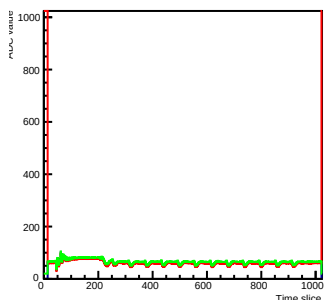
Run 1 Time mcm 0 chip 4 chan 7 s1-test3



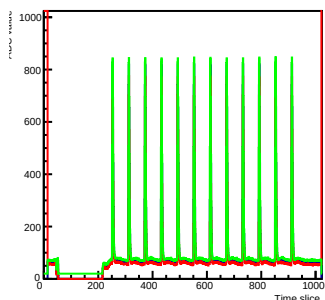
Run 1 Time mcm 0 chip 4 chan 8 s1-test3



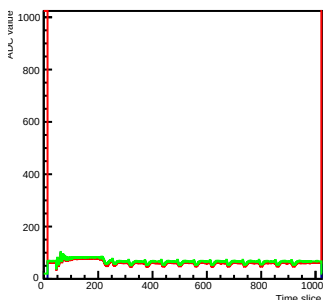
Run 1 Time mcm 0 chip 4 chan 9 s1-test3



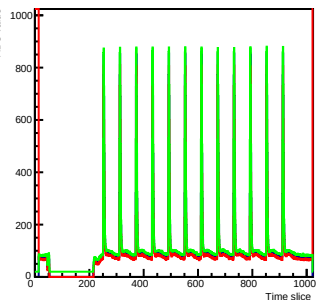
Run 1 Time mcm 0 chip 4 chan 10 s1-test3



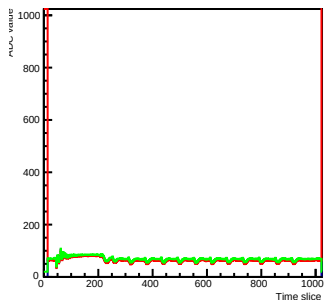
Run 1 Time mcm 0 chip 4 chan 11 s1-test3



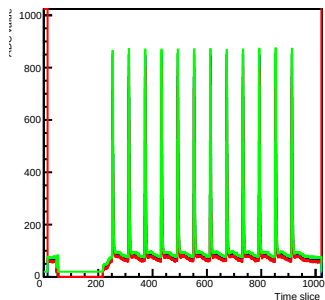
Run 1 Time mcm 0 chip 4 chan 12 s1-test3



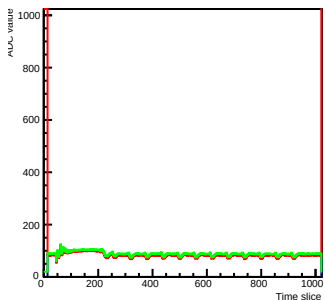
Run 1 Time mcm 0 chip 4 chan 13 s1-test3



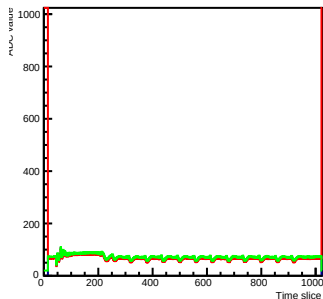
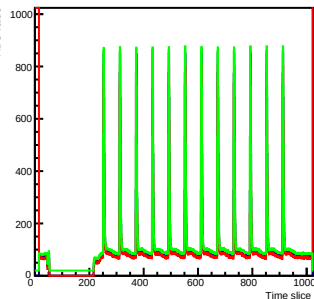
Run 1 Time mcm 0 chip 4 chan 14 s1-test3



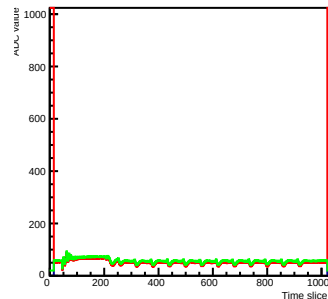
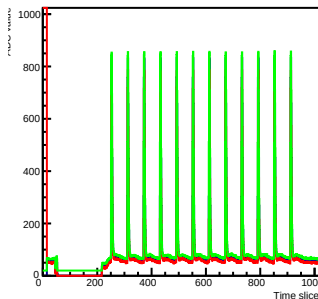
Run 1 Time mcm 0 chip 4 chan 15 s1-test3



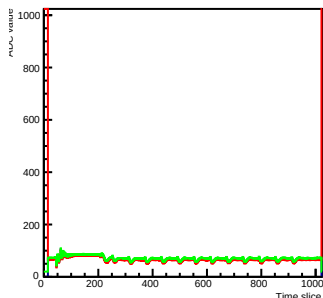
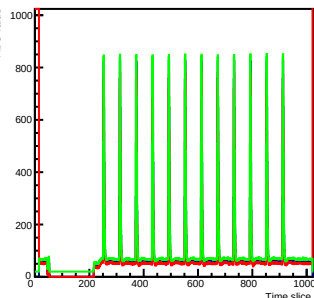
Run 1 Time mcm 0 chip 5 chan 1 s1-test3



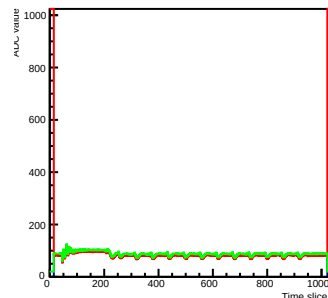
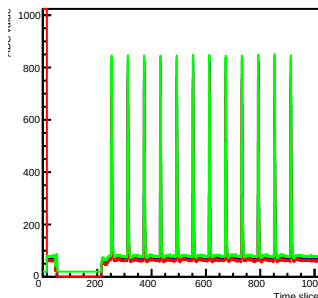
Run 1 Time mcm 0 chip 5 chan 3 s1-test3



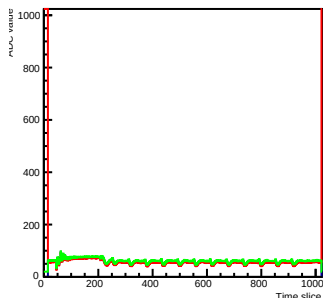
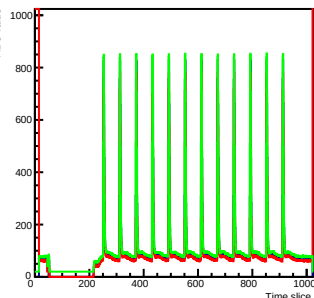
Run 1 Time mcm 0 chip 5 chan 5 s1-test3



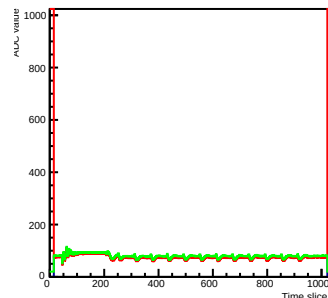
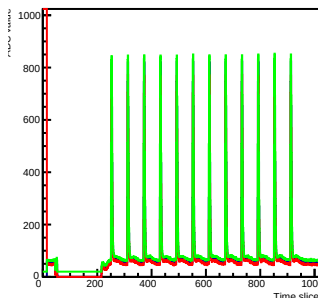
Run 1 Time mcm 0 chip 5 chan 7 s1-test3



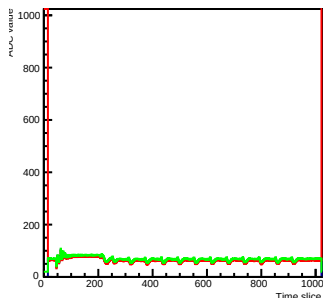
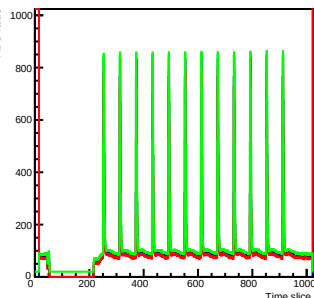
Run 1 Time mcm 0 chip 5 chan 9 s1-test3



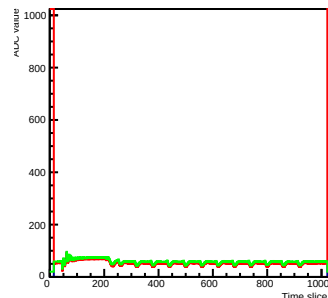
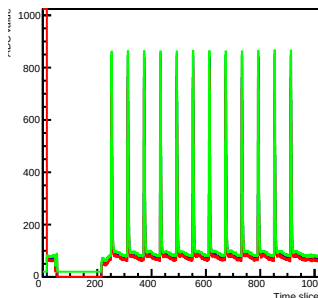
Run 1 Time mcm 0 chip 5 chan 11 s1-test3



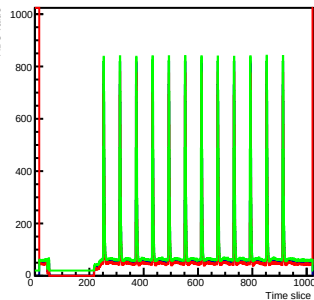
Run 1 Time mcm 0 chip 5 chan 13 s1-test3



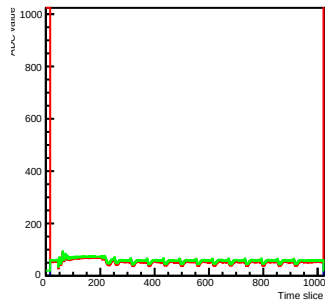
Run 1 Time mcm 0 chip 5 chan 15 s1-test3



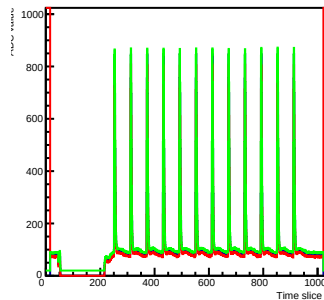
Run 1 Time mcm 0 chip 6 chan 0 s1-test3



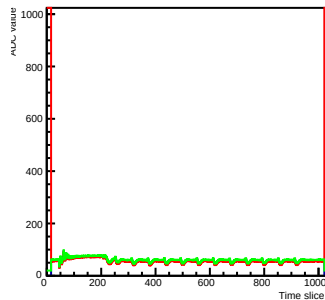
Run 1 Time mcm 0 chip 6 chan 1 s1-test3



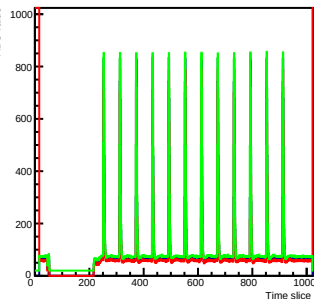
Run 1 Time mcm 0 chip 6 chan 2 s1-test3



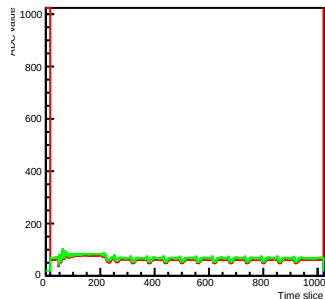
Run 1 Time mcm 0 chip 6 chan 3 s1-test3



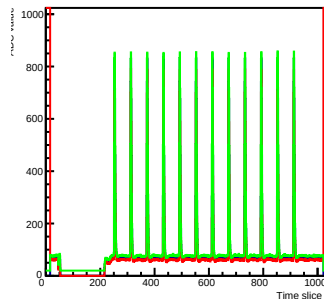
Run 1 Time mcm 0 chip 6 chan 4 s1-test3



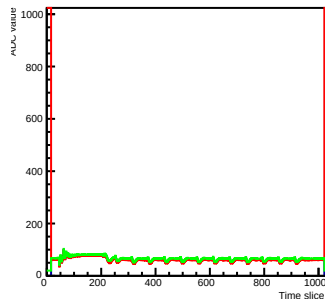
Run 1 Time mcm 0 chip 6 chan 5 s1-test3



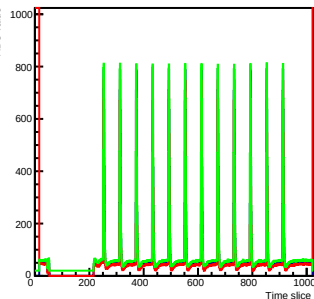
Run 1 Time mcm 0 chip 6 chan 6 s1-test3



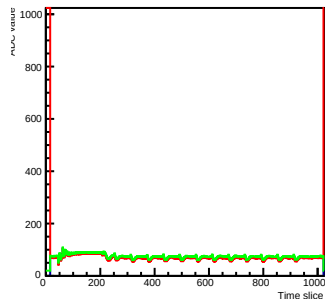
Run 1 Time mcm 0 chip 6 chan 7 s1-test3



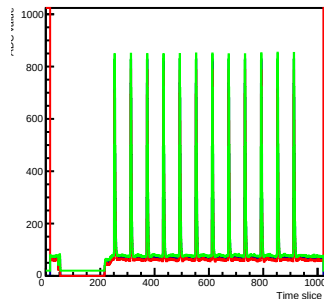
Run 1 Time mcm 0 chip 6 chan 8 s1-test3



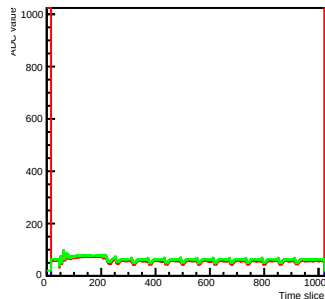
Run 1 Time mcm 0 chip 6 chan 9 s1-test3



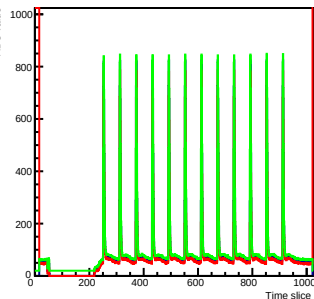
Run 1 Time mcm 0 chip 6 chan 10 s1-test3



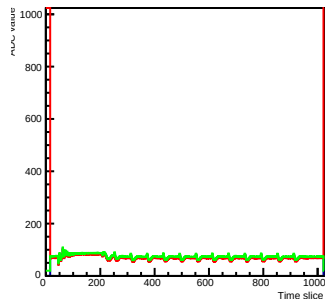
Run 1 Time mcm 0 chip 6 chan 11 s1-test3



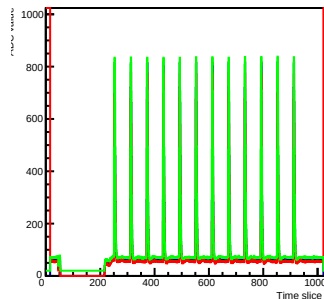
Run 1 Time mcm 0 chip 6 chan 12 s1-test3



Run 1 Time mcm 0 chip 6 chan 13 s1-test3



Run 1 Time mcm 0 chip 6 chan 14 s1-test3



Run 1 Time mcm 0 chip 6 chan 15 s1-test3

