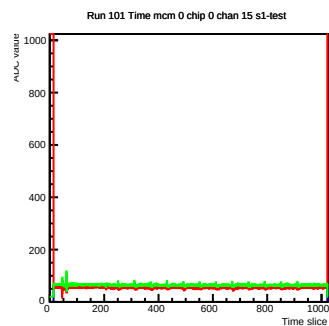
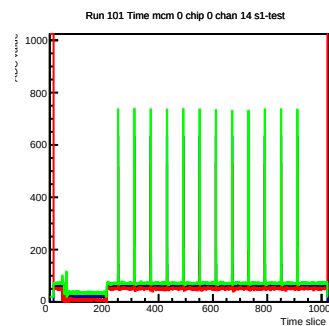
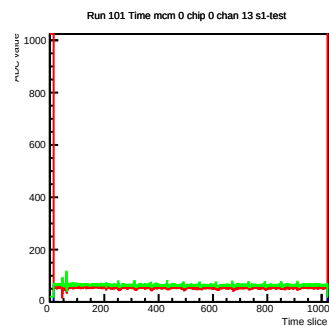
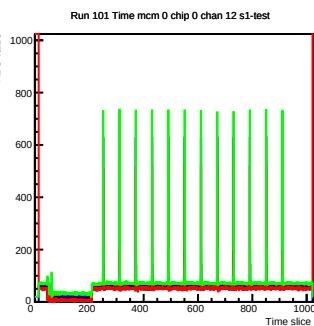
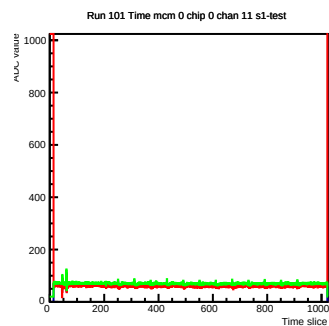
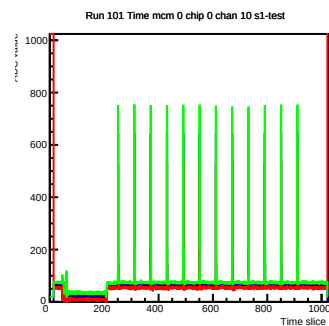
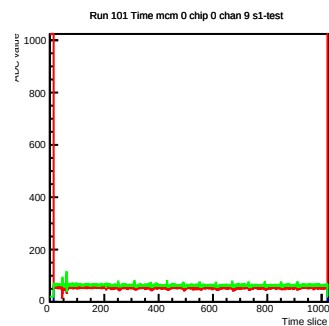
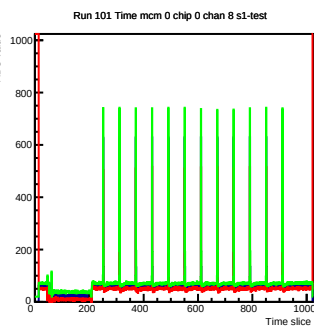
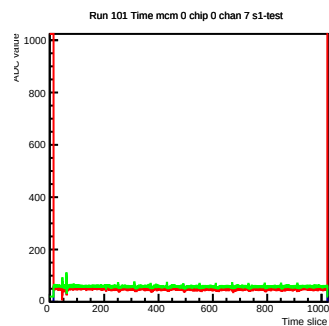
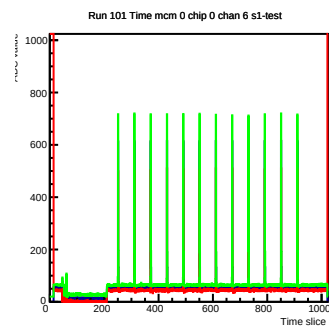
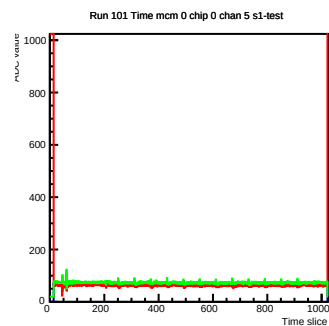
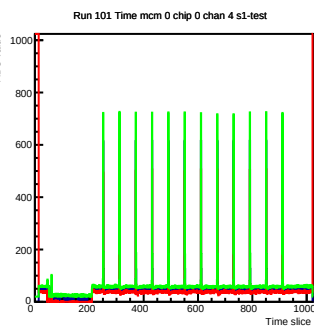
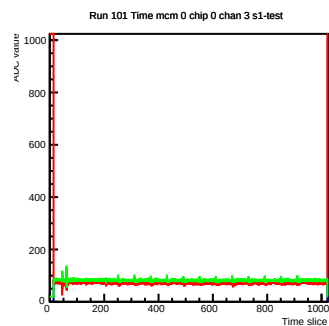
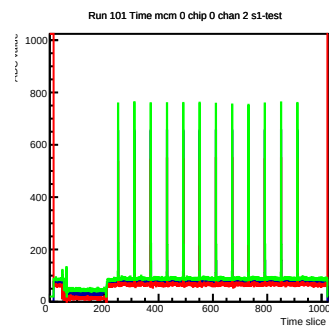
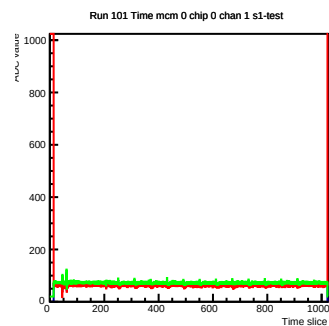
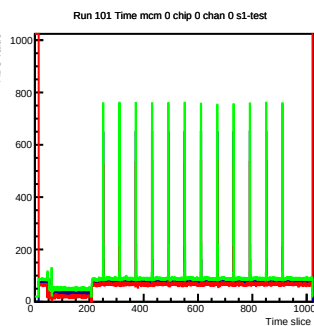
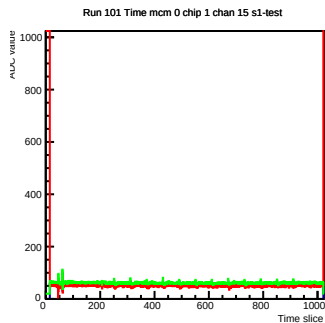
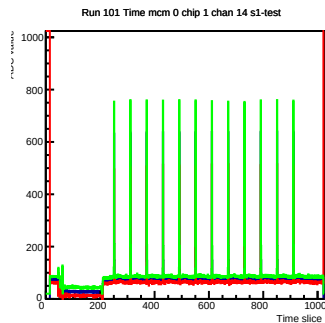
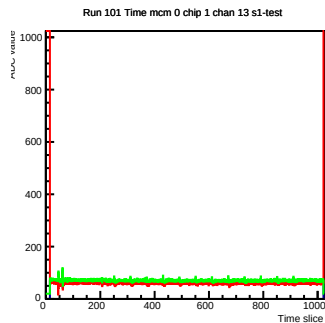
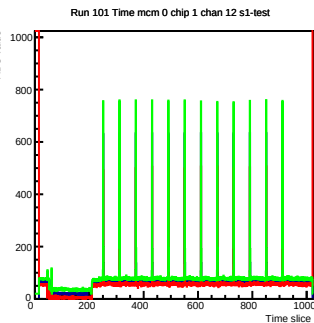
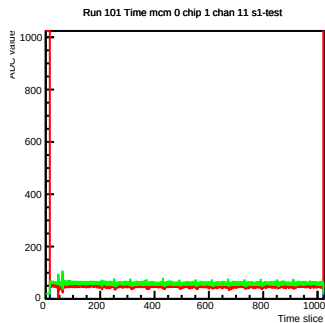
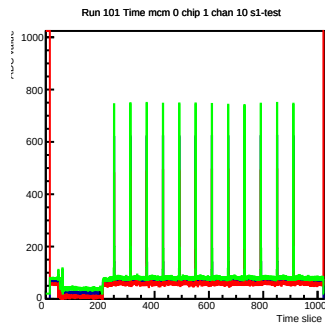
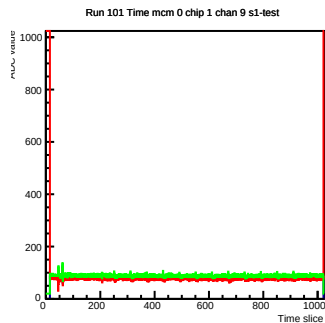
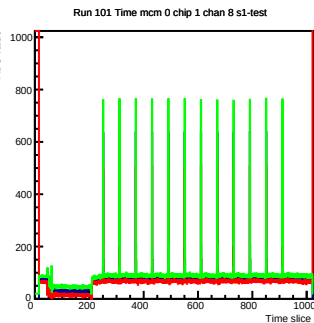
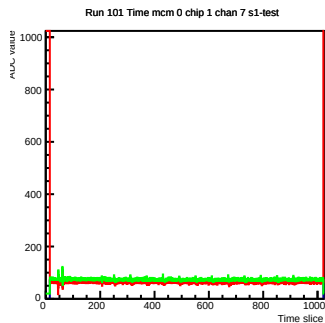
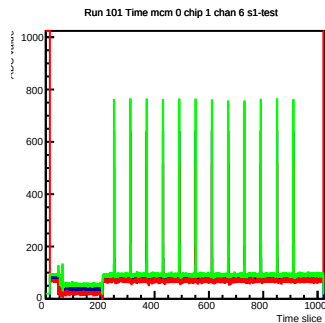
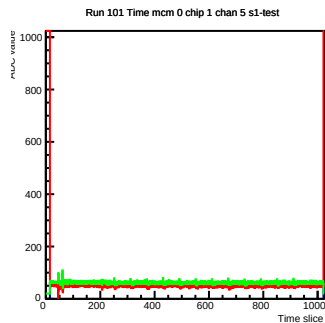
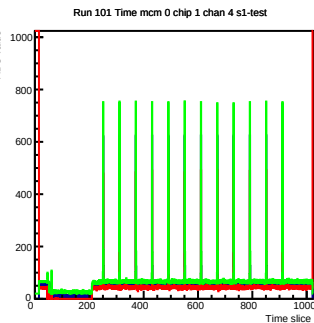
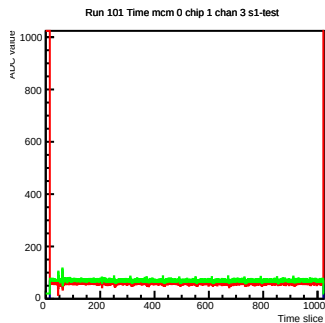
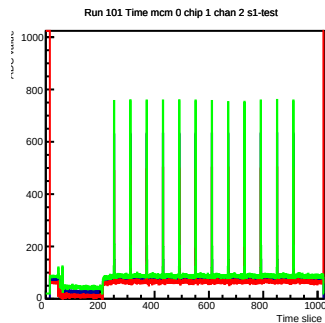
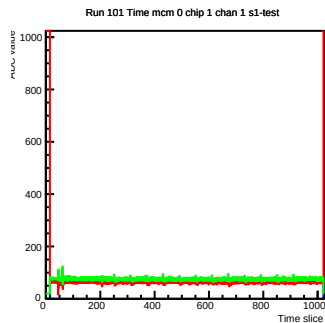
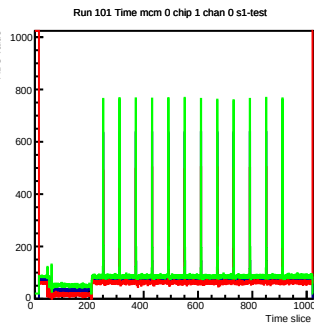
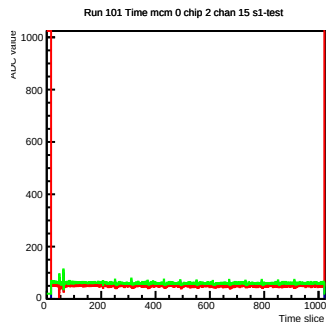
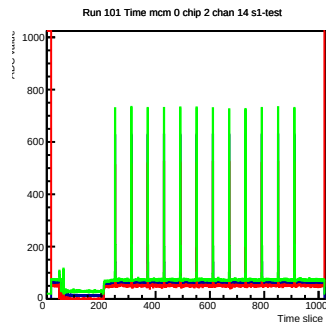
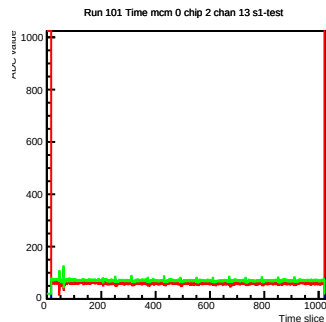
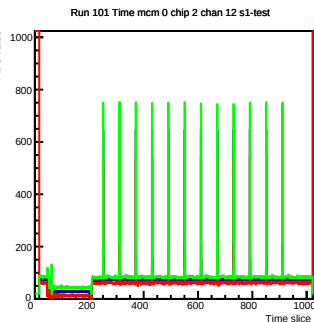
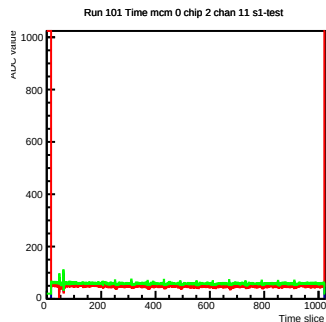
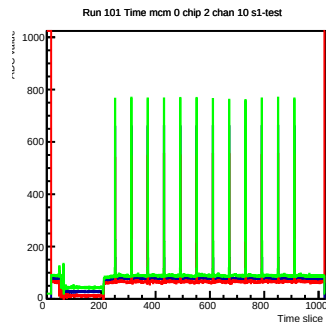
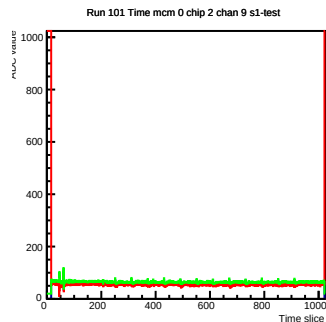
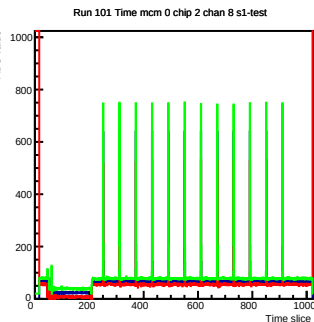
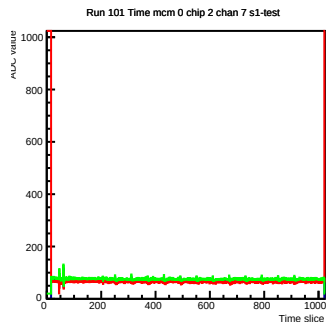
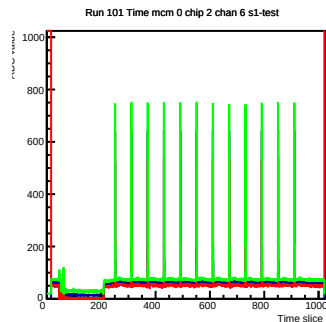
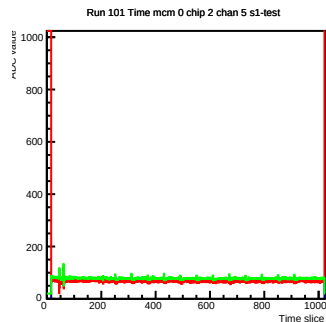
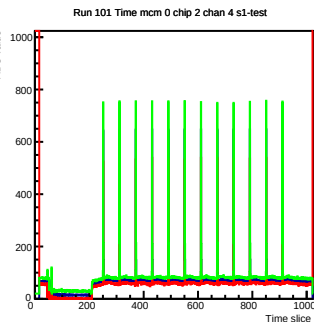
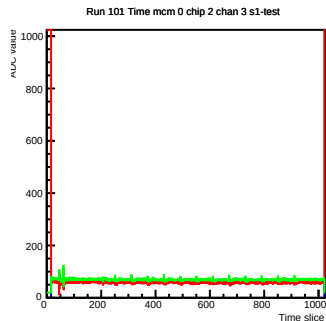
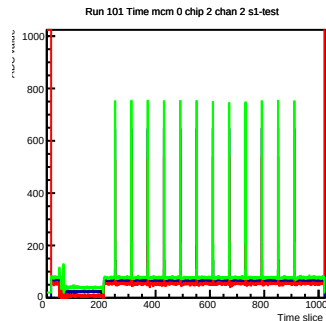
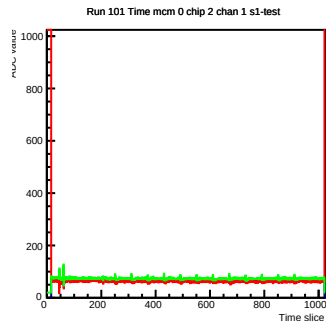
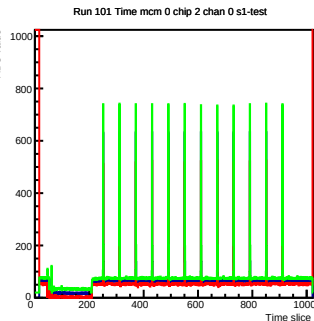
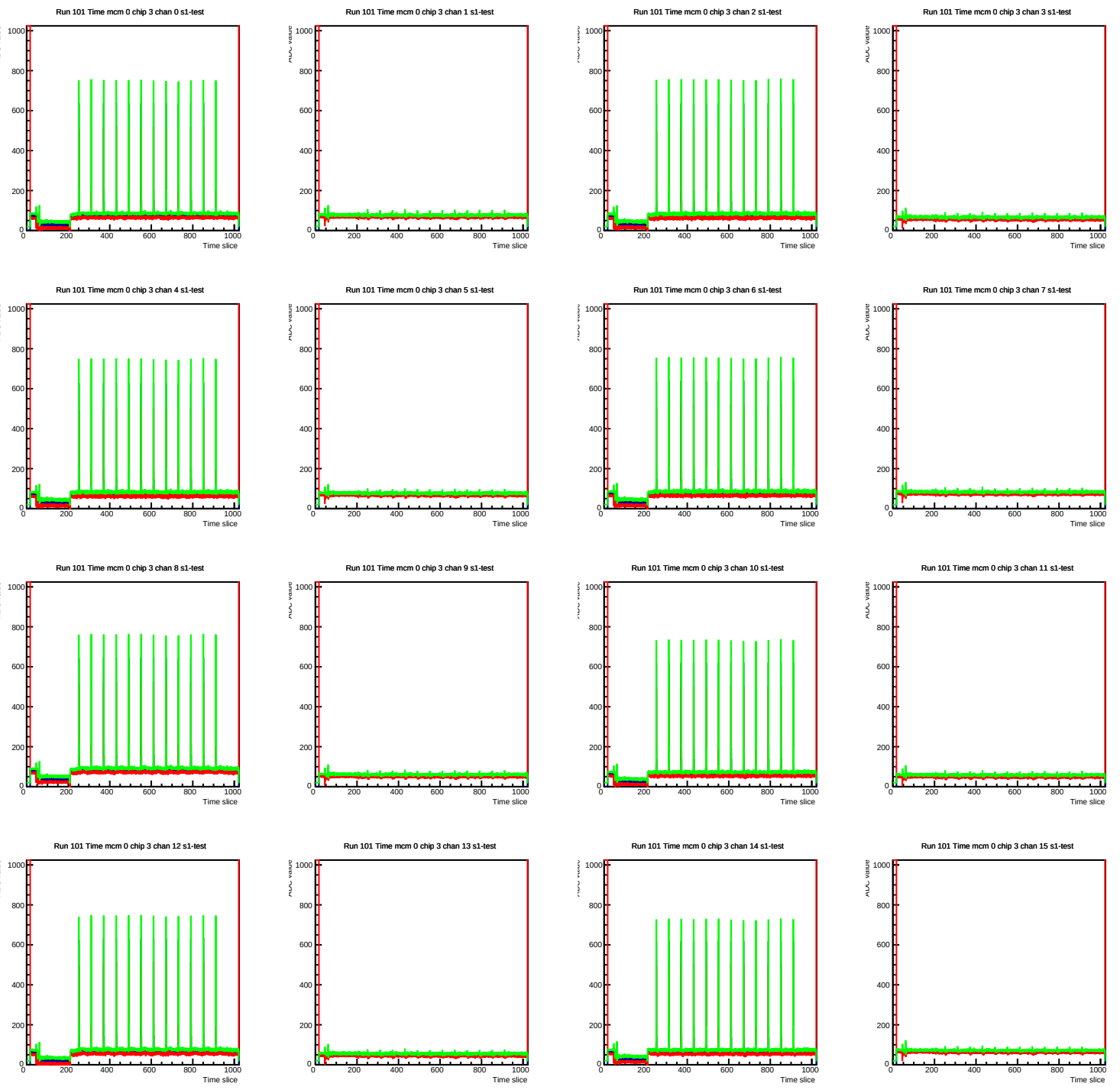
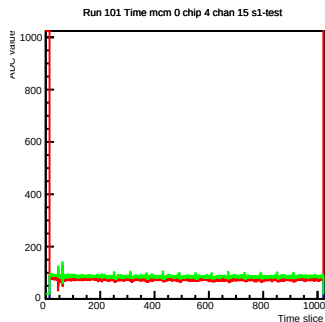
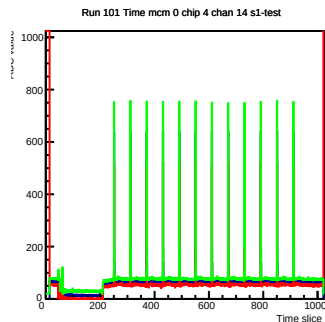
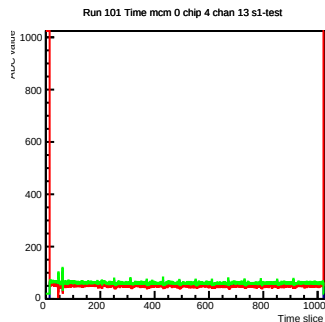
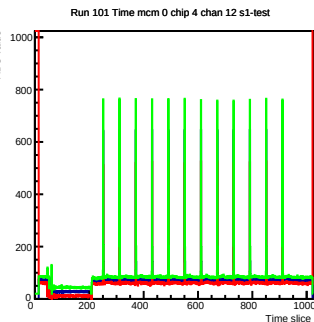
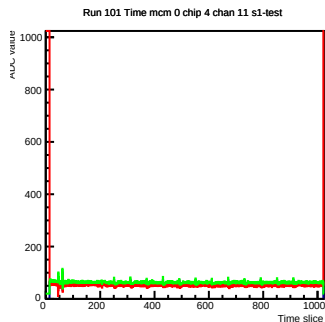
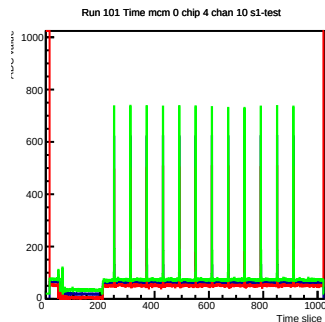
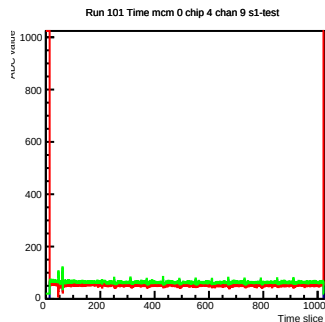
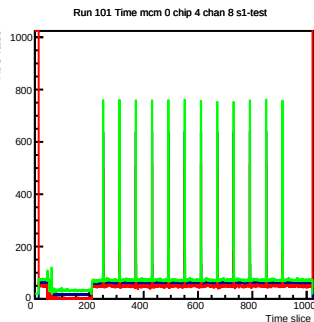
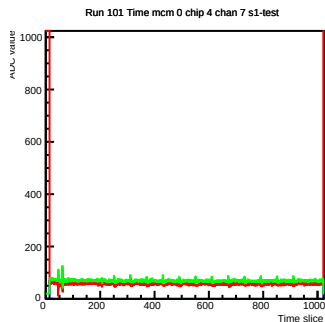
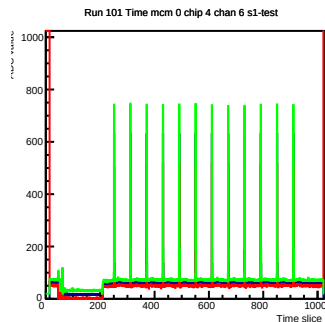
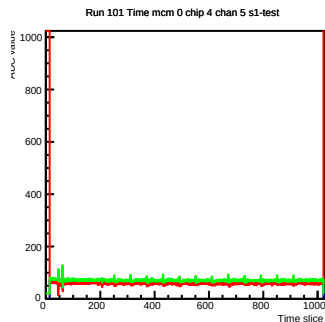
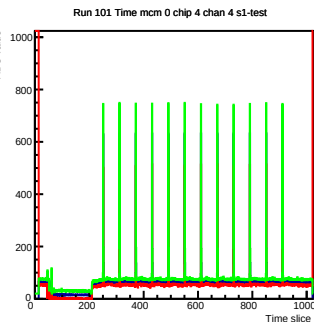
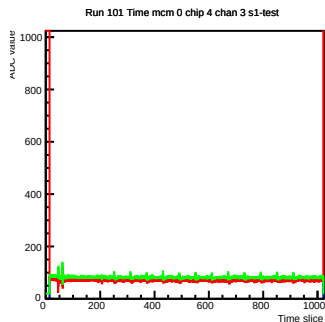
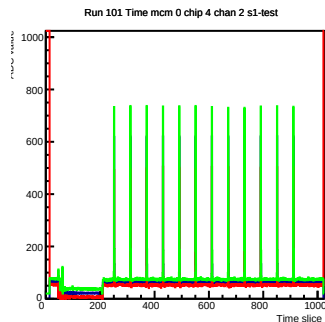
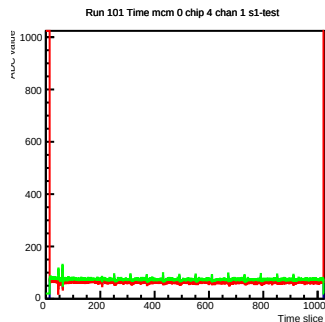
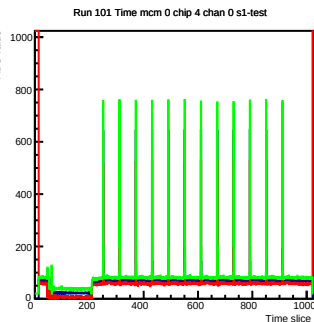




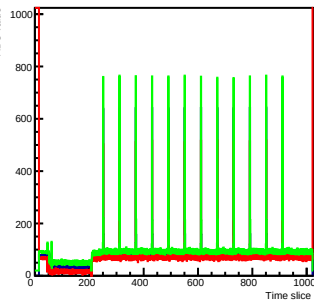




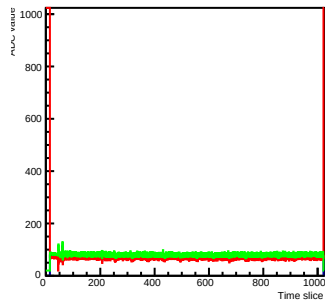




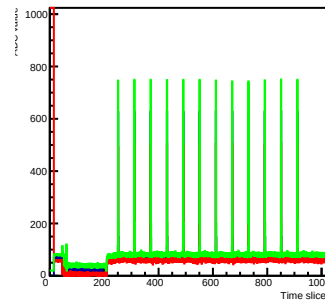
Run 101 Time mcm 0 chip 5 chan 0 s1-test



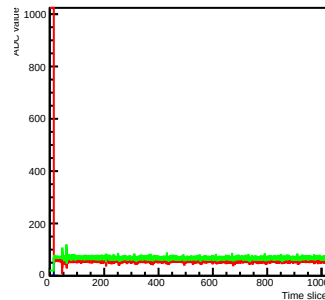
Run 101 Time mcm 0 chip 5 chan 1 s1-test



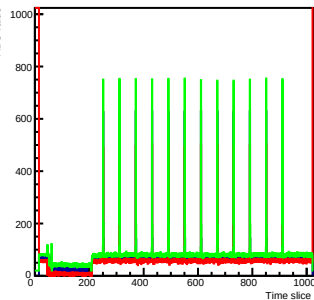
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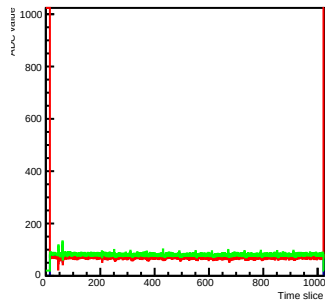
Run 101 Time mcm 0 chip 5 chan 3 s1-test



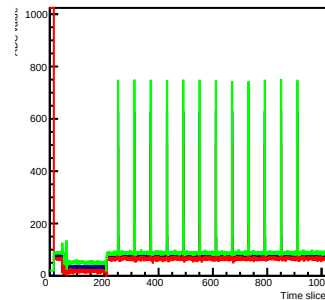
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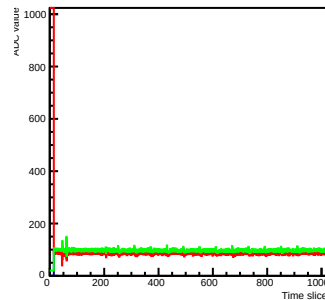
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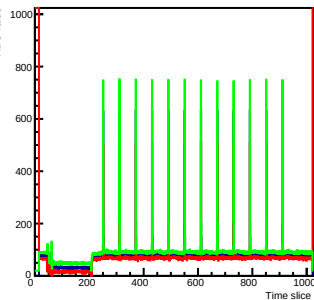
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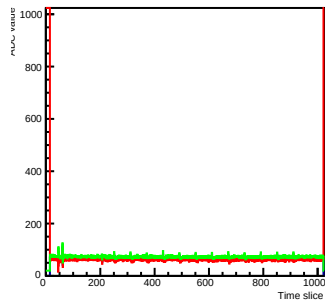
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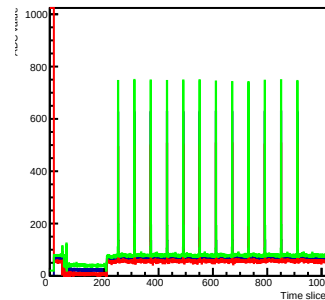
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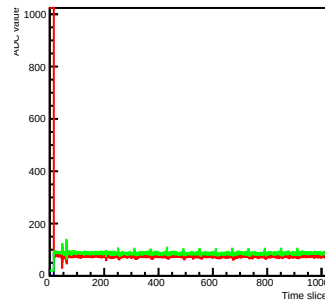
Run 101 Time mcm 0 chip 5 chan 9 s1-test



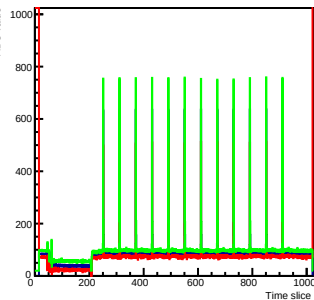
Run 101 Time mcm 0 chip 5 chan 10 s1-test



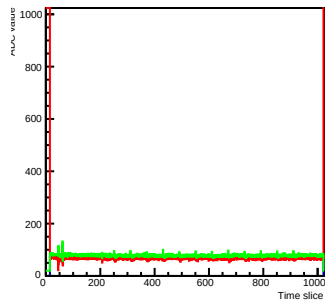
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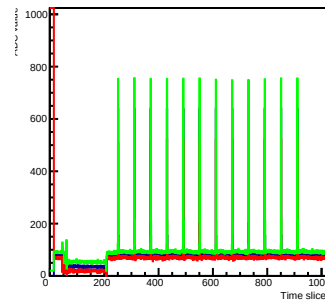
Run 101 Time mcm 0 chip 5 chan 12 s1-test



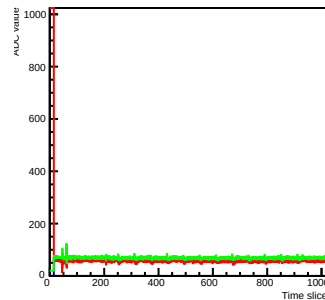
Run 101 Time mcm 0 chip 5 chan 13 s1-test

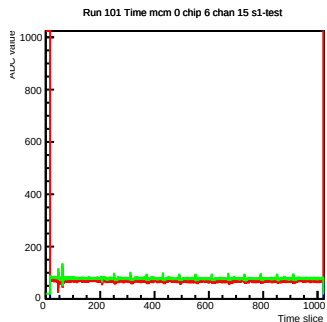
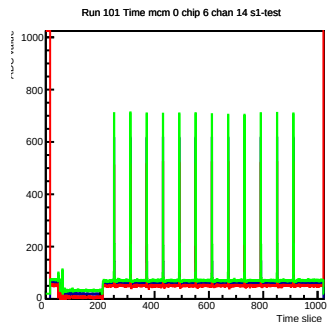
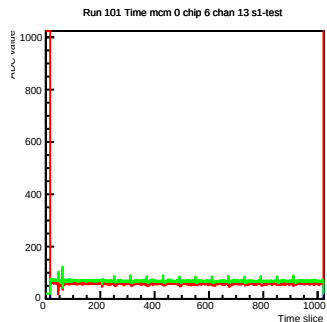
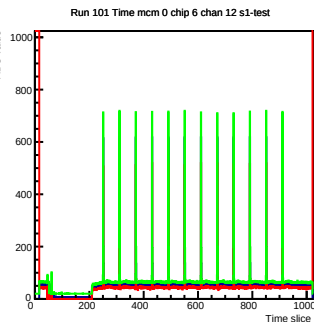
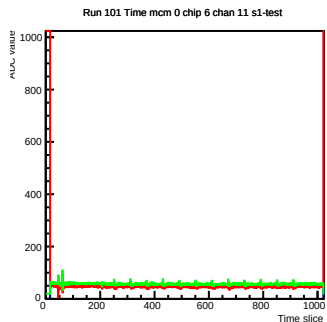
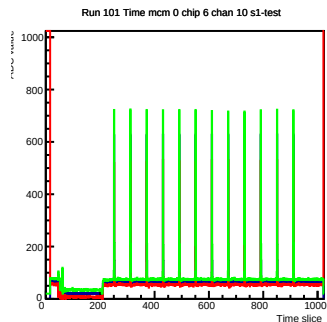
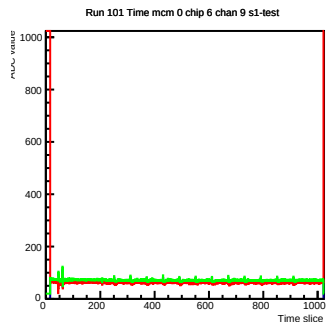
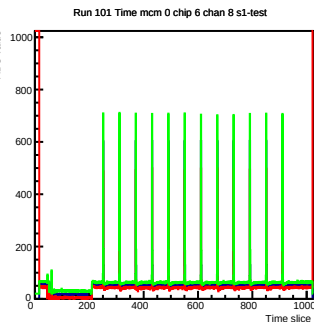
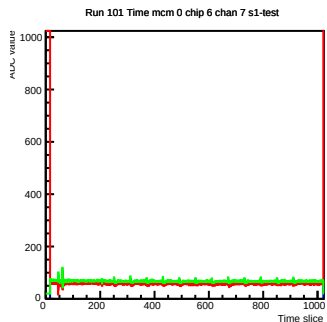
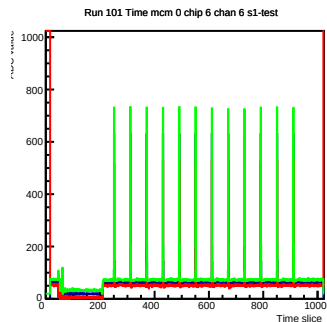
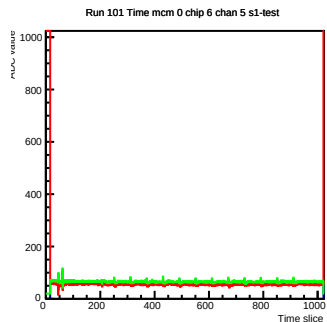
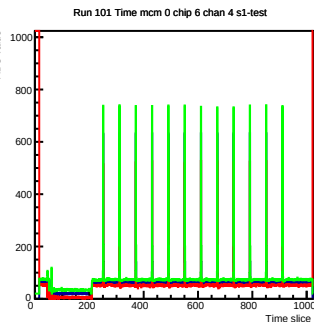
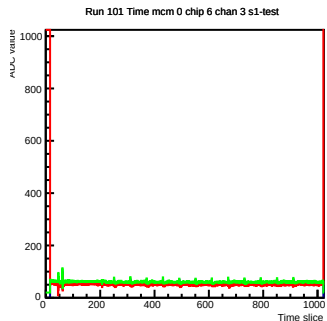
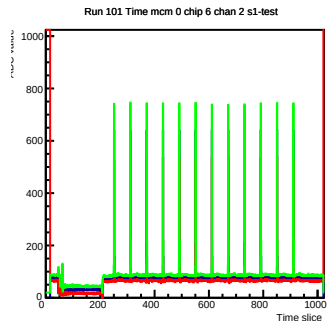
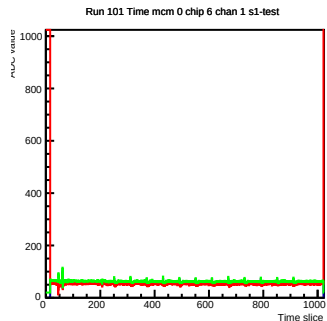
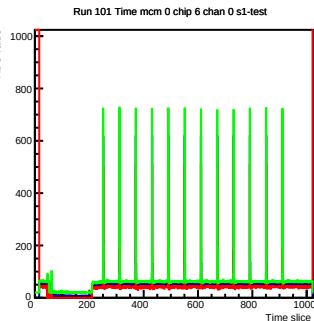


Run 101 Time mcm 0 chip 5 chan 14 s1-test

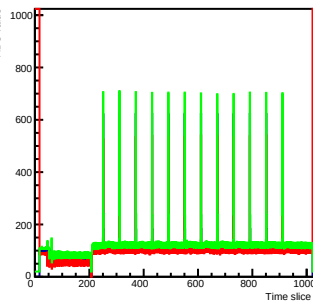


Run 101 Time mcm 0 chip 5 chan 15 s1-test

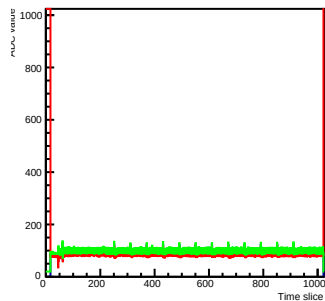




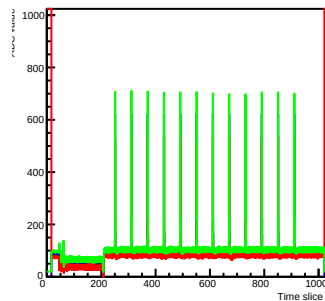
Run 101 Time mcm 0 chip 7 chan 0 s1-test



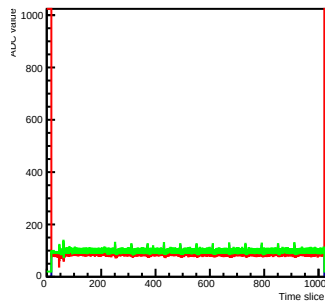
Run 101 Time mcm 0 chip 7 chan 1 s1-test



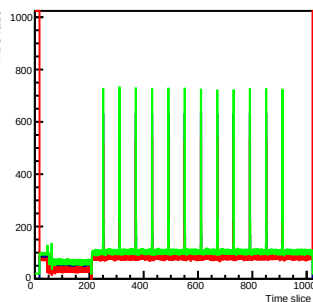
Run 101 Time mcm 0 chip 7 chan 2 s1-test



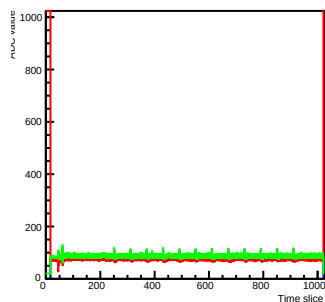
Run 101 Time mcm 0 chip 7 chan 3 s1-test



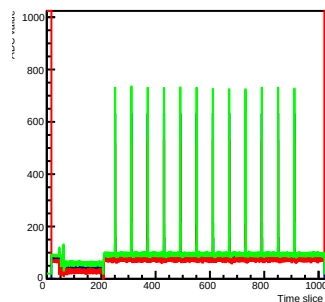
Run 101 Time mcm 0 chip 7 chan 4 s1-test



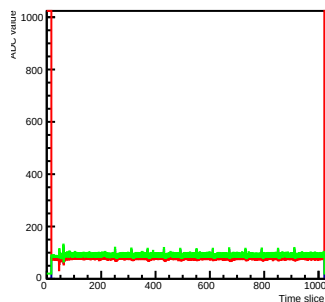
Run 101 Time mcm 0 chip 7 chan 5 s1-test



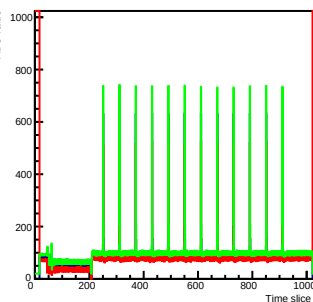
Run 101 Time mcm 0 chip 7 chan 6 s1-test



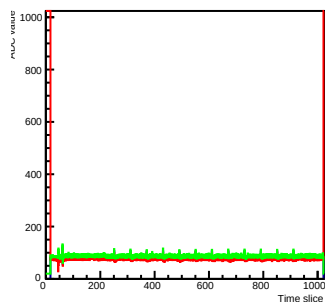
Run 101 Time mcm 0 chip 7 chan 7 s1-test



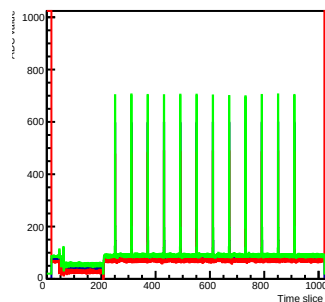
Run 101 Time mcm 0 chip 7 chan 8 s1-test



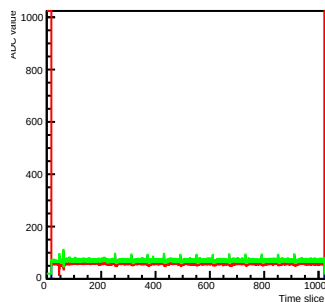
Run 101 Time mcm 0 chip 7 chan 9 s1-test



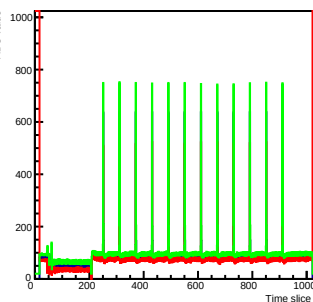
Run 101 Time mcm 0 chip 7 chan 10 s1-test



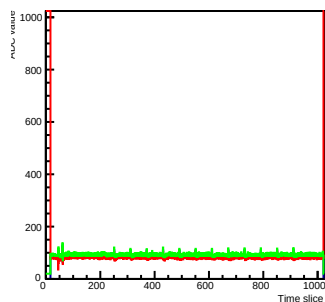
Run 101 Time mcm 0 chip 7 chan 11 s1-test



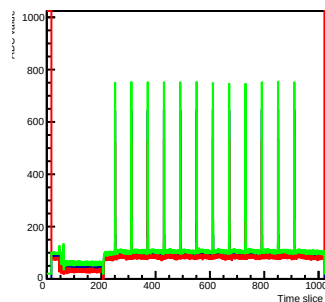
Run 101 Time mcm 0 chip 7 chan 12 s1-test



Run 101 Time mcm 0 chip 7 chan 13 s1-test



Run 101 Time mcm 0 chip 7 chan 14 s1-test



Run 101 Time mcm 0 chip 7 chan 15 s1-test

