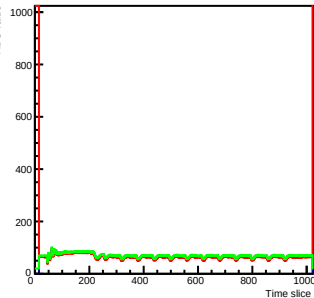
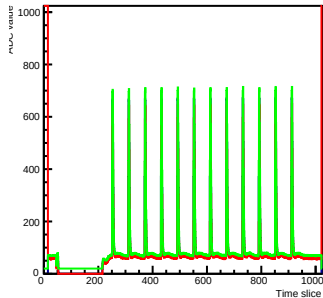




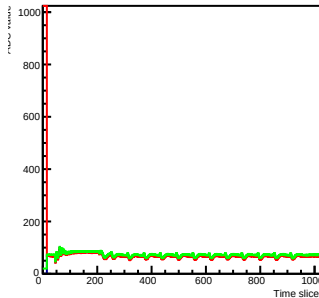
Run 2 Time mcm 0 chip 1 chan 0 s2-test3



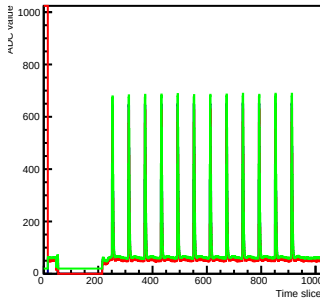
Run 2 Time mcm 0 chip 1 chan 1 s2-test3



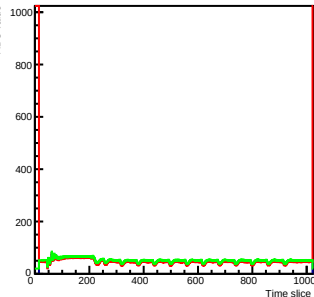
Run 2 Time mcm 0 chip 1 chan 2 s2-test3



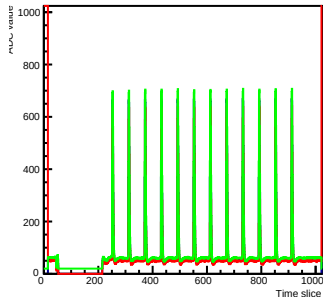
Run 2 Time mcm 0 chip 1 chan 3 s2-test3



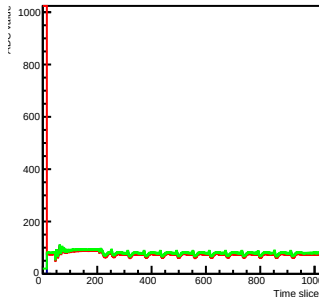
Run 2 Time mcm 0 chip 1 chan 4 s2-test3



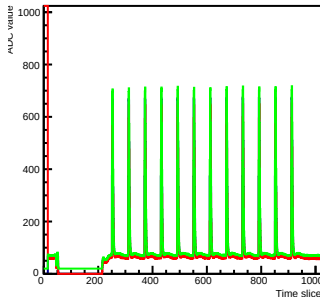
Run 2 Time mcm 0 chip 1 chan 5 s2-test3



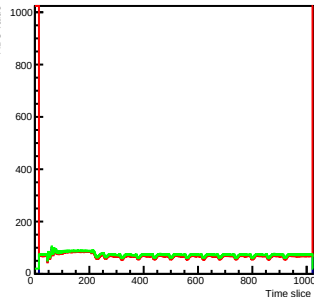
Run 2 Time mcm 0 chip 1 chan 6 s2-test3



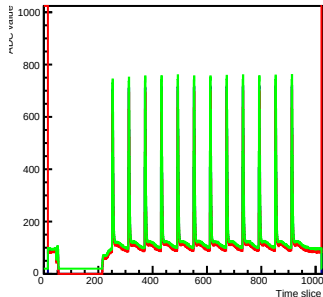
Run 2 Time mcm 0 chip 1 chan 7 s2-test3



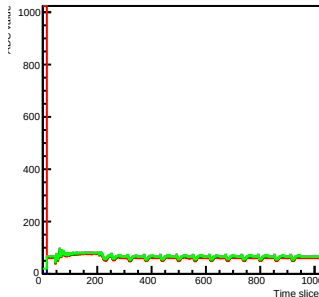
Run 2 Time mcm 0 chip 1 chan 8 s2-test3



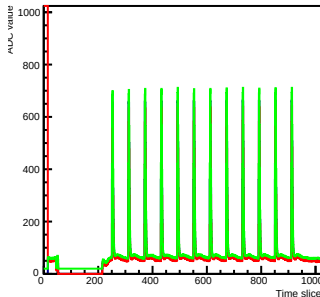
Run 2 Time mcm 0 chip 1 chan 9 s2-test3



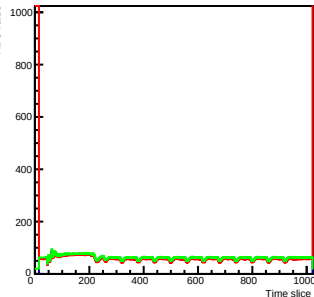
Run 2 Time mcm 0 chip 1 chan 10 s2-test3



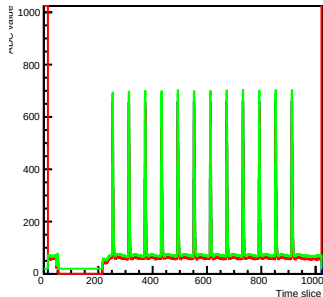
Run 2 Time mcm 0 chip 1 chan 11 s2-test3



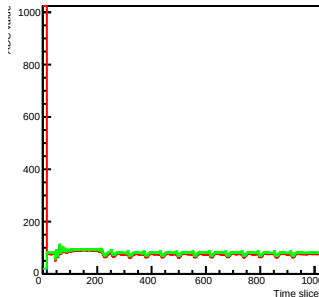
Run 2 Time mcm 0 chip 1 chan 12 s2-test3



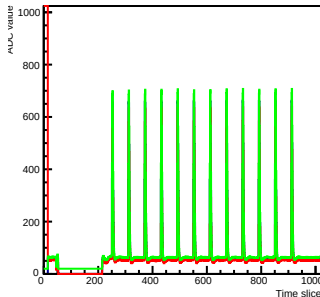
Run 2 Time mcm 0 chip 1 chan 13 s2-test3



Run 2 Time mcm 0 chip 1 chan 14 s2-test3

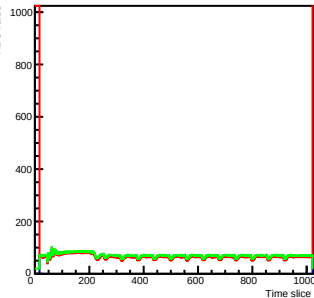


Run 2 Time mcm 0 chip 1 chan 15 s2-test3

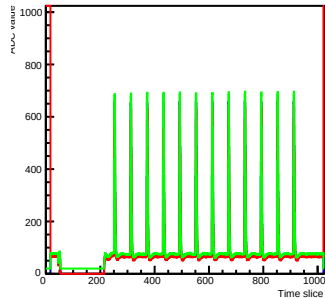




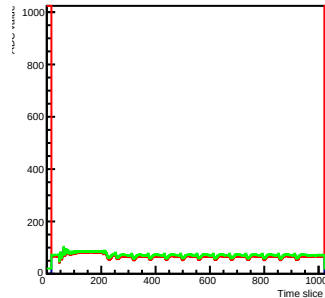
Run 2 Time mcm 0 chip 3 chan 0 s2-test3



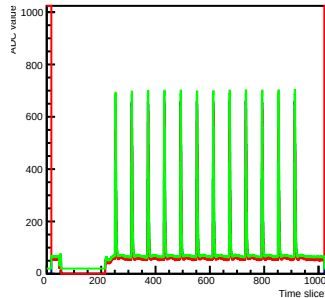
Run 2 Time mcm 0 chip 3 chan 1 s2-test3



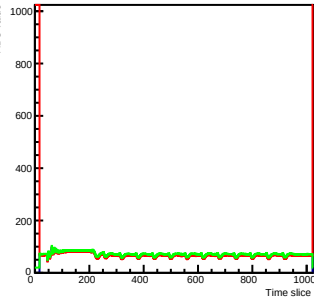
Run 2 Time mcm 0 chip 3 chan 2 s2-test3



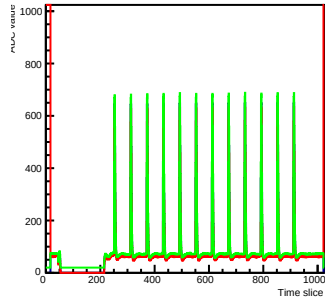
Run 2 Time mcm 0 chip 3 chan 3 s2-test3



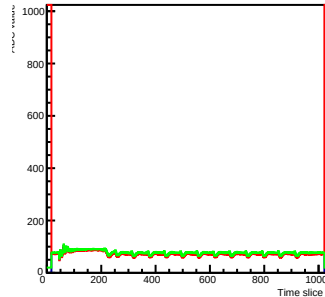
Run 2 Time mcm 0 chip 3 chan 4 s2-test3



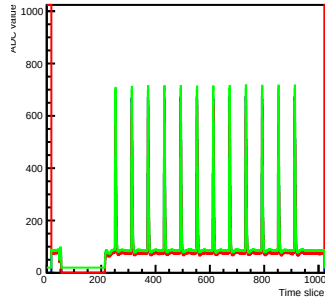
Run 2 Time mcm 0 chip 3 chan 5 s2-test3



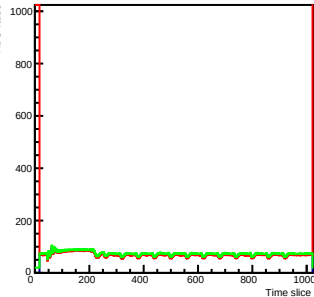
Run 2 Time mcm 0 chip 3 chan 6 s2-test3



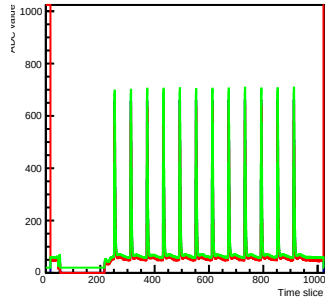
Run 2 Time mcm 0 chip 3 chan 7 s2-test3



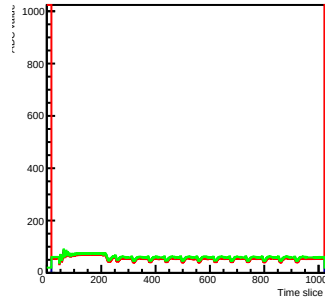
Run 2 Time mcm 0 chip 3 chan 8 s2-test3



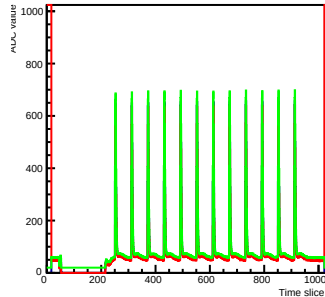
Run 2 Time mcm 0 chip 3 chan 9 s2-test3



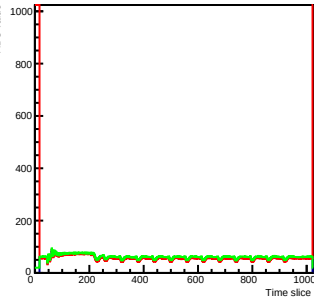
Run 2 Time mcm 0 chip 3 chan 10 s2-test3



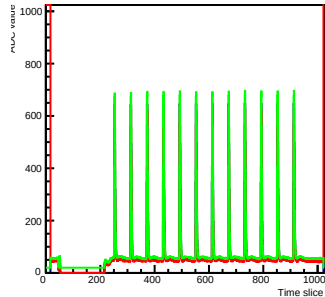
Run 2 Time mcm 0 chip 3 chan 11 s2-test3



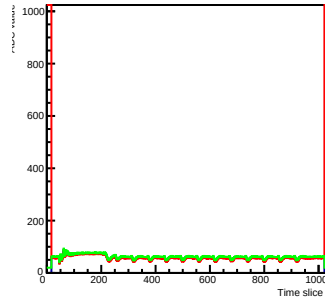
Run 2 Time mcm 0 chip 3 chan 12 s2-test3



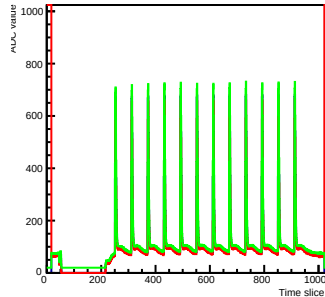
Run 2 Time mcm 0 chip 3 chan 13 s2-test3



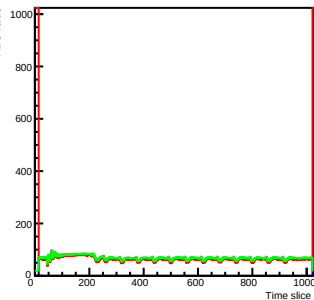
Run 2 Time mcm 0 chip 3 chan 14 s2-test3



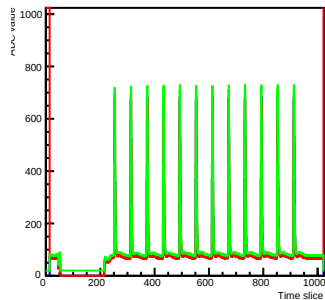
Run 2 Time mcm 0 chip 3 chan 15 s2-test3



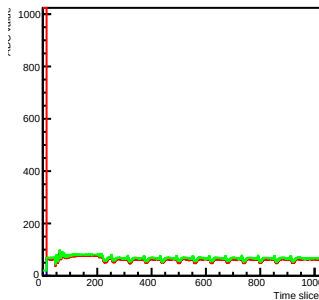
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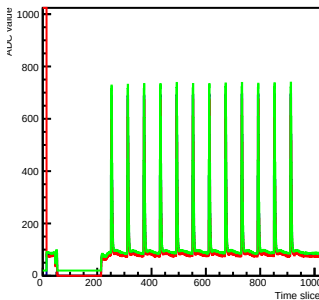
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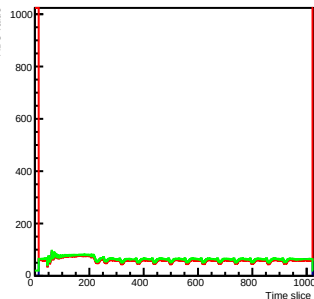
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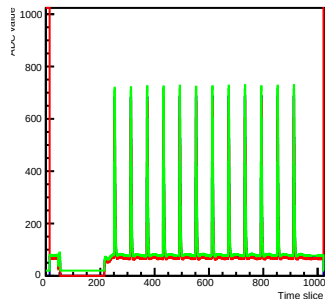
Run 2 Time mcm 0 chip 4 chan 3 s2-test3



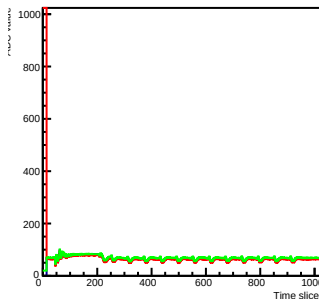
Run 2 Time mcm 0 chip 4 chan 4 s2-test3



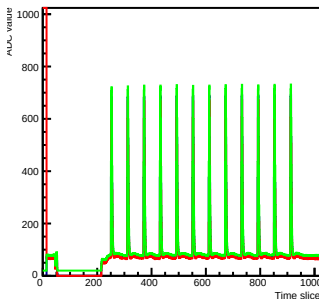
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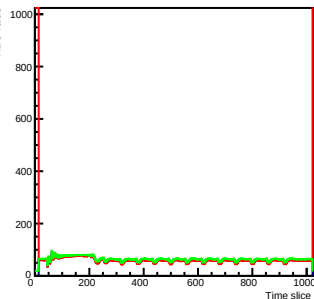
Run 2 Time mcm 0 chip 4 chan 6 s2-test3



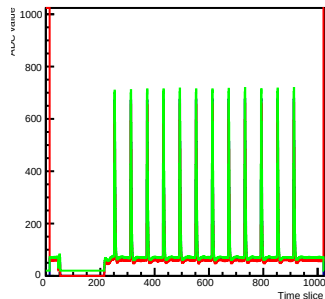
Run 2 Time mcm 0 chip 4 chan 7 s2-test3



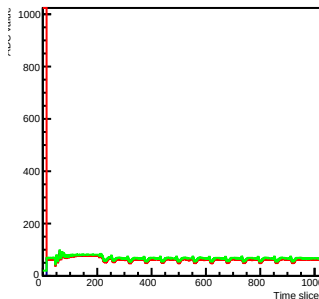
Run 2 Time mcm 0 chip 4 chan 8 s2-test3



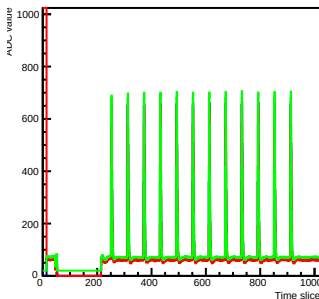
Run 2 Time mcm 0 chip 4 chan 9 s2-test3



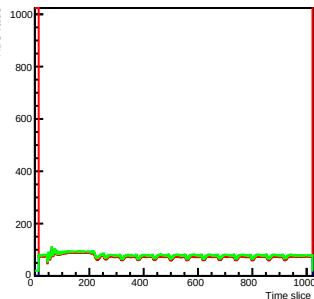
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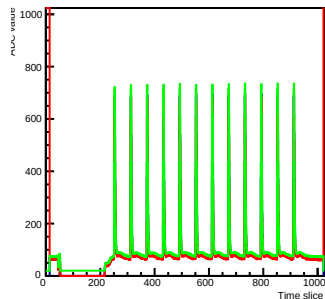
Run 2 Time mcm 0 chip 4 chan 11 s2-test3



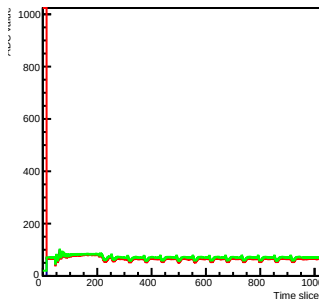
Run 2 Time mcm 0 chip 4 chan 12 s2-test3



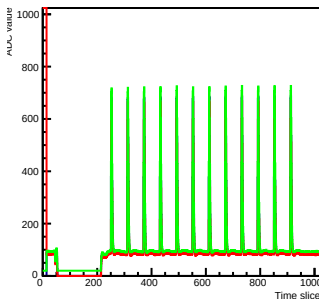
Run 2 Time mcm 0 chip 4 chan 13 s2-test3



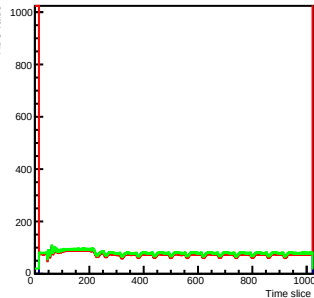
Run 2 Time mcm 0 chip 4 chan 14 s2-test3



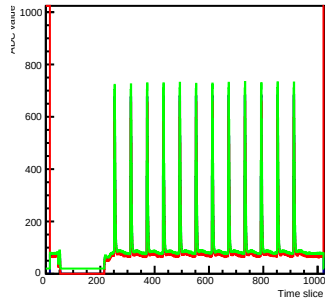
Run 2 Time mcm 0 chip 4 chan 15 s2-test3



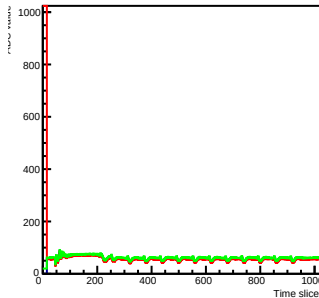
Run 2 Time mcm 0 chip 5 chan 0 s2-test3



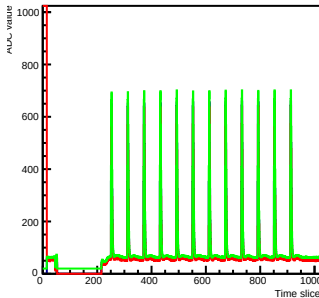
Run 2 Time mcm 0 chip 5 chan 1 s2-test3



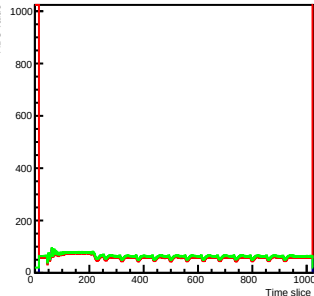
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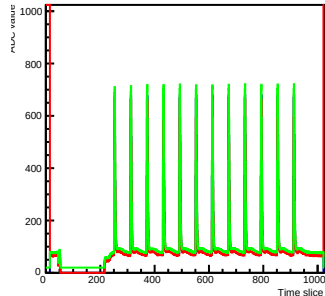
Run 2 Time mcm 0 chip 5 chan 3 s2-test3



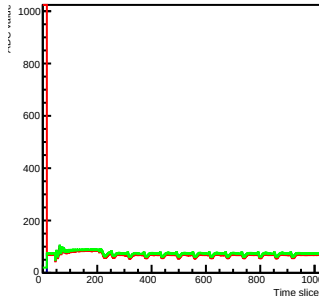
Run 2 Time mcm 0 chip 5 chan 4 s2-test3



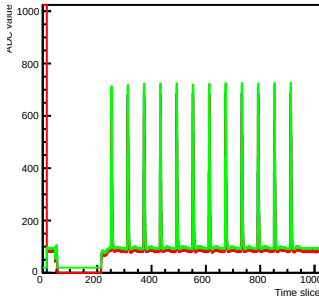
Run 2 Time mcm 0 chip 5 chan 5 s2-test3



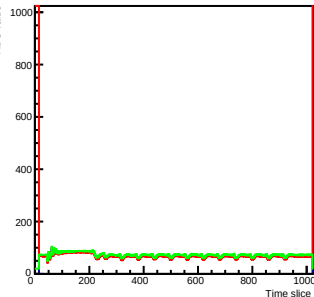
Run 2 Time mcm 0 chip 5 chan 6 s2-test3



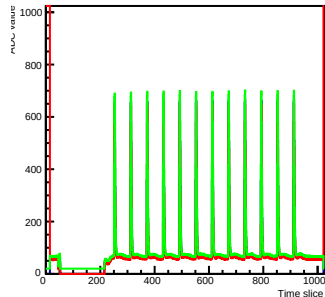
Run 2 Time mcm 0 chip 5 chan 7 s2-test3



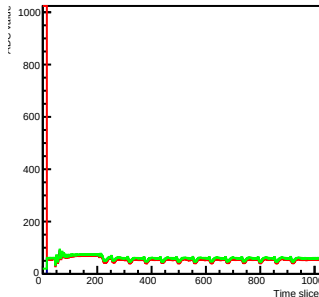
Run 2 Time mcm 0 chip 5 chan 8 s2-test3



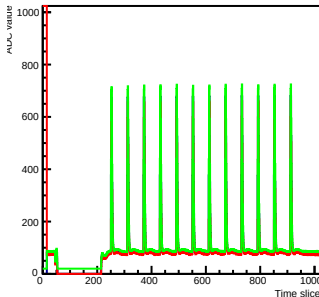
Run 2 Time mcm 0 chip 5 chan 9 s2-test3



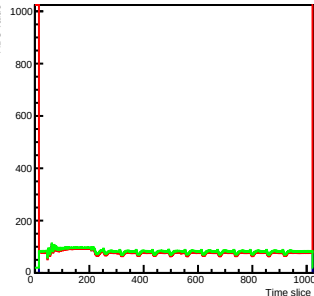
Run 2 Time mcm 0 chip 5 chan 10 s2-test3



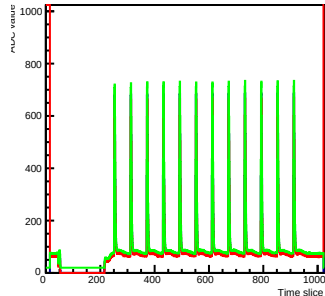
Run 2 Time mcm 0 chip 5 chan 11 s2-test3



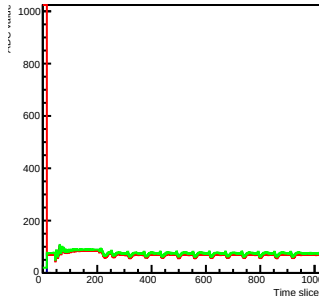
Run 2 Time mcm 0 chip 5 chan 12 s2-test3



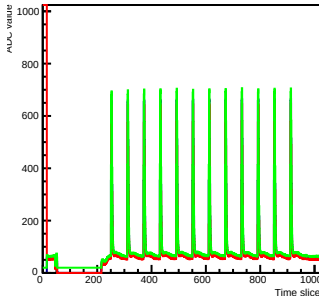
Run 2 Time mcm 0 chip 5 chan 13 s2-test3



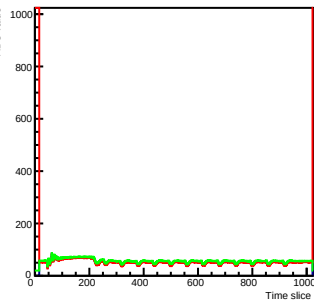
Run 2 Time mcm 0 chip 5 chan 14 s2-test3



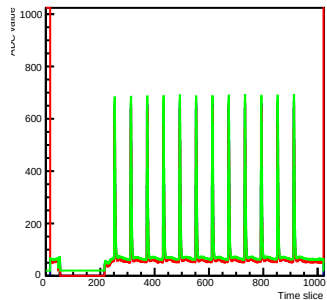
Run 2 Time mcm 0 chip 5 chan 15 s2-test3



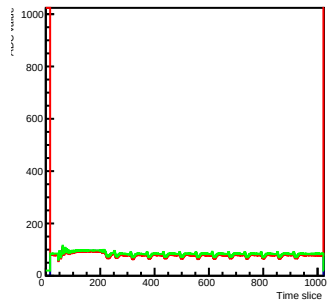
Run 2 Time mcm 0 chip 6 chan 0 s2-test3



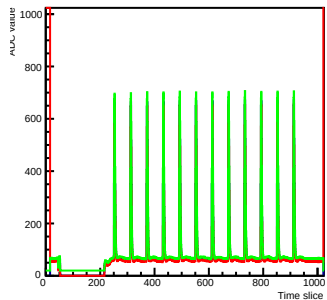
Run 2 Time mcm 0 chip 6 chan 1 s2-test3



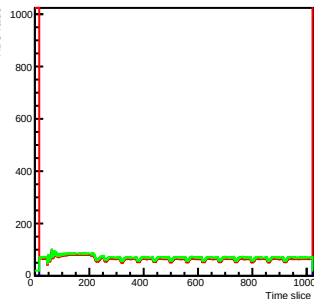
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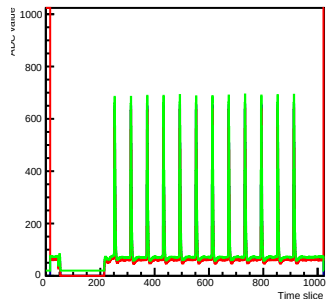
Run 2 Time mcm 0 chip 6 chan 3 s2-test3



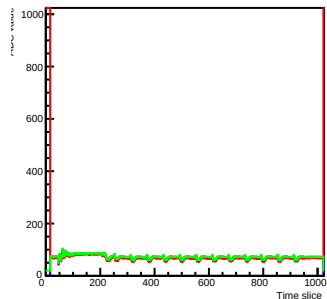
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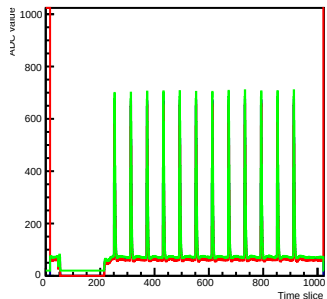
Run 2 Time mcm 0 chip 6 chan 5 s2-test3



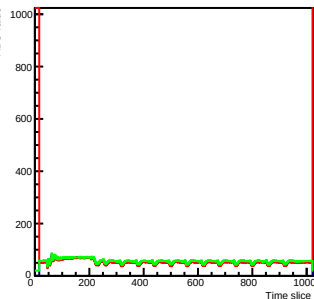
Run 2 Time mcm 0 chip 6 chan 6 s2-test3



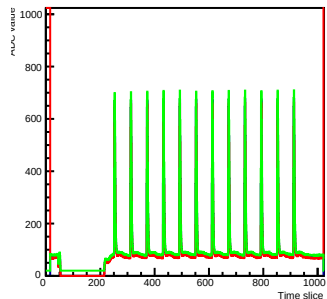
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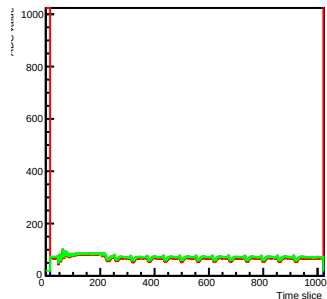
Run 2 Time mcm 0 chip 6 chan 8 s2-test3



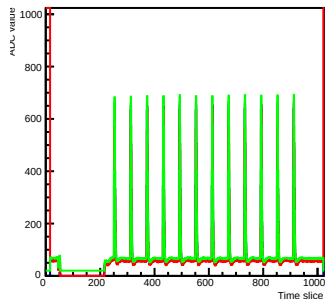
Run 2 Time mcm 0 chip 6 chan 9 s2-test3



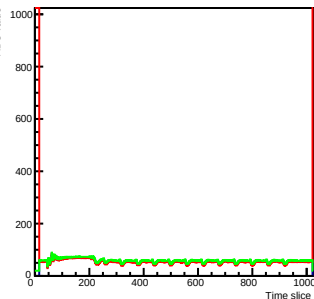
Run 2 Time mcm 0 chip 6 chan 10 s2-test3



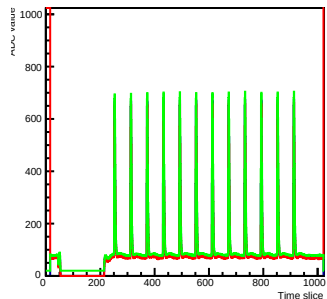
Run 2 Time mcm 0 chip 6 chan 11 s2-test3



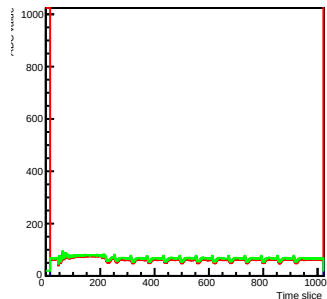
Run 2 Time mcm 0 chip 6 chan 12 s2-test3



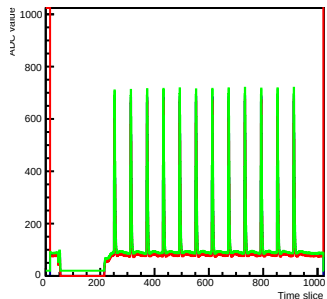
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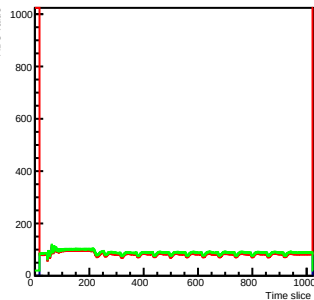
Run 2 Time mcm 0 chip 6 chan 14 s2-test3



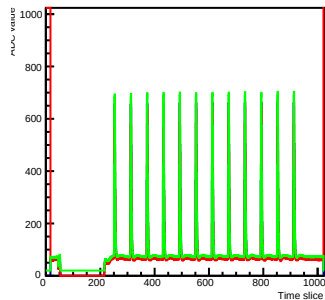
Run 2 Time mcm 0 chip 6 chan 15 s2-test3



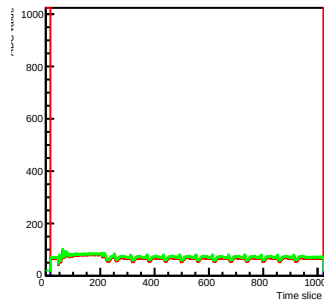
Run 2 Time mcm 0 chip 7 chan 0 s2-test3



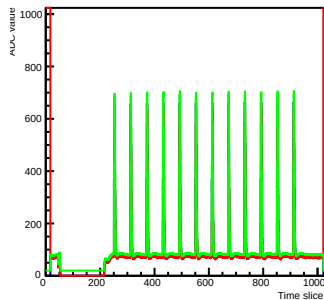
Run 2 Time mcm 0 chip 7 chan 1 s2-test3



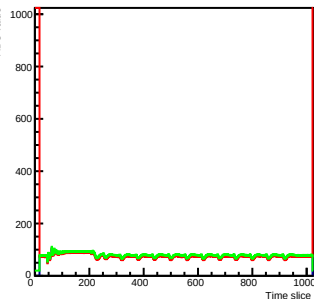
Run 2 Time mcm 0 chip 7 chan 2 s2-test3



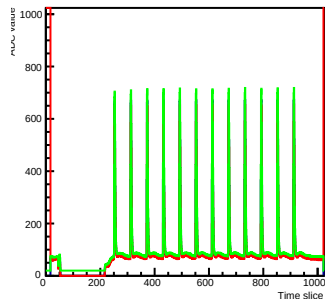
Run 2 Time mcm 0 chip 7 chan 3 s2-test3



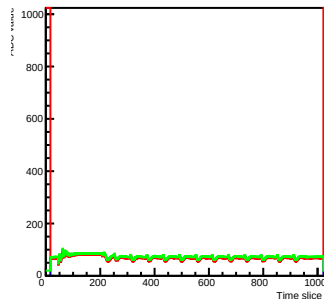
Run 2 Time mcm 0 chip 7 chan 4 s2-test3



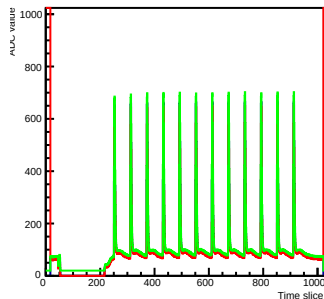
Run 2 Time mcm 0 chip 7 chan 5 s2-test3



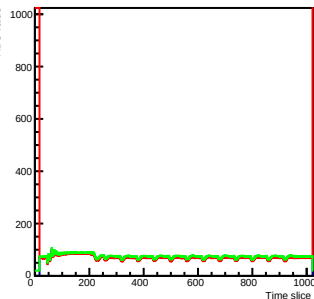
Run 2 Time mcm 0 chip 7 chan 6 s2-test3



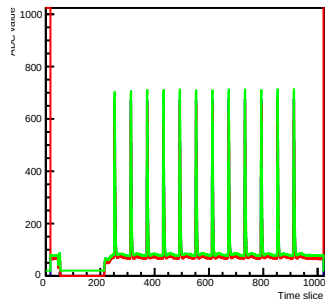
Run 2 Time mcm 0 chip 7 chan 7 s2-test3



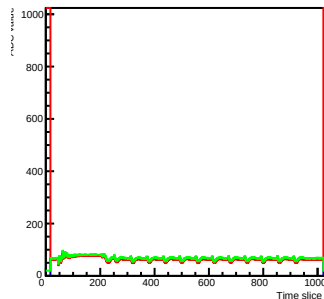
Run 2 Time mcm 0 chip 7 chan 8 s2-test3



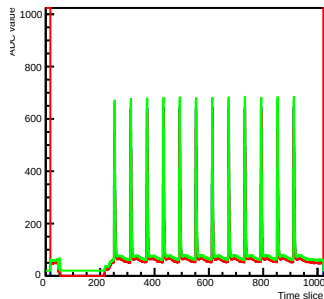
Run 2 Time mcm 0 chip 7 chan 9 s2-test3



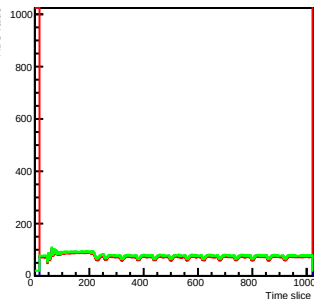
Run 2 Time mcm 0 chip 7 chan 10 s2-test3



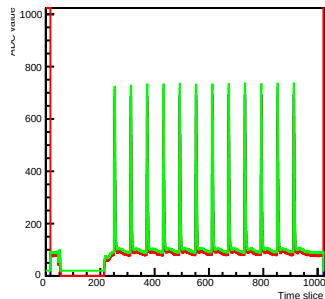
Run 2 Time mcm 0 chip 7 chan 11 s2-test3



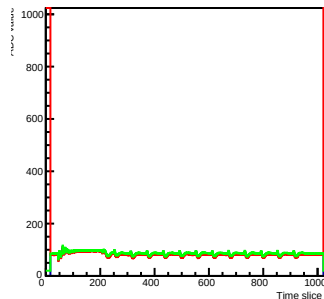
Run 2 Time mcm 0 chip 7 chan 12 s2-test3



Run 2 Time mcm 0 chip 7 chan 13 s2-test3



Run 2 Time mcm 0 chip 7 chan 14 s2-test3



Run 2 Time mcm 0 chip 7 chan 15 s2-test3

