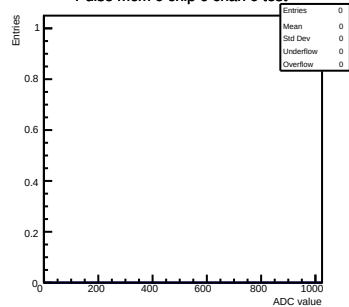
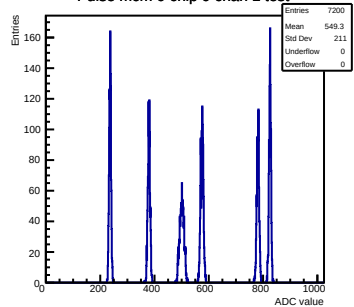


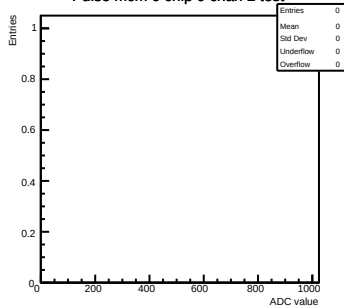
Pulse mcm 0 chip 0 chan 0 test



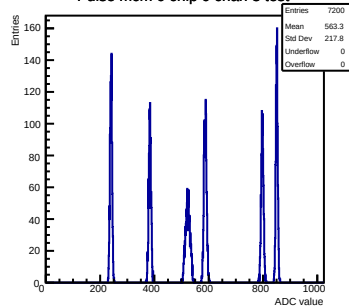
Pulse mcm 0 chip 0 chan 1 test



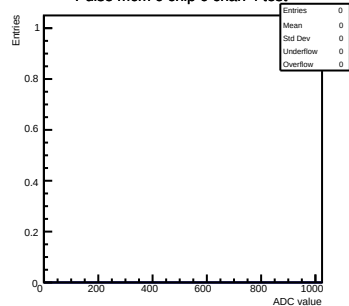
Pulse mcm 0 chip 0 chan 2 test



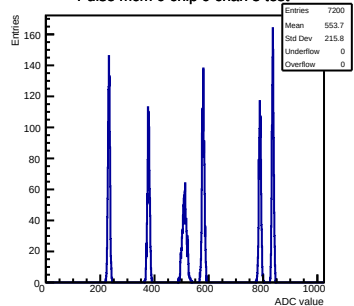
Pulse mcm 0 chip 0 chan 3 test



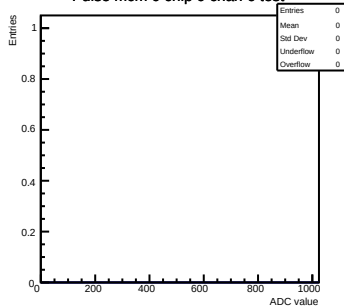
Pulse mcm 0 chip 0 chan 4 test



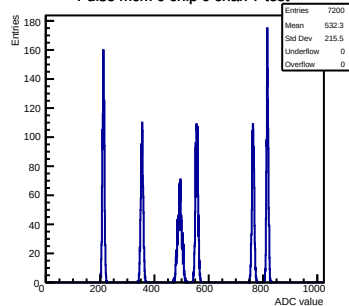
Pulse mcm 0 chip 0 chan 5 test



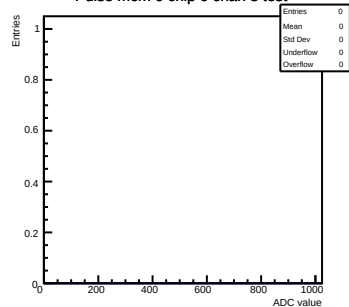
Pulse mcm 0 chip 0 chan 6 test



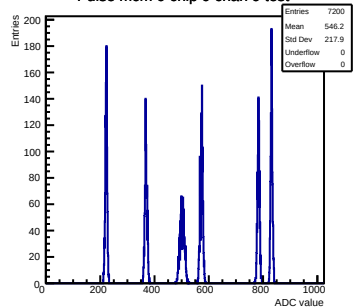
Pulse mcm 0 chip 0 chan 7 test



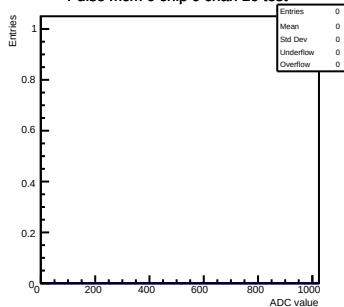
Pulse mcm 0 chip 0 chan 8 test



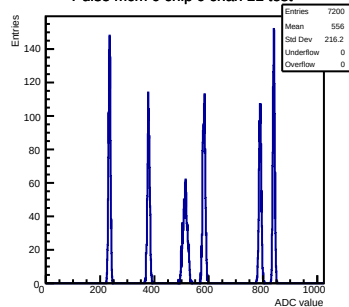
Pulse mcm 0 chip 0 chan 9 test



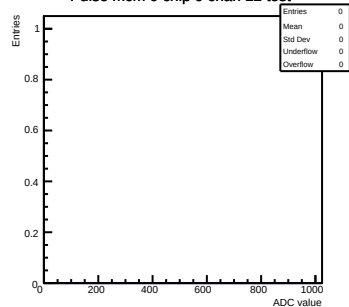
Pulse mcm 0 chip 0 chan 10 test



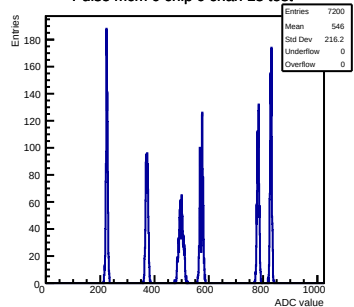
Pulse mcm 0 chip 0 chan 11 test



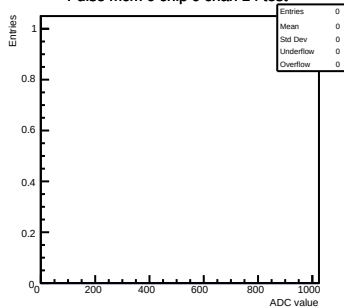
Pulse mcm 0 chip 0 chan 12 test



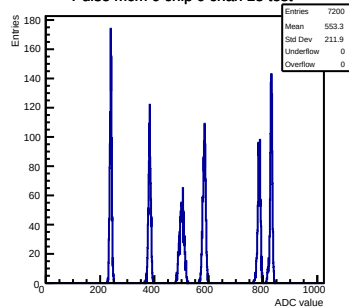
Pulse mcm 0 chip 0 chan 13 test



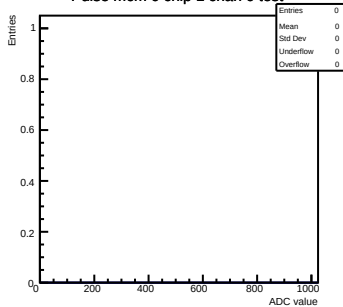
Pulse mcm 0 chip 0 chan 14 test



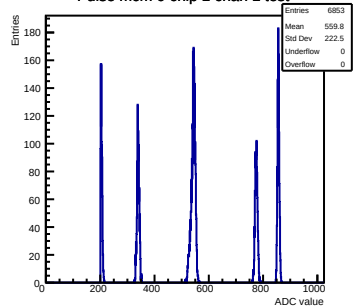
Pulse mcm 0 chip 0 chan 15 test



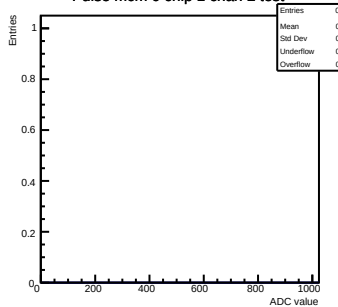
Pulse mcm 0 chip 1 chan 0 test



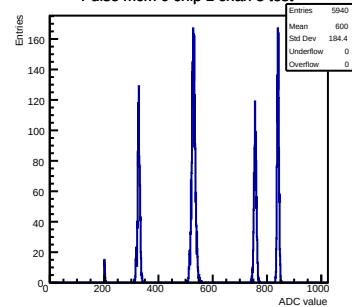
Pulse mcm 0 chip 1 chan 1 test



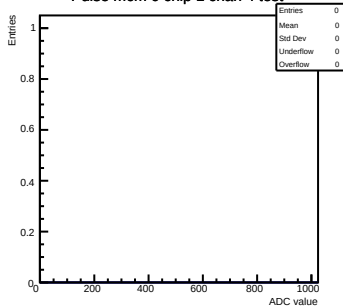
Pulse mcm 0 chip 1 chan 2 test



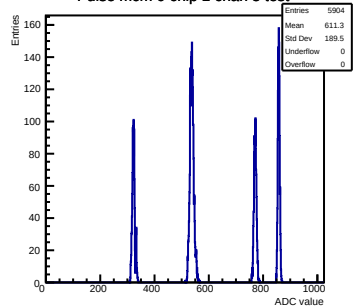
Pulse mcm 0 chip 1 chan 3 test



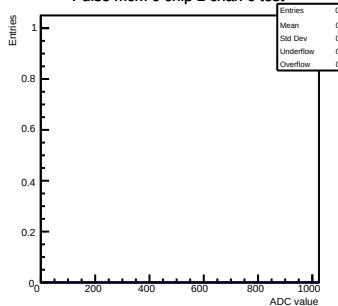
Pulse mcm 0 chip 1 chan 4 test



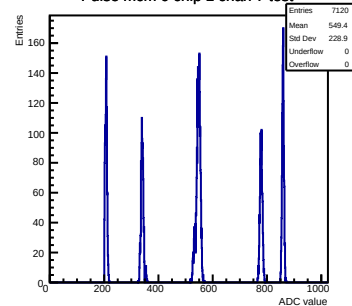
Pulse mcm 0 chip 1 chan 5 test



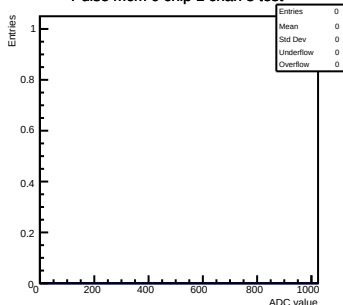
Pulse mcm 0 chip 1 chan 6 test



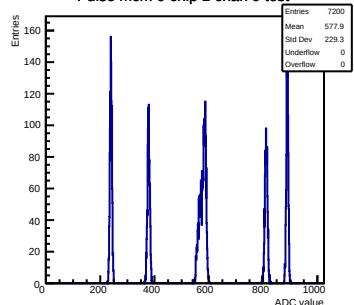
Pulse mcm 0 chip 1 chan 7 test



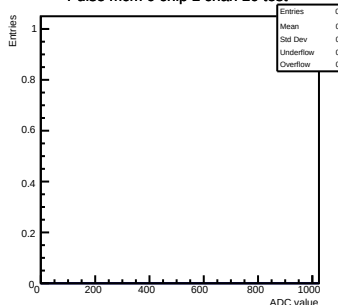
Pulse mcm 0 chip 1 chan 8 test



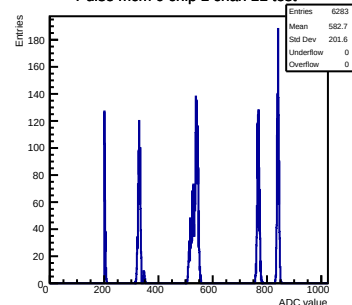
Pulse mcm 0 chip 1 chan 9 test



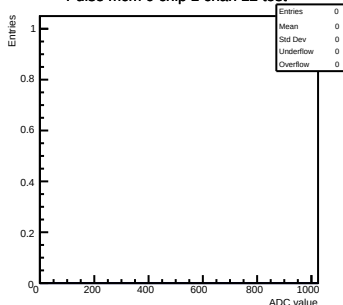
Pulse mcm 0 chip 1 chan 10 test



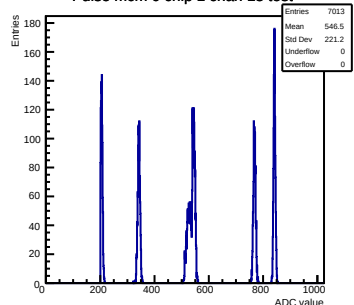
Pulse mcm 0 chip 1 chan 11 test



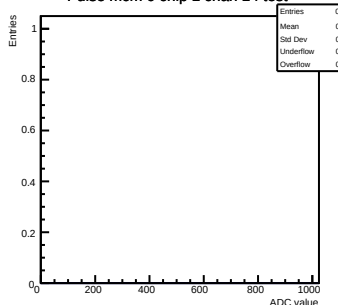
Pulse mcm 0 chip 1 chan 12 test



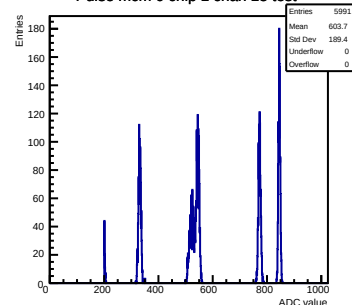
Pulse mcm 0 chip 1 chan 13 test



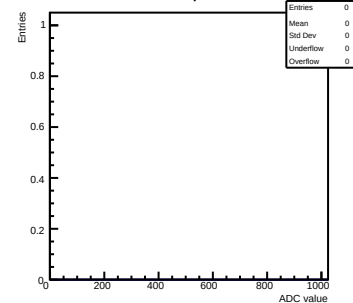
Pulse mcm 0 chip 1 chan 14 test



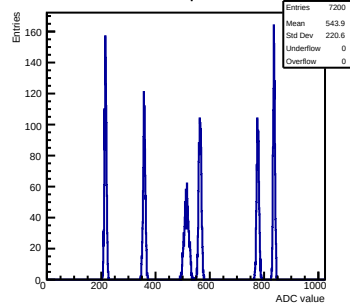
Pulse mcm 0 chip 1 chan 15 test



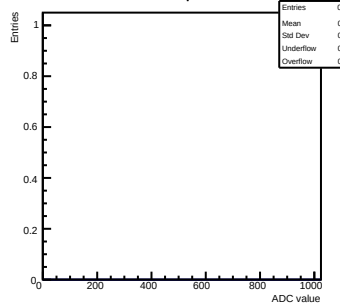
Pulse mcm 0 chip 2 chan 0 test



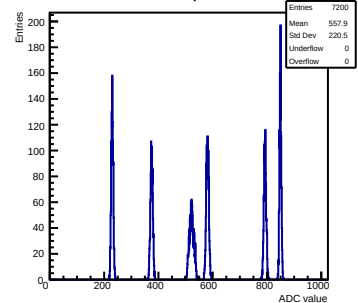
Pulse mcm 0 chip 2 chan 1 test



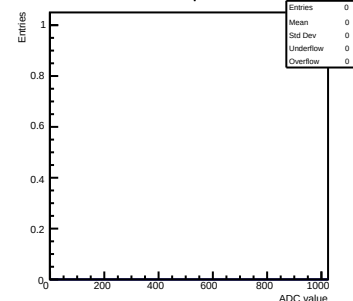
Pulse mcm 0 chip 2 chan 2 test



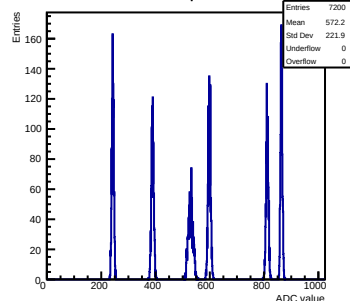
Pulse mcm 0 chip 2 chan 3 test



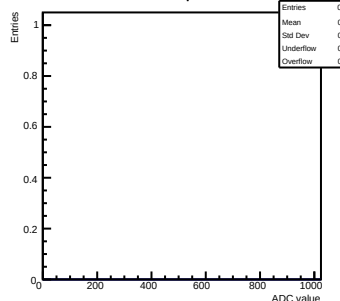
Pulse mcm 0 chip 2 chan 4 test



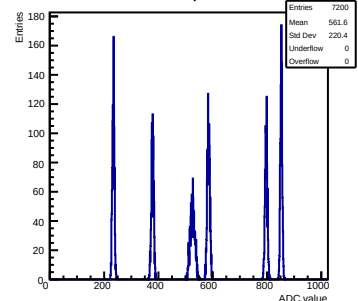
Pulse mcm 0 chip 2 chan 5 test



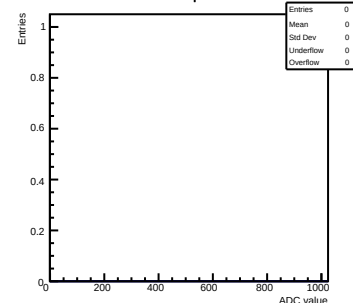
Pulse mcm 0 chip 2 chan 6 test



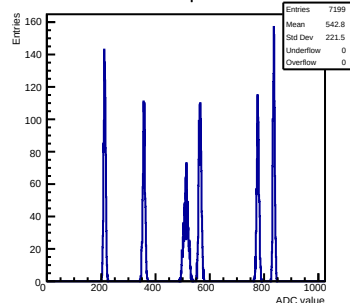
Pulse mcm 0 chip 2 chan 7 test



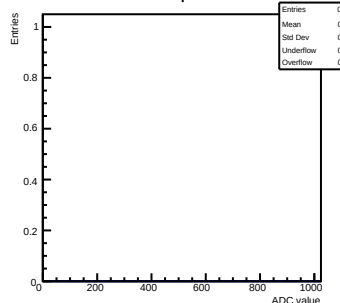
Pulse mcm 0 chip 2 chan 8 test



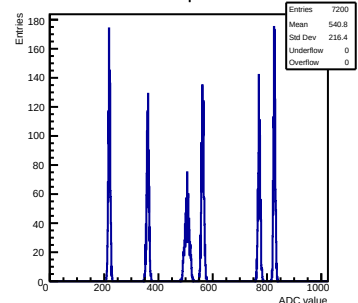
Pulse mcm 0 chip 2 chan 9 test



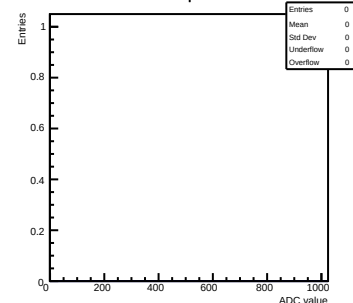
Pulse mcm 0 chip 2 chan 10 test



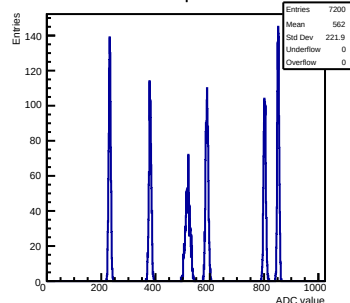
Pulse mcm 0 chip 2 chan 11 test



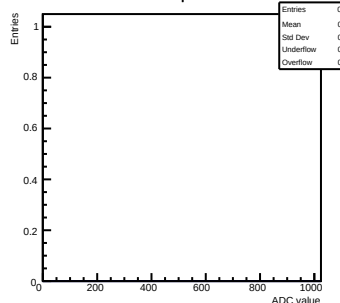
Pulse mcm 0 chip 2 chan 12 test



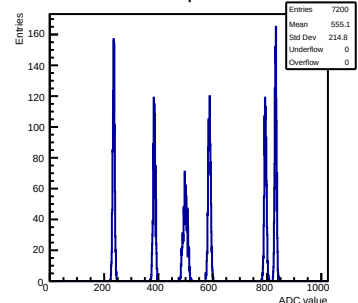
Pulse mcm 0 chip 2 chan 13 test



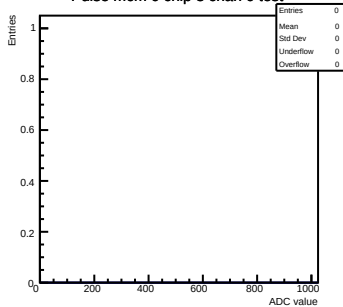
Pulse mcm 0 chip 2 chan 14 test



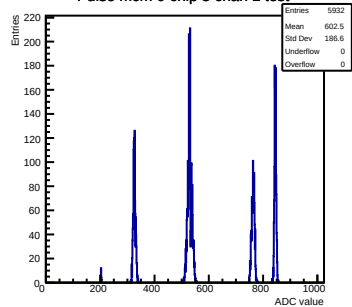
Pulse mcm 0 chip 2 chan 15 test



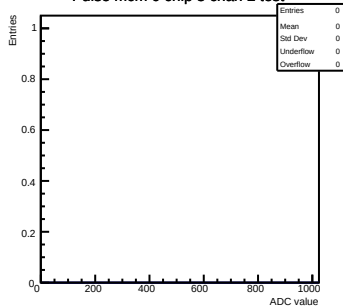
Pulse mcm 0 chip 3 chan 0 test



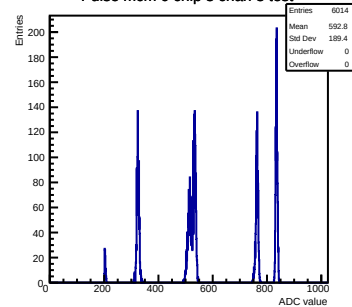
Pulse mcm 0 chip 3 chan 1 test



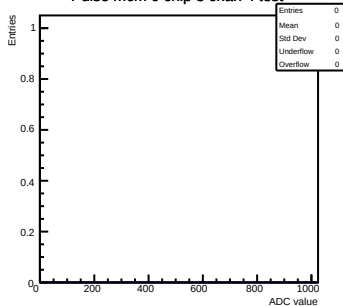
Pulse mcm 0 chip 3 chan 2 test



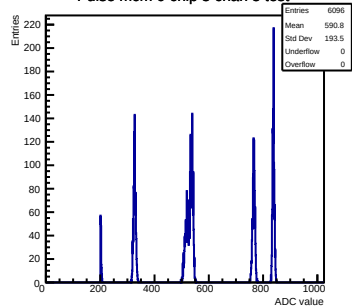
Pulse mcm 0 chip 3 chan 3 test



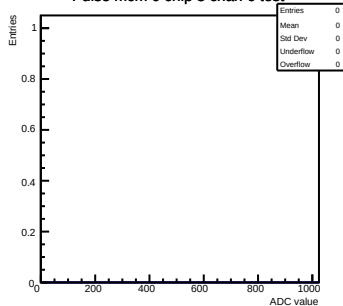
Pulse mcm 0 chip 3 chan 4 test



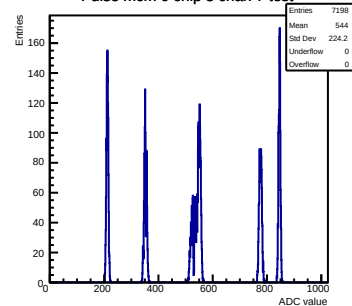
Pulse mcm 0 chip 3 chan 5 test



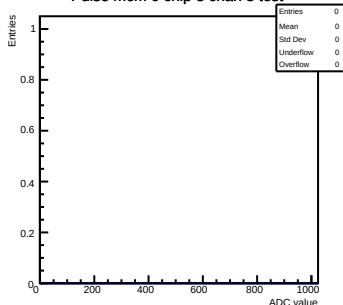
Pulse mcm 0 chip 3 chan 6 test



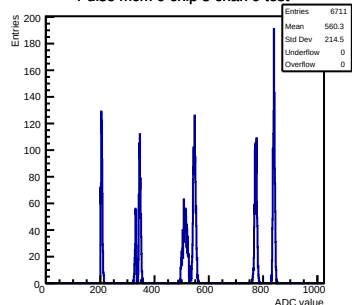
Pulse mcm 0 chip 3 chan 7 test



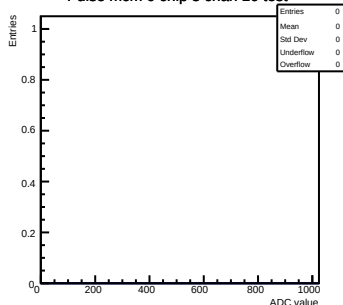
Pulse mcm 0 chip 3 chan 8 test



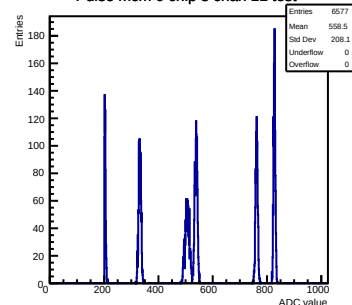
Pulse mcm 0 chip 3 chan 9 test



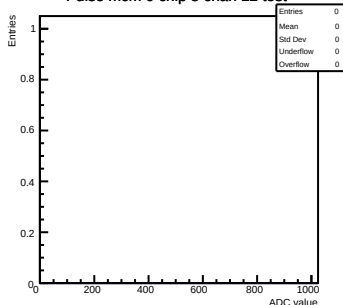
Pulse mcm 0 chip 3 chan 10 test



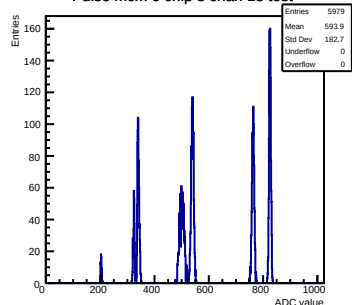
Pulse mcm 0 chip 3 chan 11 test



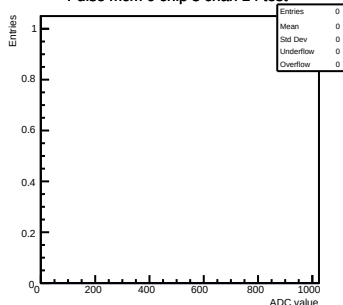
Pulse mcm 0 chip 3 chan 12 test



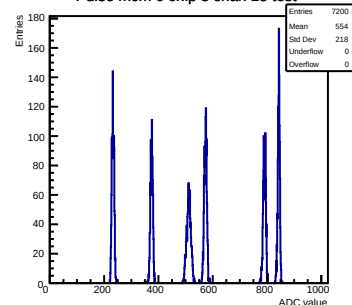
Pulse mcm 0 chip 3 chan 13 test



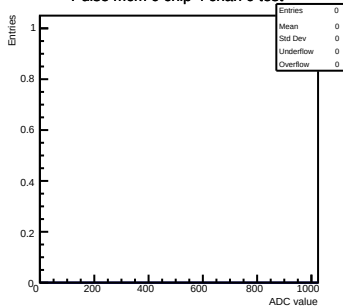
Pulse mcm 0 chip 3 chan 14 test



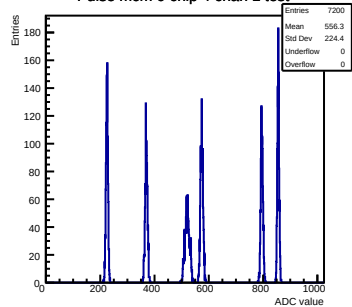
Pulse mcm 0 chip 3 chan 15 test



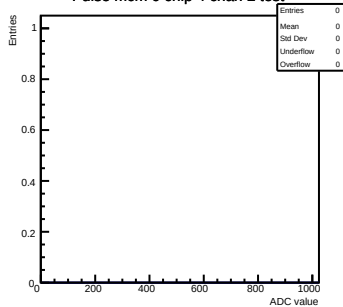
Pulse mcm 0 chip 4 chan 0 test



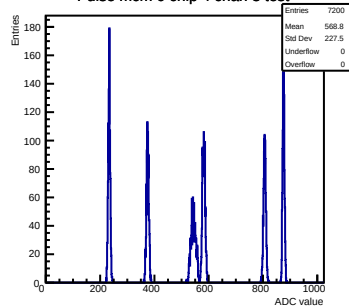
Pulse mcm 0 chip 4 chan 1 test



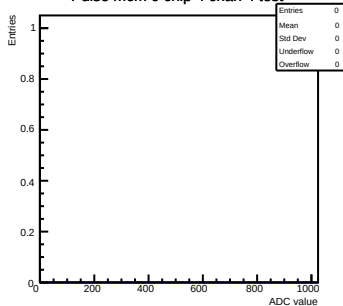
Pulse mcm 0 chip 4 chan 2 test



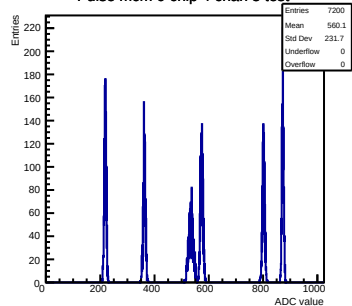
Pulse mcm 0 chip 4 chan 3 test



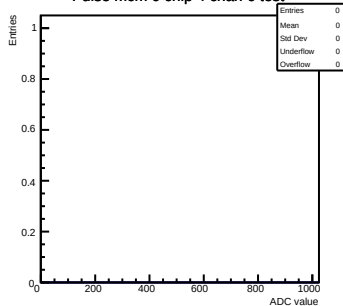
Pulse mcm 0 chip 4 chan 4 test



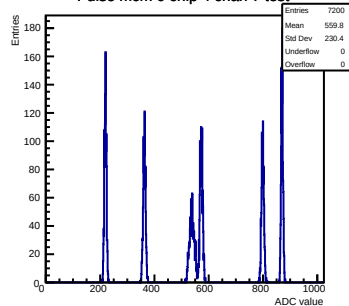
Pulse mcm 0 chip 4 chan 5 test



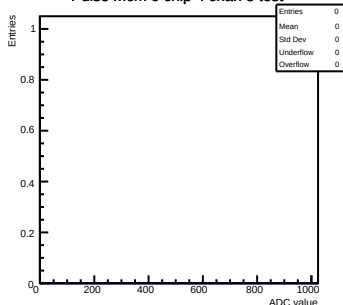
Pulse mcm 0 chip 4 chan 6 test



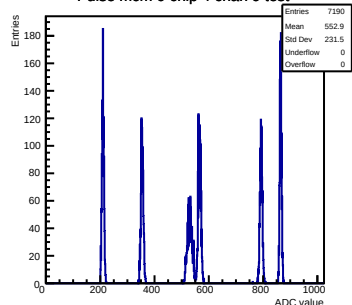
Pulse mcm 0 chip 4 chan 7 test



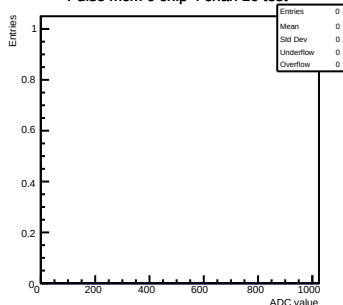
Pulse mcm 0 chip 4 chan 8 test



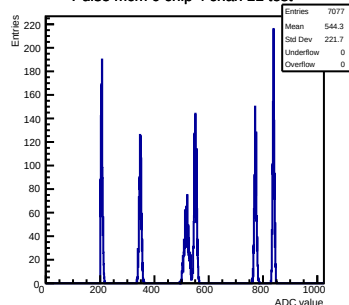
Pulse mcm 0 chip 4 chan 9 test



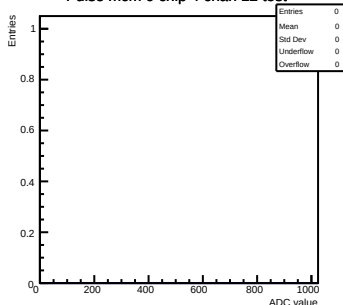
Pulse mcm 0 chip 4 chan 10 test



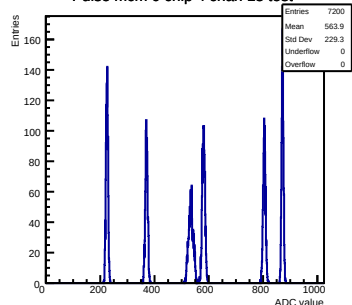
Pulse mcm 0 chip 4 chan 11 test



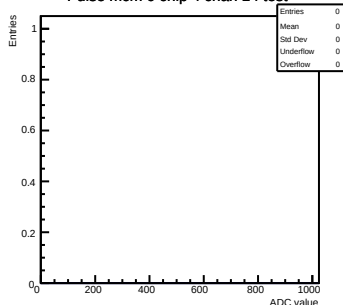
Pulse mcm 0 chip 4 chan 12 test



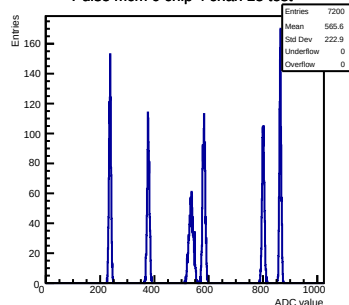
Pulse mcm 0 chip 4 chan 13 test



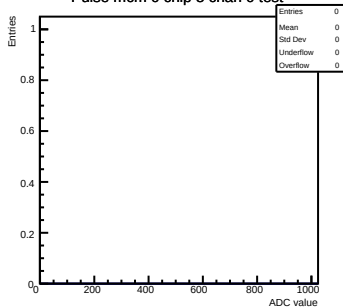
Pulse mcm 0 chip 4 chan 14 test



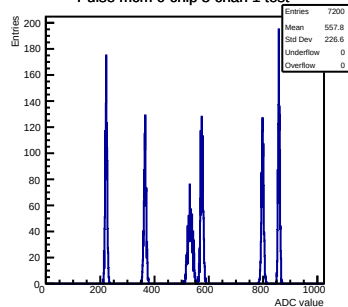
Pulse mcm 0 chip 4 chan 15 test



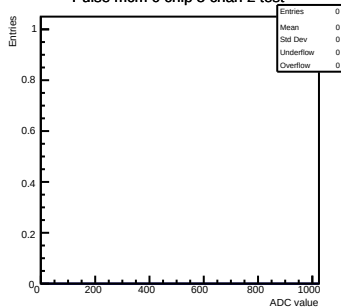
Pulse mcm 0 chip 5 chan 0 test



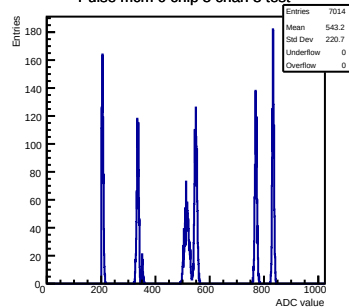
Pulse mcm 0 chip 5 chan 1 test



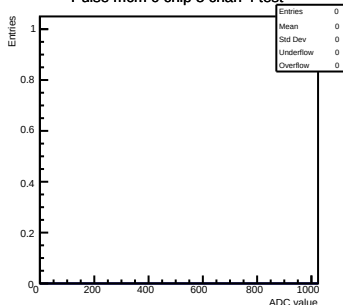
Pulse mcm 0 chip 5 chan 2 test



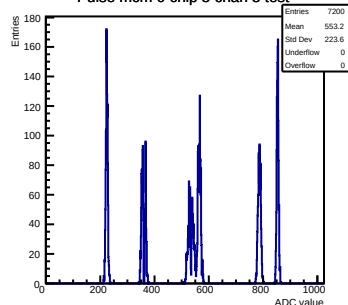
Pulse mcm 0 chip 5 chan 3 test



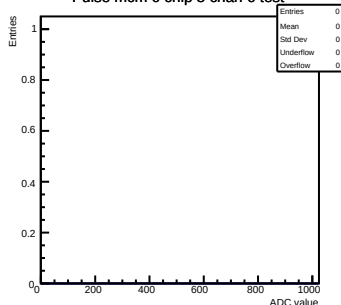
Pulse mcm 0 chip 5 chan 4 test



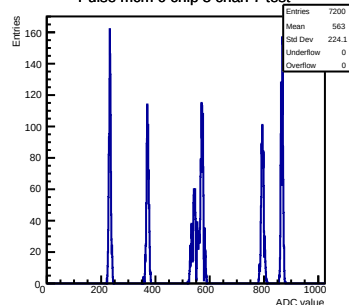
Pulse mcm 0 chip 5 chan 5 test



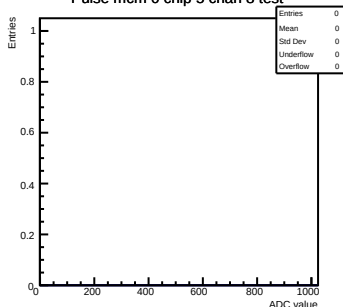
Pulse mcm 0 chip 5 chan 6 test



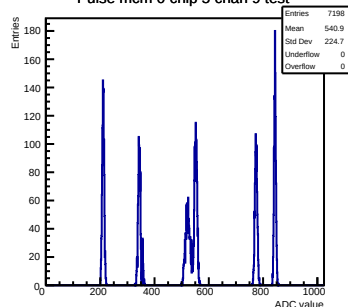
Pulse mcm 0 chip 5 chan 7 test



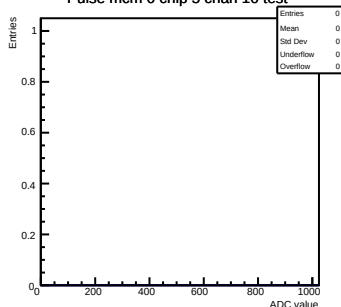
Pulse mcm 0 chip 5 chan 8 test



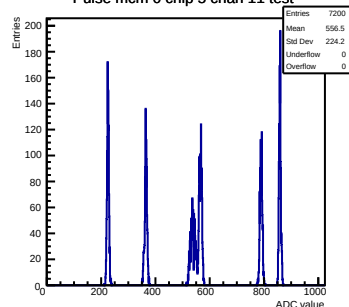
Pulse mcm 0 chip 5 chan 9 test



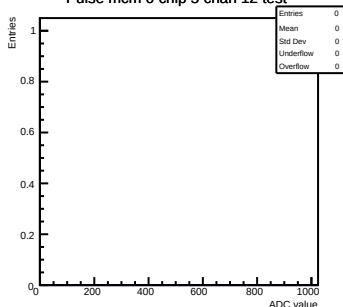
Pulse mcm 0 chip 5 chan 10 test



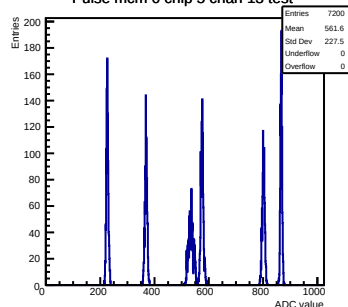
Pulse mcm 0 chip 5 chan 11 test



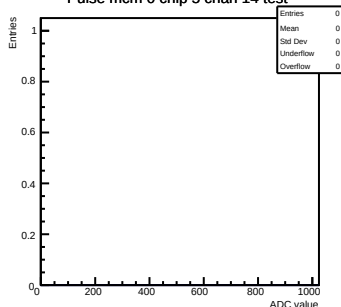
Pulse mcm 0 chip 5 chan 12 test



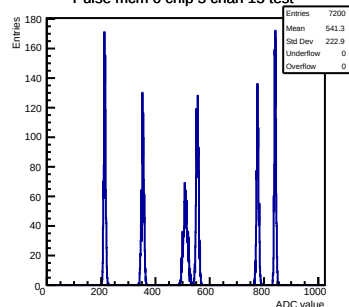
Pulse mcm 0 chip 5 chan 13 test



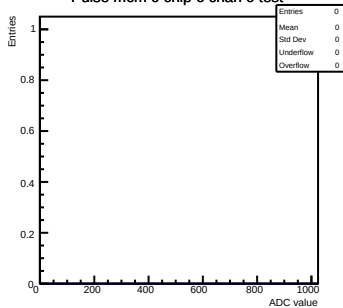
Pulse mcm 0 chip 5 chan 14 test



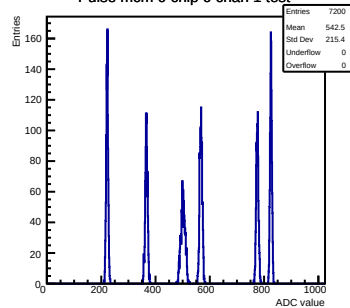
Pulse mcm 0 chip 5 chan 15 test



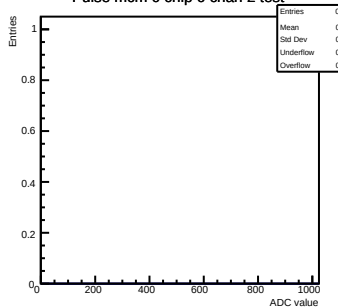
Pulse mcm 0 chip 6 chan 0 test



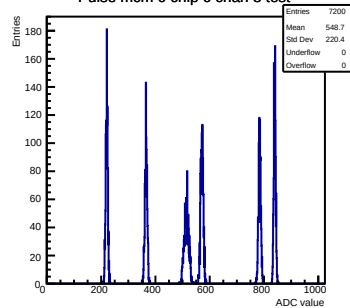
Pulse mcm 0 chip 6 chan 1 test



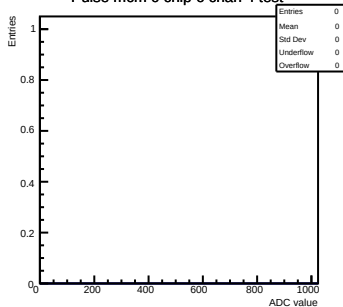
Pulse mcm 0 chip 6 chan 2 test



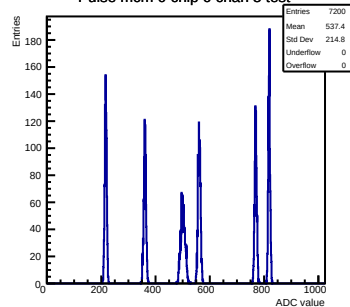
Pulse mcm 0 chip 6 chan 3 test



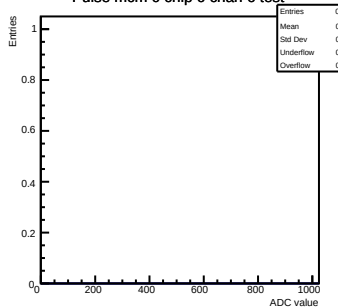
Pulse mcm 0 chip 6 chan 4 test



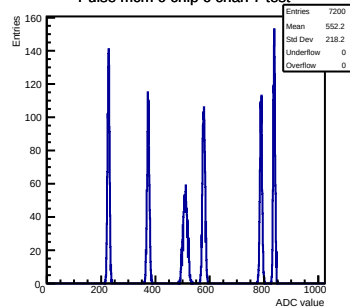
Pulse mcm 0 chip 6 chan 5 test



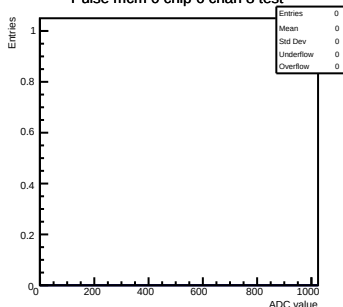
Pulse mcm 0 chip 6 chan 6 test



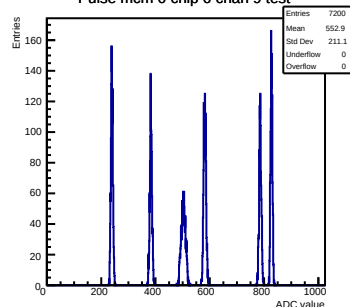
Pulse mcm 0 chip 6 chan 7 test



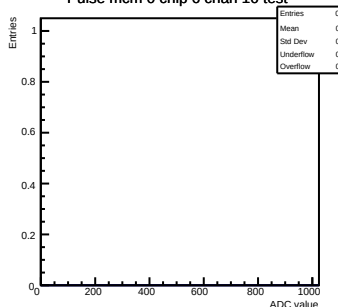
Pulse mcm 0 chip 6 chan 8 test



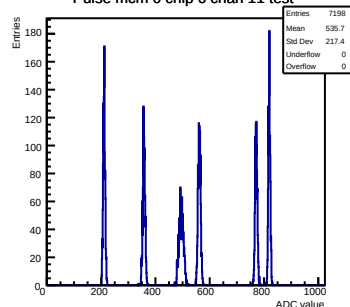
Pulse mcm 0 chip 6 chan 9 test



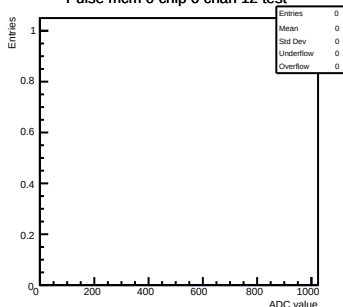
Pulse mcm 0 chip 6 chan 10 test



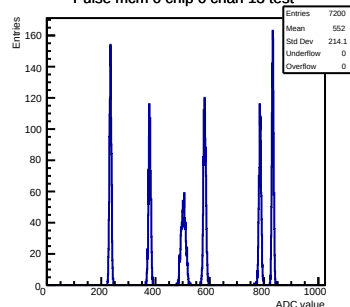
Pulse mcm 0 chip 6 chan 11 test



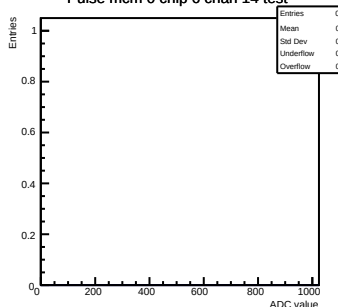
Pulse mcm 0 chip 6 chan 12 test



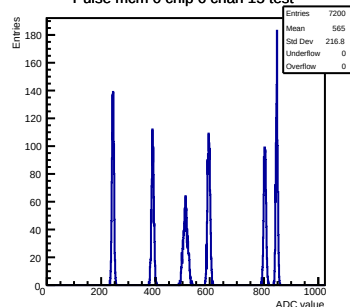
Pulse mcm 0 chip 6 chan 13 test



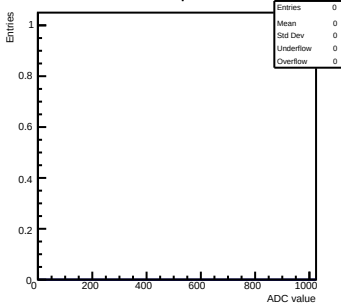
Pulse mcm 0 chip 6 chan 14 test



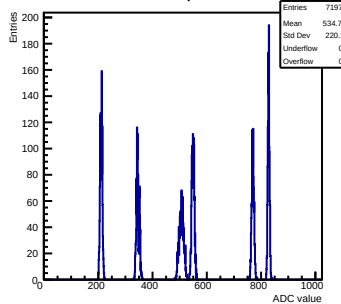
Pulse mcm 0 chip 6 chan 15 test



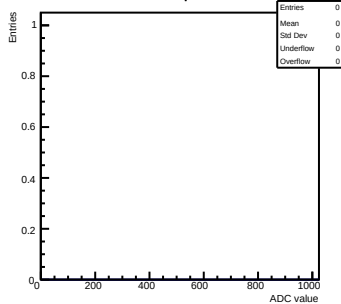
Pulse mcm 0 chip 7 chan 0 test



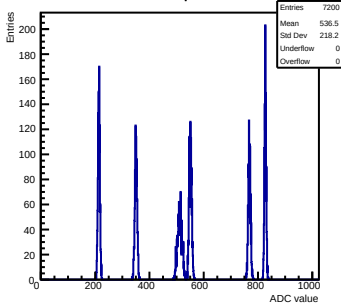
Pulse mcm 0 chip 7 chan 1 test



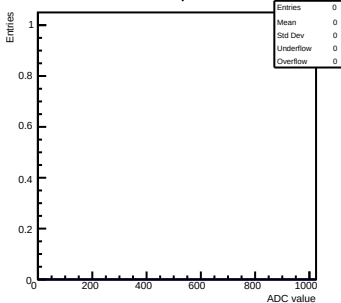
Pulse mcm 0 chip 7 chan 2 test



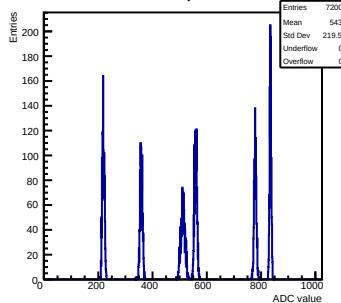
Pulse mcm 0 chip 7 chan 3 test



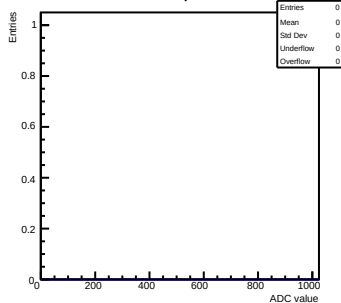
Pulse mcm 0 chip 7 chan 4 test



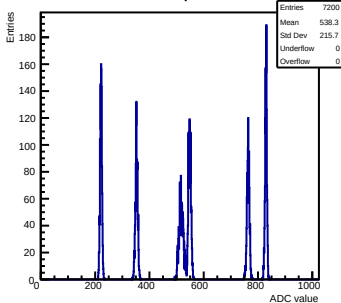
Pulse mcm 0 chip 7 chan 5 test



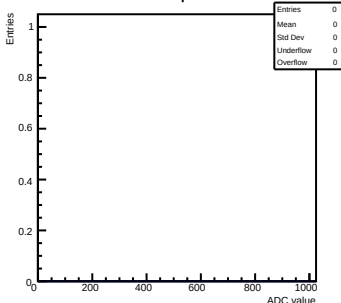
Pulse mcm 0 chip 7 chan 6 test



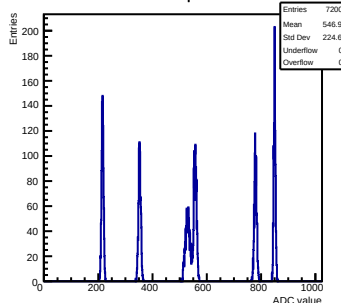
Pulse mcm 0 chip 7 chan 7 test



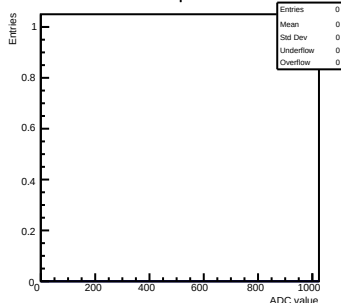
Pulse mcm 0 chip 7 chan 8 test



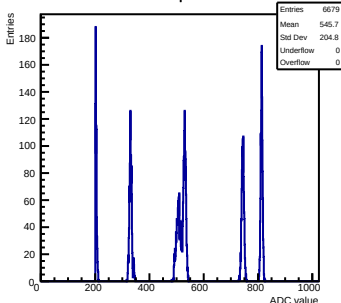
Pulse mcm 0 chip 7 chan 9 test



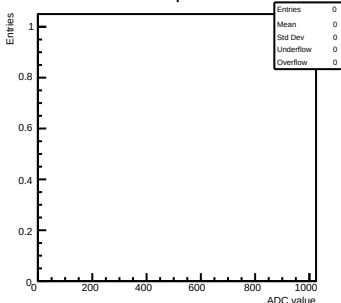
Pulse mcm 0 chip 7 chan 10 test



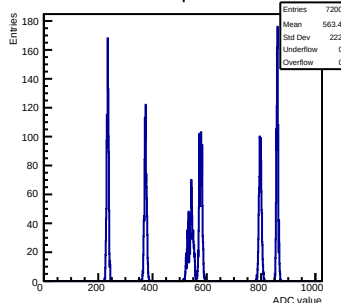
Pulse mcm 0 chip 7 chan 11 test



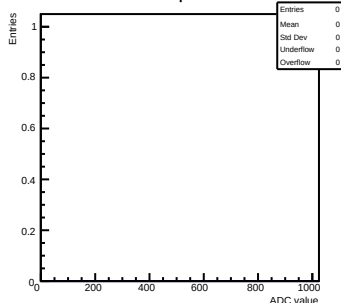
Pulse mcm 0 chip 7 chan 12 test



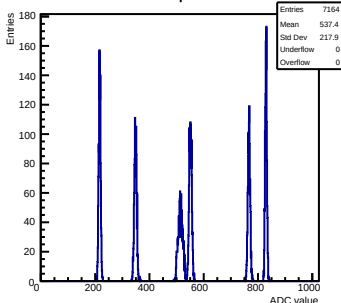
Pulse mcm 0 chip 7 chan 13 test



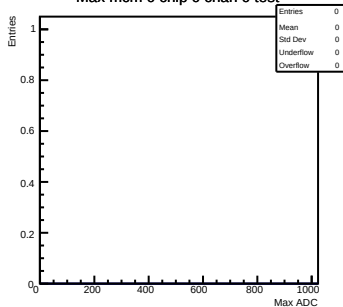
Pulse mcm 0 chip 7 chan 14 test



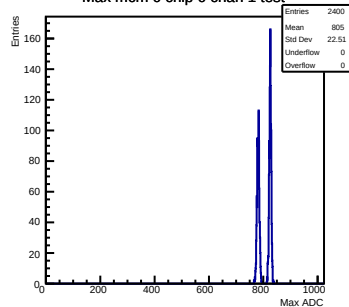
Pulse mcm 0 chip 7 chan 15 test



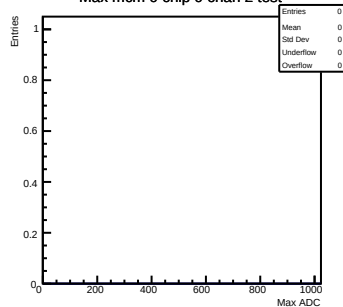
Max mcm 0 chip 0 chan 0 test



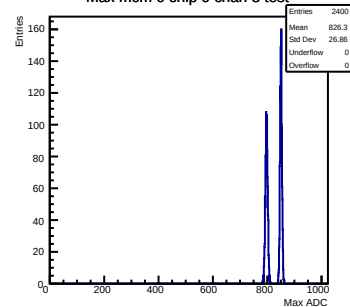
Max mcm 0 chip 0 chan 1 test



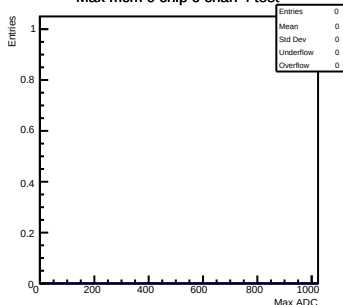
Max mcm 0 chip 0 chan 2 test



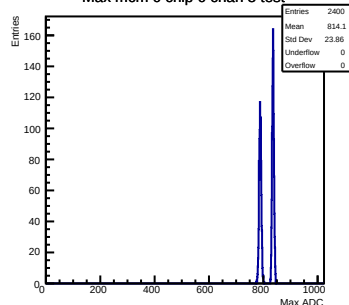
Max mcm 0 chip 0 chan 3 test



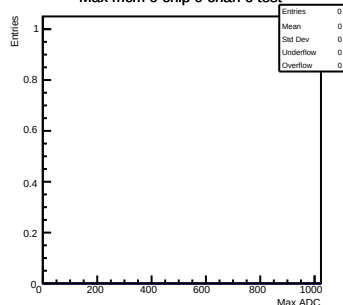
Max mcm 0 chip 0 chan 4 test



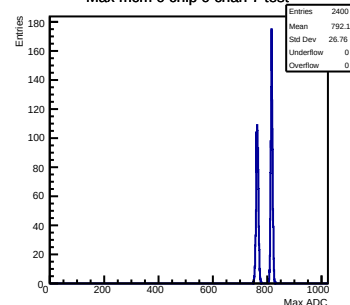
Max mcm 0 chip 0 chan 5 test



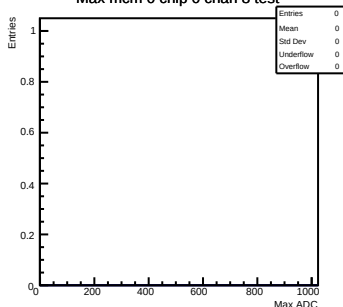
Max mcm 0 chip 0 chan 6 test



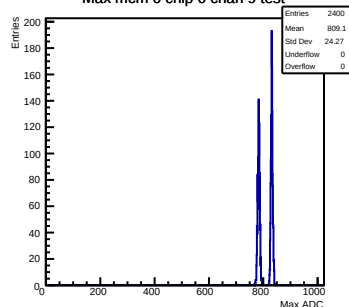
Max mcm 0 chip 0 chan 7 test



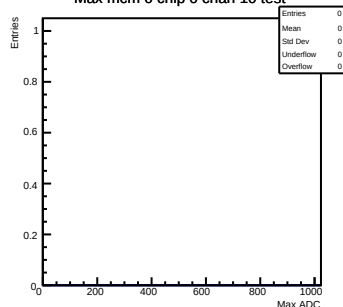
Max mcm 0 chip 0 chan 8 test



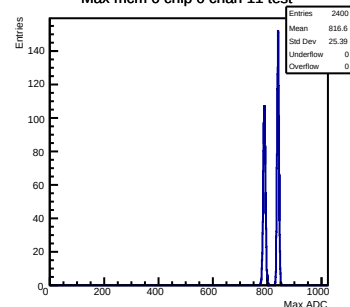
Max mcm 0 chip 0 chan 9 test



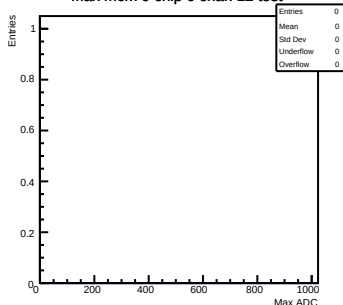
Max mcm 0 chip 0 chan 10 test



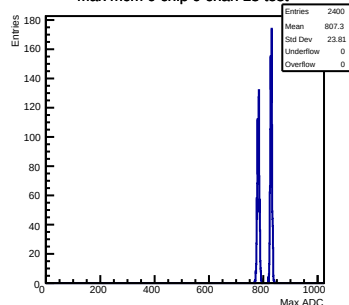
Max mcm 0 chip 0 chan 11 test



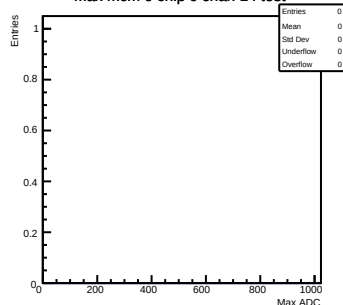
Max mcm 0 chip 0 chan 12 test



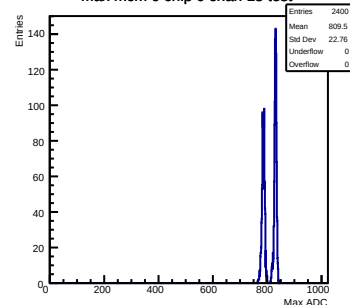
Max mcm 0 chip 0 chan 13 test



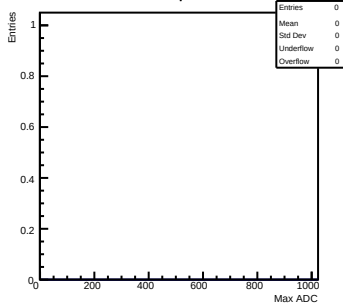
Max mcm 0 chip 0 chan 14 test



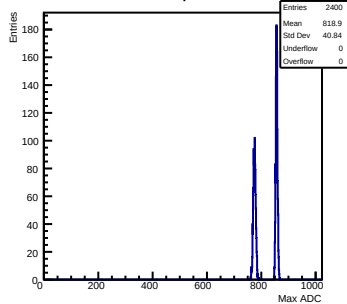
Max mcm 0 chip 0 chan 15 test



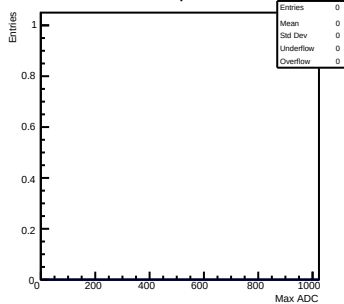
Max mcm 0 chip 1 chan 0 test



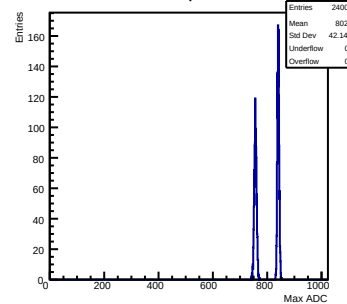
Max mcm 0 chip 1 chan 1 test



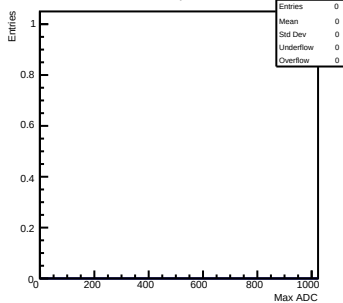
Max mcm 0 chip 1 chan 2 test



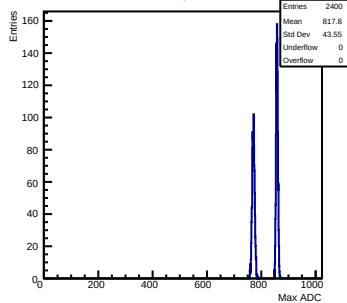
Max mcm 0 chip 1 chan 3 test



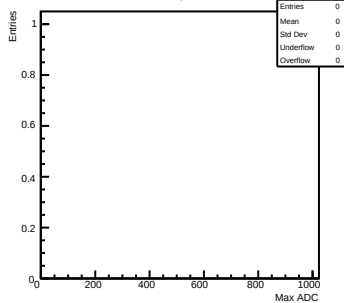
Max mcm 0 chip 1 chan 4 test



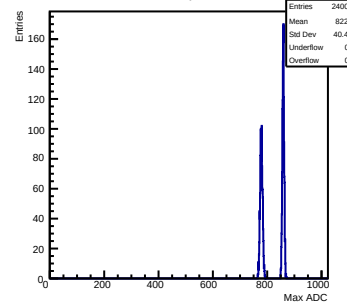
Max mcm 0 chip 1 chan 5 test



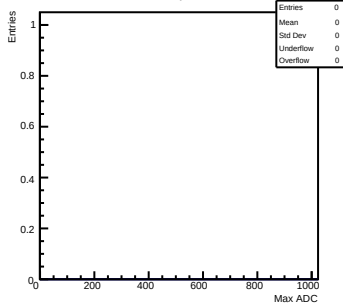
Max mcm 0 chip 1 chan 6 test



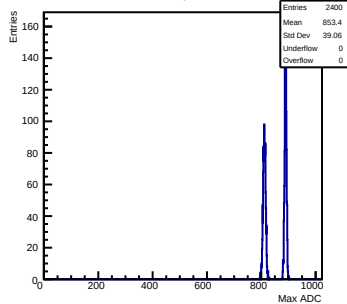
Max mcm 0 chip 1 chan 7 test



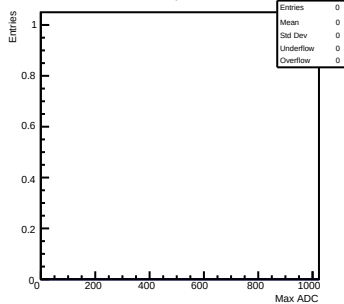
Max mcm 0 chip 1 chan 8 test



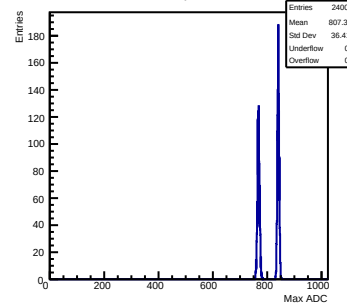
Max mcm 0 chip 1 chan 9 test



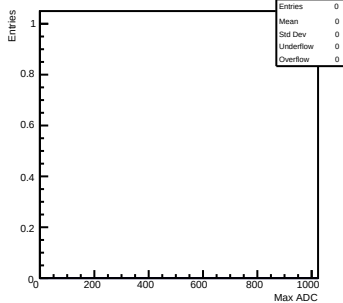
Max mcm 0 chip 1 chan 10 test



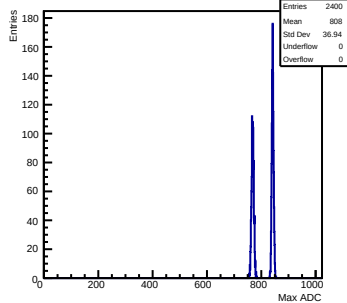
Max mcm 0 chip 1 chan 11 test



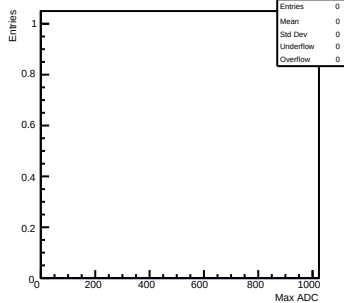
Max mcm 0 chip 1 chan 12 test



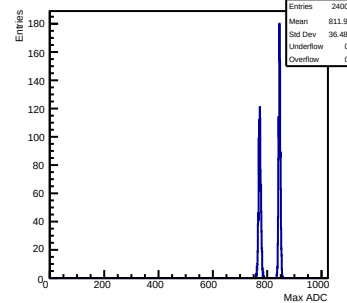
Max mcm 0 chip 1 chan 13 test



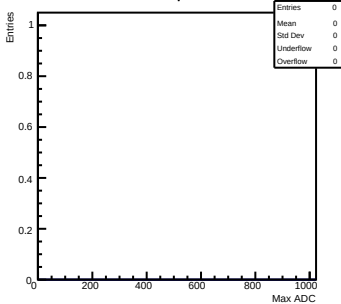
Max mcm 0 chip 1 chan 14 test



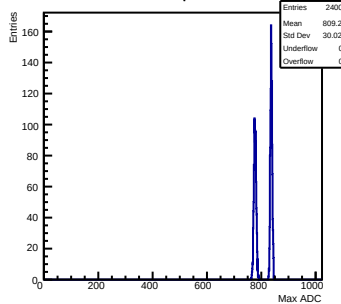
Max mcm 0 chip 1 chan 15 test



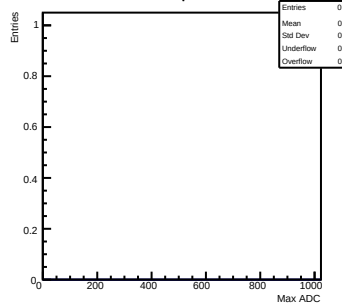
Max mcm 0 chip 2 chan 0 test



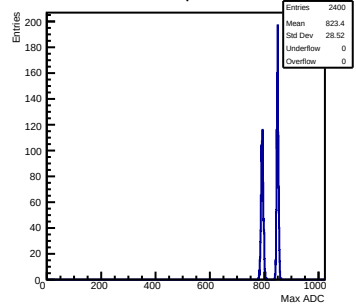
Max mcm 0 chip 2 chan 1 test



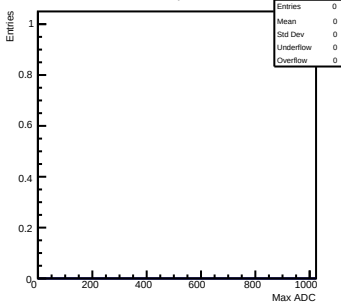
Max mcm 0 chip 2 chan 2 test



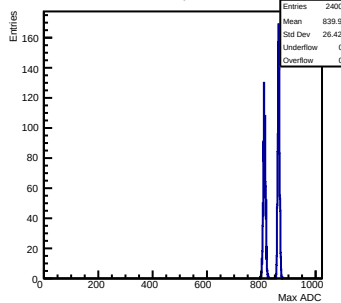
Max mcm 0 chip 2 chan 3 test



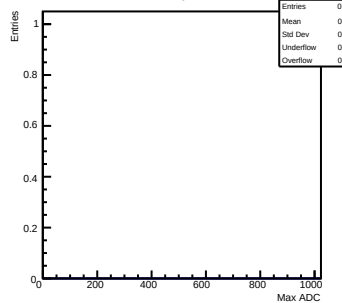
Max mcm 0 chip 2 chan 4 test



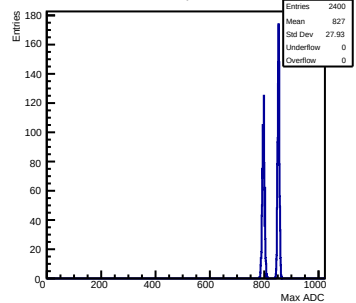
Max mcm 0 chip 2 chan 5 test



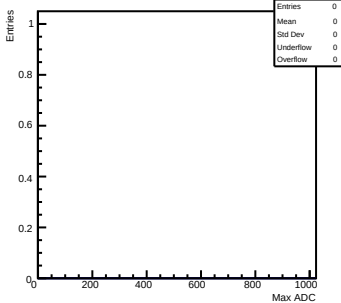
Max mcm 0 chip 2 chan 6 test



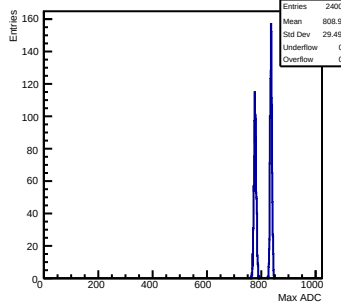
Max mcm 0 chip 2 chan 7 test



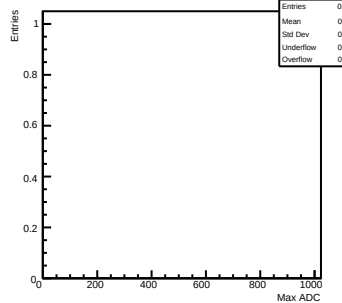
Max mcm 0 chip 2 chan 8 test



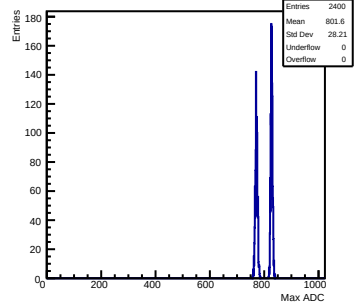
Max mcm 0 chip 2 chan 9 test



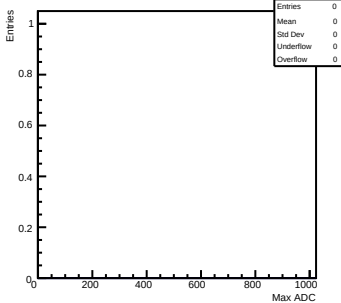
Max mcm 0 chip 2 chan 10 test



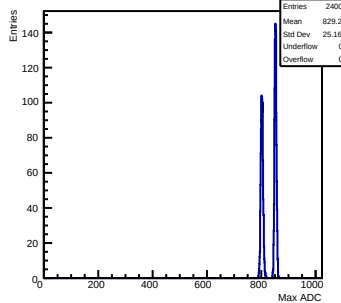
Max mcm 0 chip 2 chan 11 test



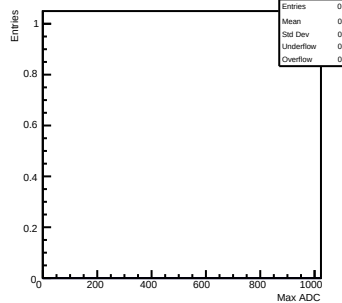
Max mcm 0 chip 2 chan 12 test



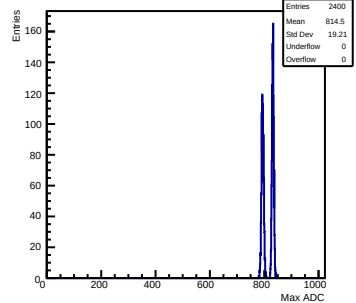
Max mcm 0 chip 2 chan 13 test



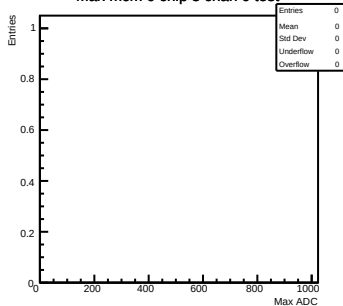
Max mcm 0 chip 2 chan 14 test



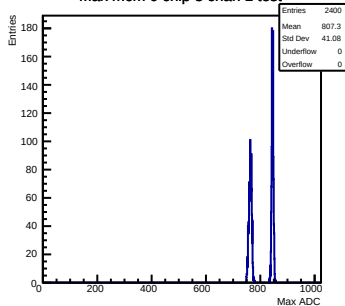
Max mcm 0 chip 2 chan 15 test



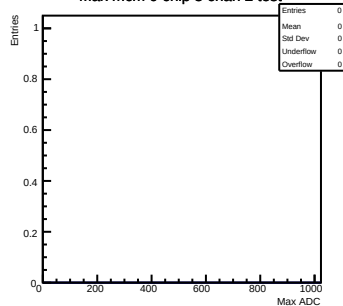
Max mcm 0 chip 3 chan 0 test



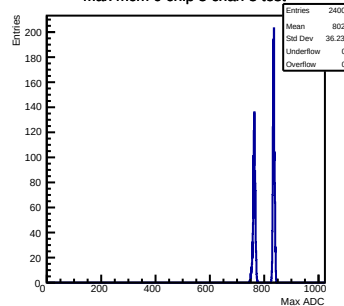
Max mcm 0 chip 3 chan 1 test



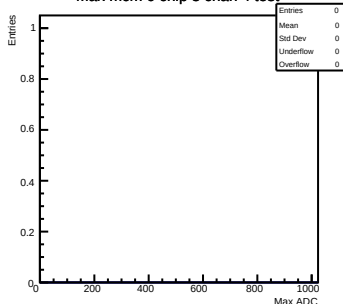
Max mcm 0 chip 3 chan 2 test



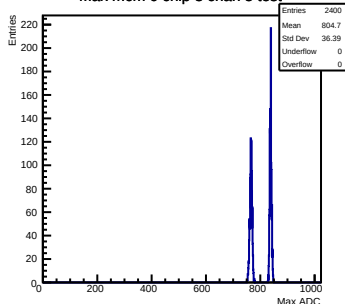
Max mcm 0 chip 3 chan 3 test



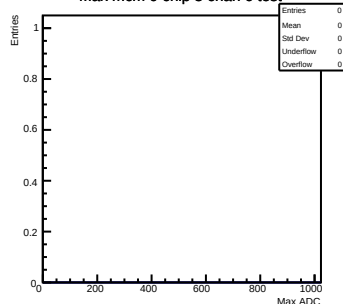
Max mcm 0 chip 3 chan 4 test



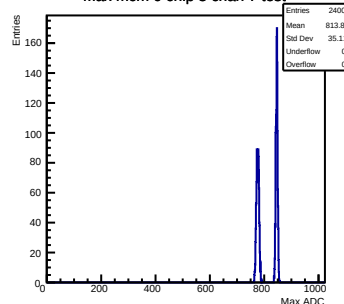
Max mcm 0 chip 3 chan 5 test



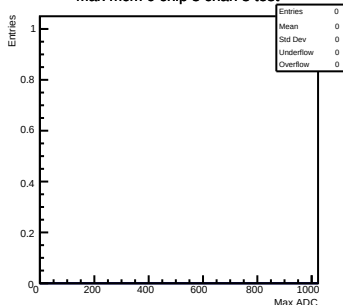
Max mcm 0 chip 3 chan 6 test



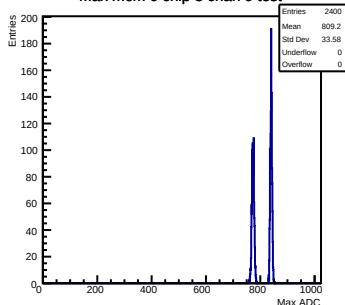
Max mcm 0 chip 3 chan 7 test



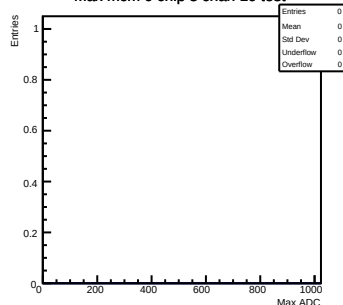
Max mcm 0 chip 3 chan 8 test



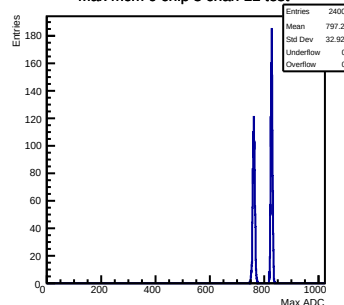
Max mcm 0 chip 3 chan 9 test



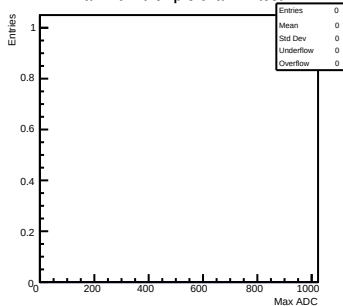
Max mcm 0 chip 3 chan 10 test



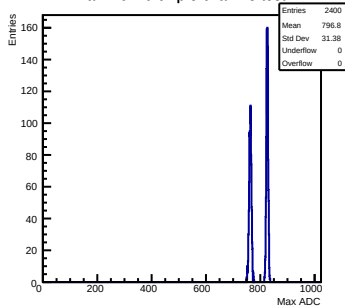
Max mcm 0 chip 3 chan 11 test



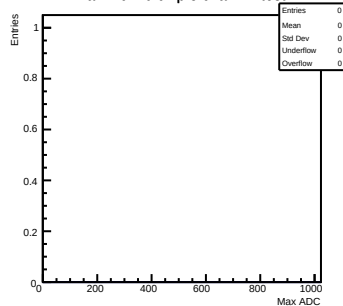
Max mcm 0 chip 3 chan 12 test



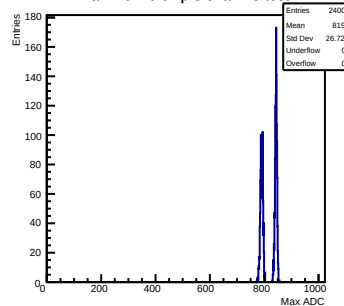
Max mcm 0 chip 3 chan 13 test



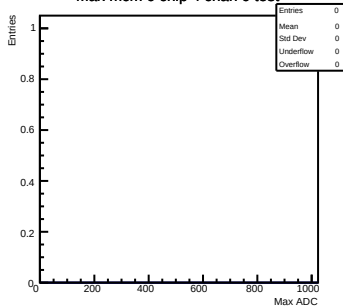
Max mcm 0 chip 3 chan 14 test



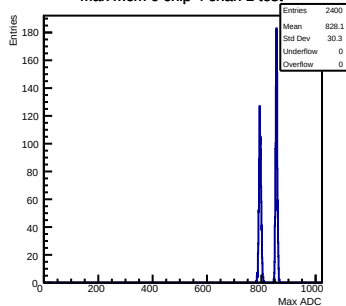
Max mcm 0 chip 3 chan 15 test



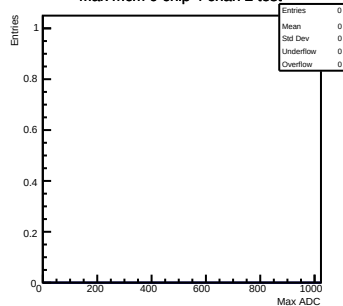
Max mcm 0 chip 4 chan 0 test



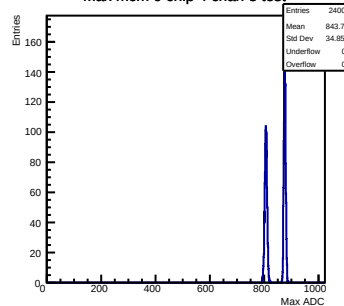
Max mcm 0 chip 4 chan 1 test



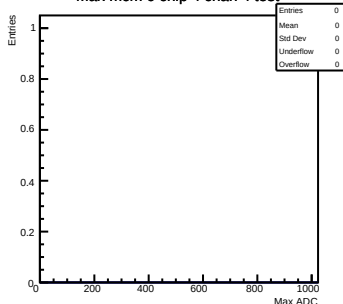
Max mcm 0 chip 4 chan 2 test



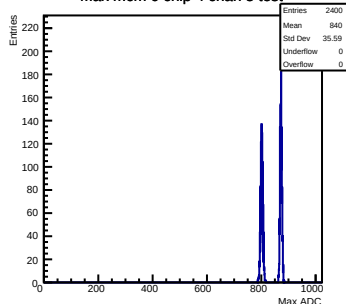
Max mcm 0 chip 4 chan 3 test



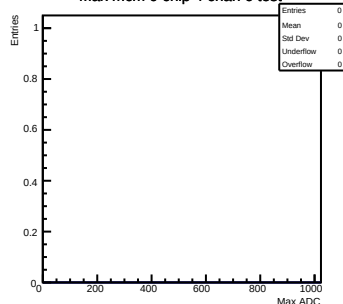
Max mcm 0 chip 4 chan 4 test



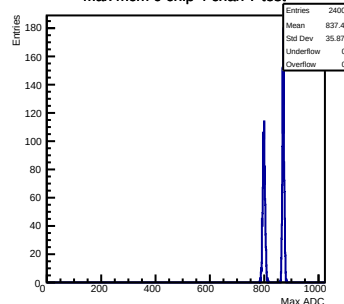
Max mcm 0 chip 4 chan 5 test



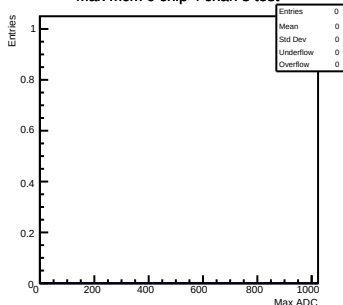
Max mcm 0 chip 4 chan 6 test



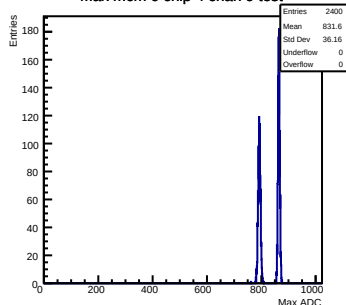
Max mcm 0 chip 4 chan 7 test



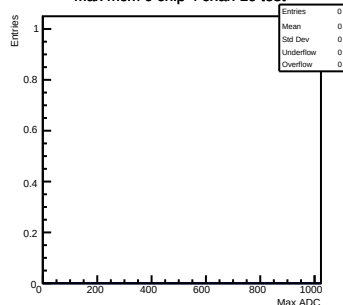
Max mcm 0 chip 4 chan 8 test



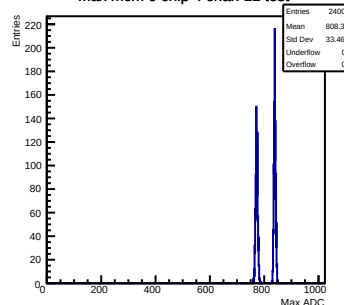
Max mcm 0 chip 4 chan 9 test



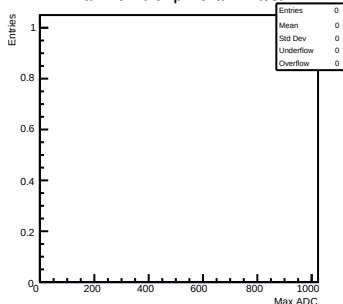
Max mcm 0 chip 4 chan 10 test



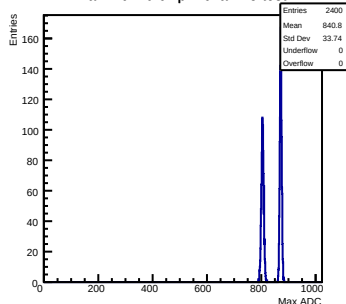
Max mcm 0 chip 4 chan 11 test



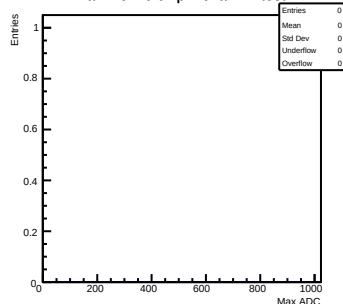
Max mcm 0 chip 4 chan 12 test



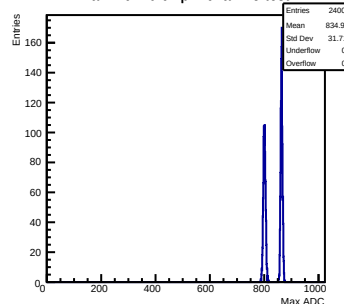
Max mcm 0 chip 4 chan 13 test



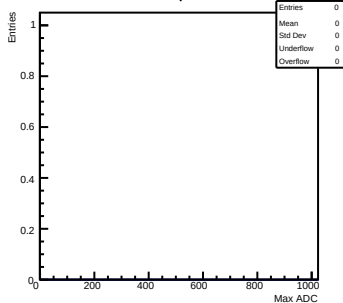
Max mcm 0 chip 4 chan 14 test



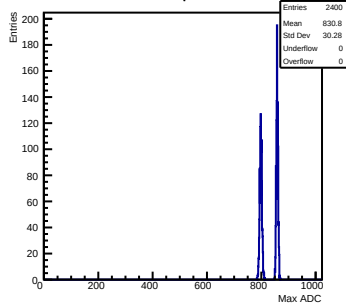
Max mcm 0 chip 4 chan 15 test



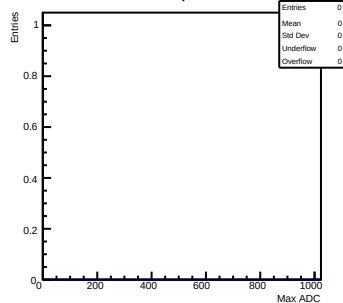
Max mcm 0 chip 5 chan 0 test



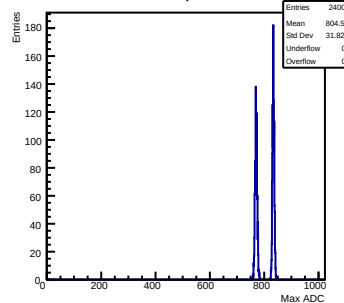
Max mcm 0 chip 5 chan 1 test



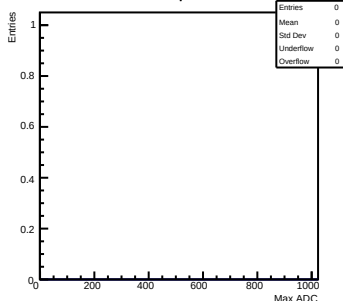
Max mcm 0 chip 5 chan 2 test



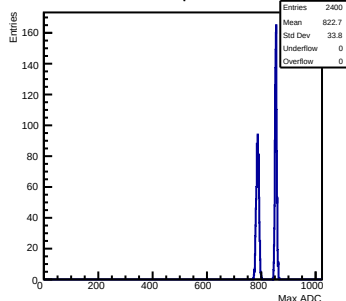
Max mcm 0 chip 5 chan 3 test



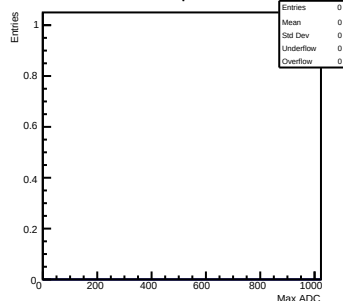
Max mcm 0 chip 5 chan 4 test



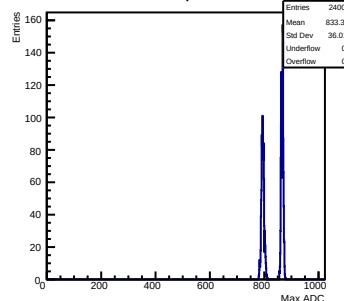
Max mcm 0 chip 5 chan 5 test



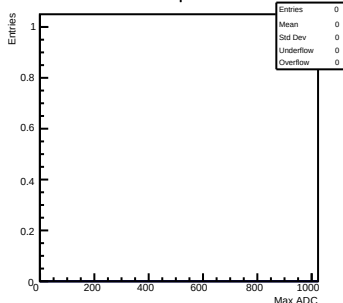
Max mcm 0 chip 5 chan 6 test



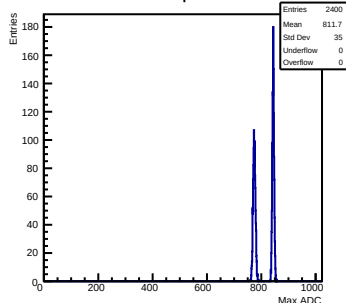
Max mcm 0 chip 5 chan 7 test



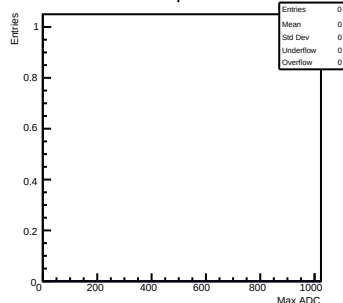
Max mcm 0 chip 5 chan 8 test



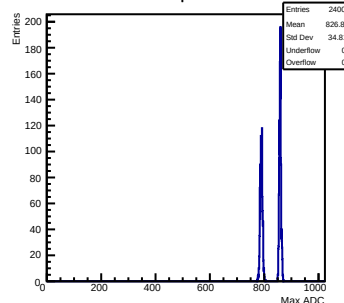
Max mcm 0 chip 5 chan 9 test



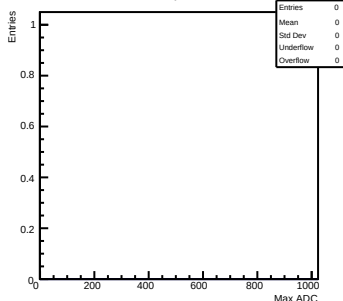
Max mcm 0 chip 5 chan 10 test



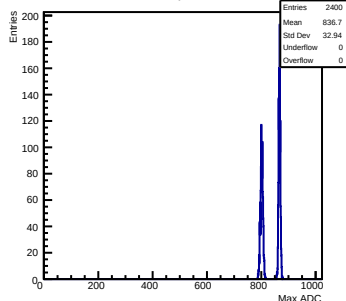
Max mcm 0 chip 5 chan 11 test



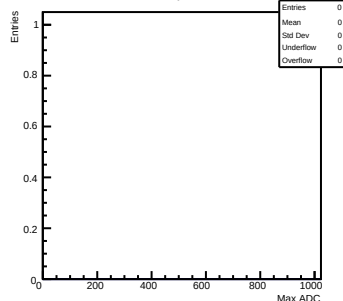
Max mcm 0 chip 5 chan 12 test



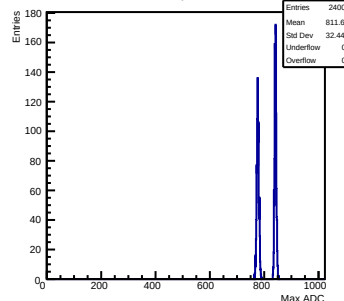
Max mcm 0 chip 5 chan 13 test



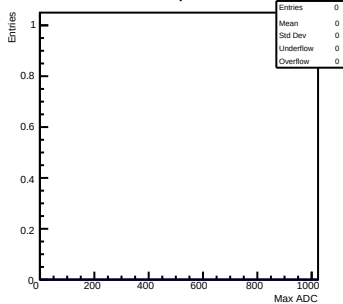
Max mcm 0 chip 5 chan 14 test



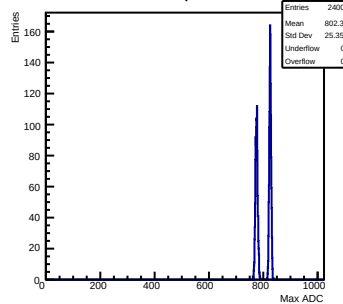
Max mcm 0 chip 5 chan 15 test



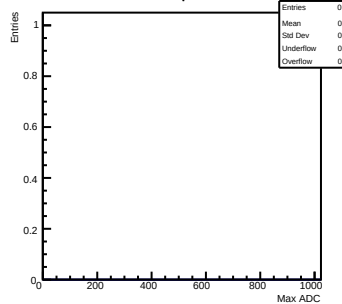
Max mcm 0 chip 6 chan 0 test



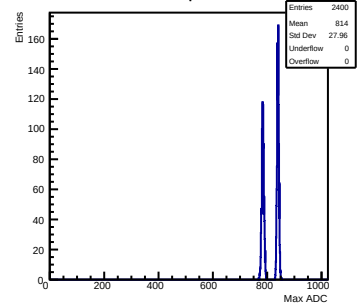
Max mcm 0 chip 6 chan 1 test



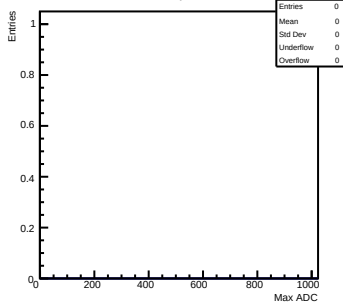
Max mcm 0 chip 6 chan 2 test



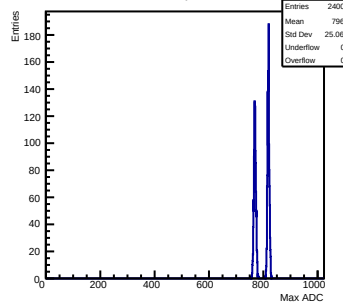
Max mcm 0 chip 6 chan 3 test



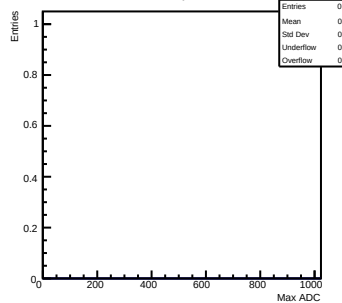
Max mcm 0 chip 6 chan 4 test



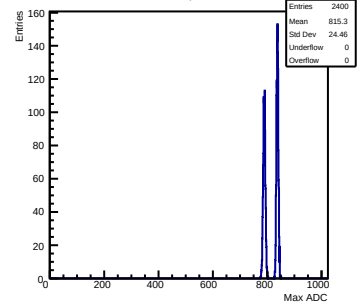
Max mcm 0 chip 6 chan 5 test



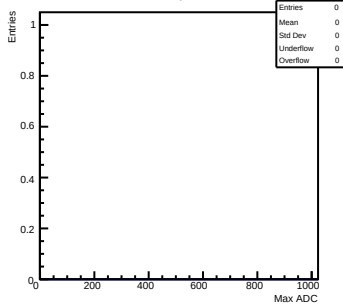
Max mcm 0 chip 6 chan 6 test



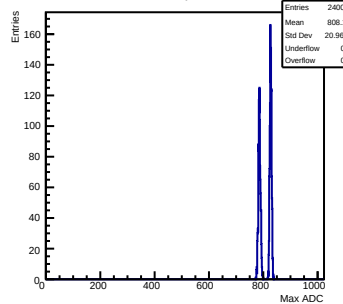
Max mcm 0 chip 6 chan 7 test



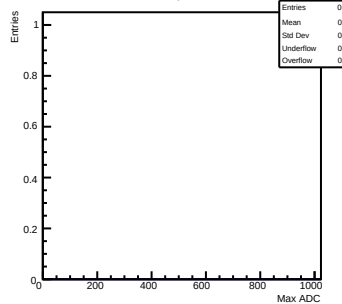
Max mcm 0 chip 6 chan 8 test



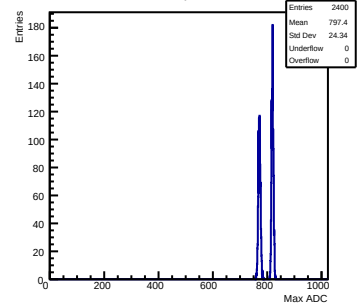
Max mcm 0 chip 6 chan 9 test



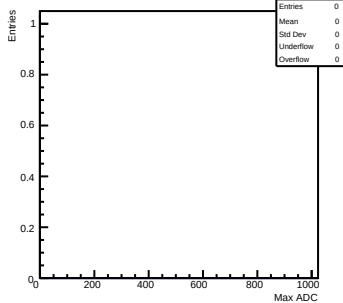
Max mcm 0 chip 6 chan 10 test



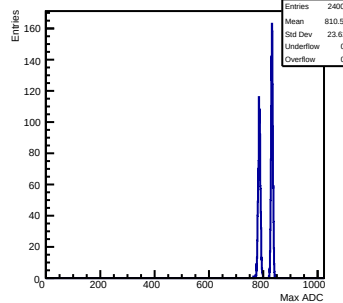
Max mcm 0 chip 6 chan 11 test



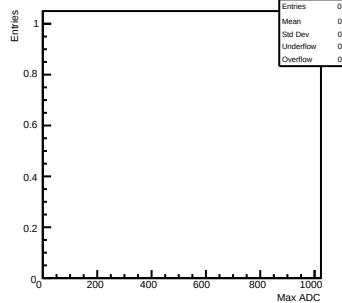
Max mcm 0 chip 6 chan 12 test



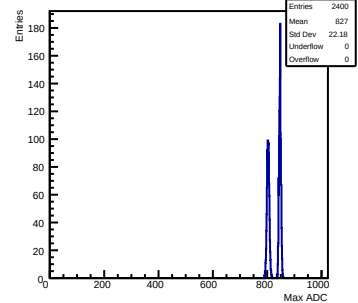
Max mcm 0 chip 6 chan 13 test



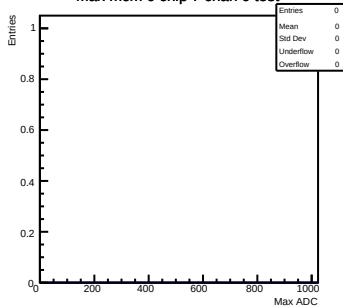
Max mcm 0 chip 6 chan 14 test



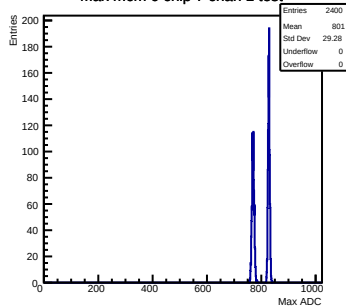
Max mcm 0 chip 6 chan 15 test



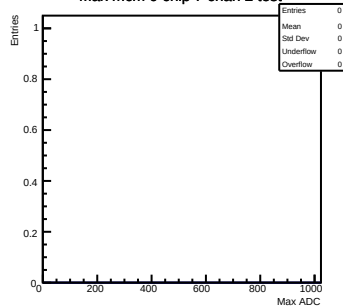
Max mcm 0 chip 7 chan 0 test



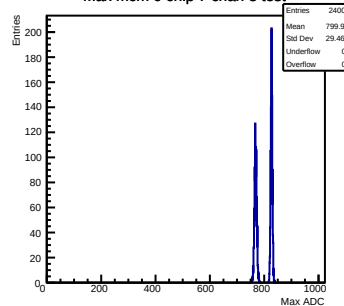
Max mcm 0 chip 7 chan 1 test



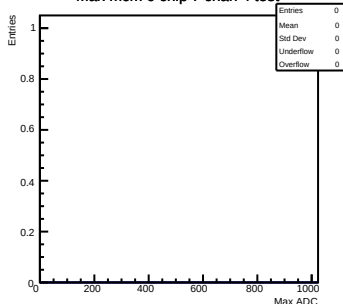
Max mcm 0 chip 7 chan 2 test



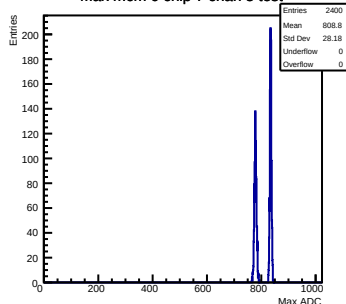
Max mcm 0 chip 7 chan 3 test



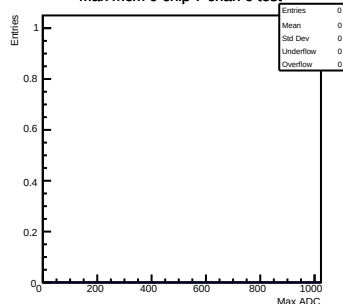
Max mcm 0 chip 7 chan 4 test



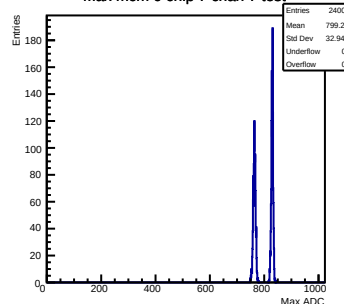
Max mcm 0 chip 7 chan 5 test



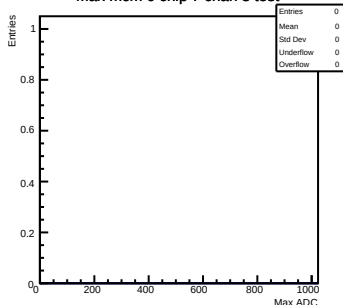
Max mcm 0 chip 7 chan 6 test



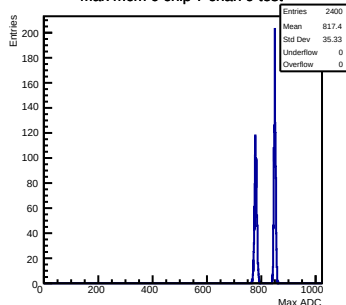
Max mcm 0 chip 7 chan 7 test



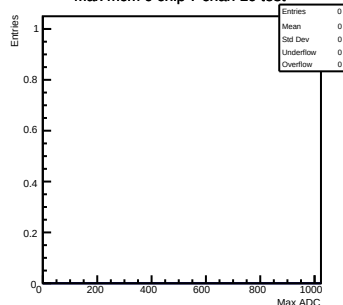
Max mcm 0 chip 7 chan 8 test



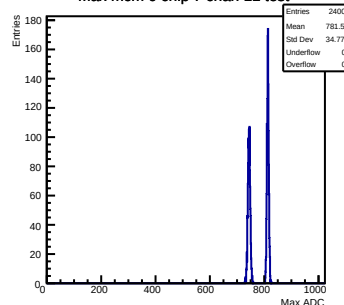
Max mcm 0 chip 7 chan 9 test



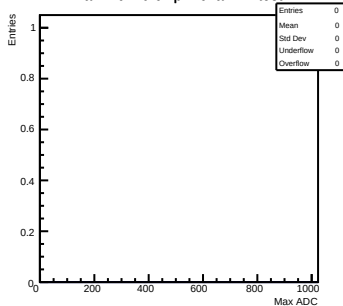
Max mcm 0 chip 7 chan 10 test



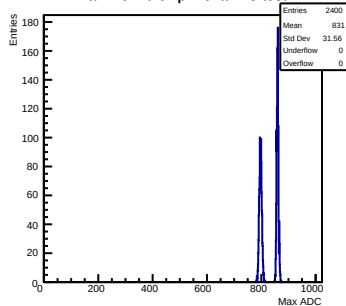
Max mcm 0 chip 7 chan 11 test



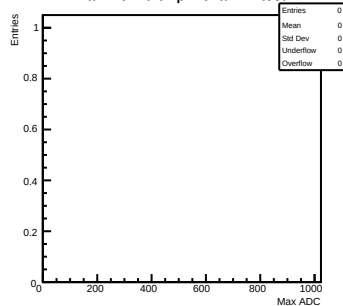
Max mcm 0 chip 7 chan 12 test



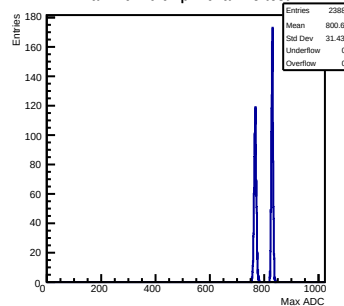
Max mcm 0 chip 7 chan 13 test



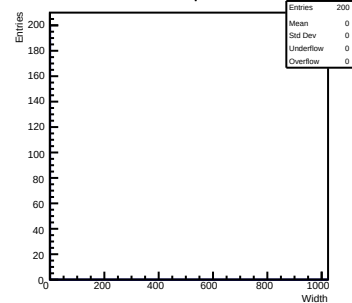
Max mcm 0 chip 7 chan 14 test



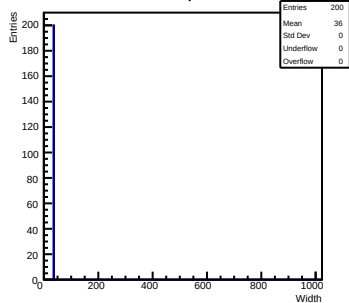
Max mcm 0 chip 7 chan 15 test



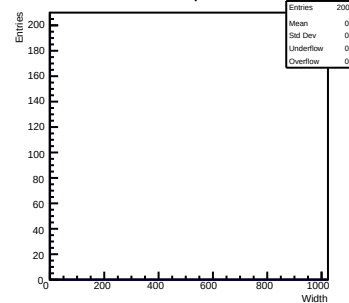
Width mcm 0 chip 0 chan 0 test



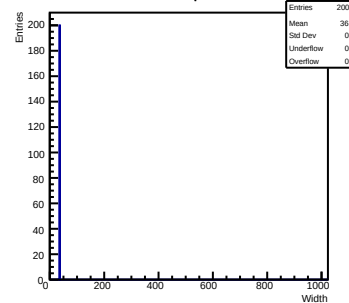
Width mcm 0 chip 0 chan 1 test



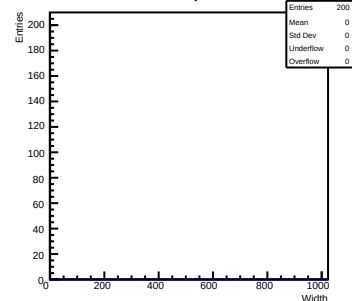
Width mcm 0 chip 0 chan 2 tes



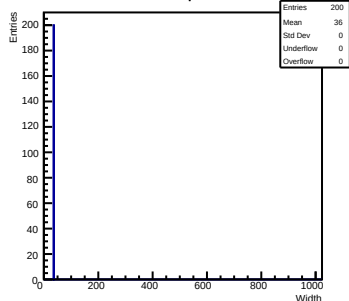
Width mcm 0 chip 0 chan 3 test



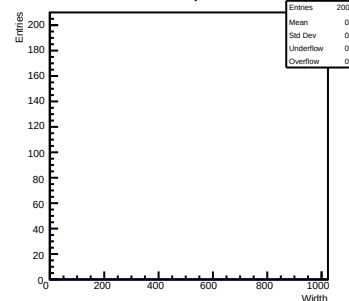
Width mcm 0 chip 0 chan 4 test



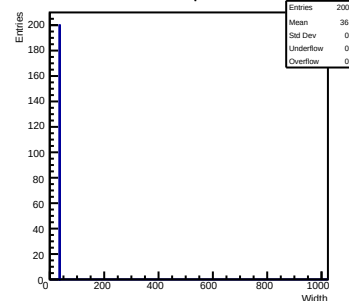
Width mcm 0 chip 0 chan 5 test



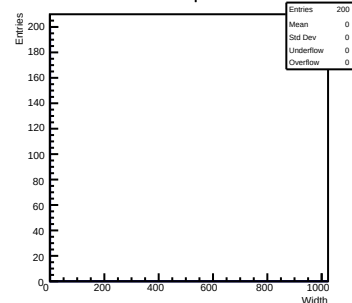
Width mcm 0 chip 0 chan 6 tes



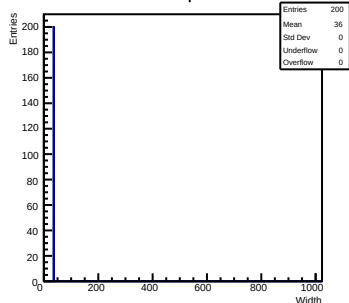
Width mcm 0 chip 0 chan 7 tes



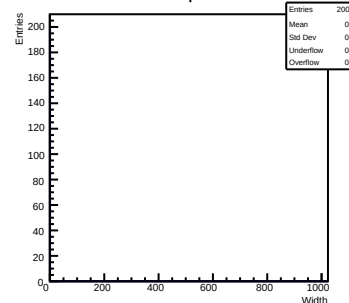
Width mcm 0 chip 0 chan 8 test



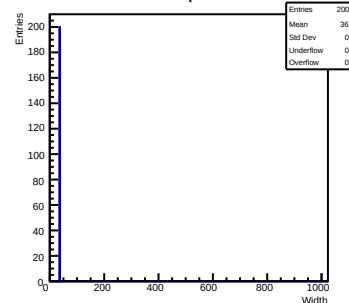
Width mcm 0 chip 0 chan 9 test



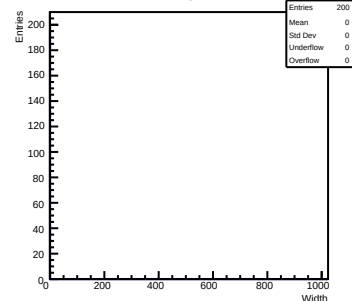
Width mcm 0 chip 0 chan 10 tes



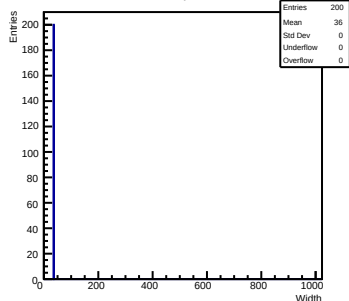
Width mcm 0 chip 0 chan 11 test



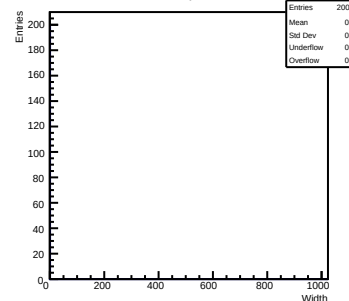
Width mcm 0 chip 0 chan 12 tes



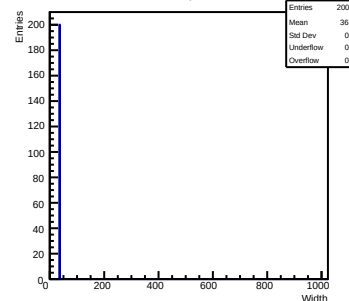
Width mcm 0 chip 0 chan 13 test

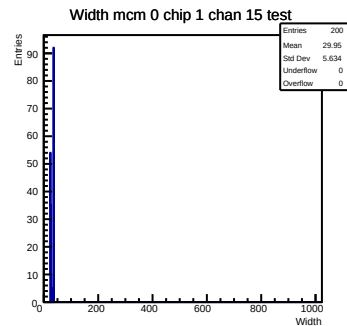
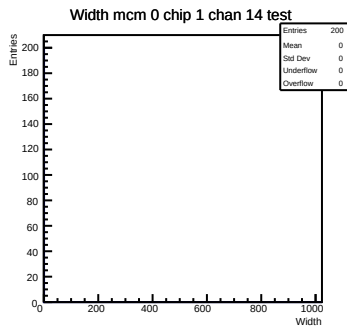
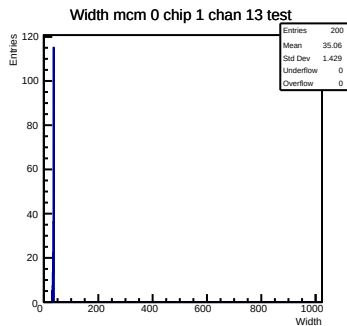
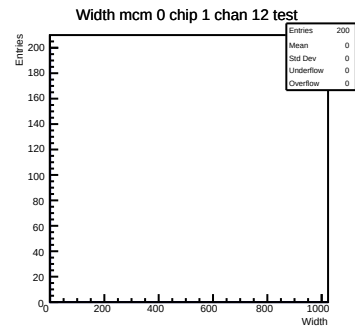
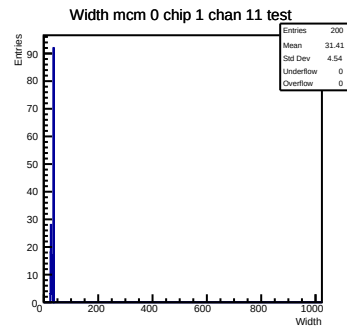
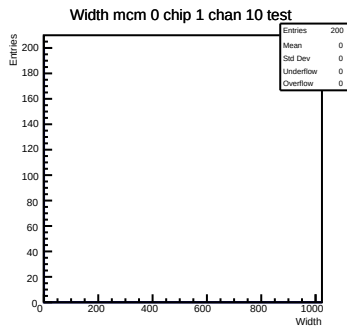
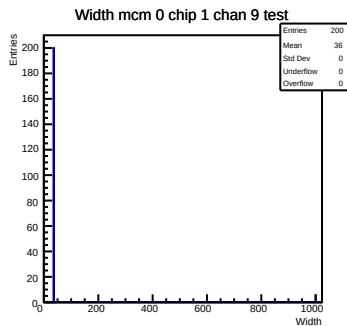
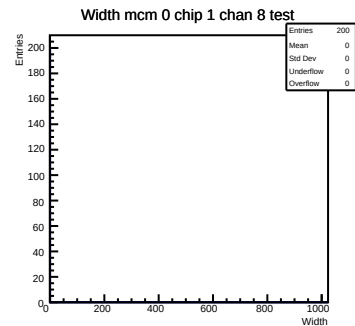
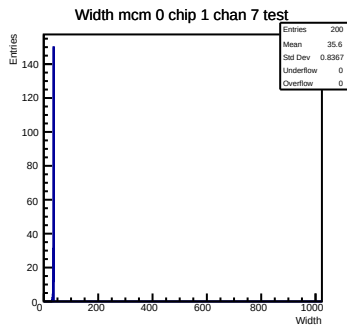
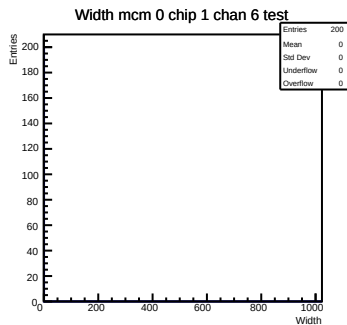
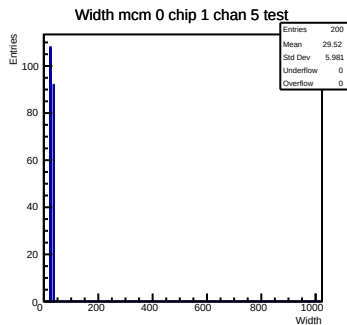
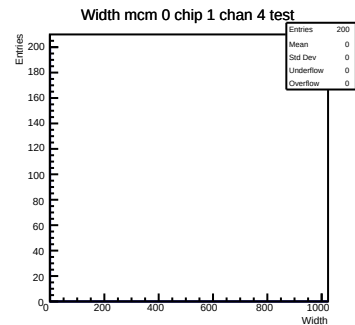
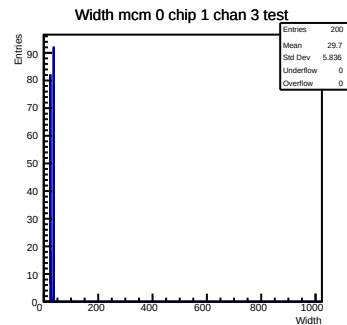
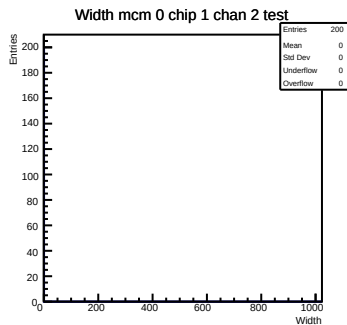
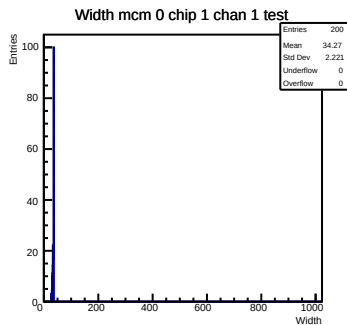
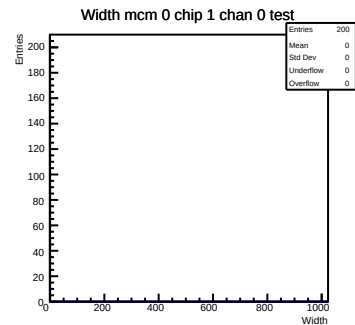


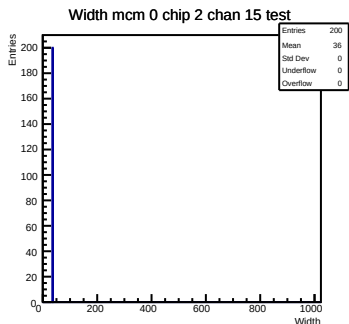
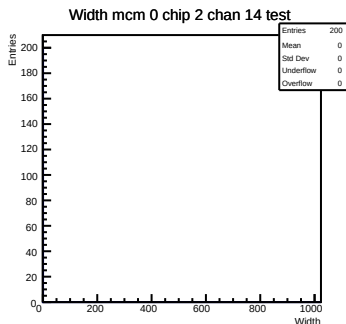
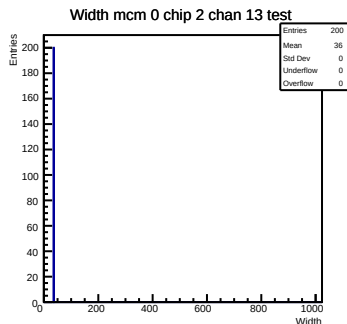
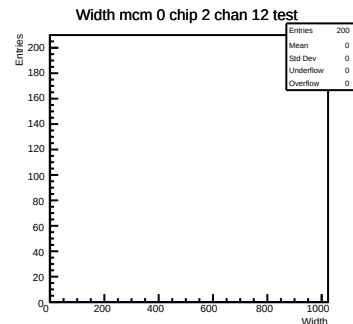
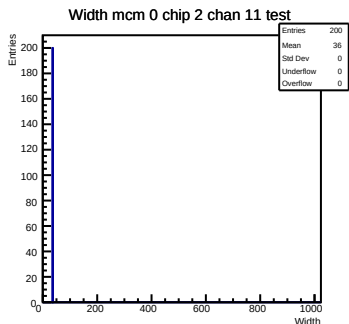
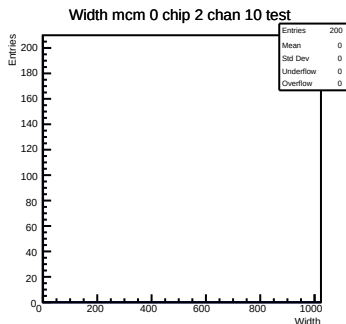
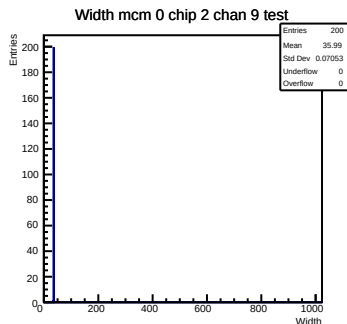
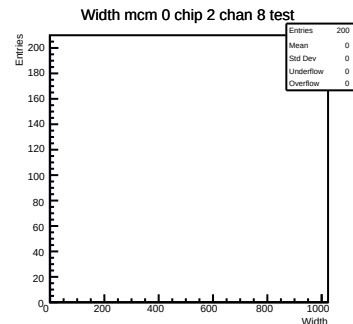
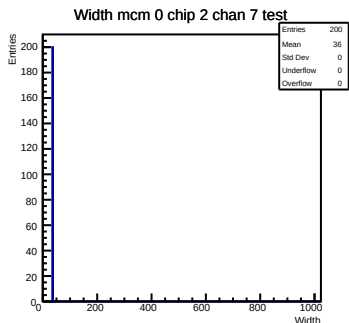
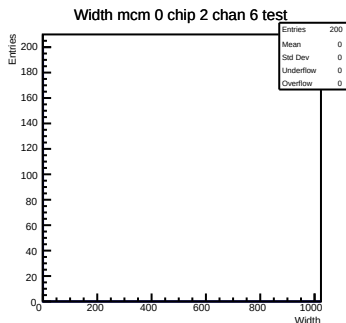
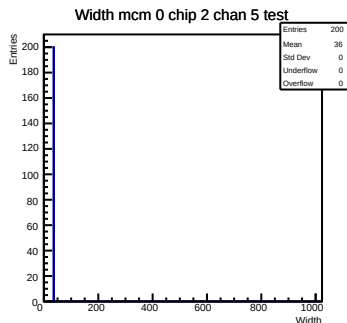
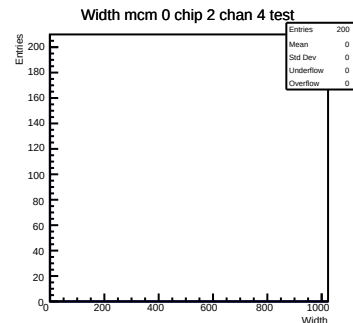
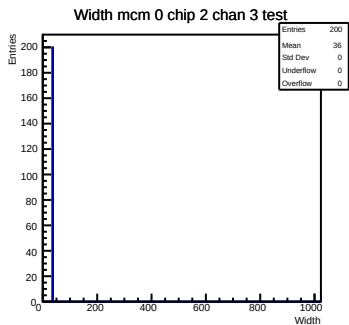
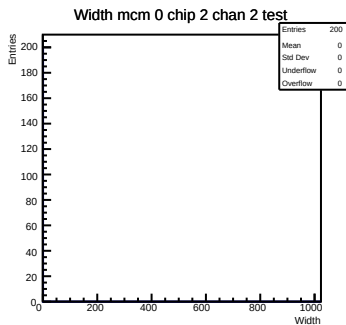
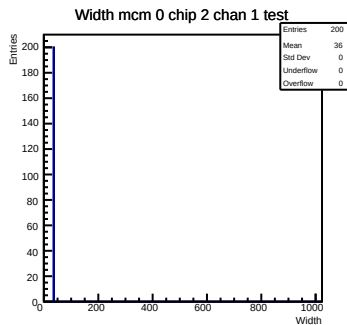
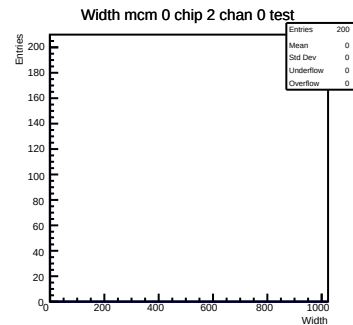
Width mcm 0 chip 0 chan 14 tes

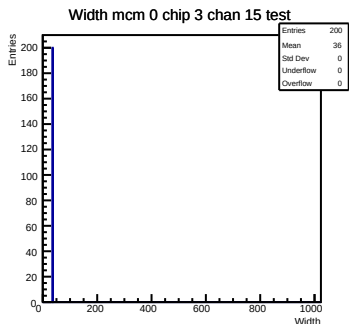
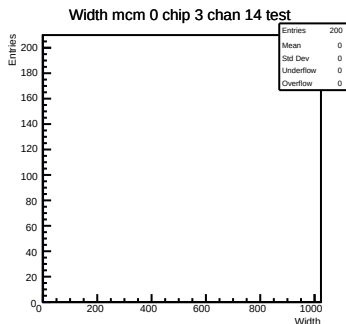
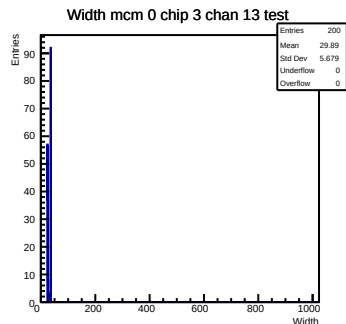
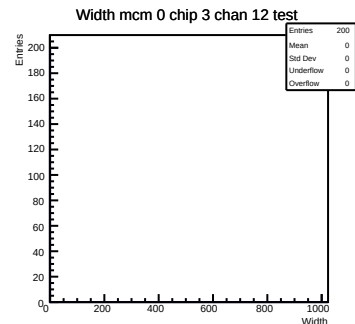
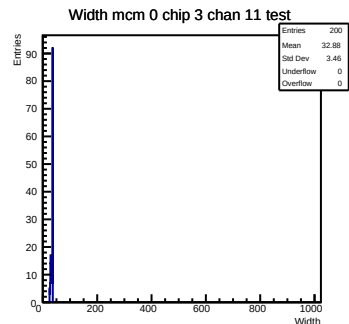
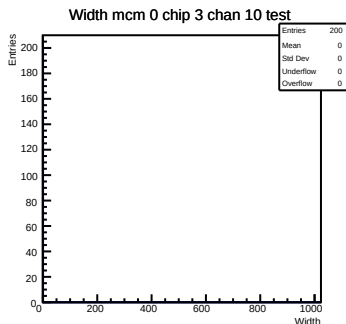
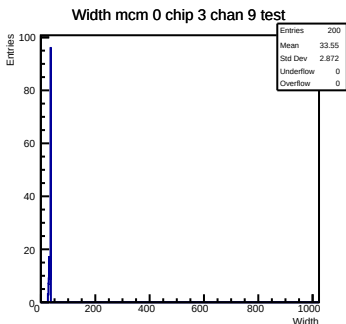
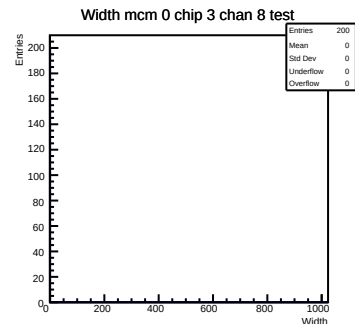
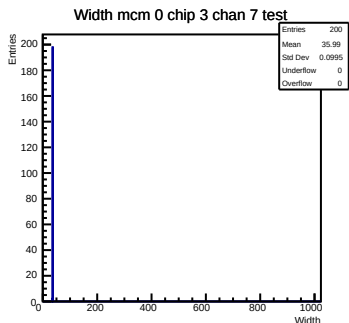
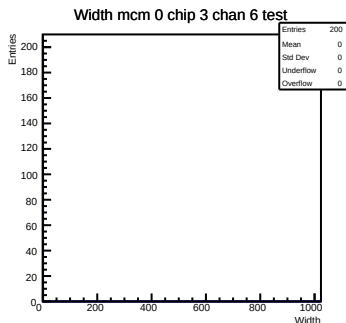
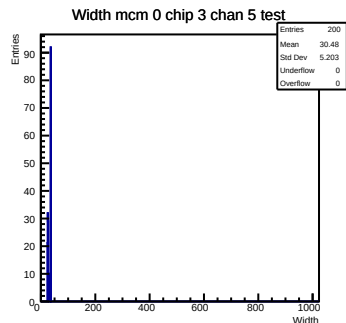
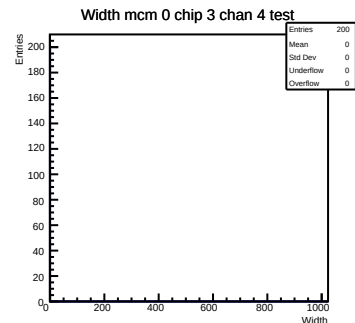
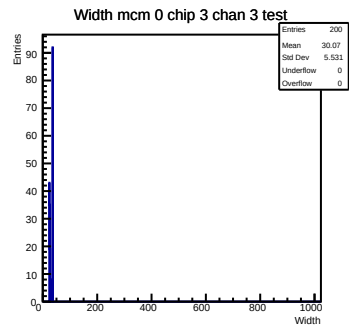
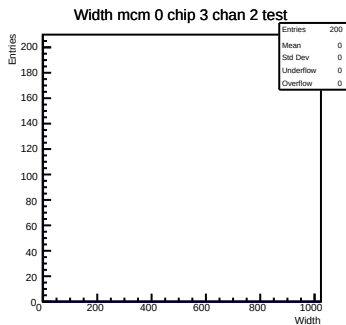
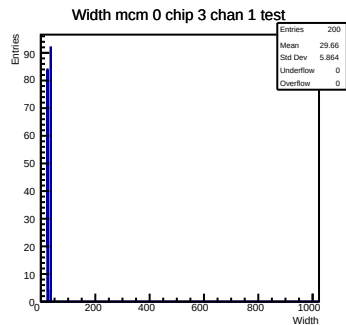
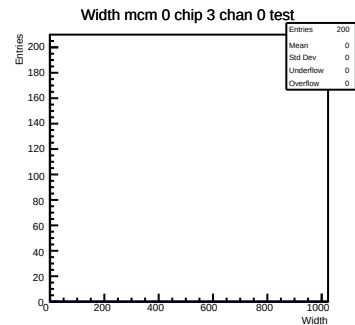


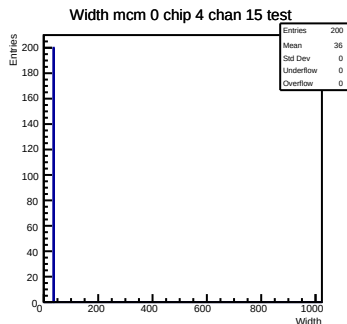
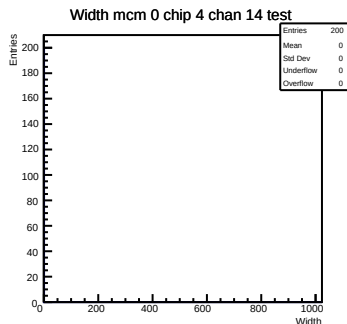
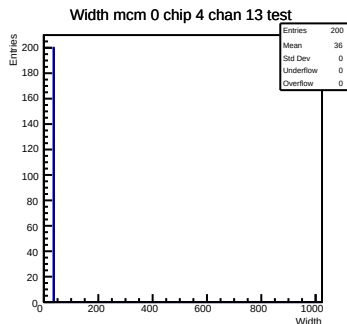
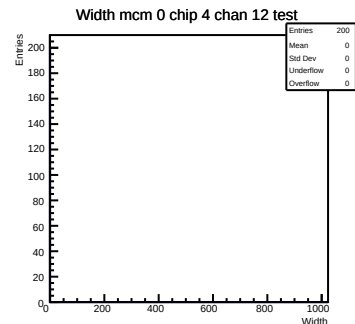
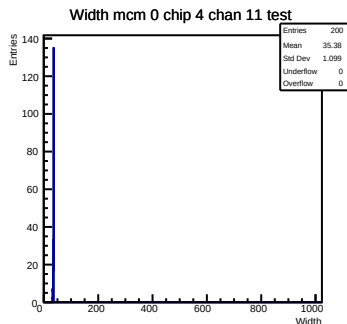
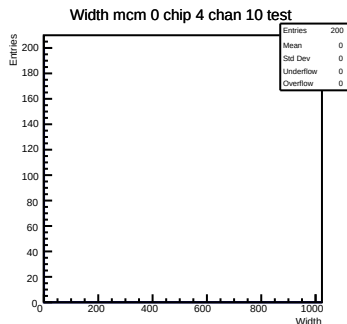
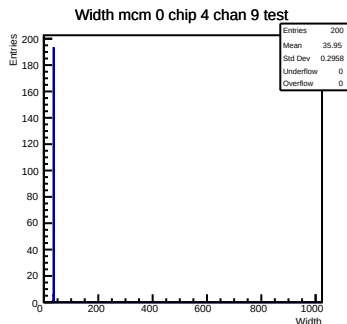
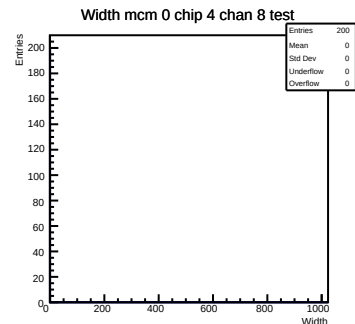
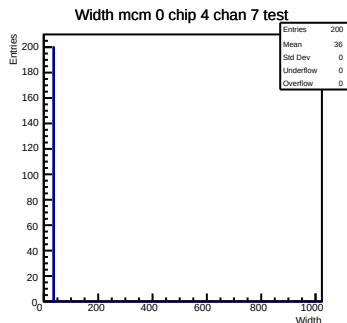
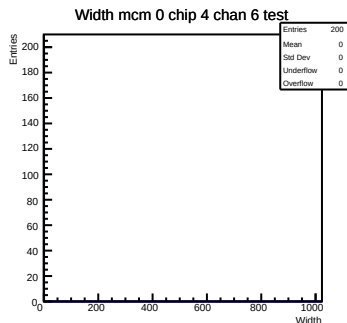
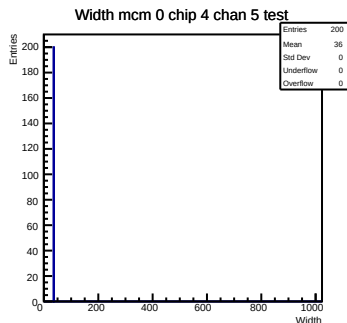
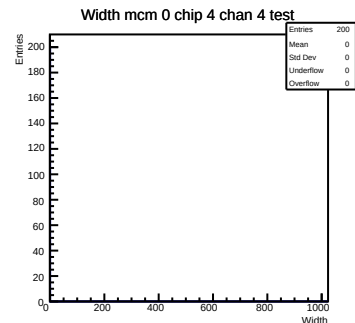
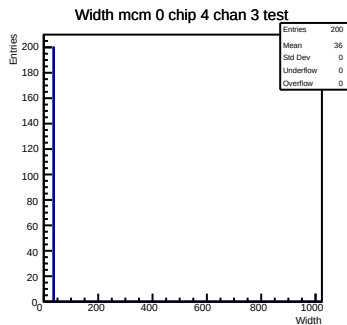
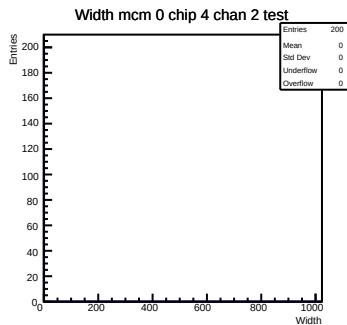
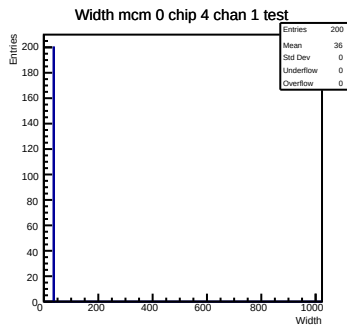
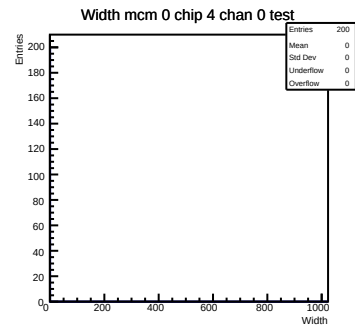
Width mcm 0 chip 0 chan 15 test

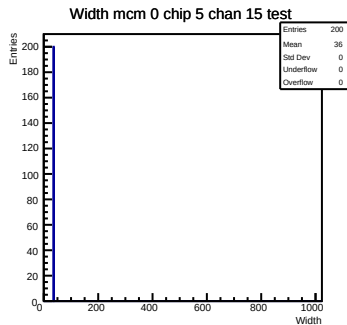
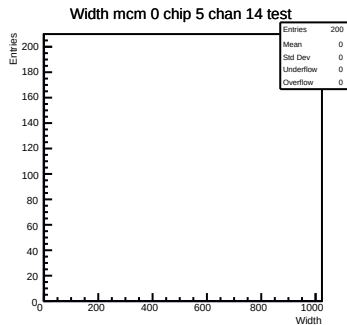
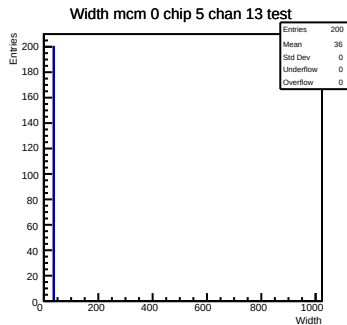
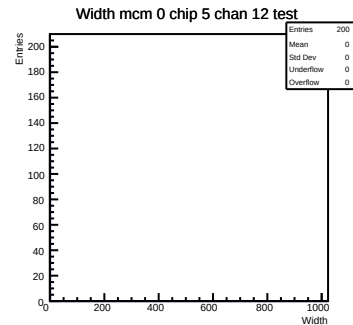
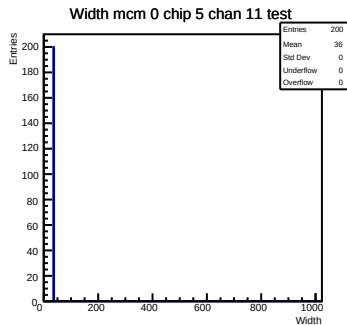
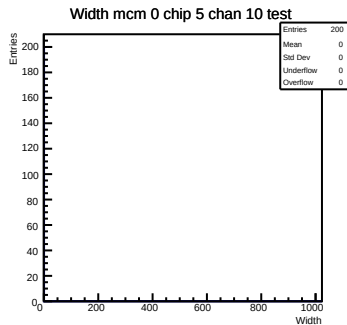
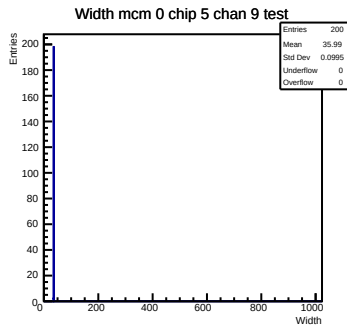
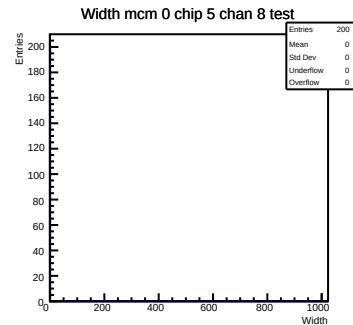
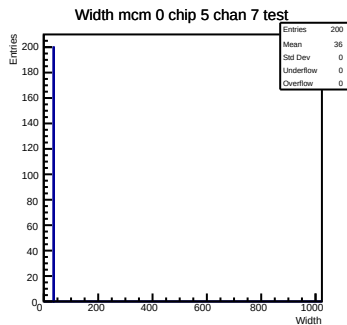
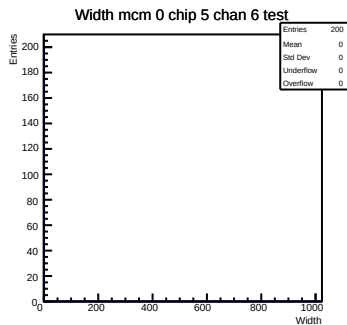
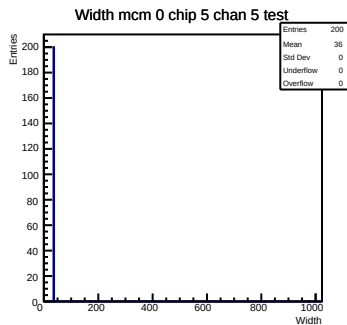
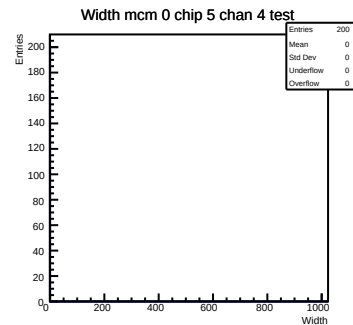
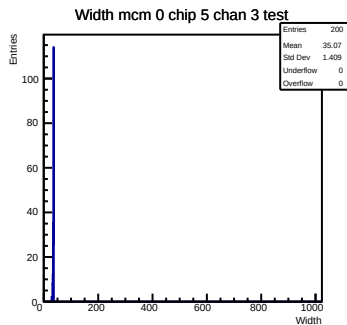
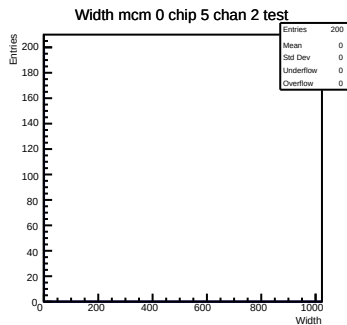
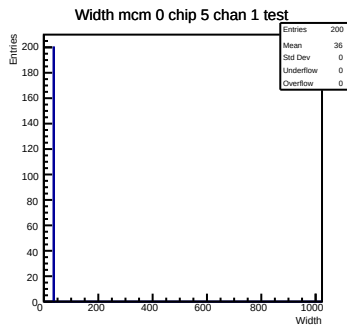
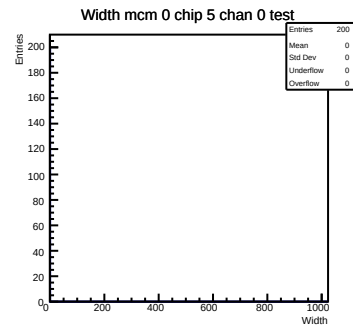




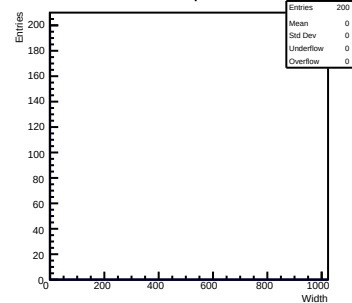




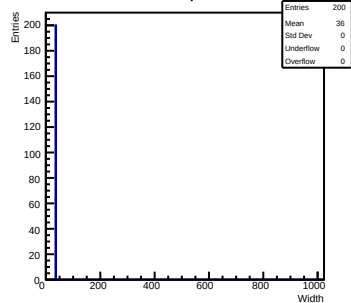




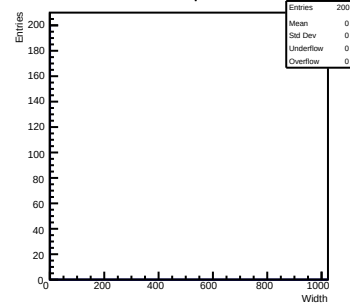
Width mcm 0 chip 6 chan 0 test



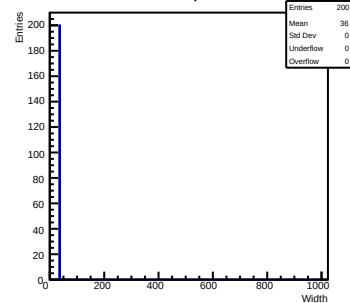
Width mcm 0 chip 6 chan 1 test



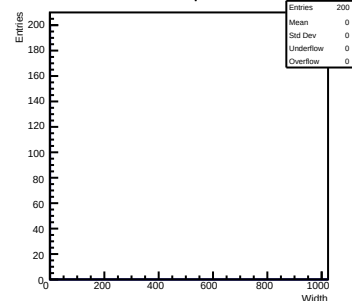
Width mcm 0 chip 6 chan 2 tes



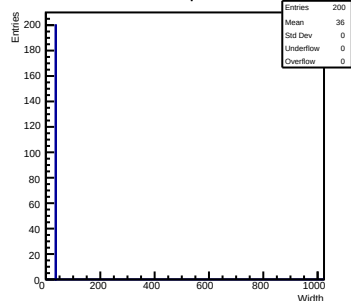
Width mcm 0 chip 6 chan 3 tes



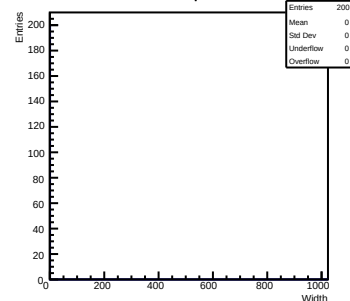
Width mcm 0 chip 6 chan 4 test



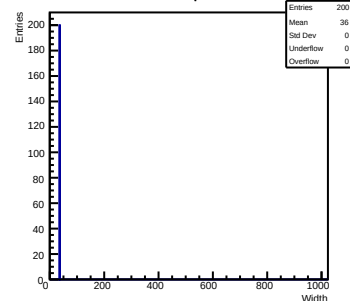
Width mcm 0 chip 6 chan 5 test



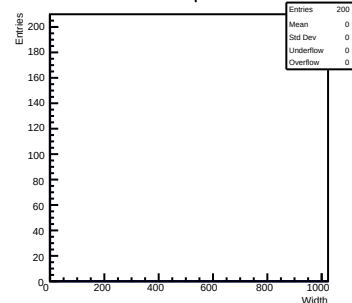
Width mcm 0 chip 6 chan 6 tes



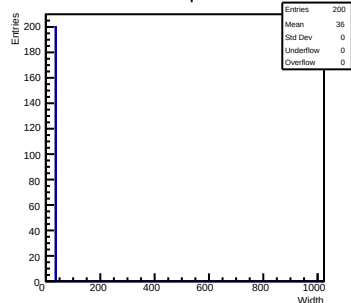
Width mcm 0 chip 6 chan 7 tes



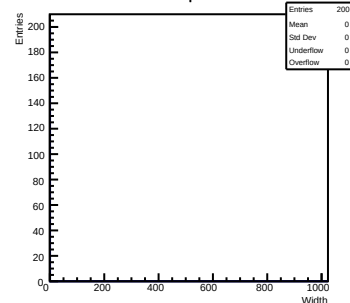
Width mcm 0 chip 6 chan 8 test



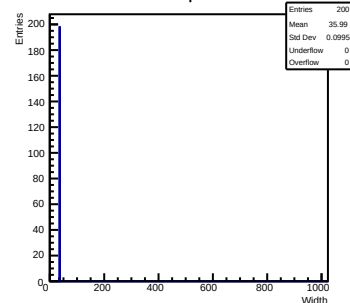
Width mcm 0 chip 6 chan 9 test



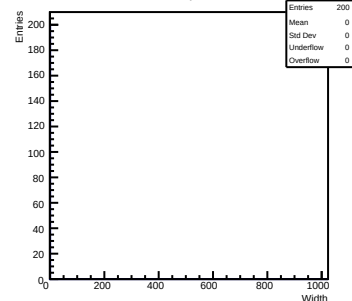
Width mcm 0 chip 6 chan 10 tes



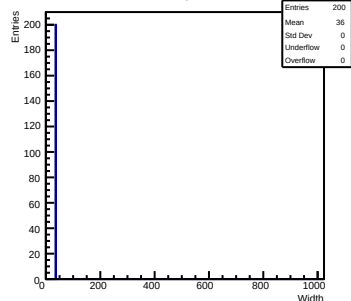
Width mcm 0 chip 6 chan 11 test



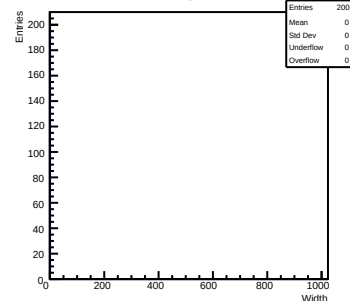
Width mcm 0 chip 6 chan 12 tes



Width mcm 0 chip 6 chan 13 tes



Width mcm 0 chip 6 chan 14 tes



Width mcm 0 chip 6 chan 15 tes

