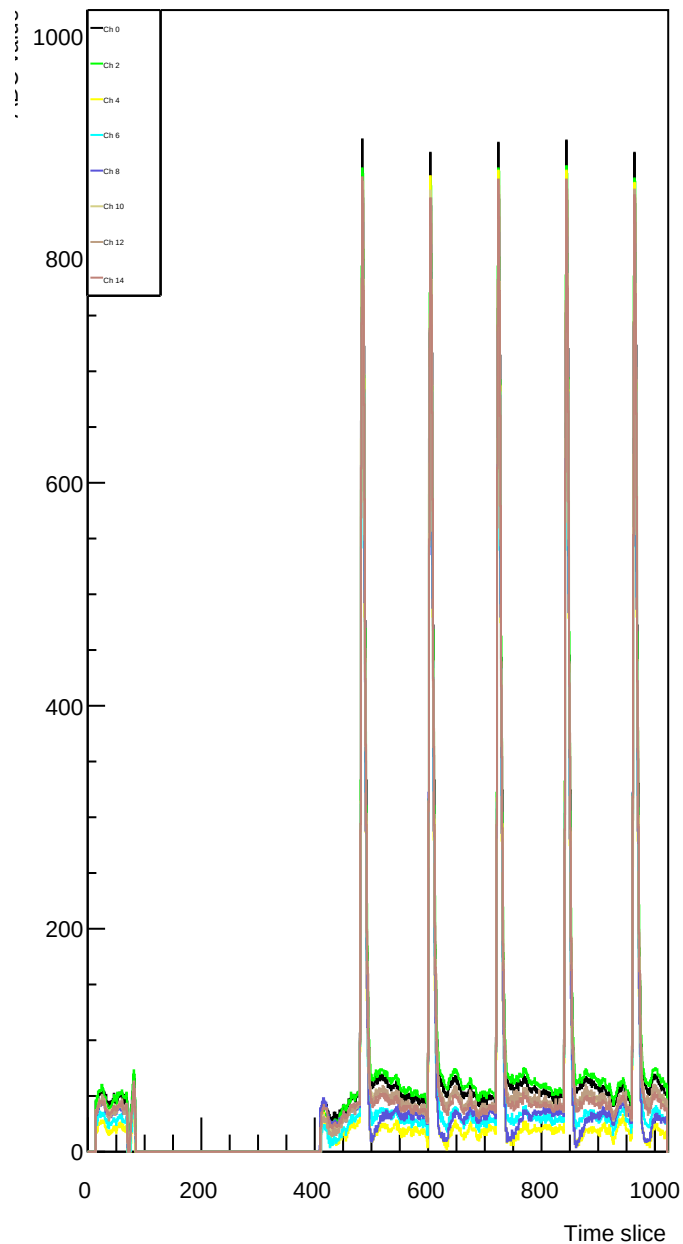
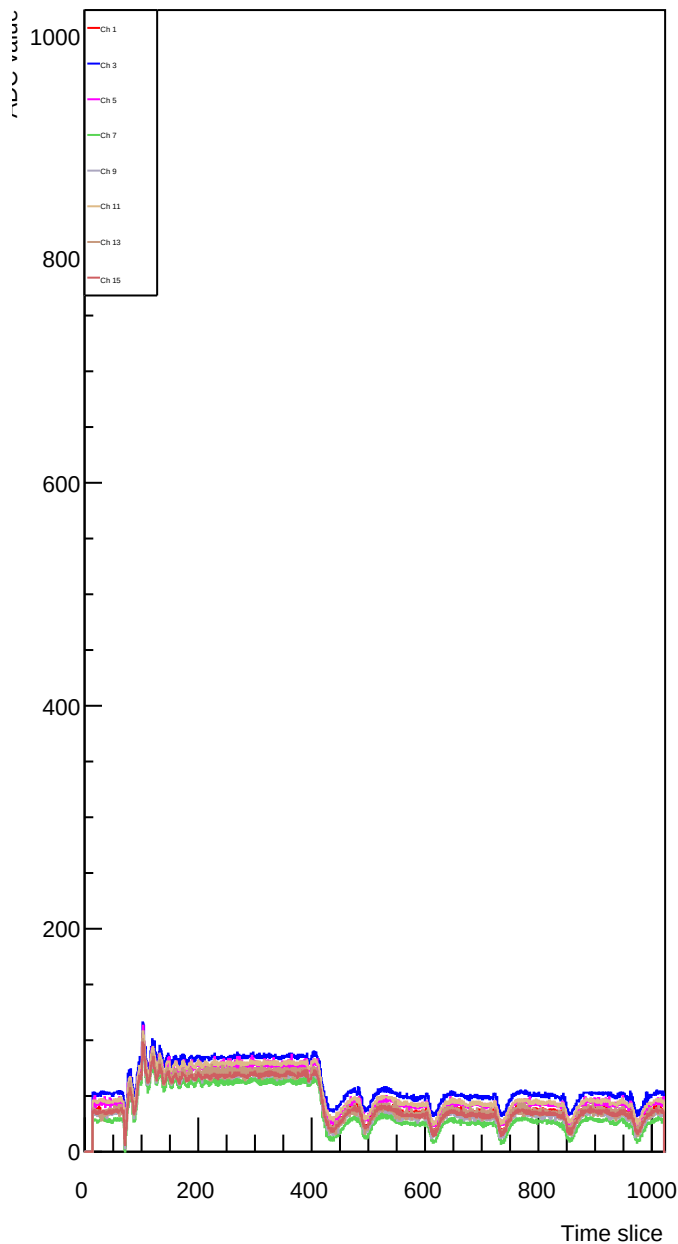


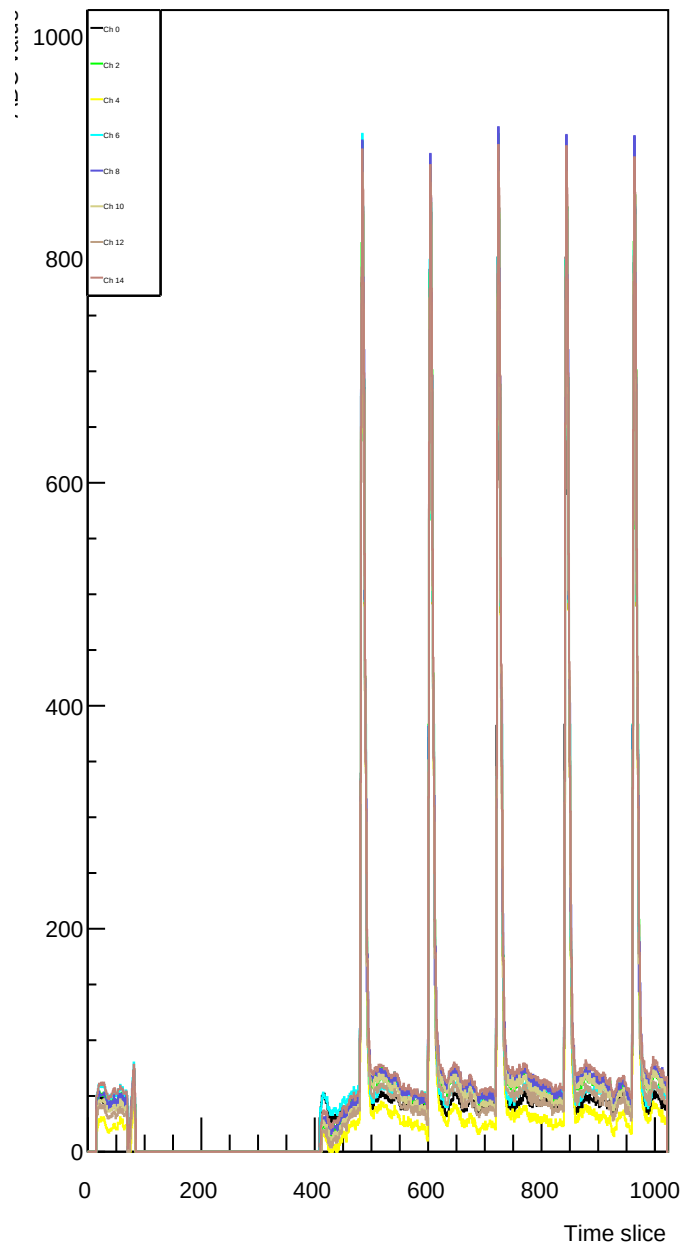
Run 0 event 5 mcm 0 chip 0 s1-clk3 even ch



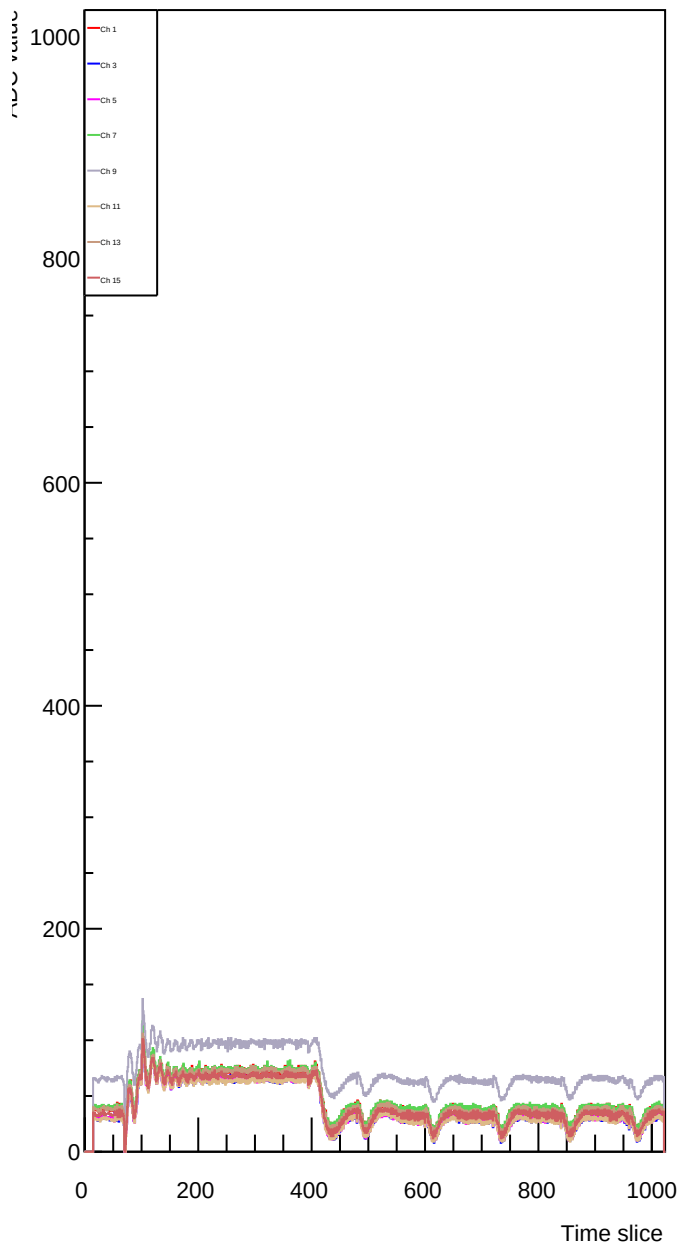
Run 0 event 5 mcm 0 chip 0 s1-clk3 odd ch



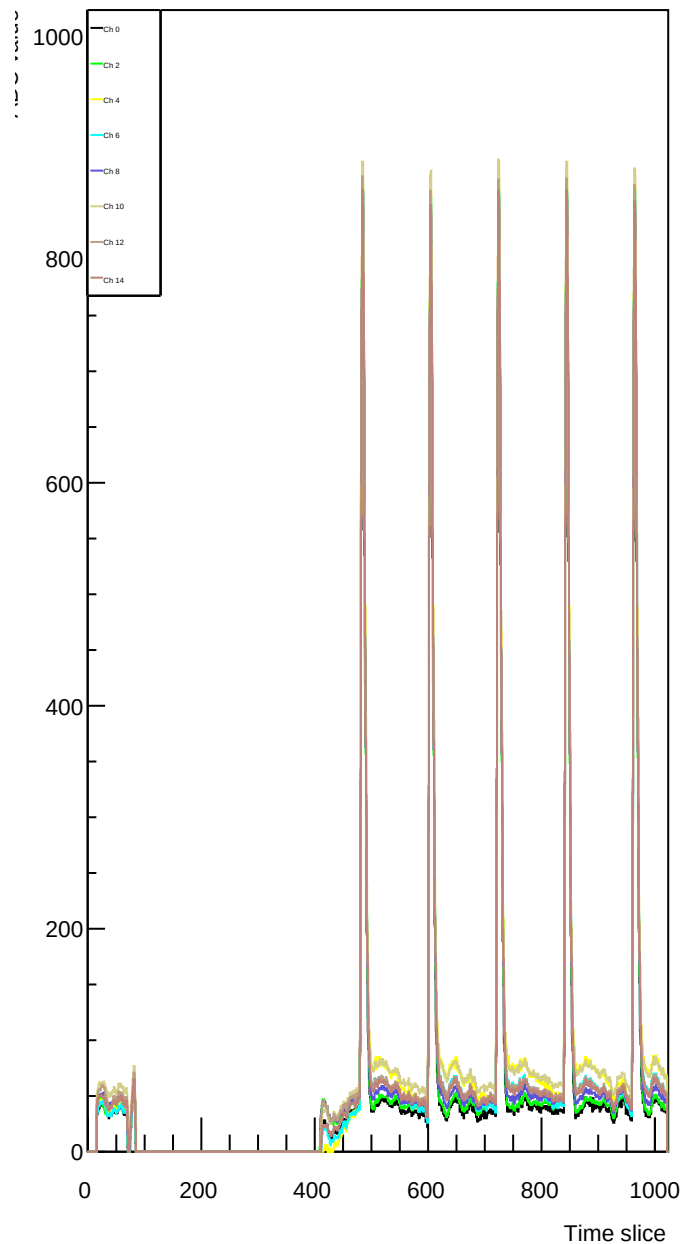
Run 0 event 5 mcm 0 chip 1 s1-clk3 even ch



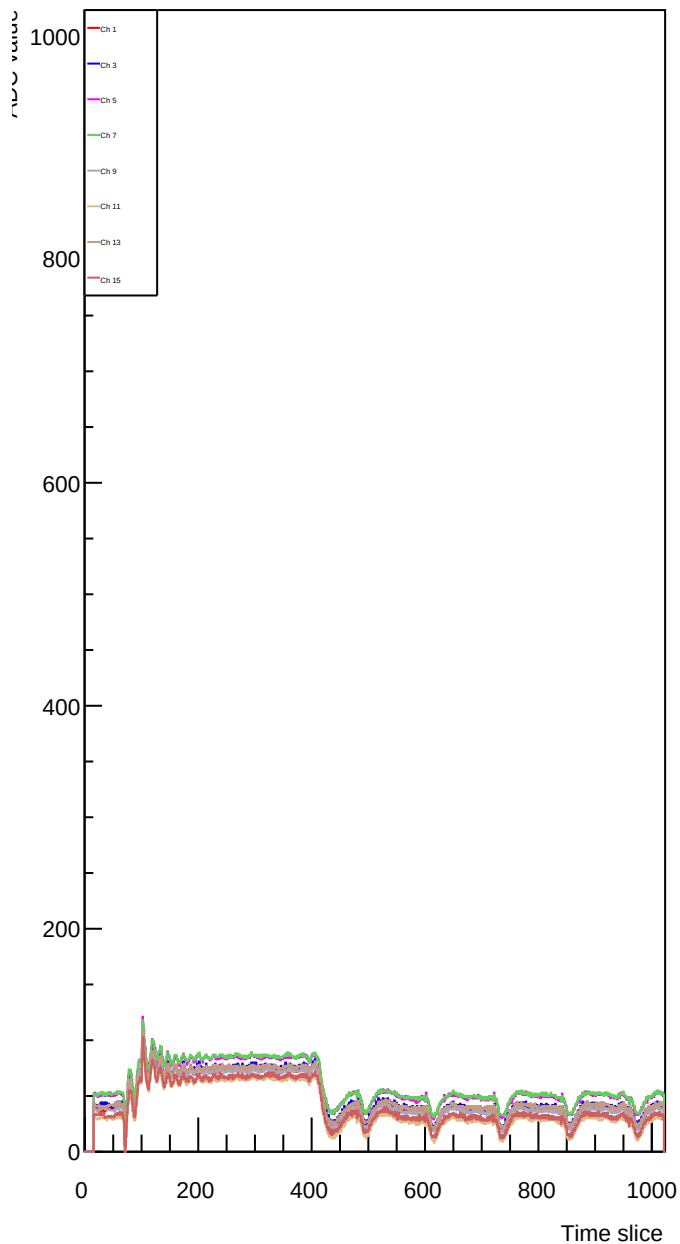
Run 0 event 5 mcm 0 chip 1 s1-clk3 odd ch



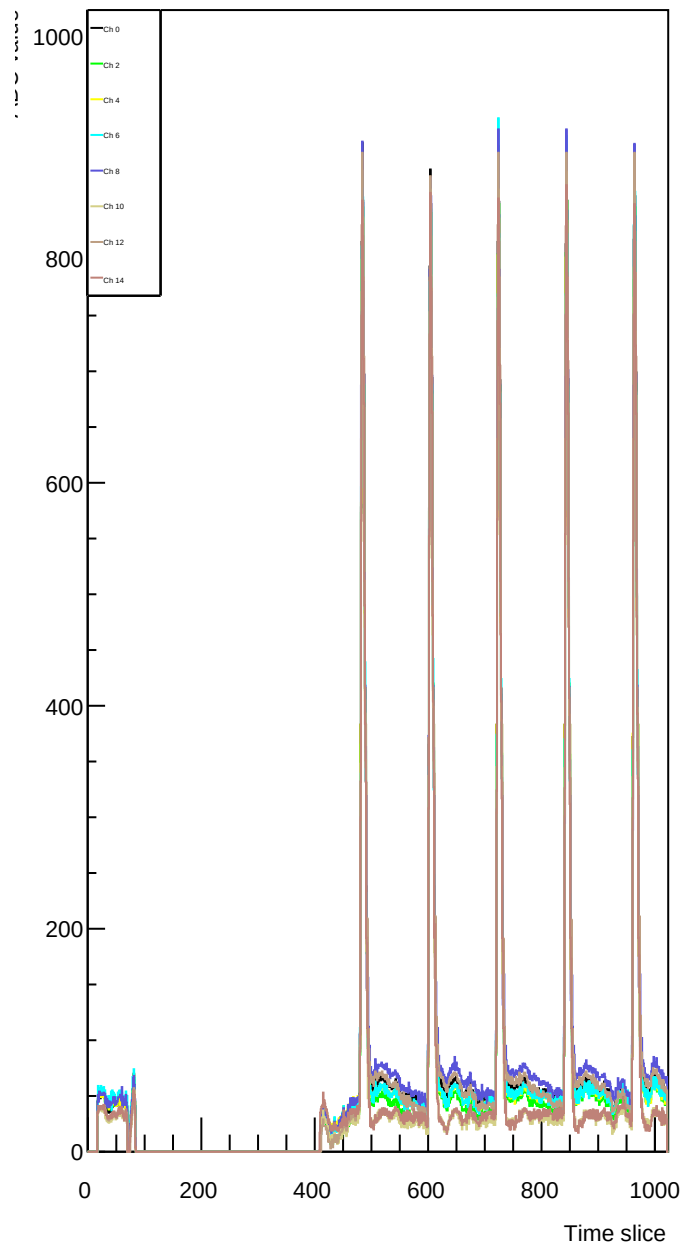
Run 0 event 5 mcm 0 chip 2 s1-clk3 even ch



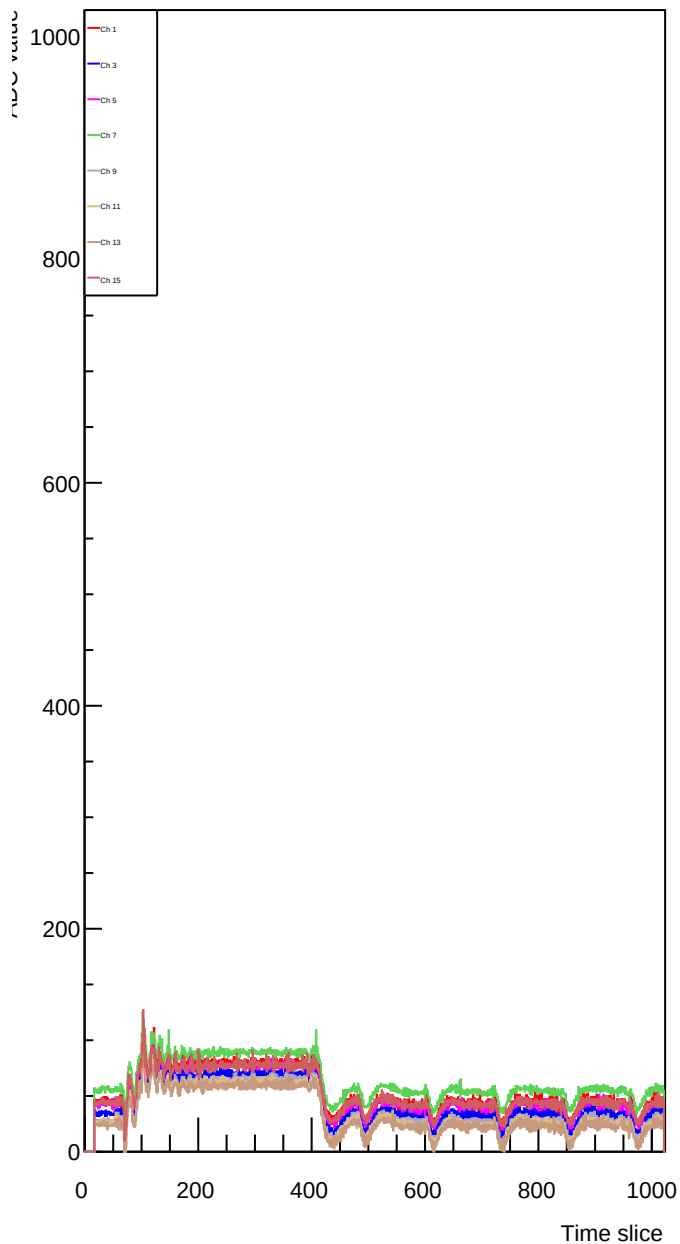
Run 0 event 5 mcm 0 chip 2 s1-clk3 odd ch



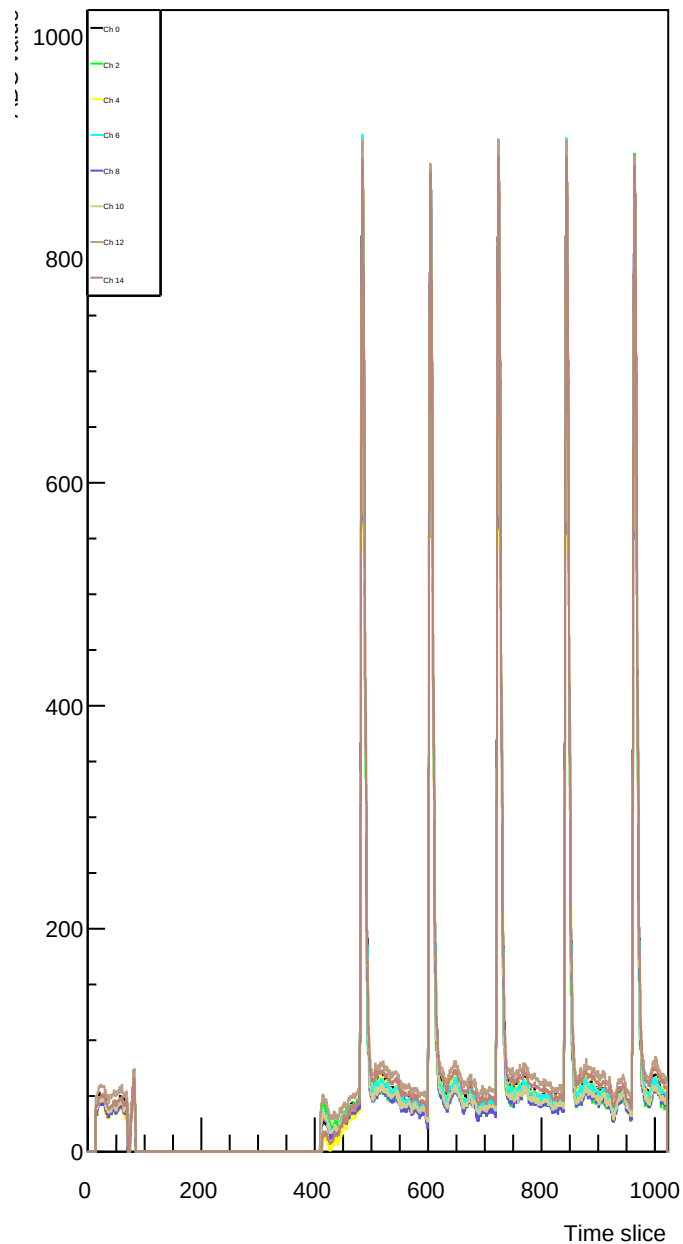
Run 0 event 5 mcm 0 chip 3 s1-clk3 even ch



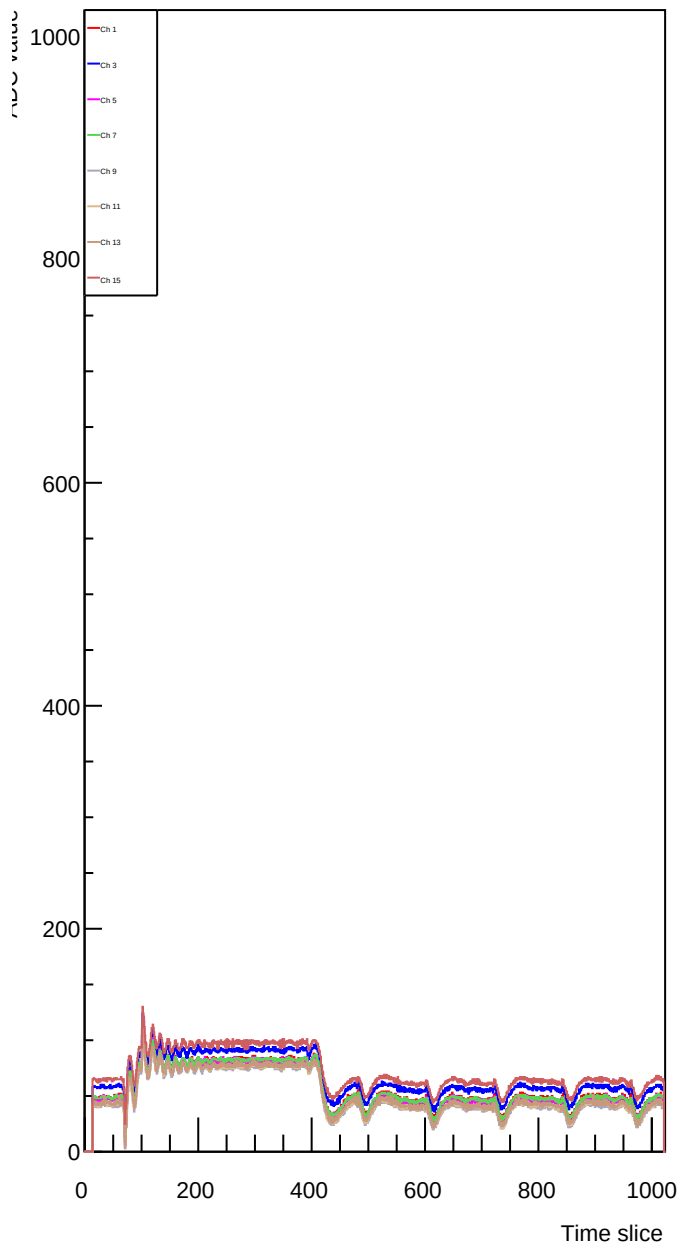
Run 0 event 5 mcm 0 chip 3 s1-clk3 odd ch



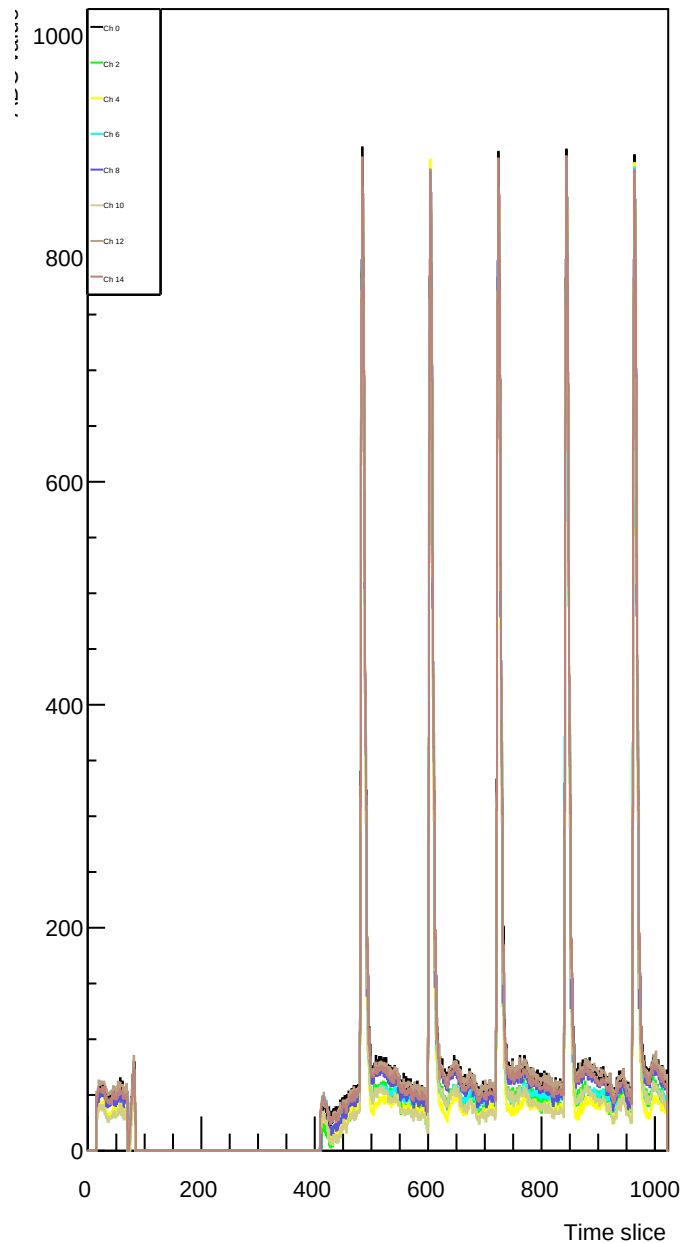
Run 0 event 5 mcm 0 chip 4 s1-clk3 even ch



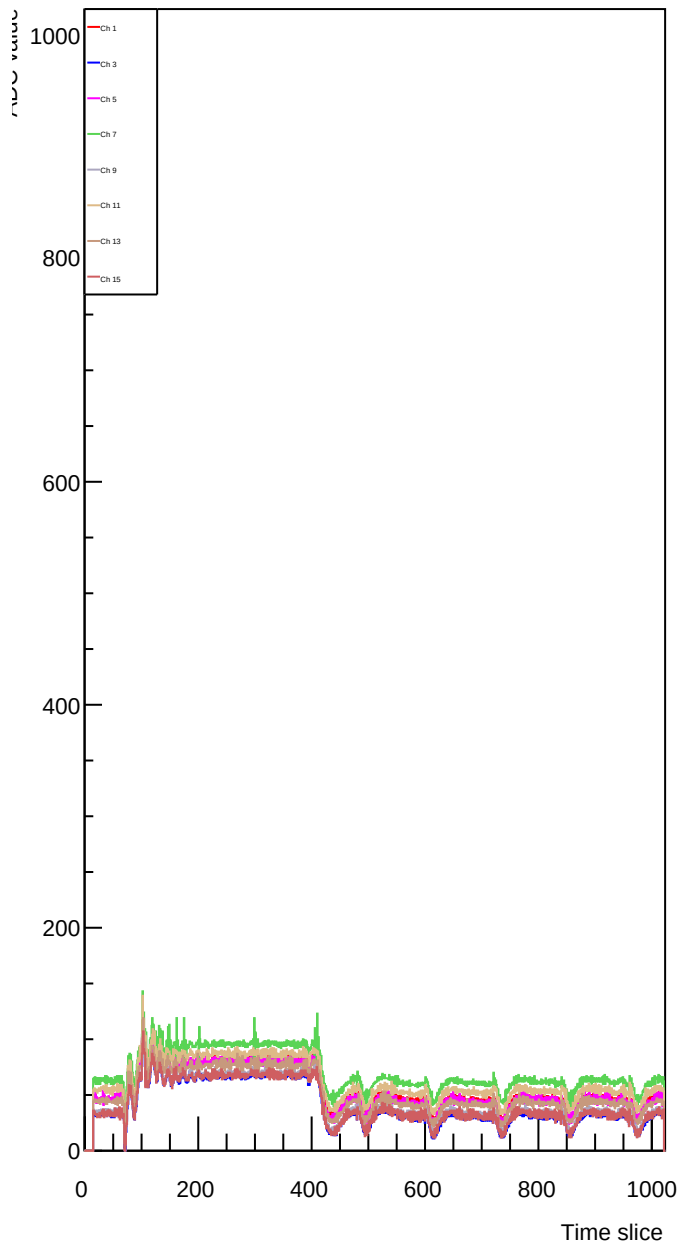
Run 0 event 5 mcm 0 chip 4 s1-clk3 odd ch



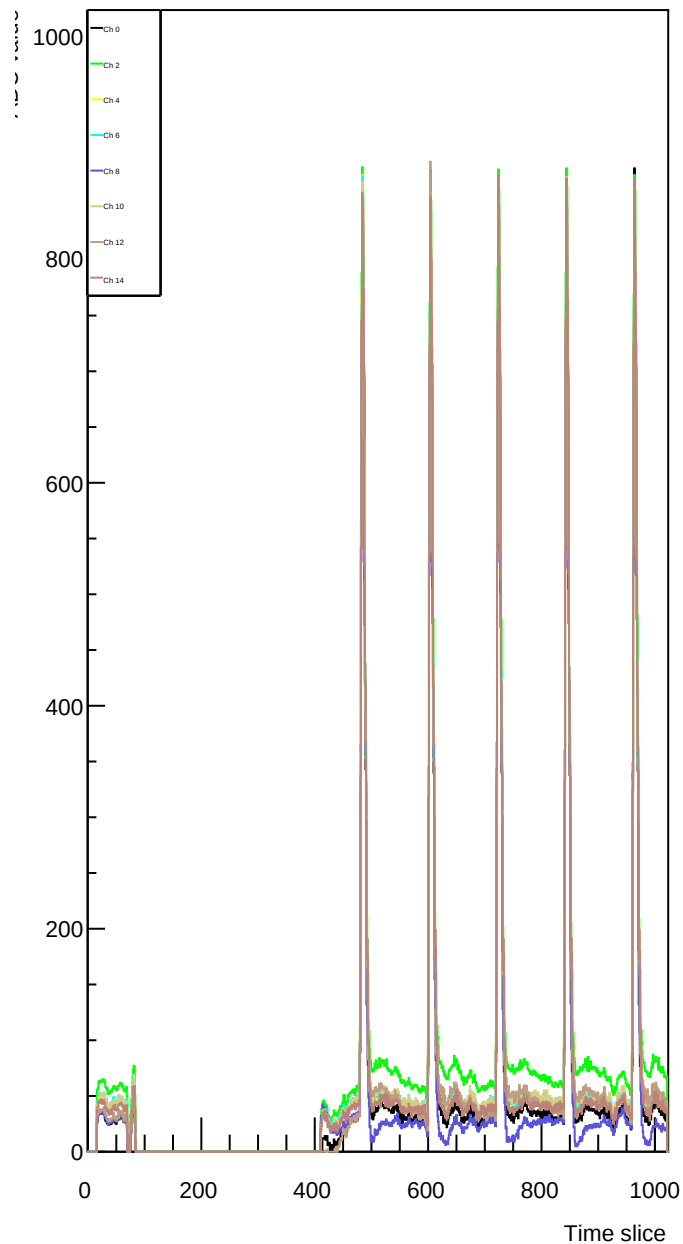
Run 0 event 5 mcm 0 chip 5 s1-clk3 even ch



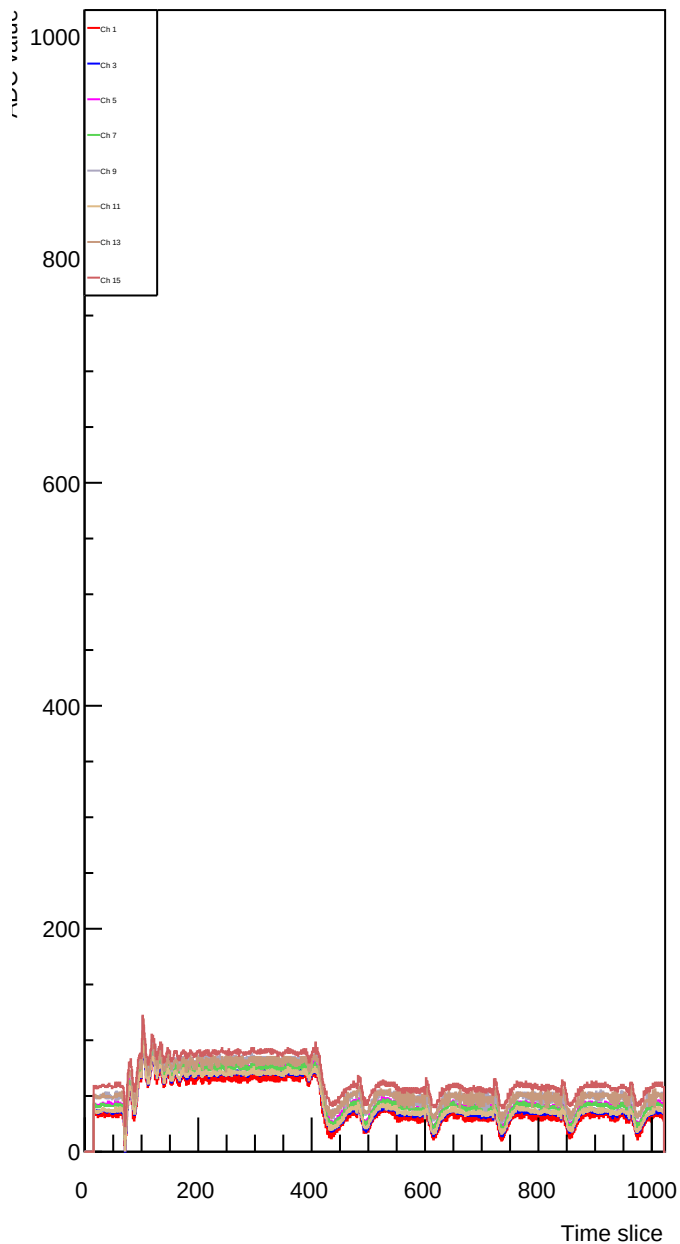
Run 0 event 5 mcm 0 chip 5 s1-clk3 odd ch



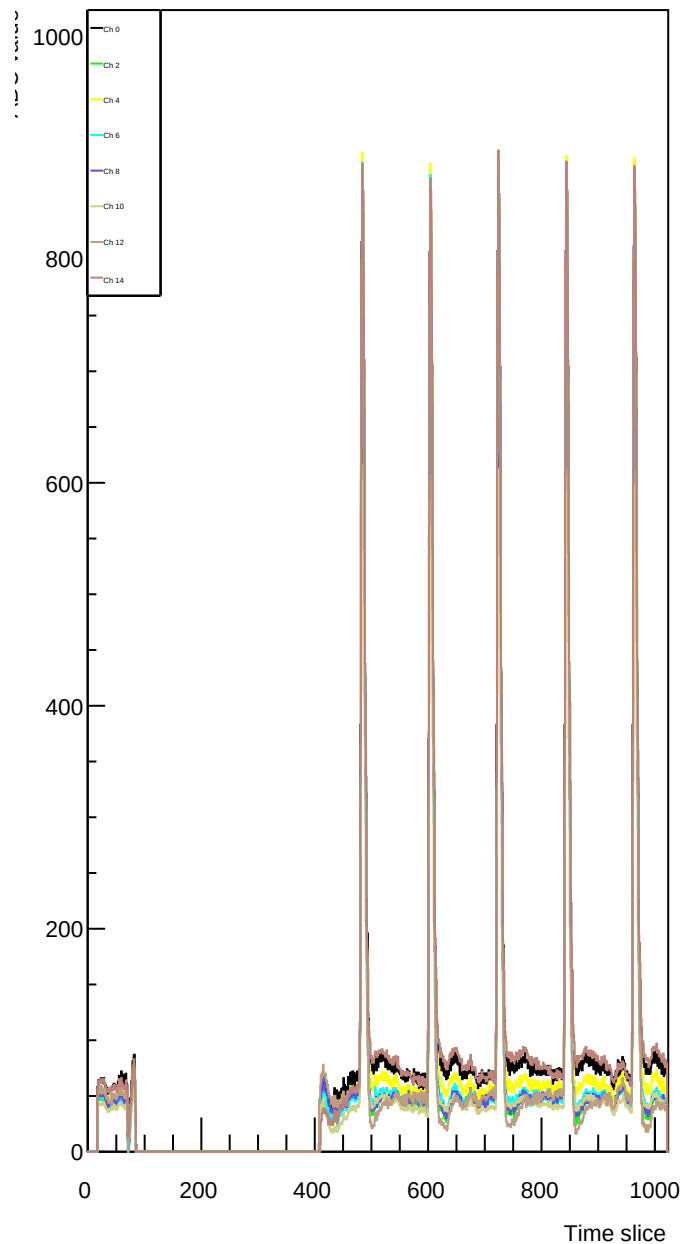
Run 0 event 5 mcm 0 chip 6 s1-clk3 even ch



Run 0 event 5 mcm 0 chip 6 s1-clk3 odd ch



Run 0 event 5 mcm 0 chip 7 s1-clk3 even ch



Run 0 event 5 mcm 0 chip 7 s1-clk3 odd ch

