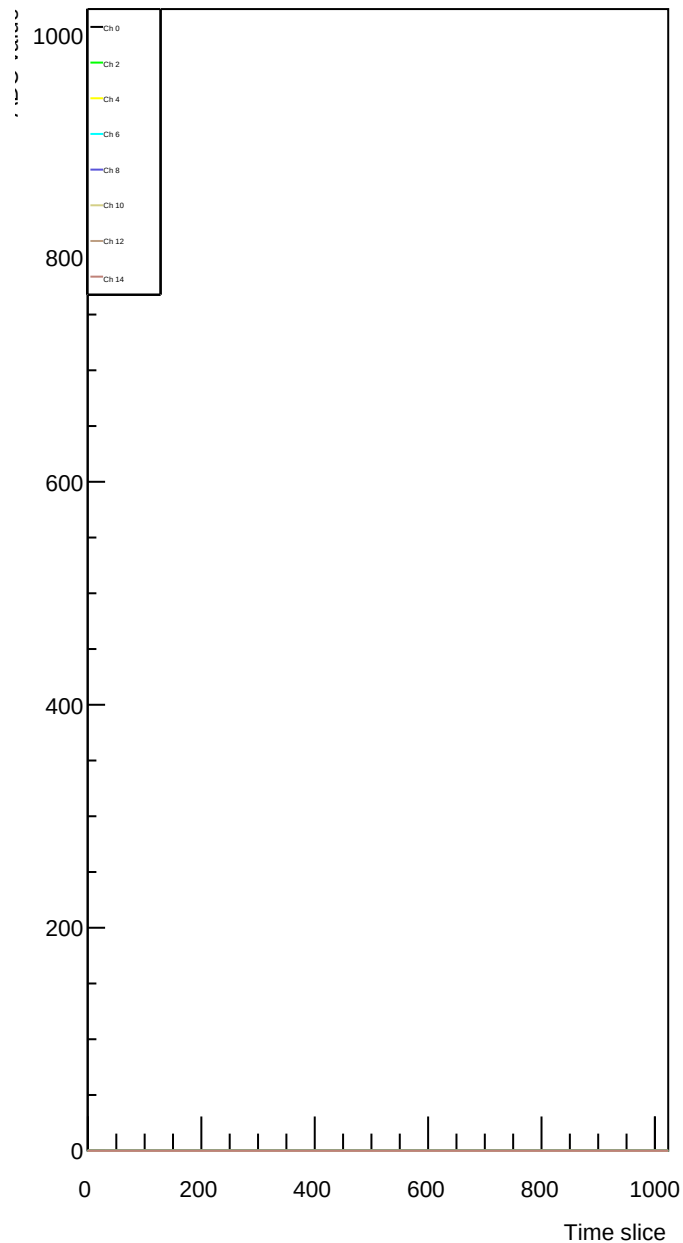
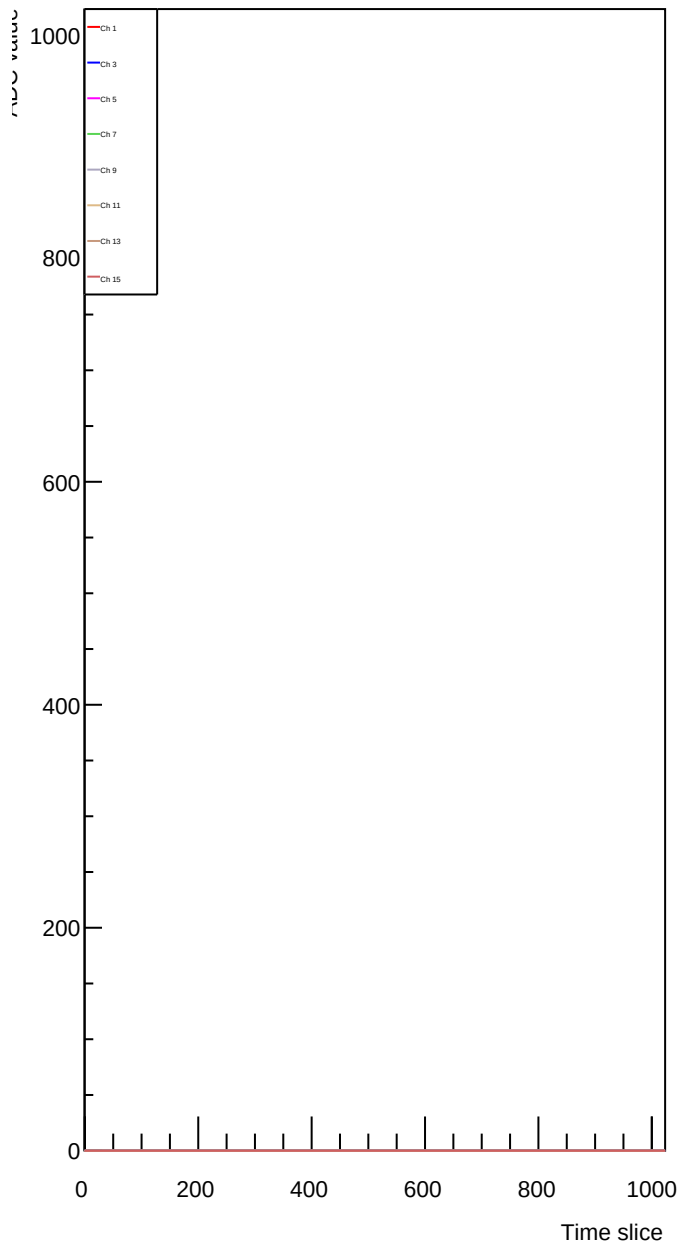


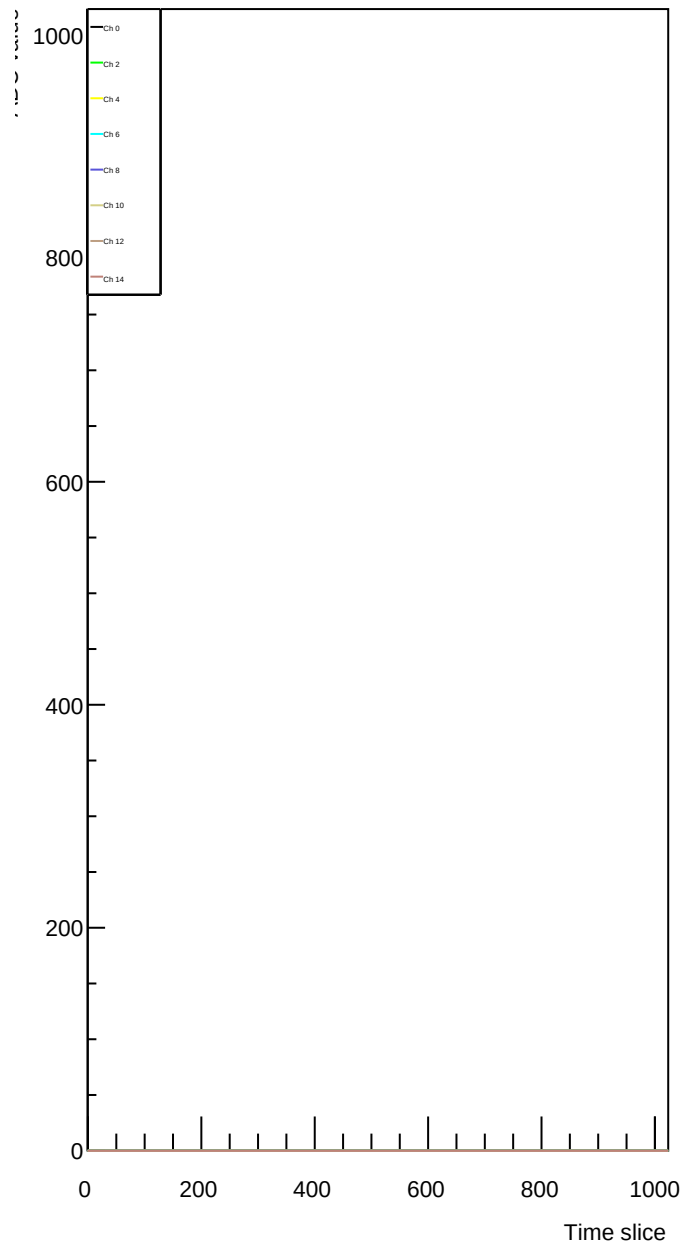
Run 0 event 5 mcm 0 chip 0 s3-clk2 even ch



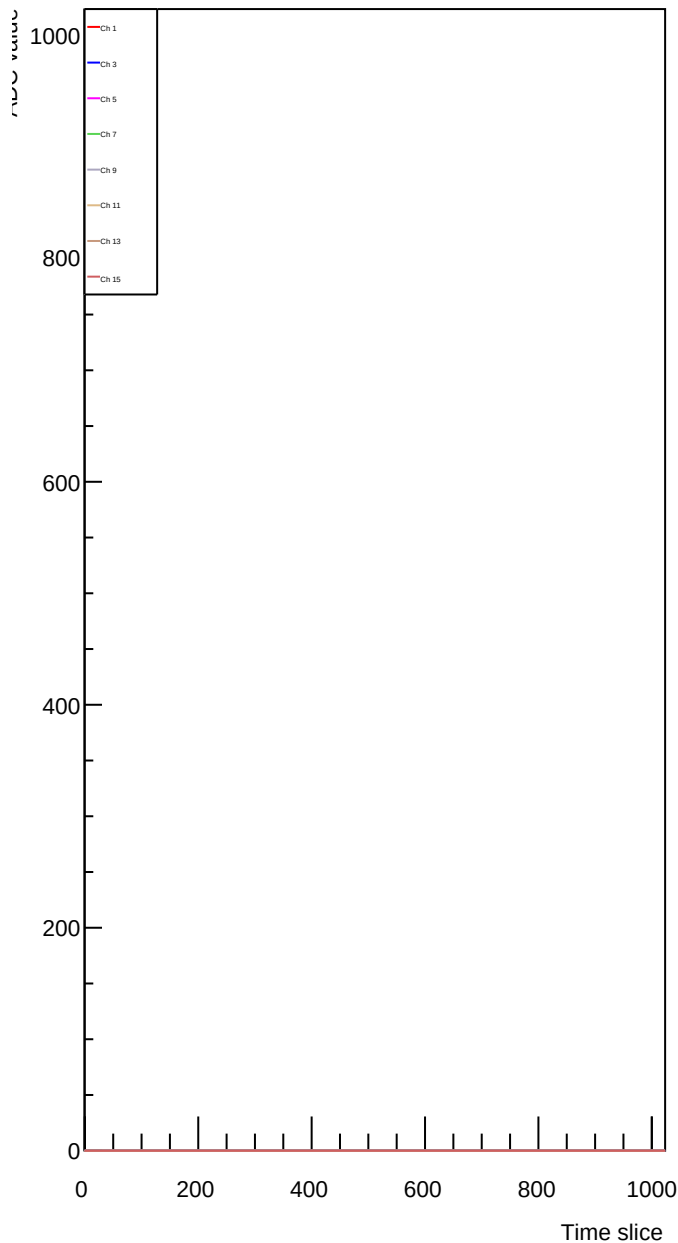
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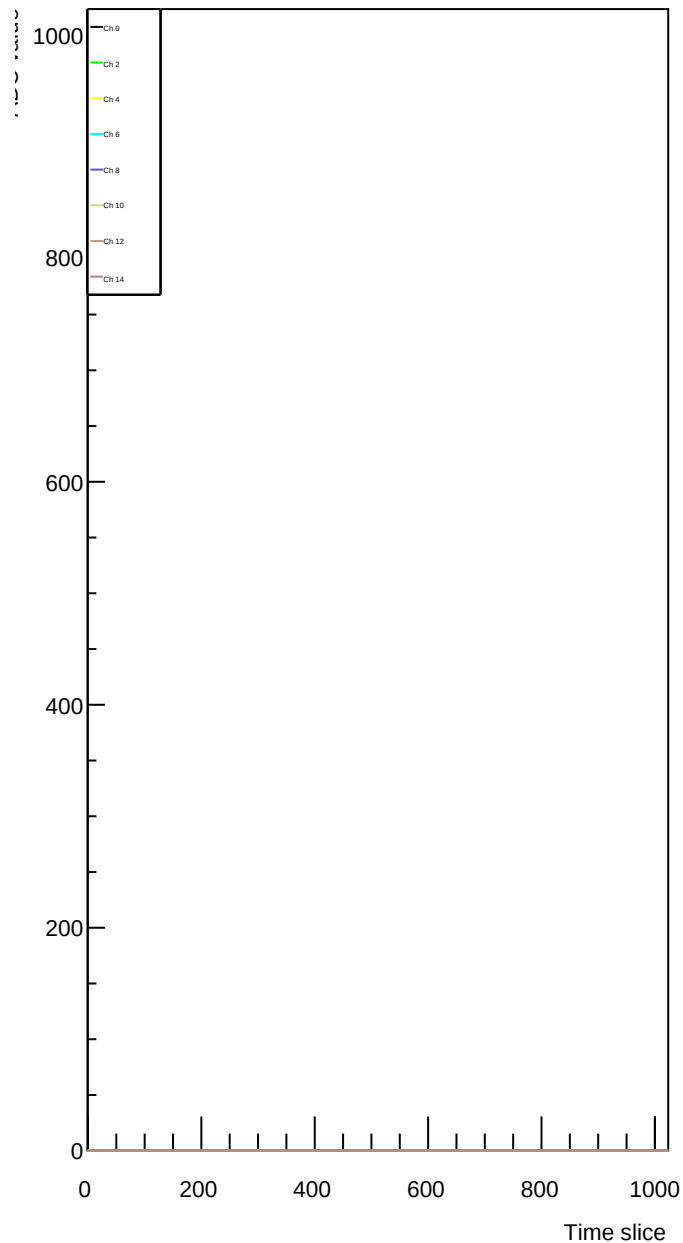
Run 0 event 5 mcm 0 chip 1 s3-clk2 even ch



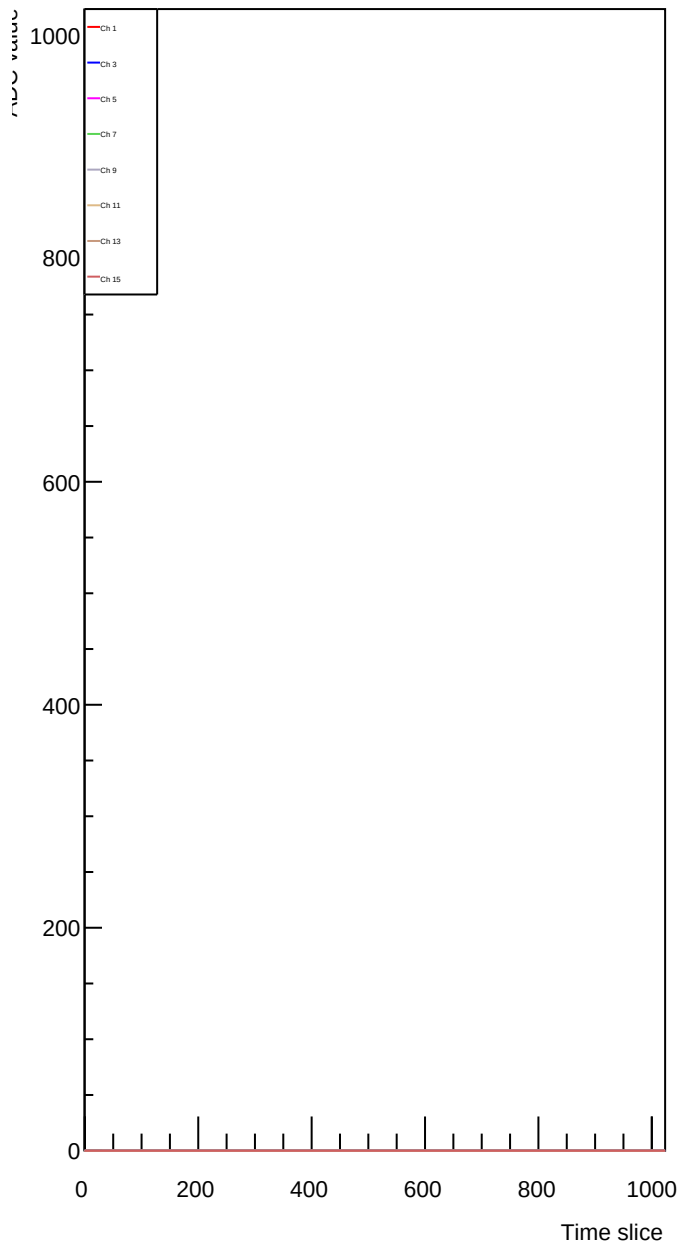
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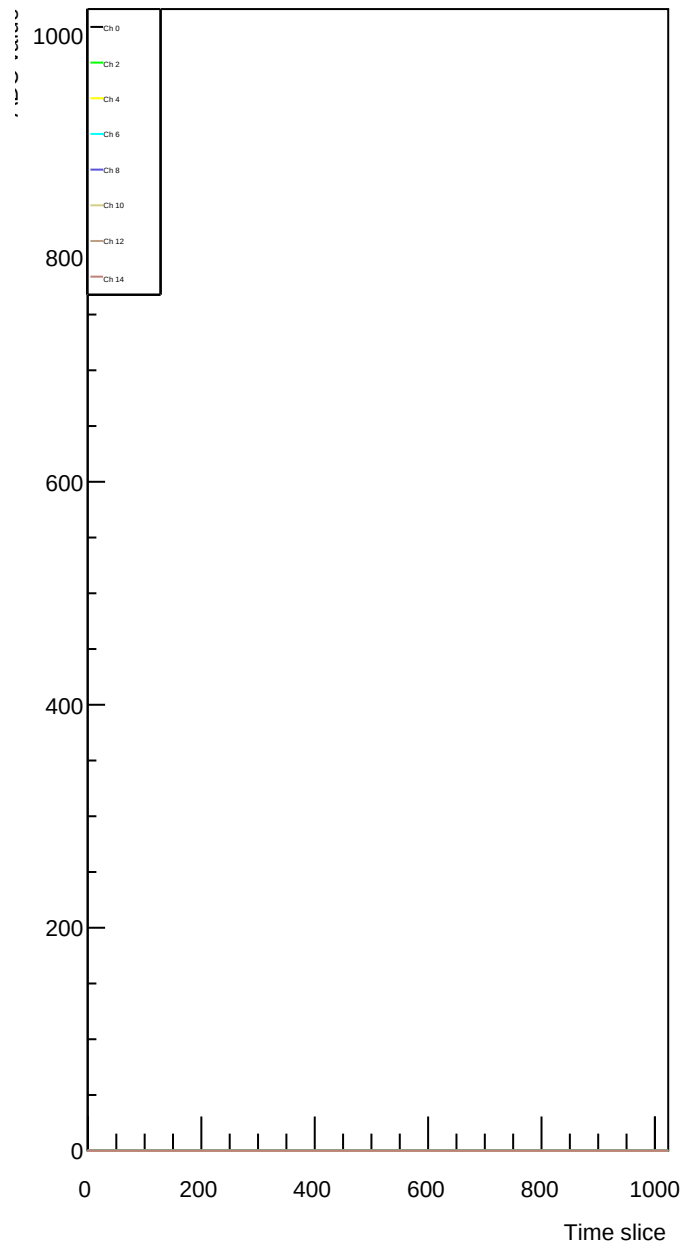
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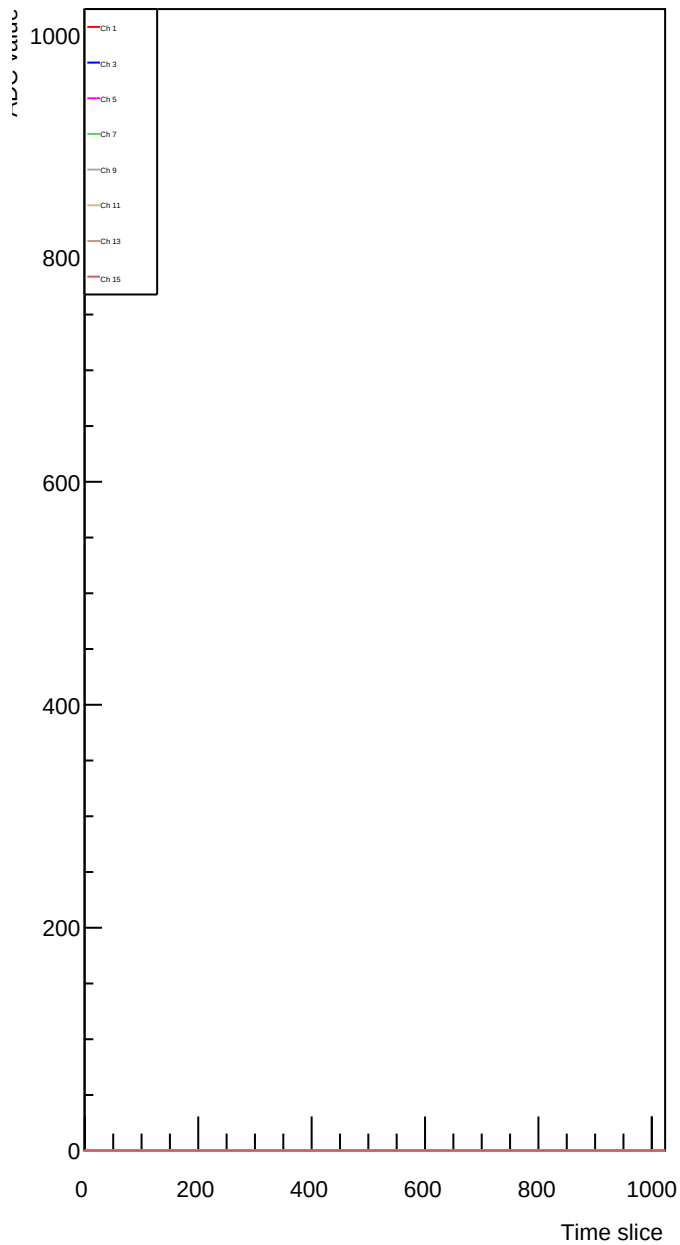
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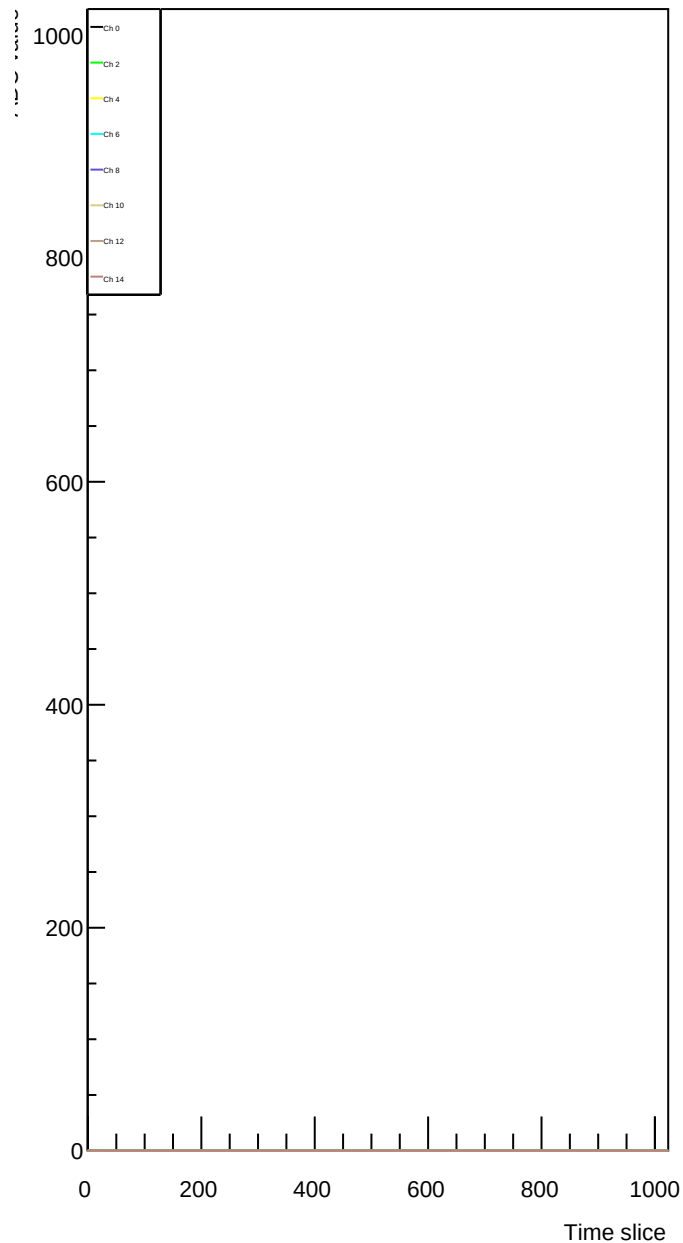
Run 0 event 5 mcm 0 chip 3 s3-clk2 even ch



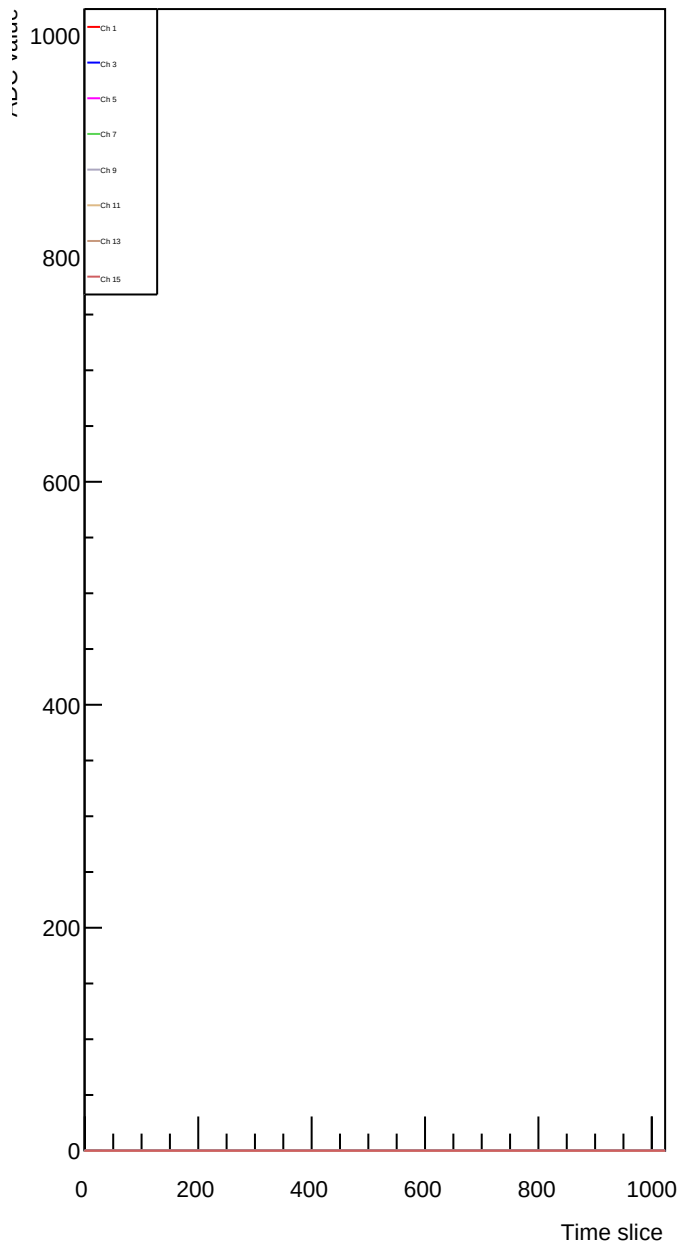
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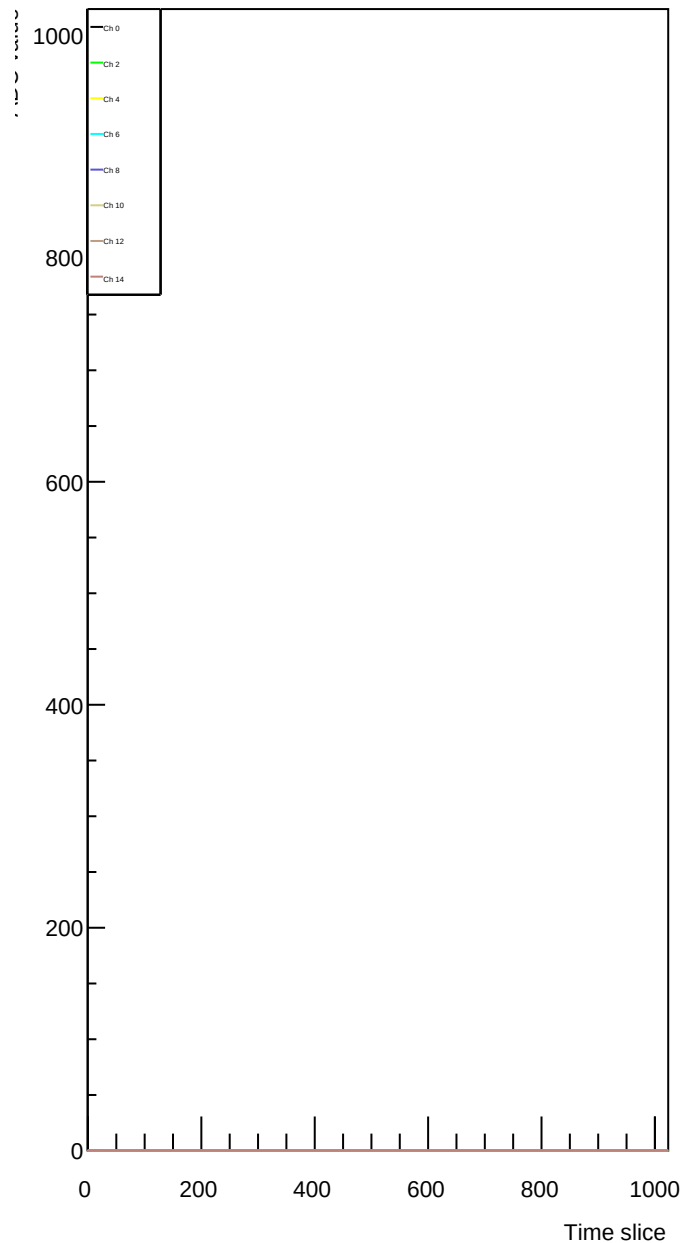
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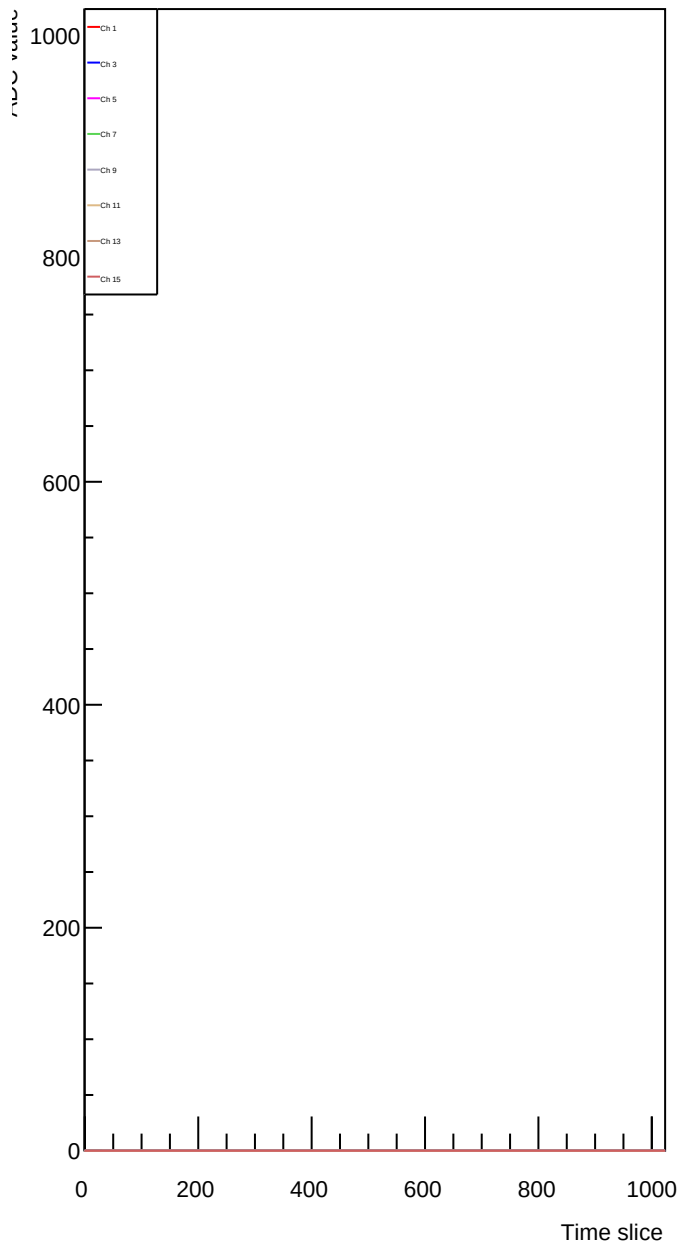
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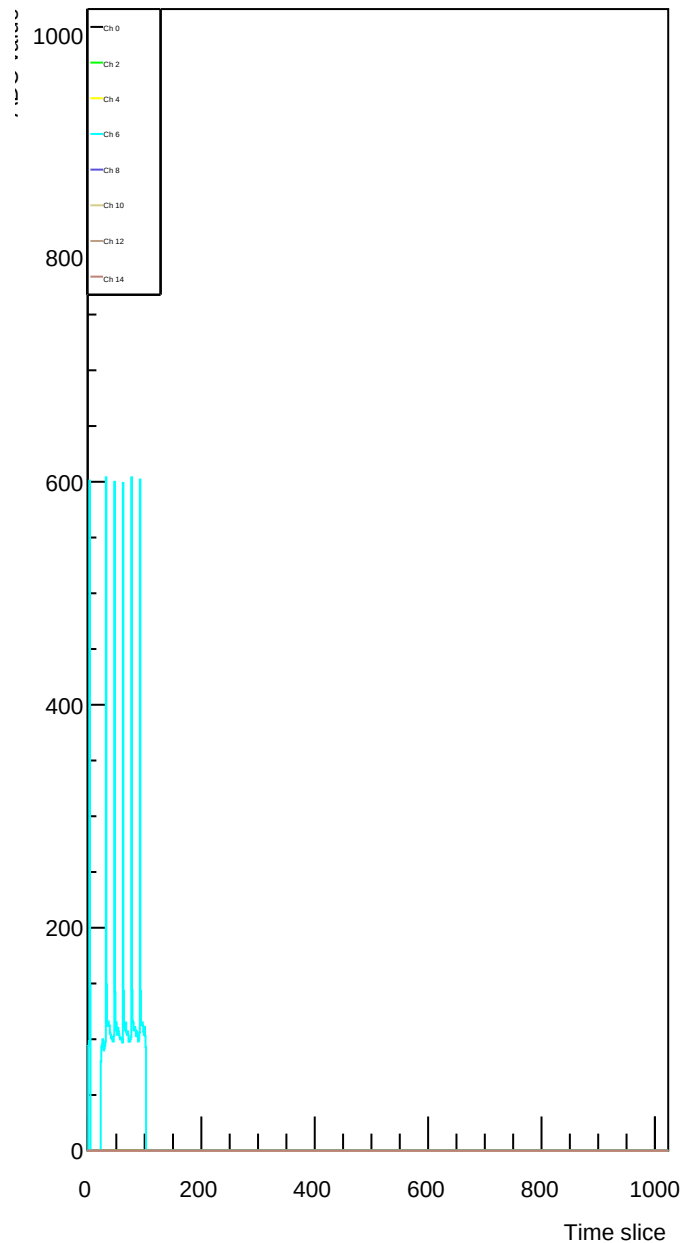
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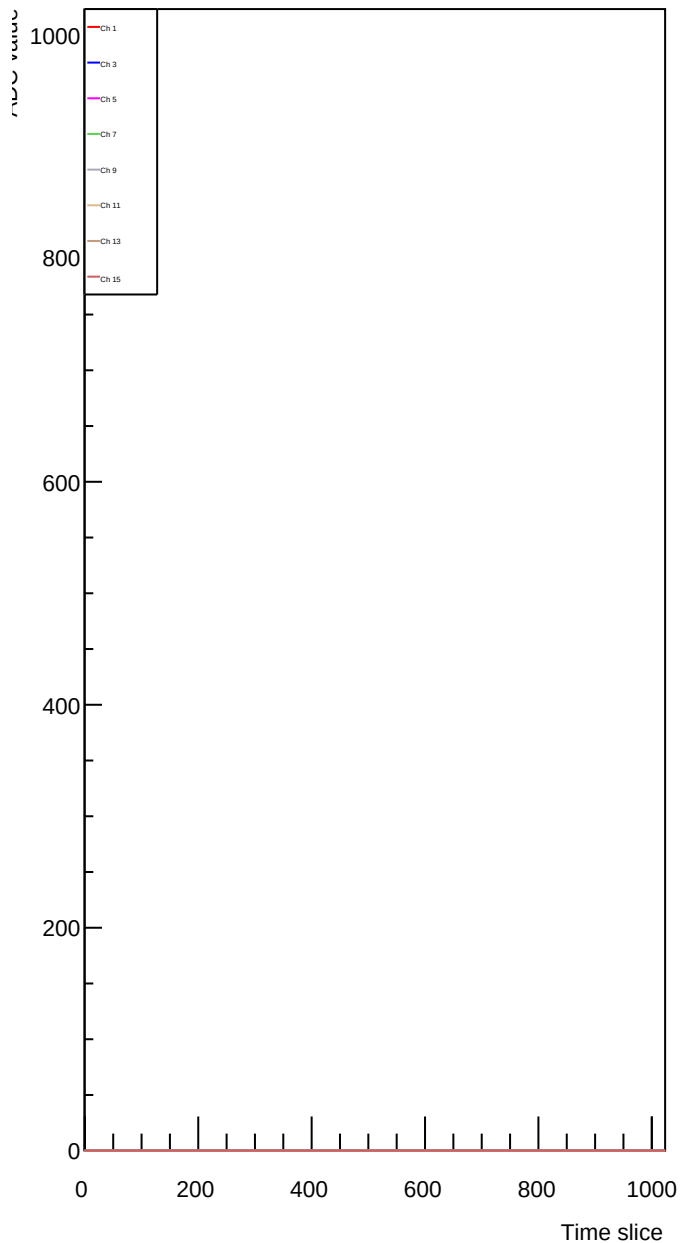
Run 0 event 5 mcm 0 chip 5 s3-clk2 odd ch



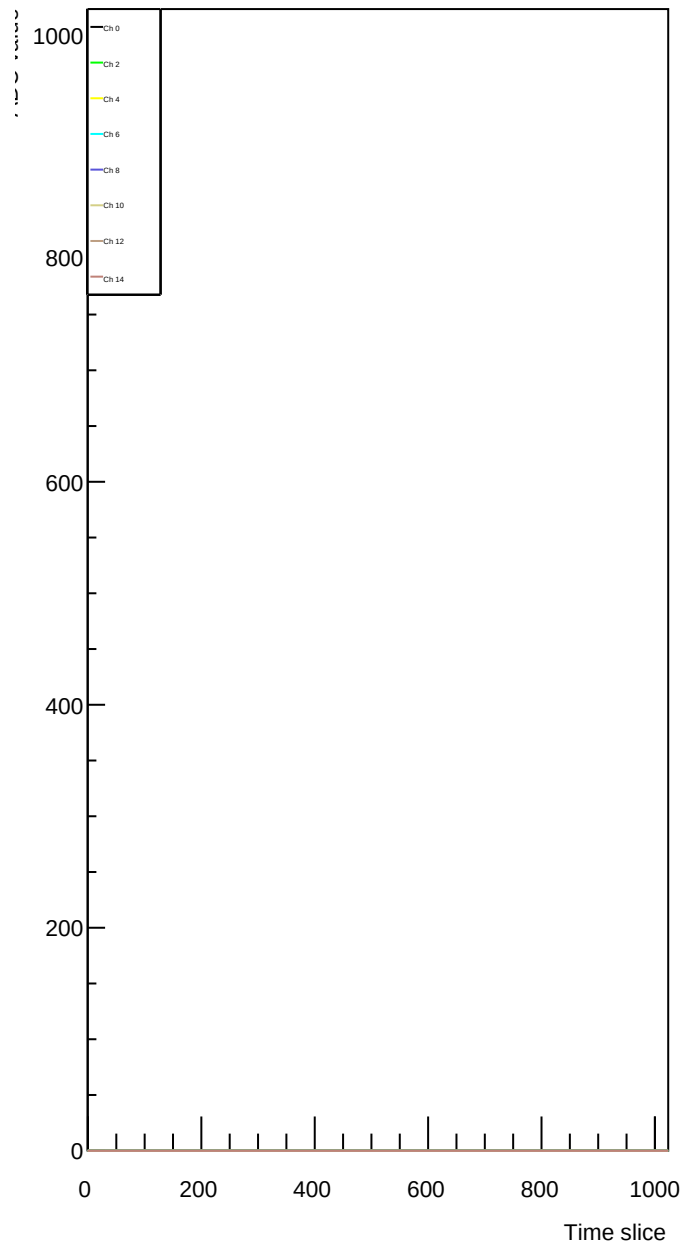
Run 0 event 5 mcm 0 chip 6 s3-clk2 even ch



Run 0 event 5 mcm 0 chip 6 s3-clk2 odd ch



Run 0 event 5 mcm 0 chip 7 s3-clk2 even ch



Run 0 event 5 mcm 0 chip 7 s3-clk2 odd ch

