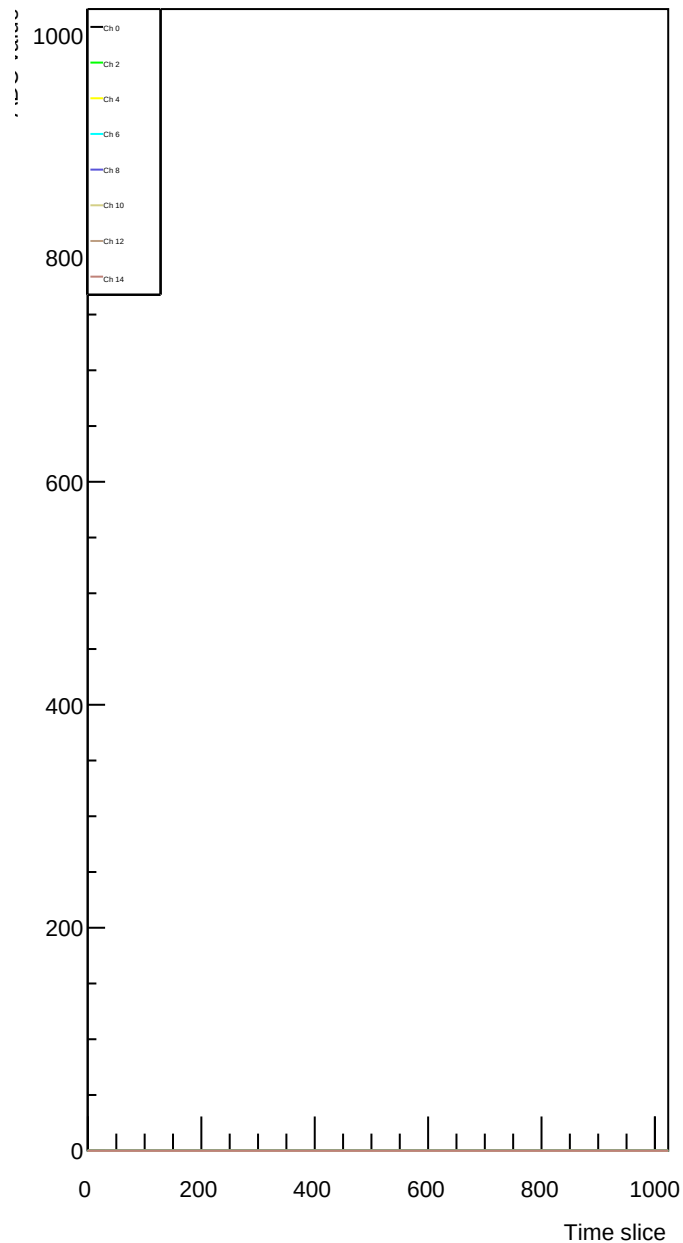
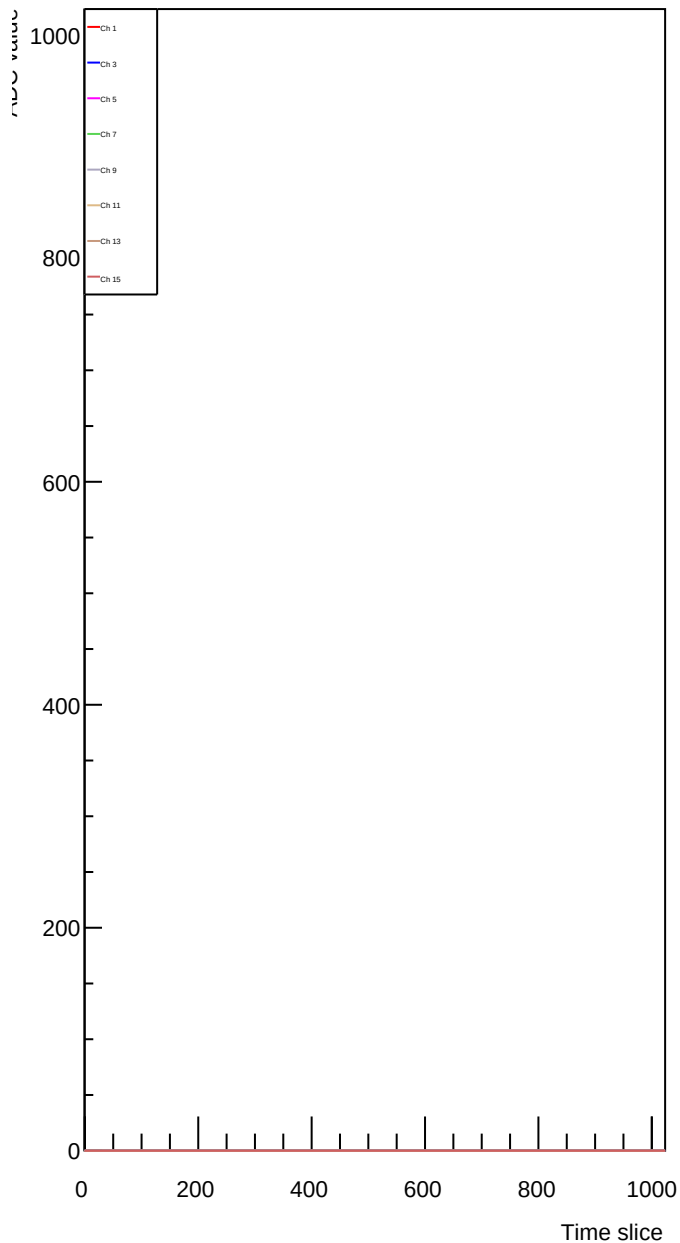


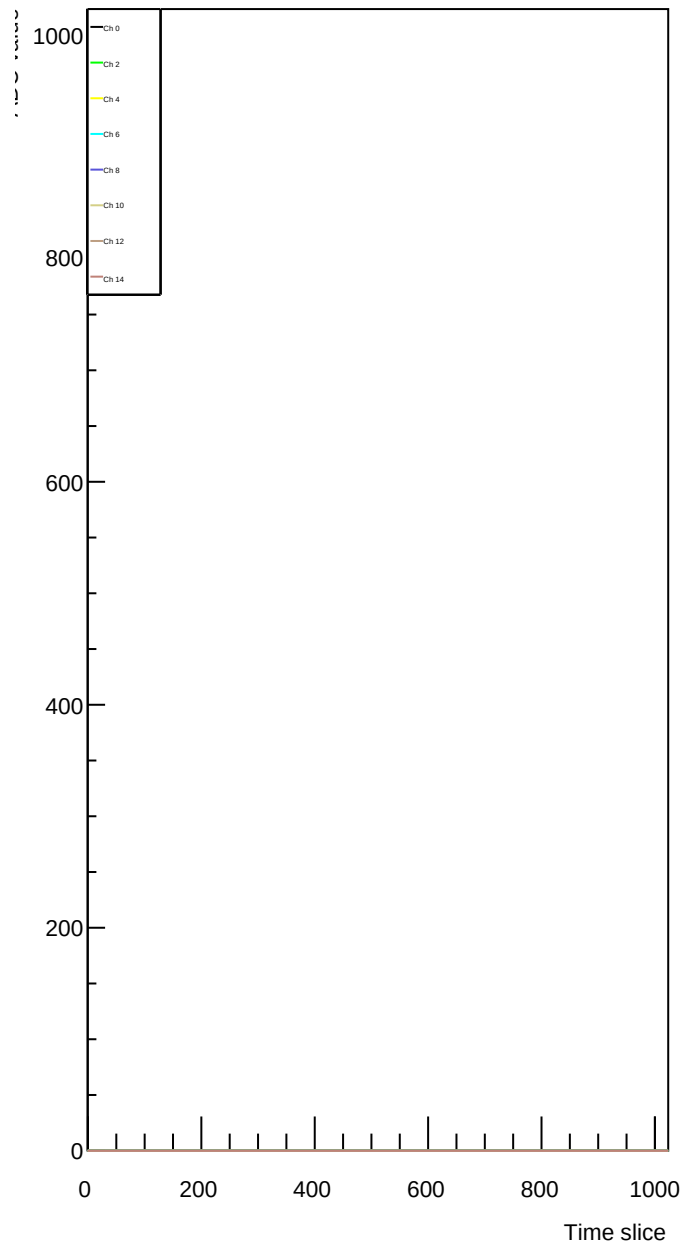
Run 0 event 7 mcm 0 chip 0 s2-clk2 even ch



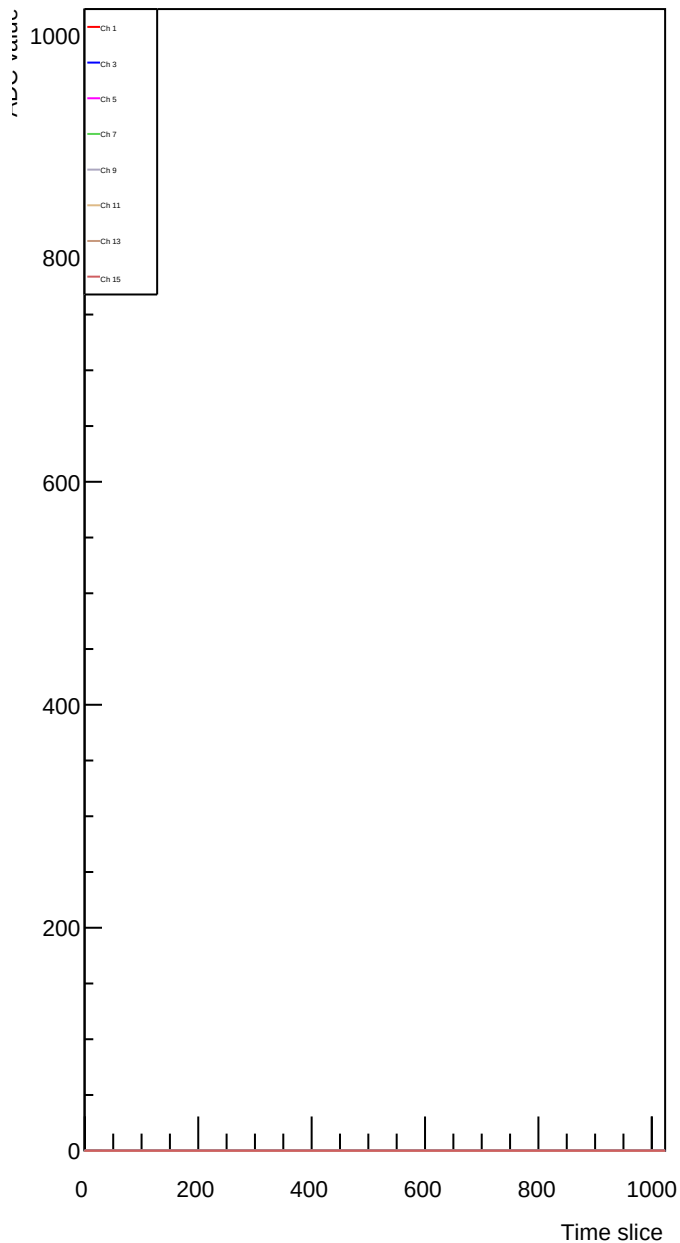
Run 0 event 7 mcm 0 chip 0 s2-clk2 odd ch



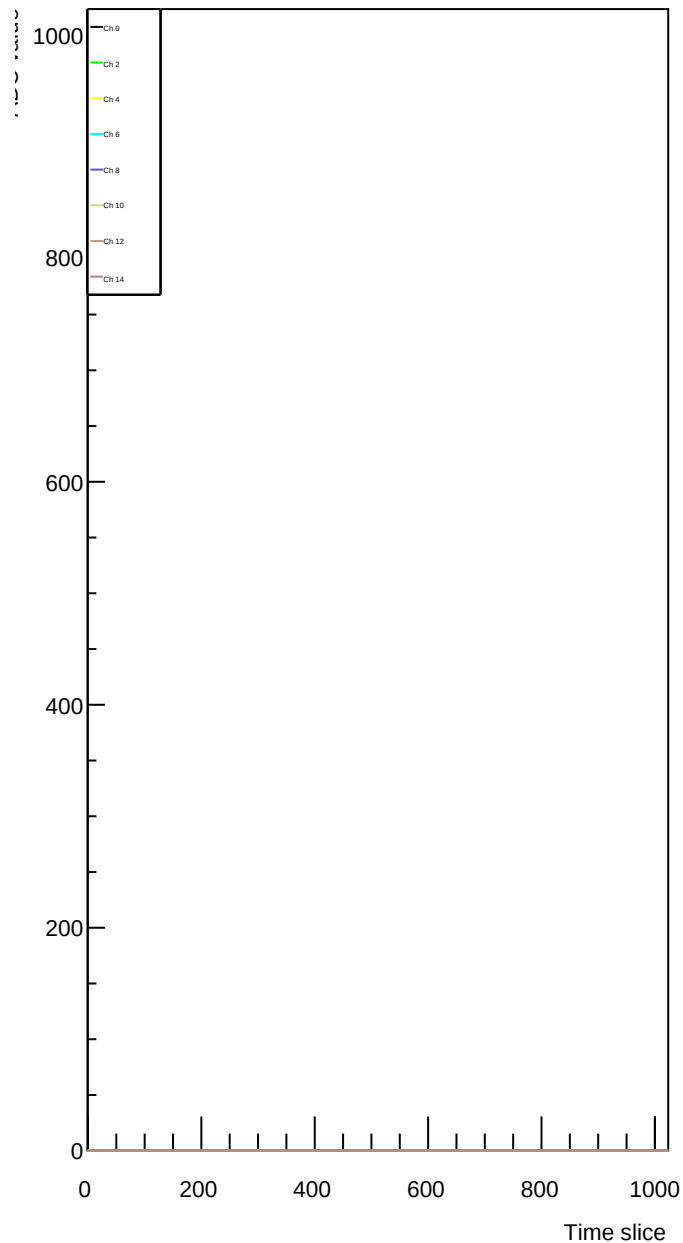
Run 0 event 7 mcm 0 chip 1 s2-clk2 even ch



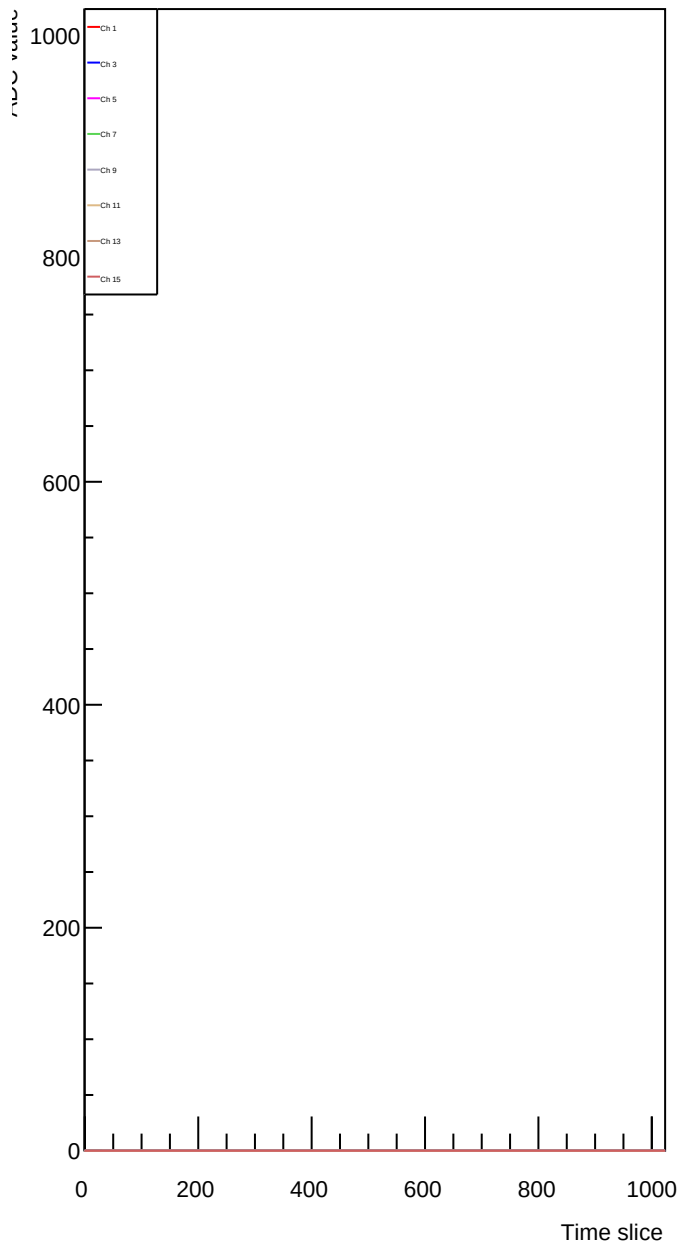
Run 0 event 7 mcm 0 chip 1 s2-clk2 odd ch



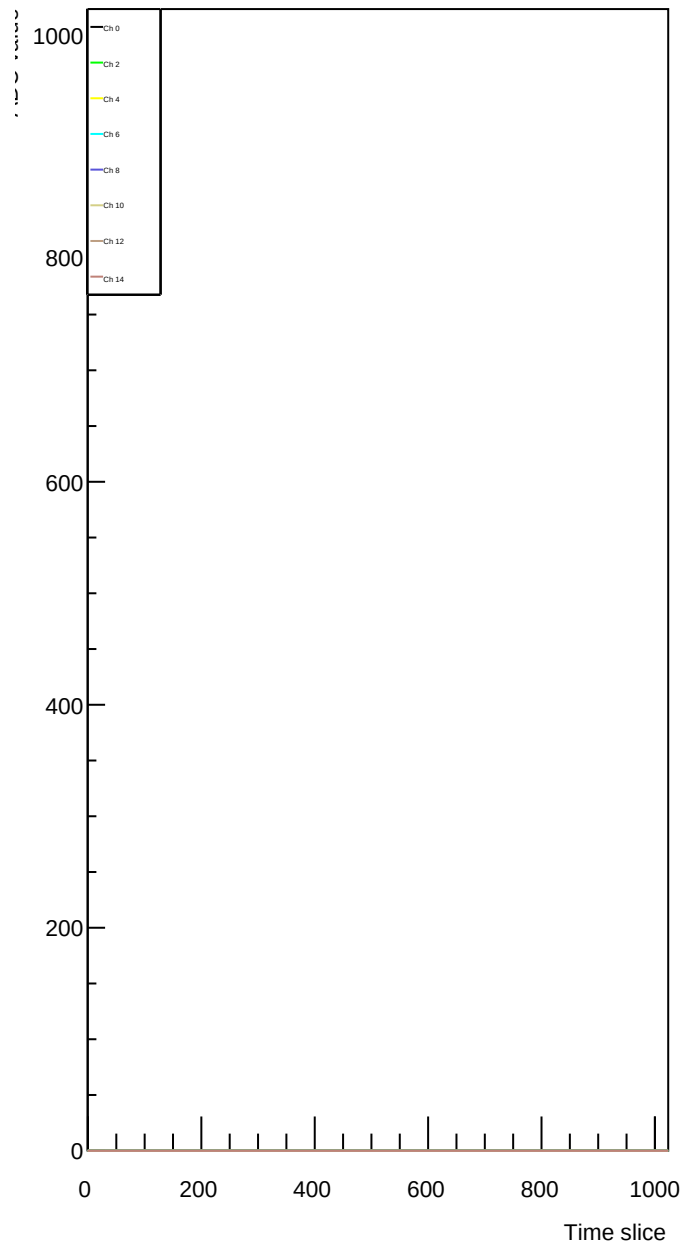
Run 0 event 7 mcm 0 chip 2 s2-clk2 even ch



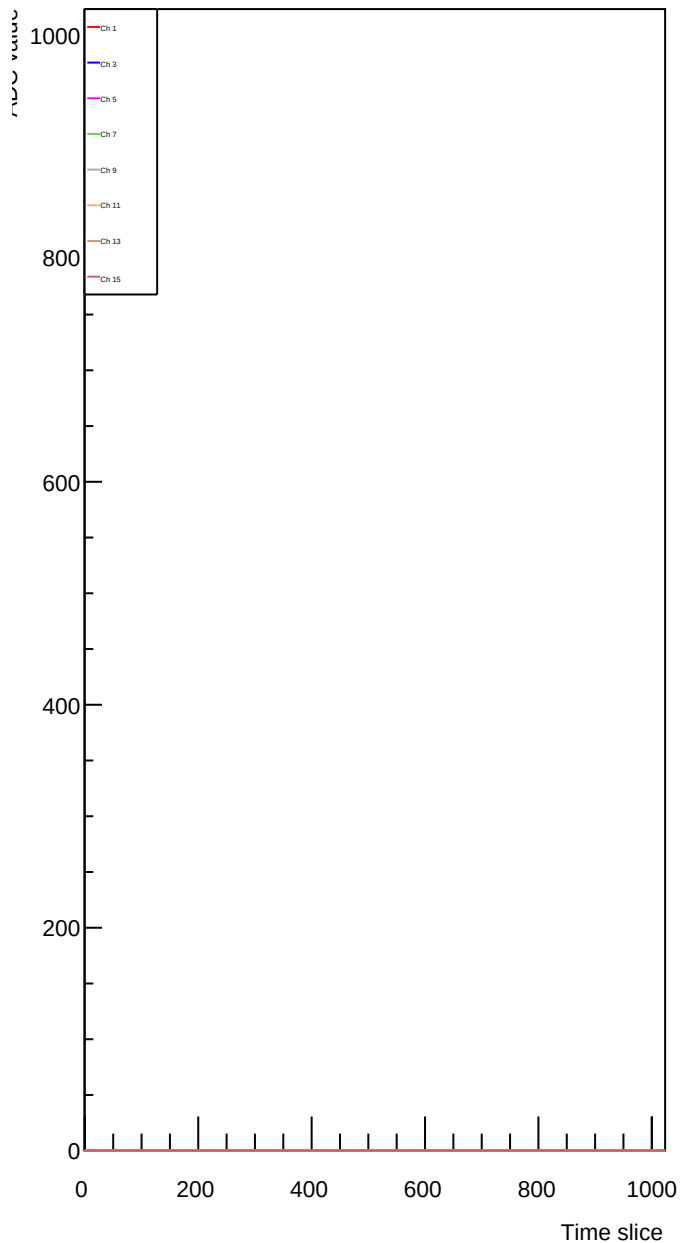
Run 0 event 7 mcm 0 chip 2 s2-clk2 odd ch



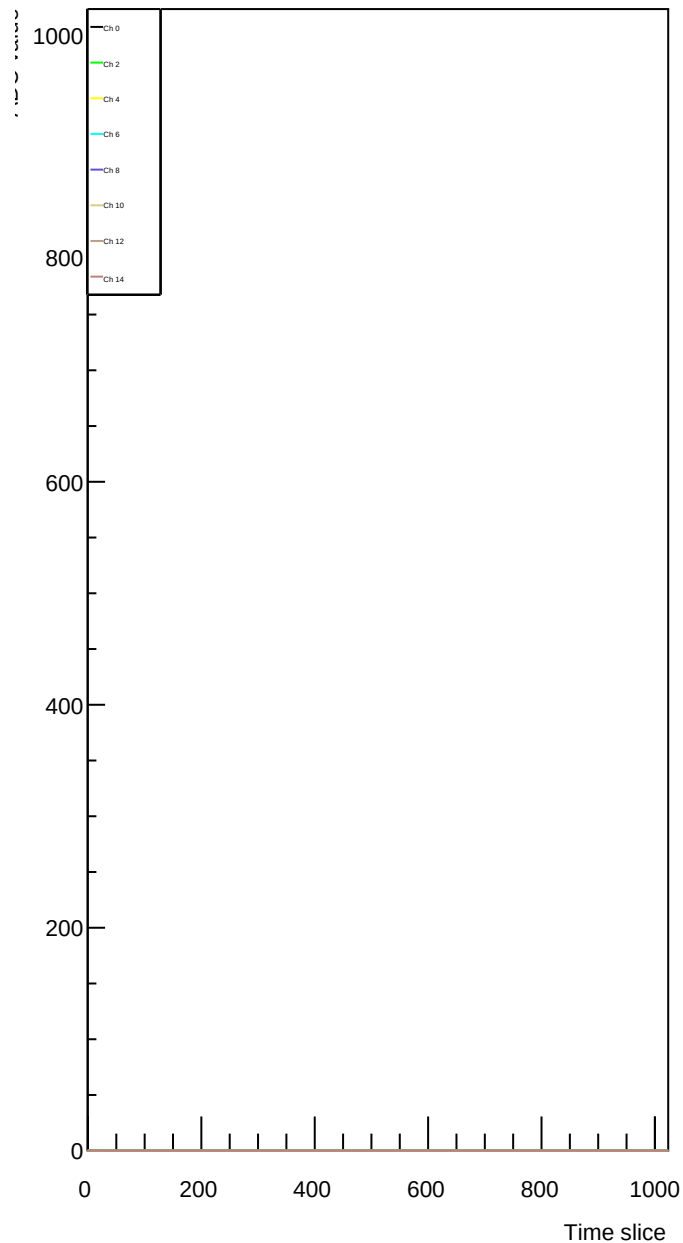
Run 0 event 7 mcm 0 chip 3 s2-clk2 even ch



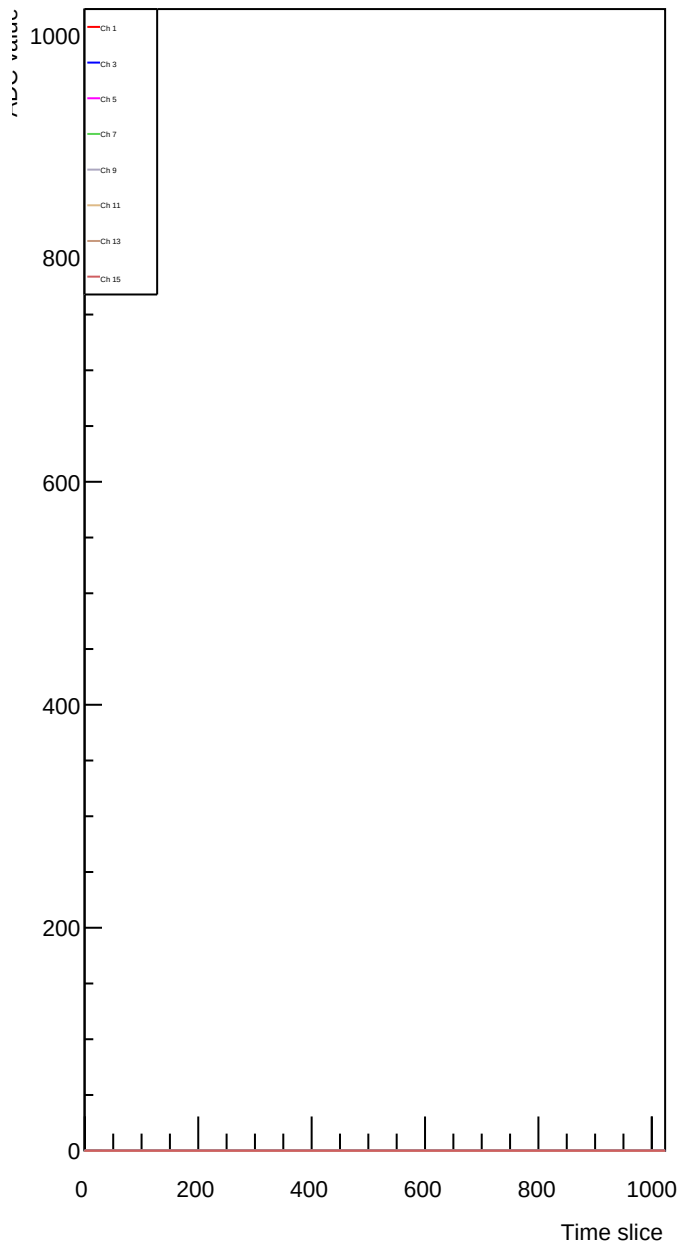
Run 0 event 7 mcm 0 chip 3 s2-clk2 odd ch



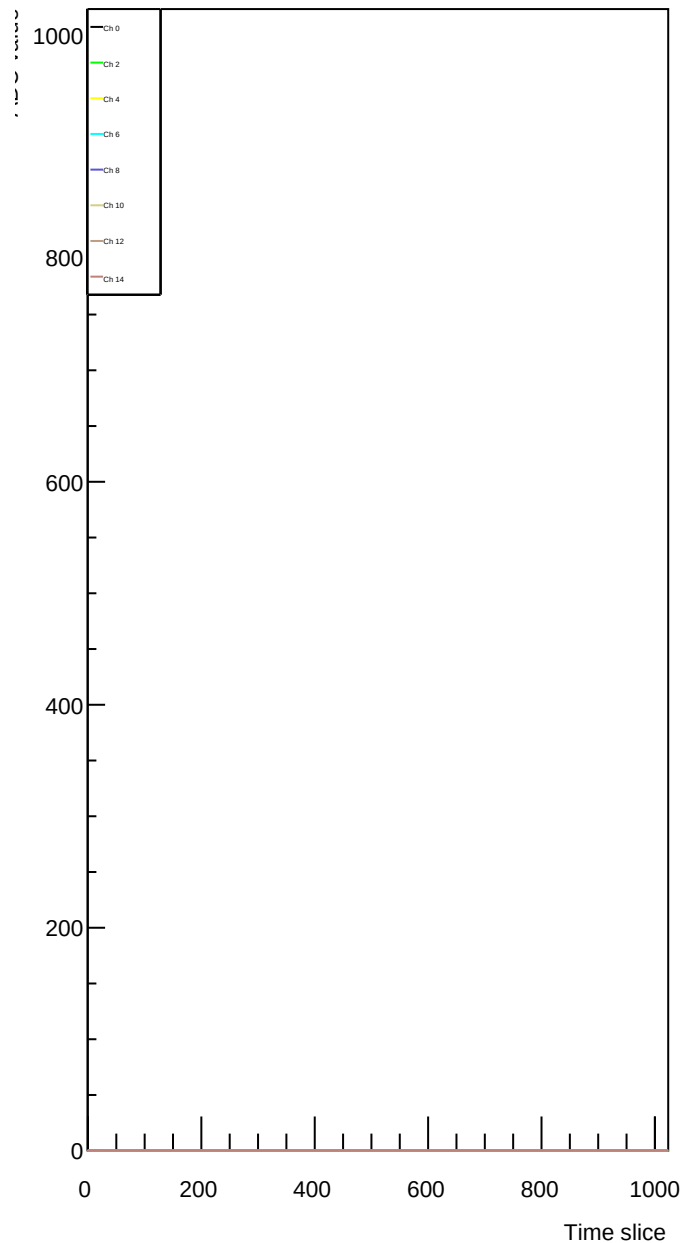
Run 0 event 7 mcm 0 chip 4 s2-clk2 even ch



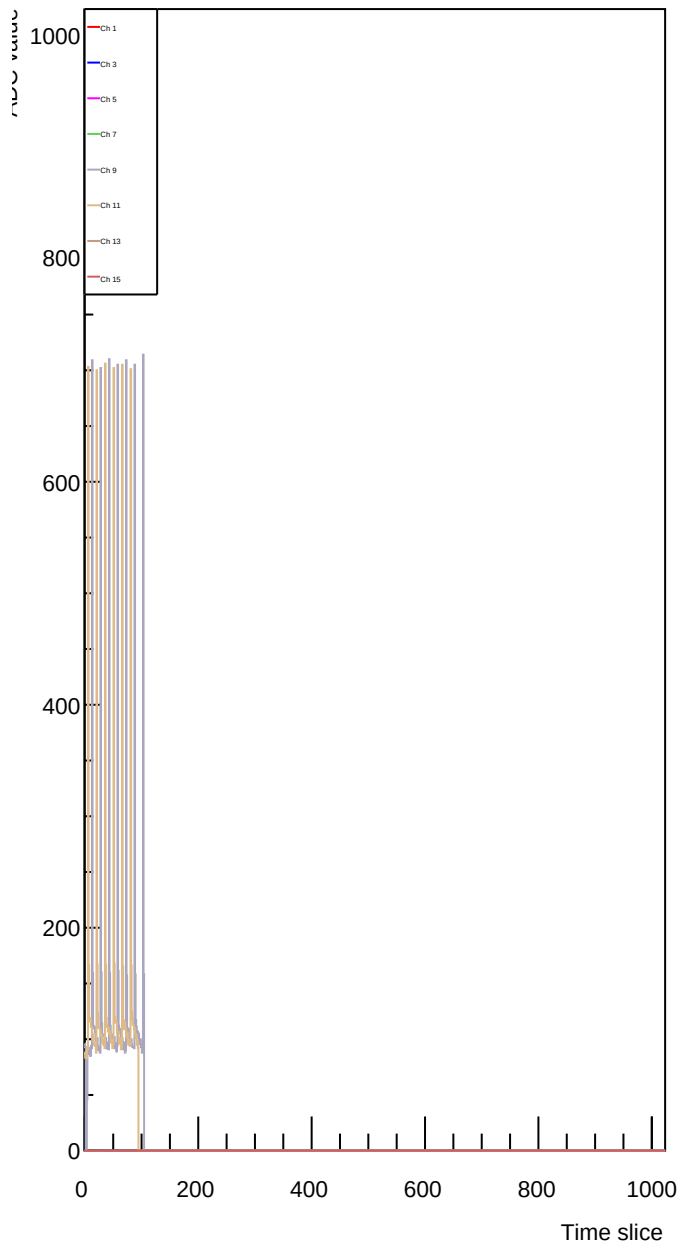
Run 0 event 7 mcm 0 chip 4 s2-clk2 odd ch



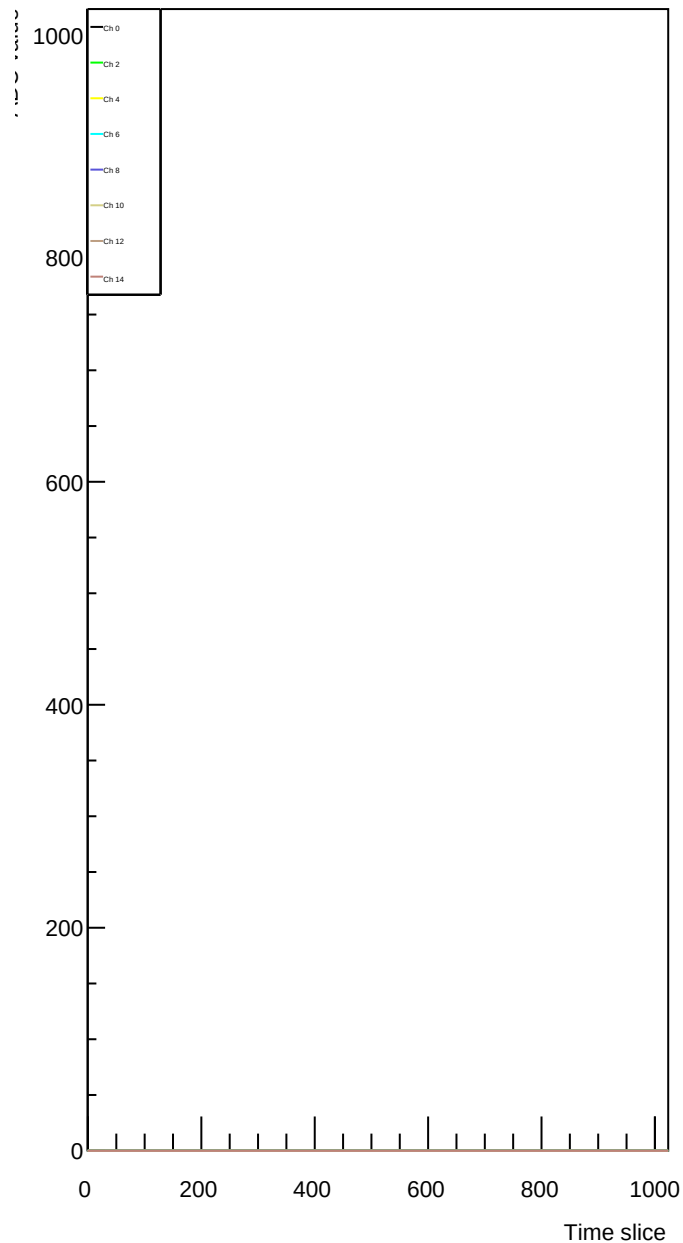
Run 0 event 7 mcm 0 chip 5 s2-clk2 even ch



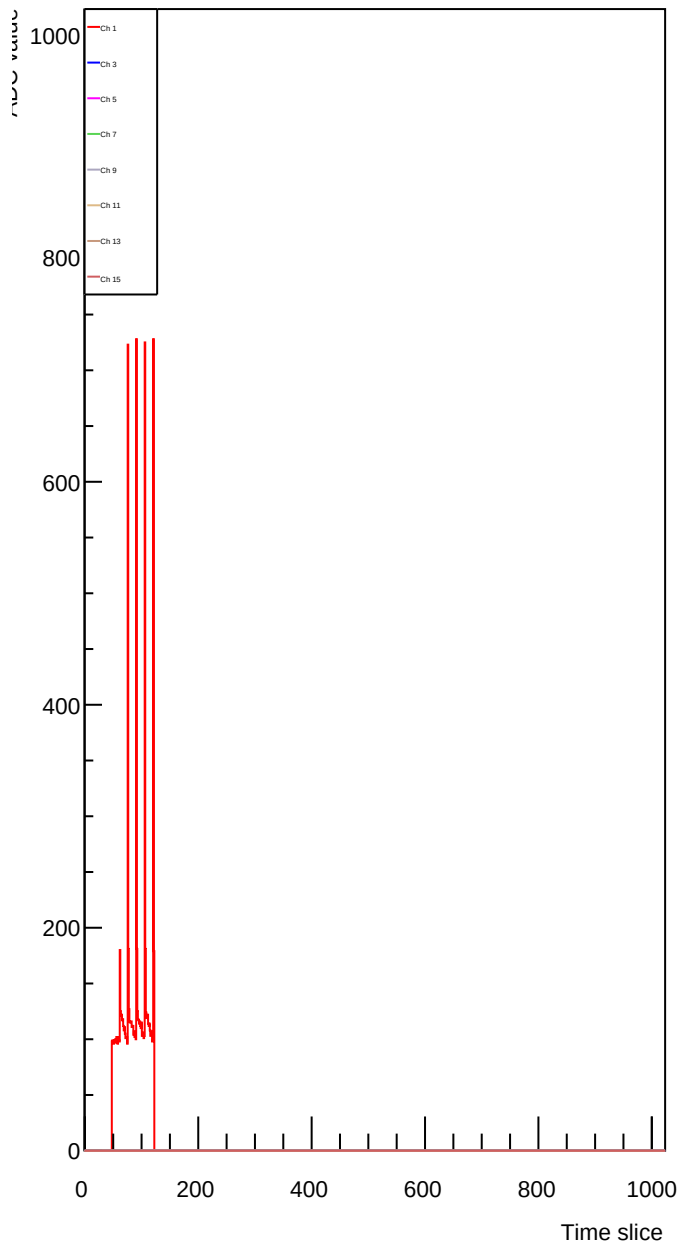
Run 0 event 7 mcm 0 chip 5 s2-clk2 odd ch



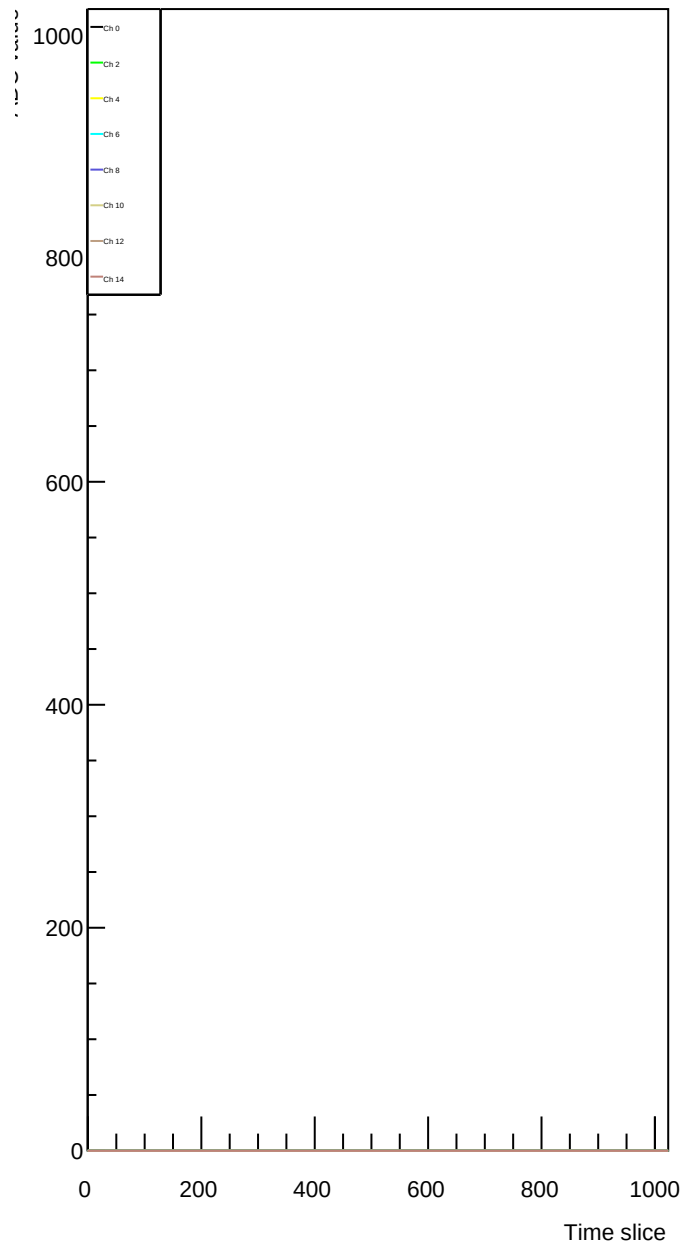
Run 0 event 7 mcm 0 chip 6 s2-clk2 even ch



Run 0 event 7 mcm 0 chip 6 s2-clk2 odd ch



Run 0 event 7 mcm 0 chip 7 s2-clk2 even ch



Run 0 event 7 mcm 0 chip 7 s2-clk2 odd ch

