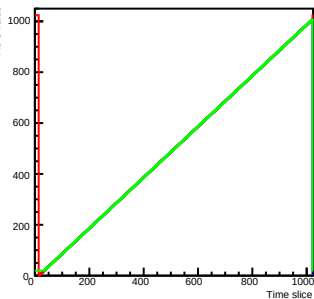
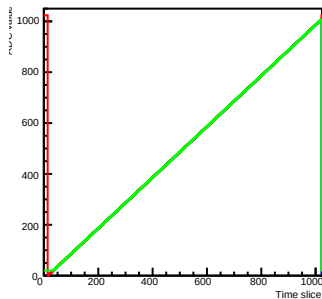


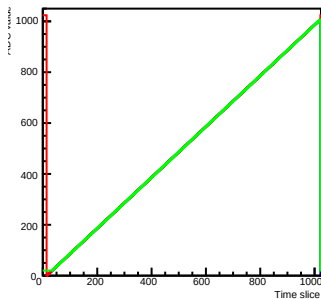
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dcl 0 chip 0 chan 0 test
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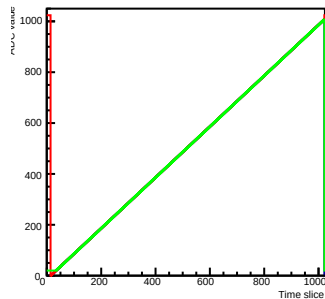
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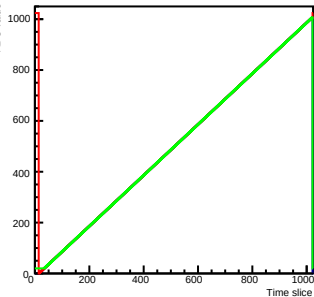
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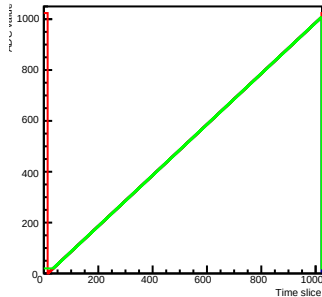
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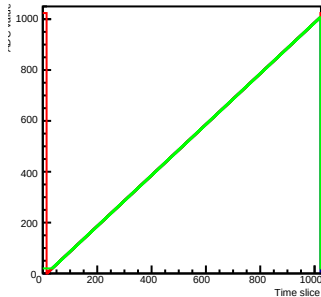
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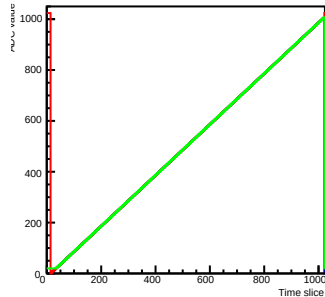
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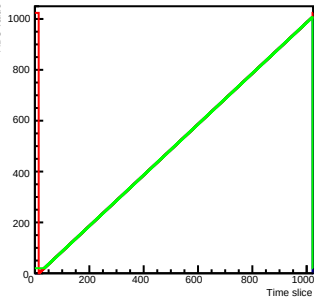
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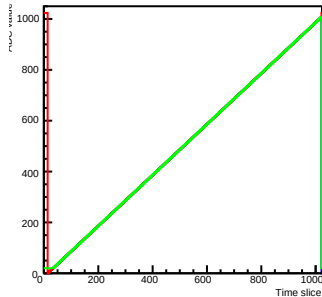
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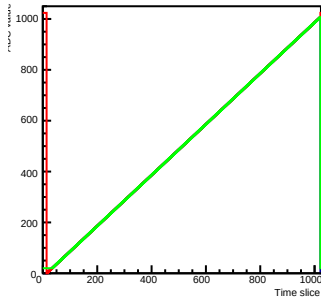
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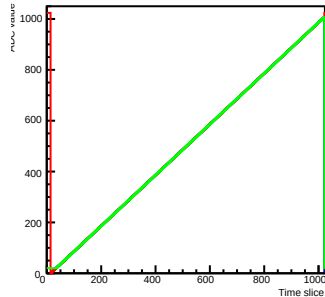
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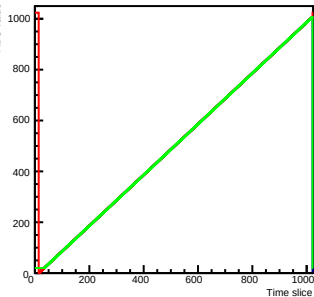
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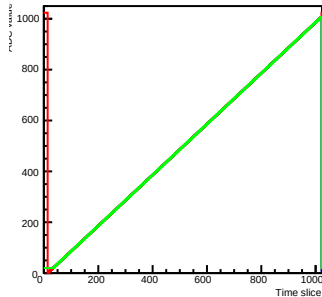
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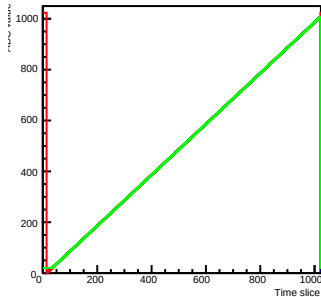
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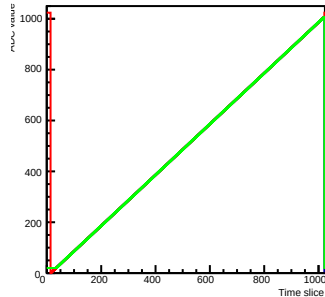
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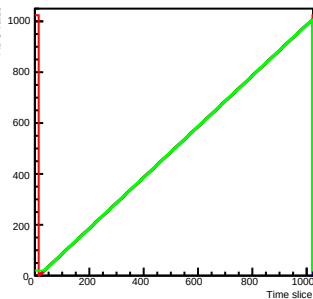
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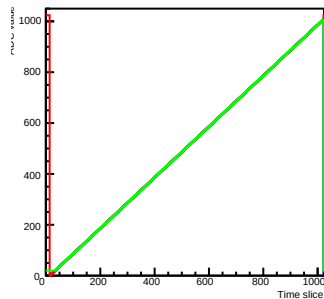
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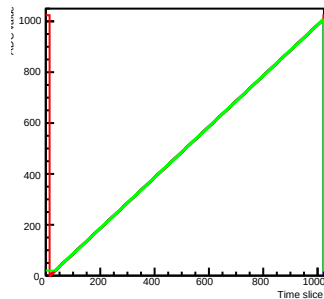
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dcl 0 chip 1 chan 0 test
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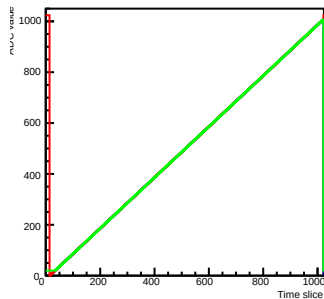
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dcl 0 chip 1 chan 1 test
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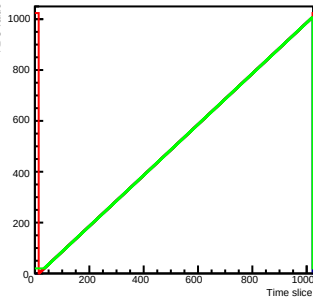
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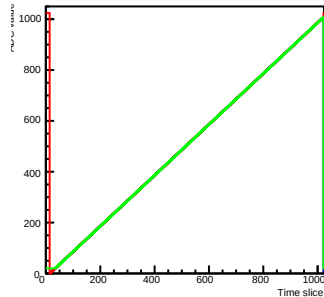
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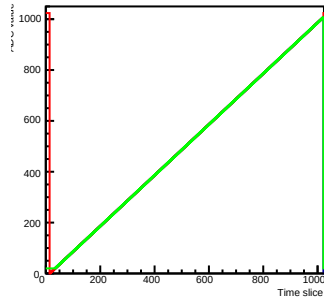
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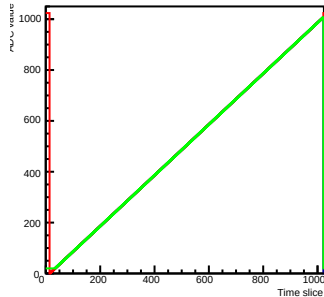
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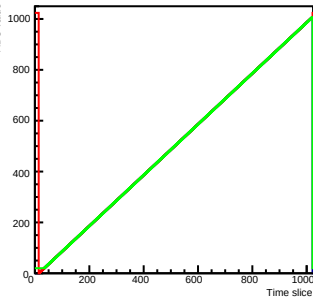
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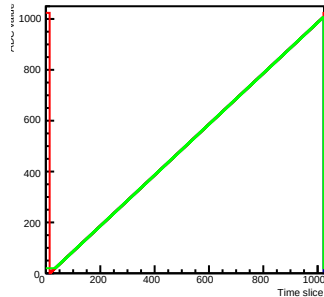
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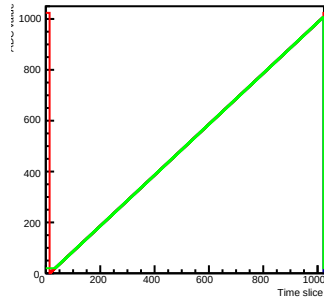
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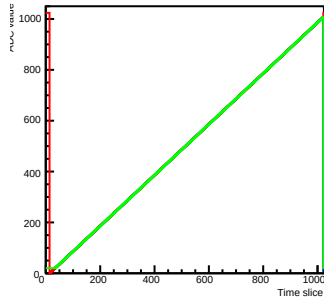
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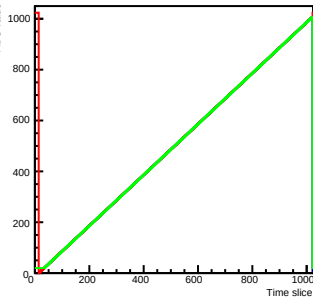
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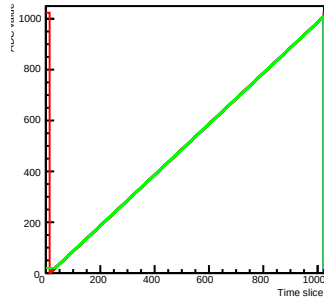
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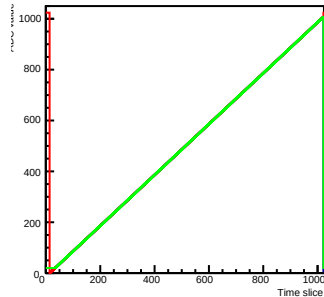
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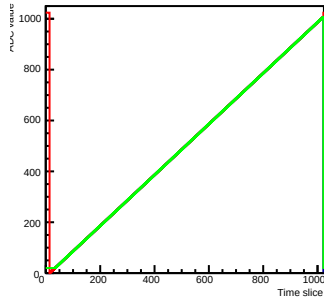
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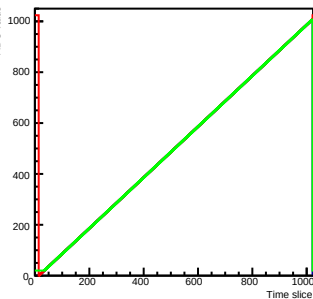
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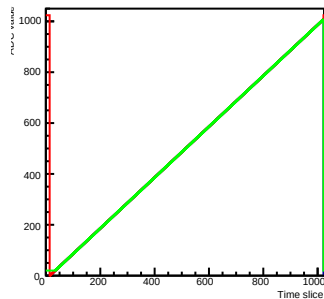
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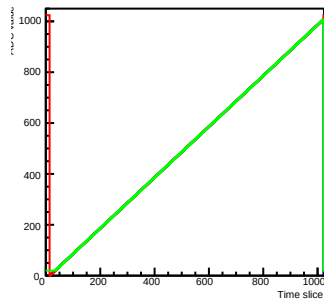
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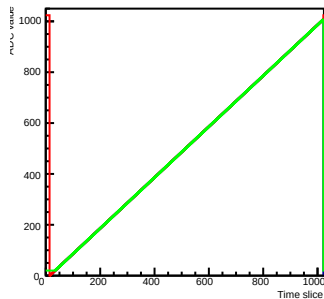
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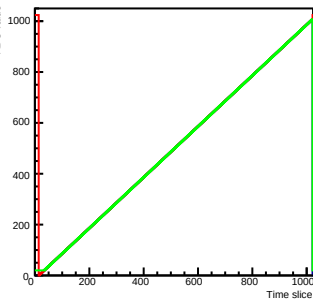
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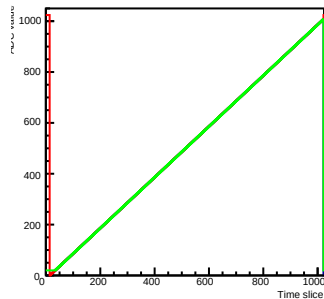
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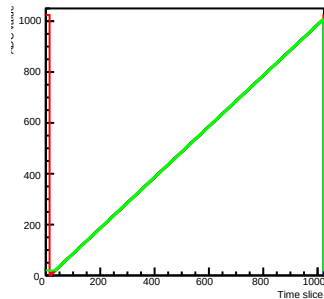
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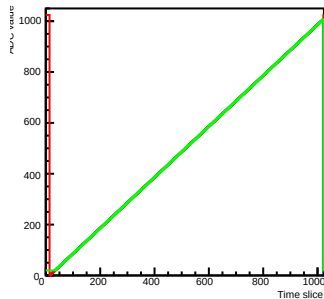
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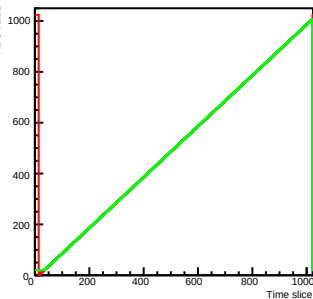
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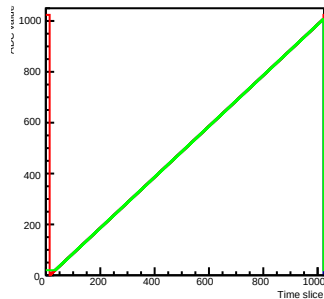
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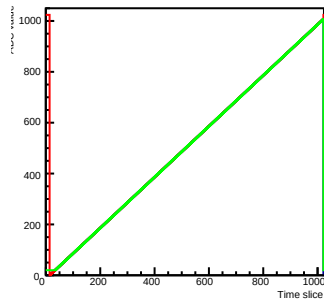
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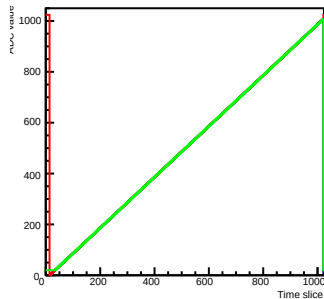
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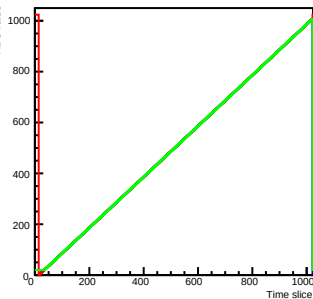
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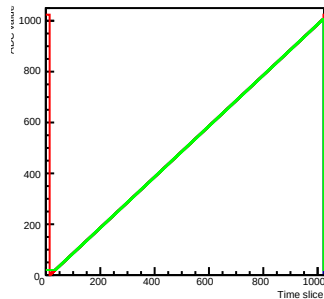
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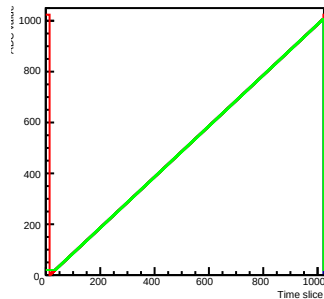
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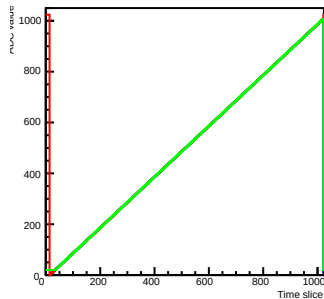
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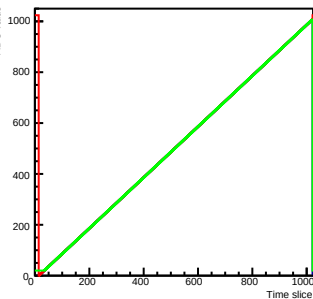
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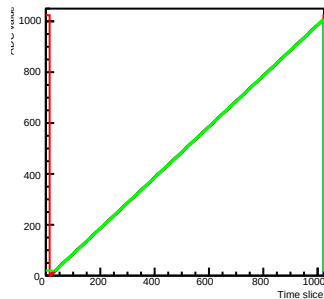
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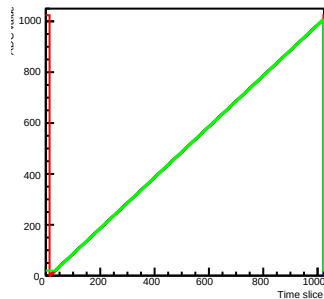
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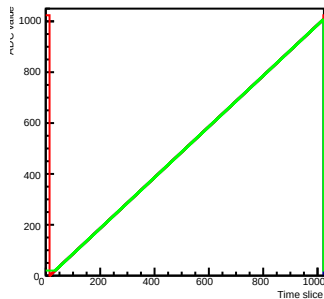
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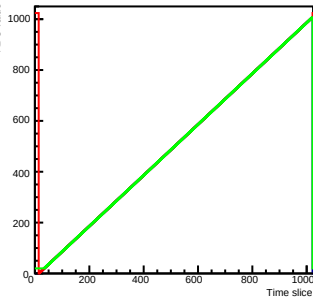
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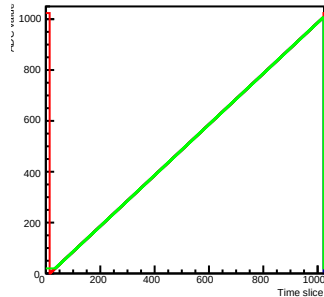
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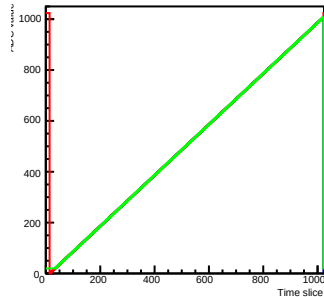
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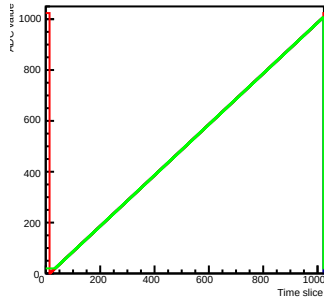
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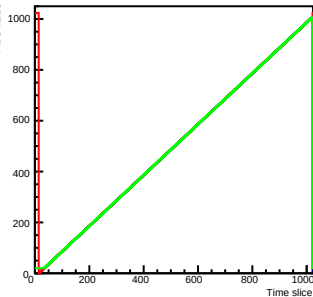
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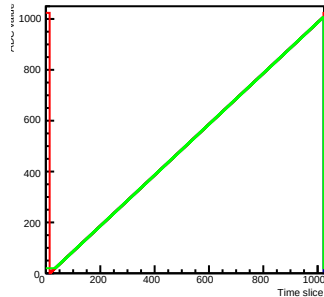
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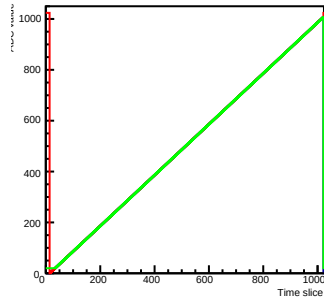
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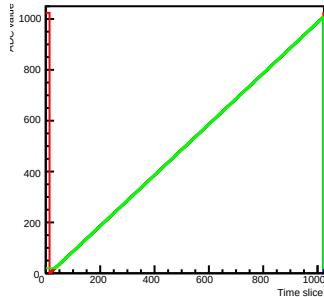
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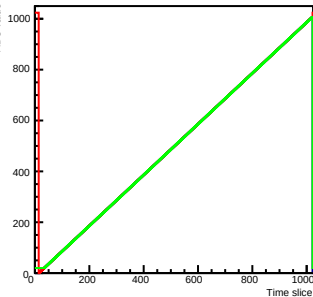
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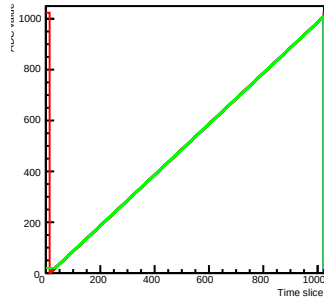
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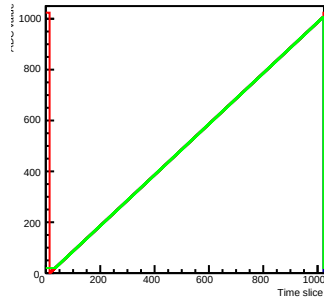
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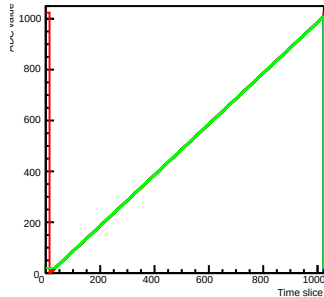
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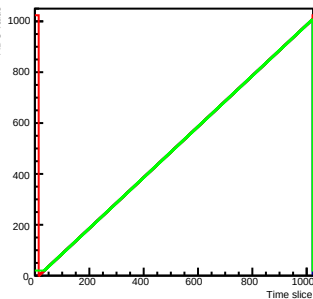
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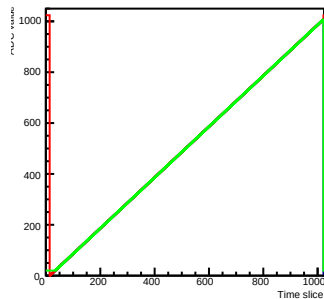
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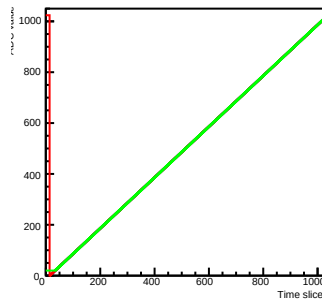
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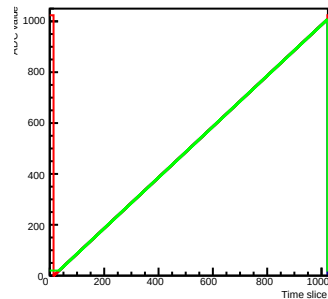
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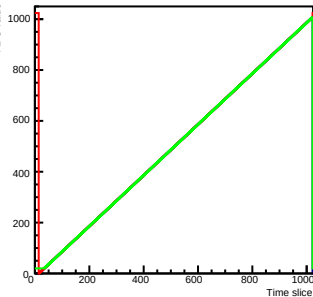
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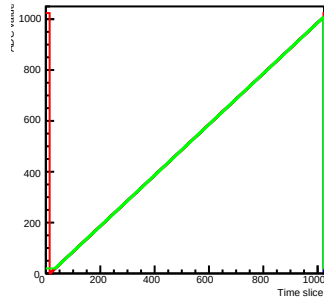
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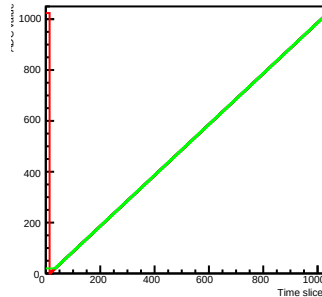
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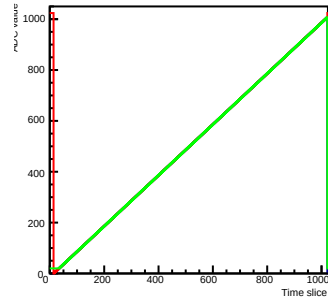
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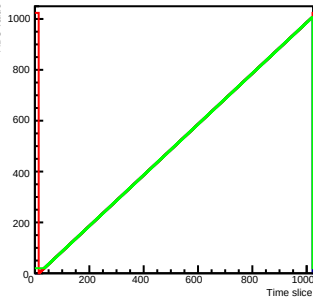
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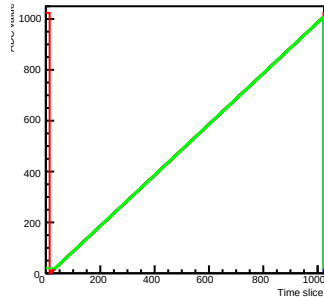
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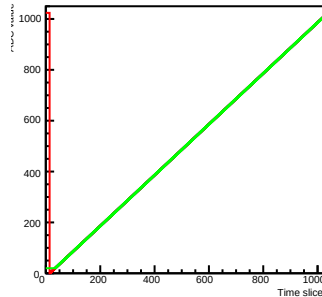
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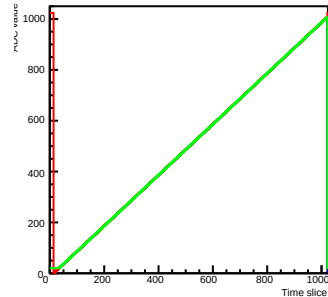
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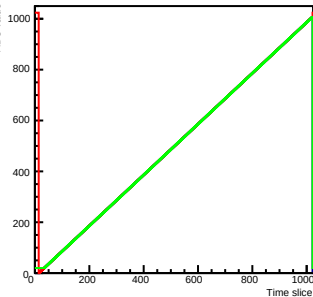
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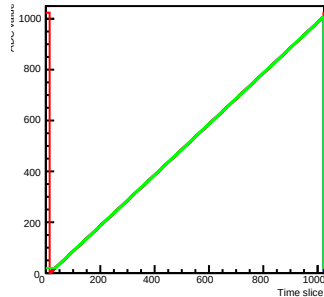
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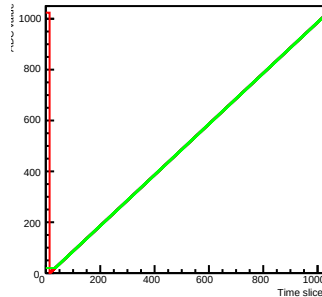
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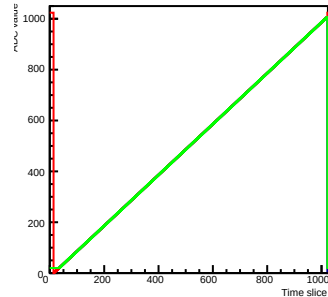
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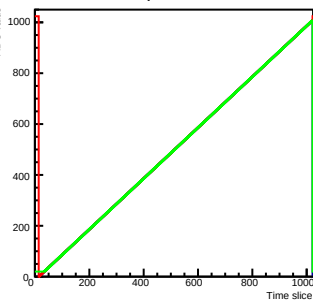
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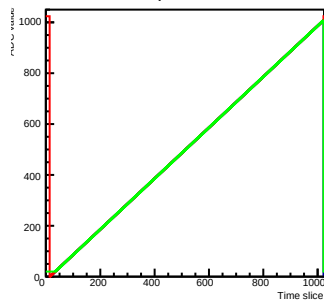
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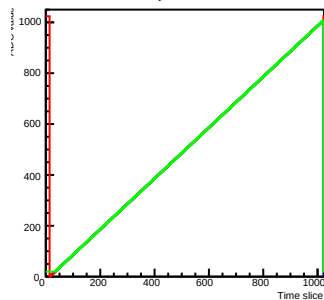
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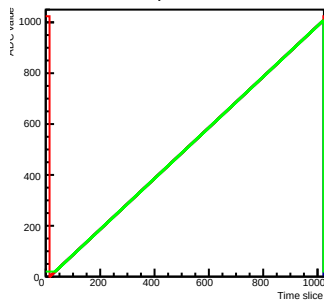
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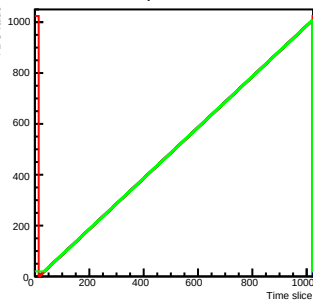
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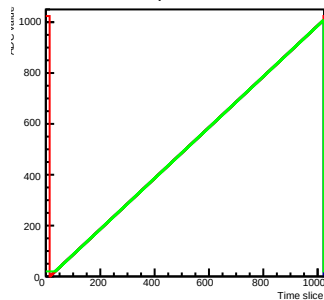
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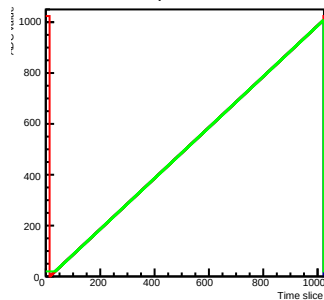
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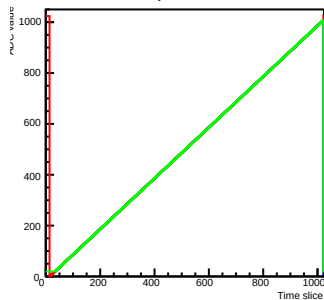
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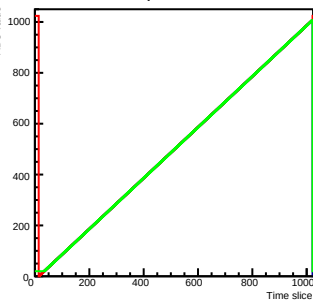
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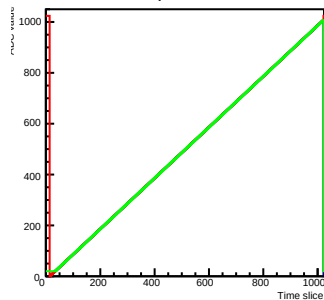
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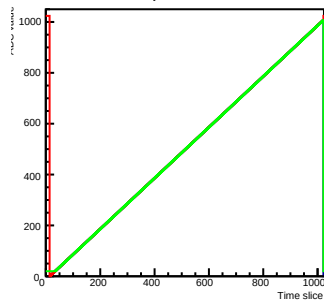
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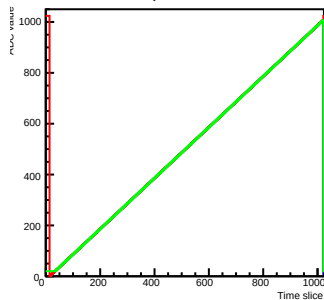
dcl 0 chip 5 chan 9 test



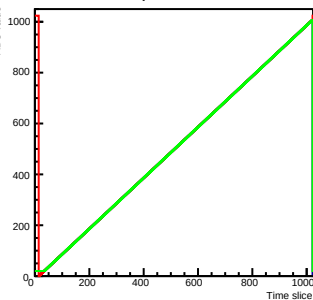
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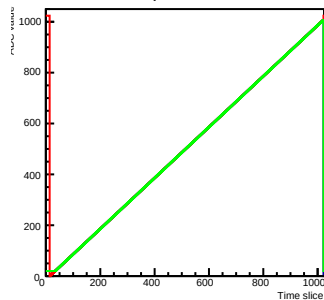
dcl 0 chip 5 chan 11 test



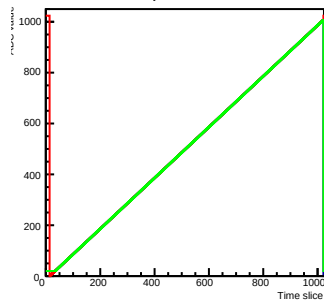
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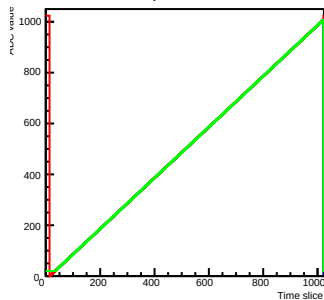
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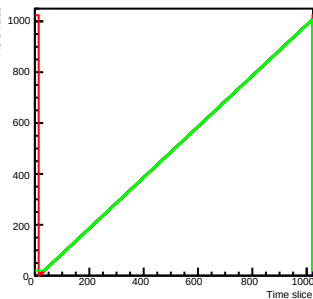
dcl 0 chip 5 chan 14 test



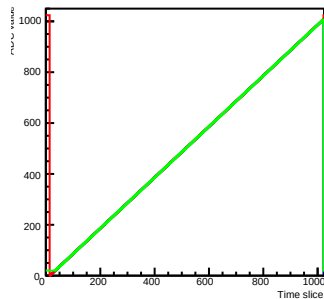
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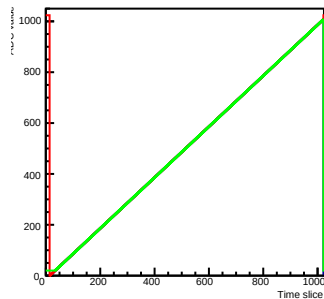
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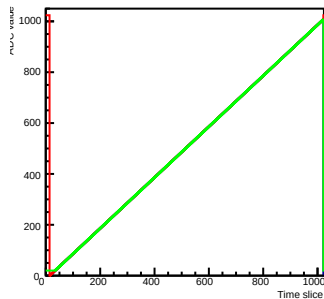
dcl 0 chip 6 chan 1 test



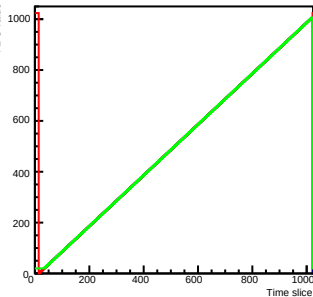
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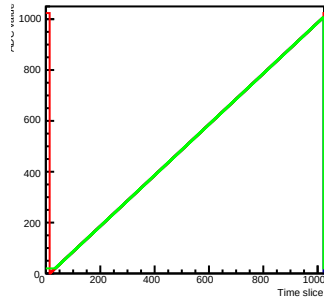
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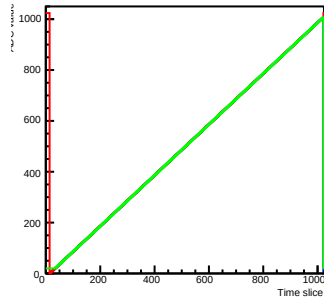
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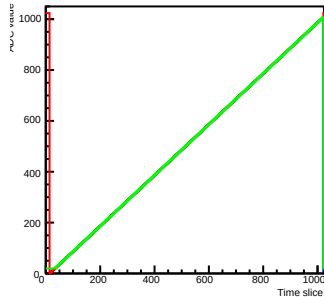
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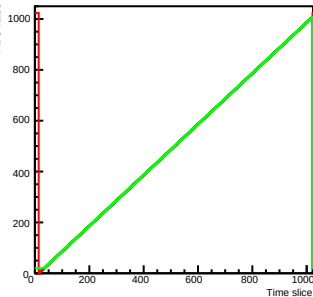
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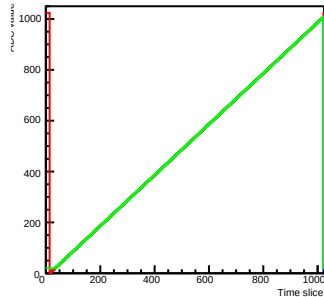
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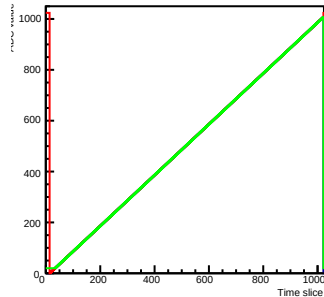
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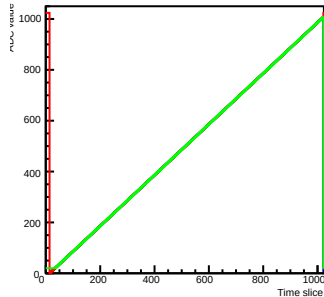
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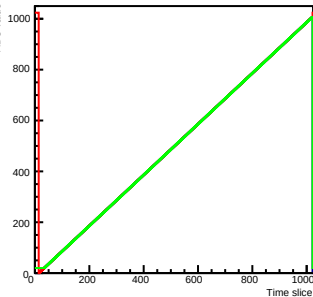
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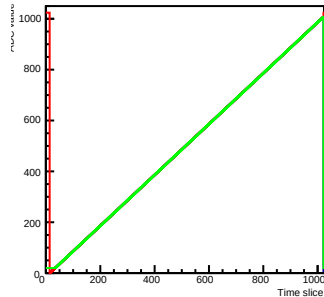
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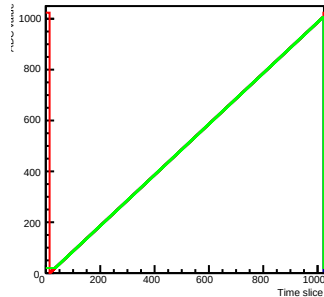
dcl 0 chip 6 chan 12 test



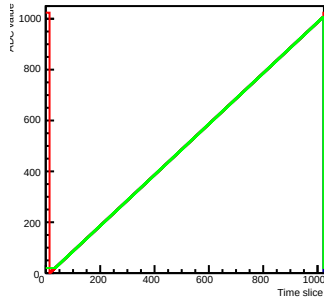
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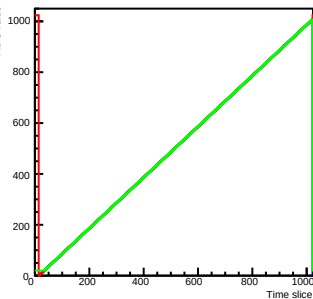
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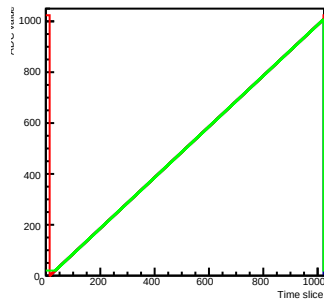
dcl 0 chip 6 chan 15 test



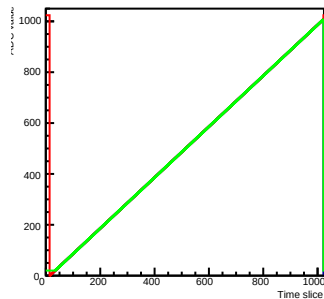
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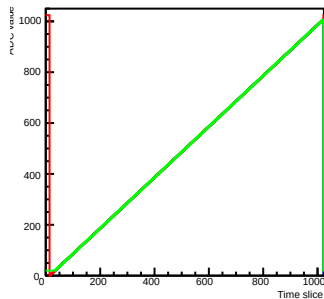
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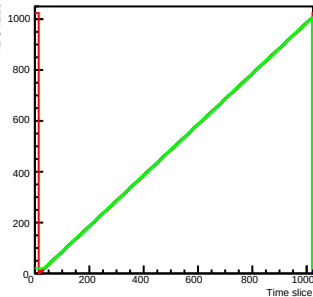
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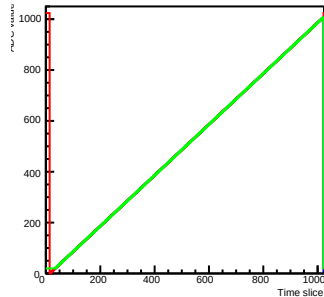
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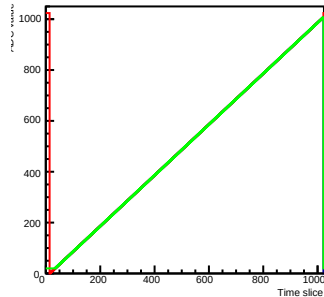
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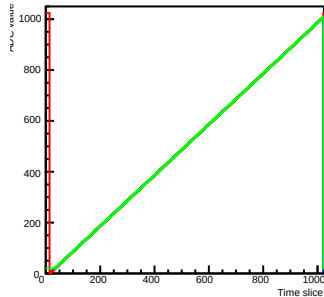
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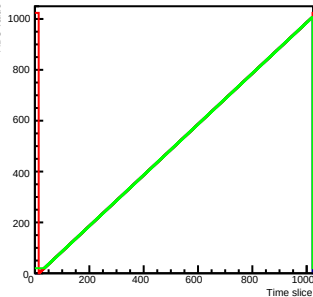
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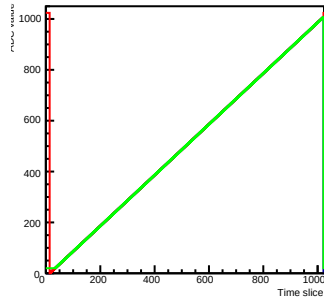
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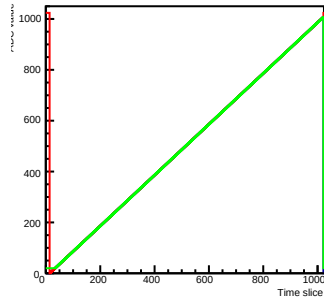
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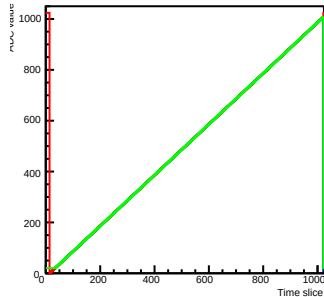
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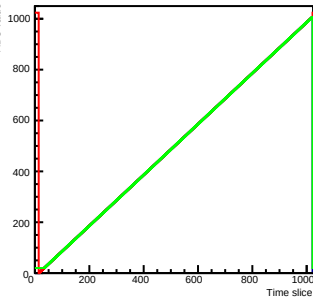
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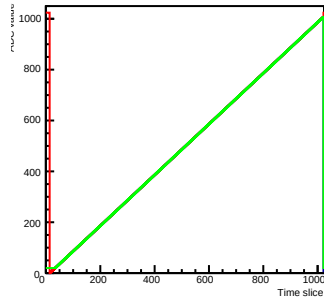
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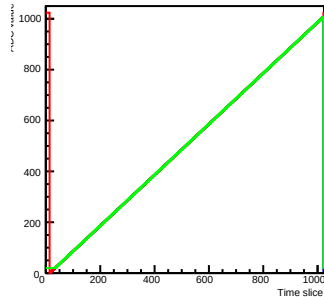
dcl 0 chip 7 chan 12 test



dcl 0 chip 7 chan 13 test



dcl 0 chip 7 chan 14 test



dcl 0 chip 7 chan 15 test

