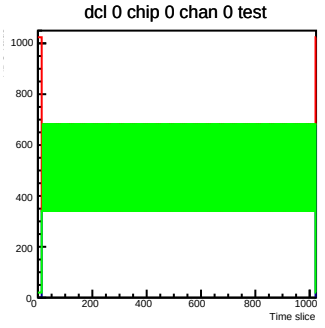
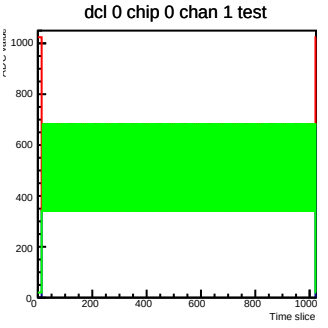
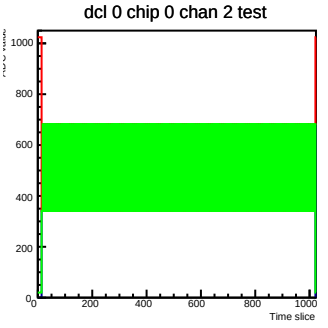
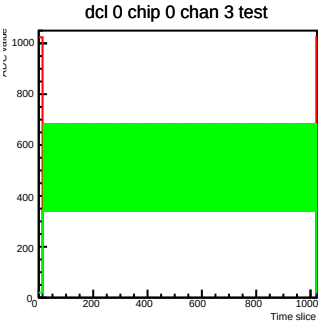
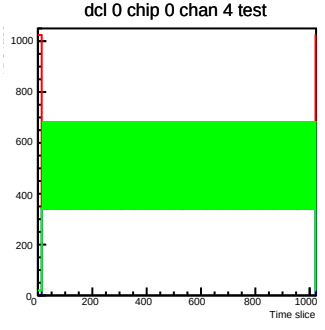
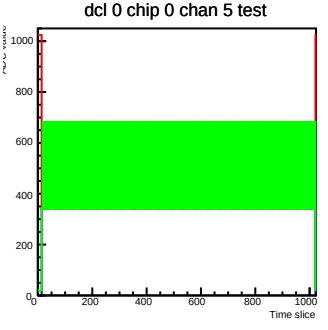

dcl 0 chip 0 chan 0 test
Time slice

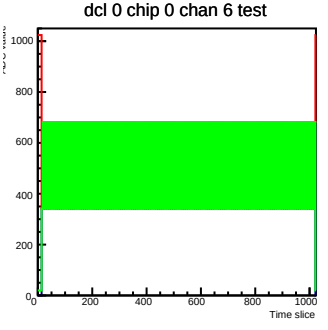

dcl 0 chip 0 chan 1 test
Time slice

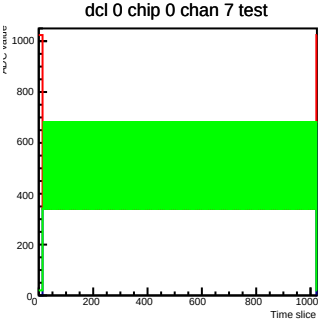

dcl 0 chip 0 chan 2 test
Time slice

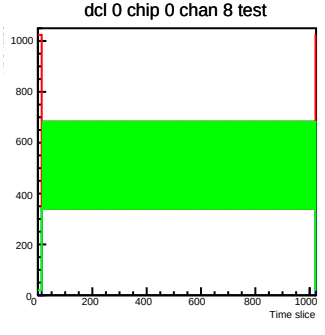

dcl 0 chip 0 chan 3 test
Time slice

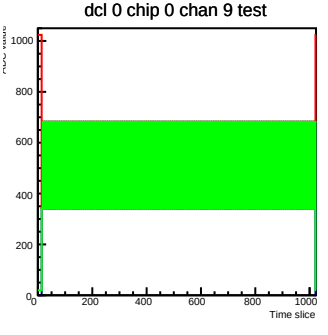

dcl 0 chip 0 chan 4 test
Time slice

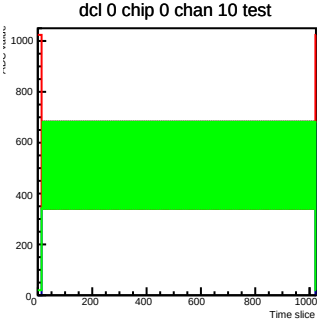

dcl 0 chip 0 chan 5 test
Time slice

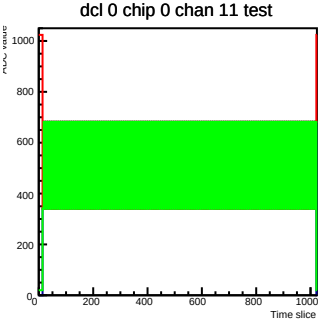

dcl 0 chip 0 chan 6 test
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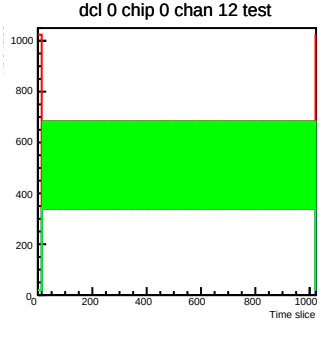

dcl 0 chip 0 chan 7 test
Time slice

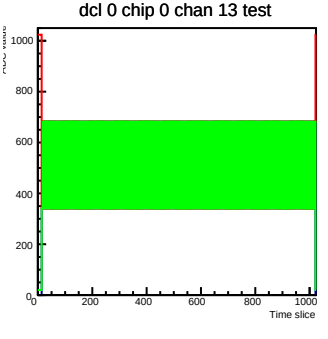

dcl 0 chip 0 chan 8 test
Time slice

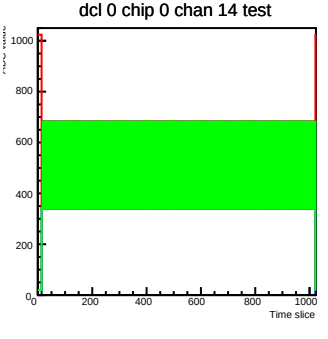

dcl 0 chip 0 chan 9 test
Time slice

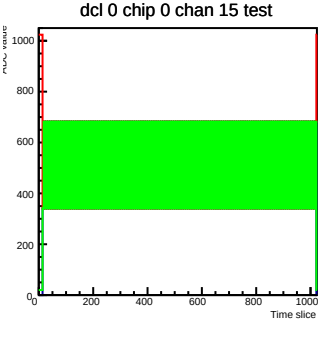

dcl 0 chip 0 chan 10 test
Time slice

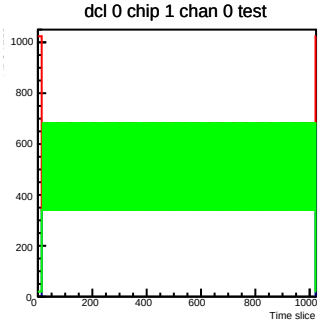

dcl 0 chip 0 chan 11 test
Time slice

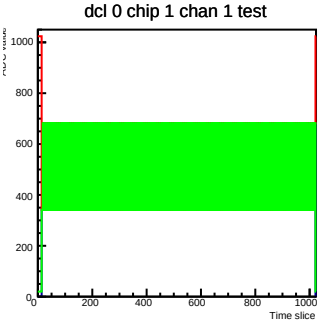

dcl 0 chip 0 chan 12 test
Time slice

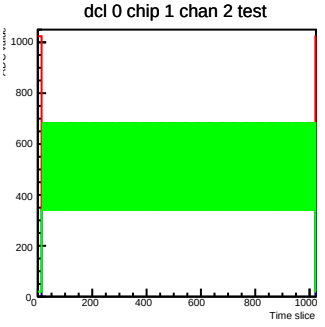

dcl 0 chip 0 chan 13 test
Time slice

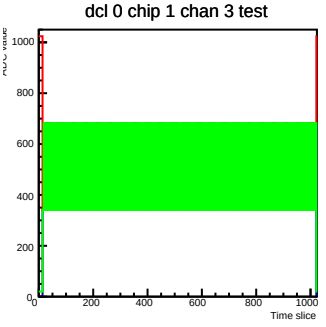

dcl 0 chip 0 chan 14 test
Time slice

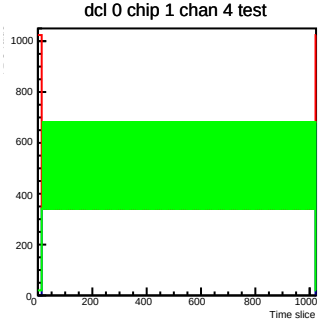

dcl 0 chip 0 chan 15 test
Time slice

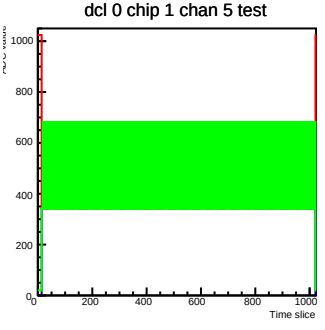

dcl 0 chip 1 chan 0 test
ADC value
Time slice

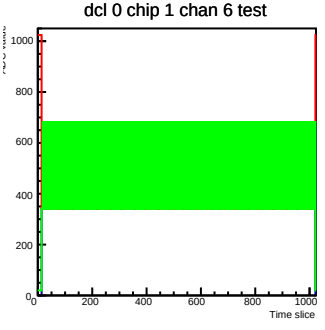

dcl 0 chip 1 chan 1 test
ADC value
Time slice

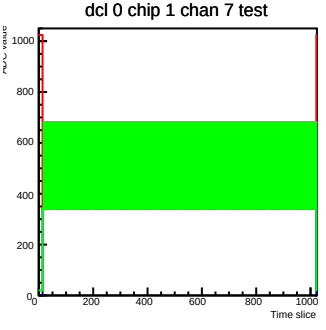

dcl 0 chip 1 chan 2 test
ADC value
Time slice

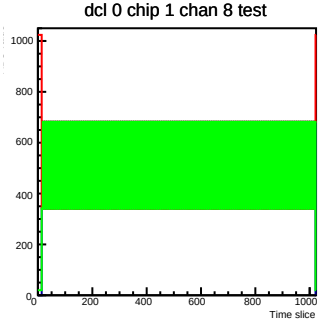

dcl 0 chip 1 chan 3 test
ADC value
Time slice

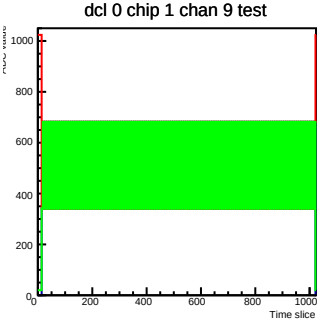

dcl 0 chip 1 chan 4 test
ADC value
Time slice

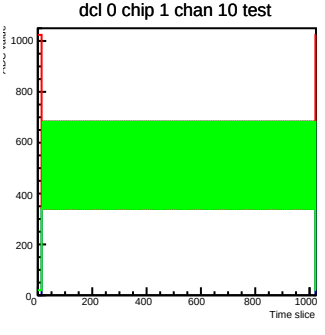

dcl 0 chip 1 chan 5 test
ADC value
Time slice

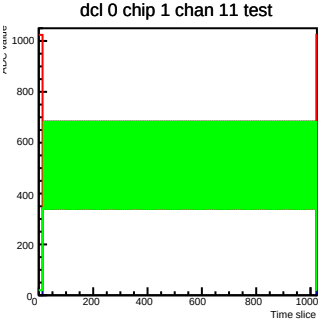

dcl 0 chip 1 chan 6 test
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Time slice

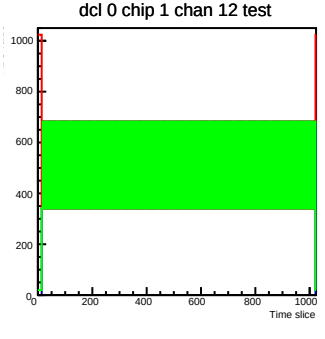

dcl 0 chip 1 chan 7 test
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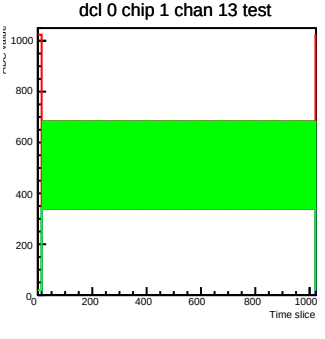

dcl 0 chip 1 chan 8 test
ADC value
Time slice

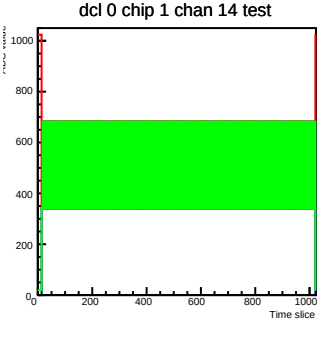

dcl 0 chip 1 chan 9 test
ADC value
Time slice

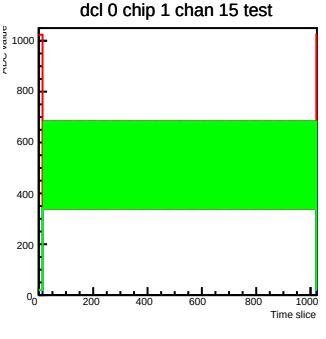

dcl 0 chip 1 chan 10 test
ADC value
Time slice

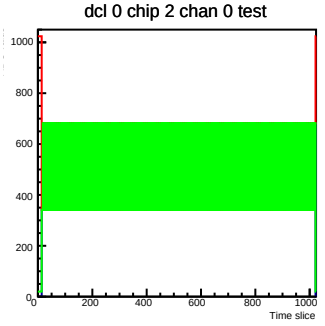

dcl 0 chip 1 chan 11 test
ADC value
Time slice

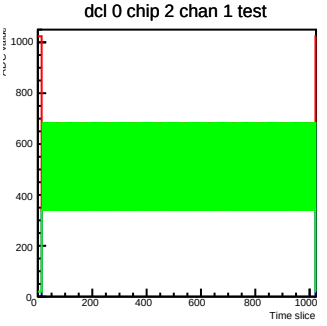

dcl 0 chip 1 chan 12 test
ADC value
Time slice

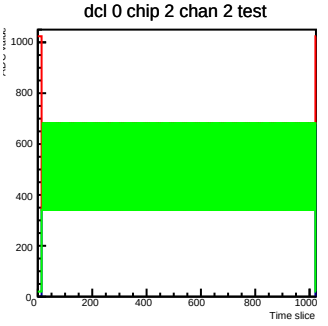

dcl 0 chip 1 chan 13 test
ADC value
Time slice

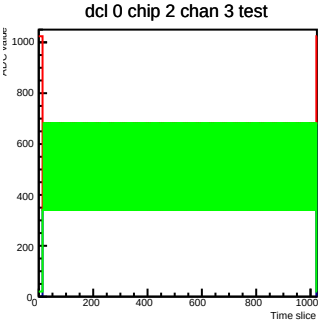

dcl 0 chip 1 chan 14 test
ADC value
Time slice

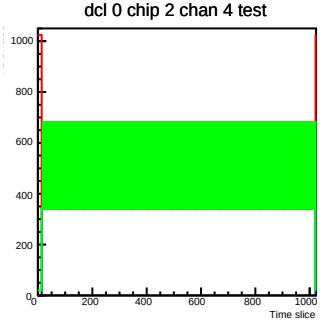

dcl 0 chip 1 chan 15 test
ADC value
Time slice

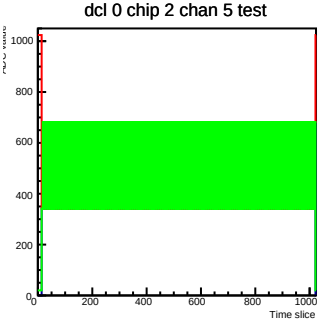

dcl 0 chip 2 chan 0 test
ADC value
Time slice

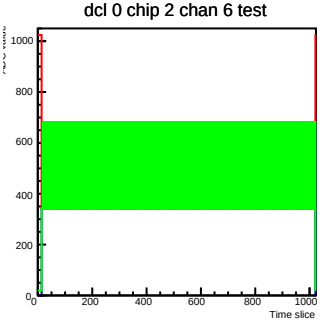

dcl 0 chip 2 chan 1 test
ADC value
Time slice

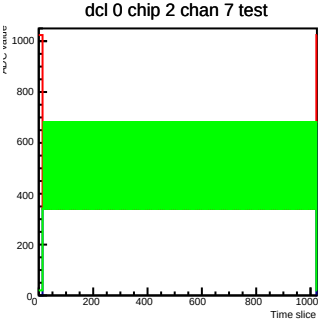

dcl 0 chip 2 chan 2 test
ADC value
Time slice

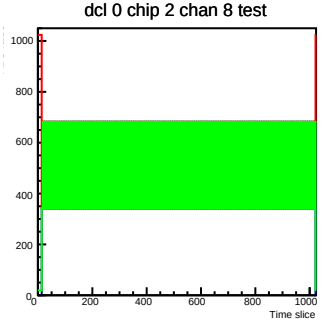

dcl 0 chip 2 chan 3 test
ADC value
Time slice

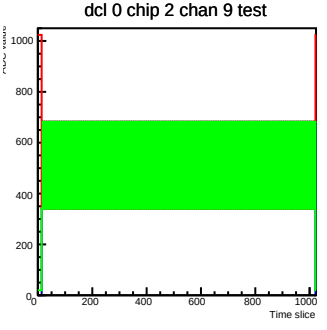

dcl 0 chip 2 chan 4 test
ADC value
Time slice

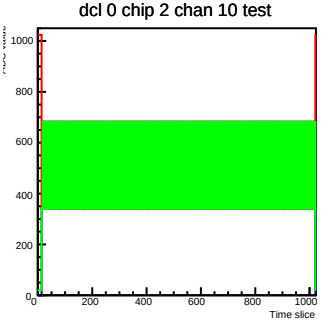

dcl 0 chip 2 chan 5 test
ADC value
Time slice

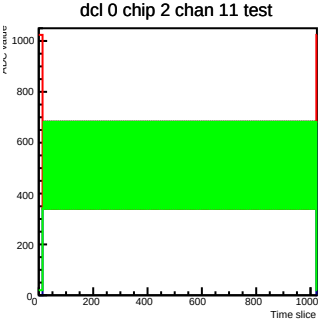

dcl 0 chip 2 chan 6 test
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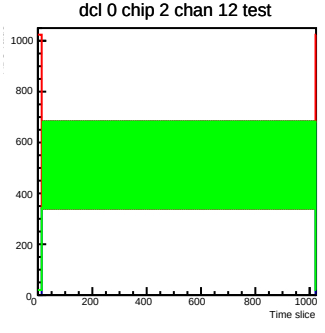

dcl 0 chip 2 chan 7 test
ADC value
Time slice

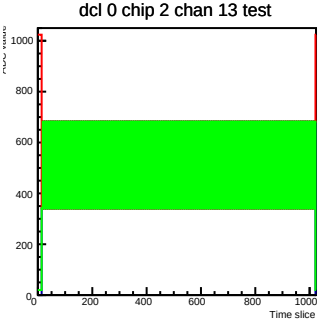

dcl 0 chip 2 chan 8 test
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Time slice

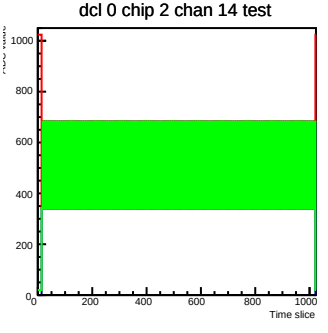

dcl 0 chip 2 chan 9 test
ADC value
Time slice

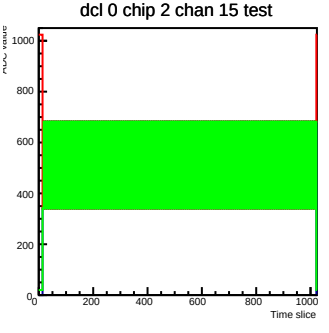

dcl 0 chip 2 chan 10 test
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Time slice

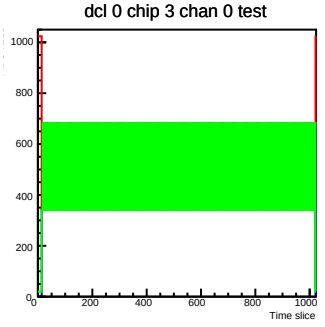

dcl 0 chip 2 chan 11 test
ADC value
Time slice

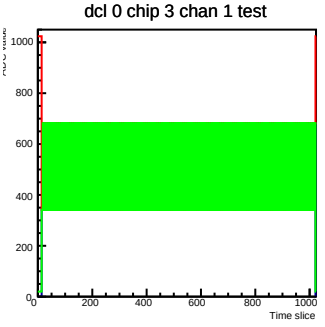

dcl 0 chip 2 chan 12 test
ADC value
Time slice

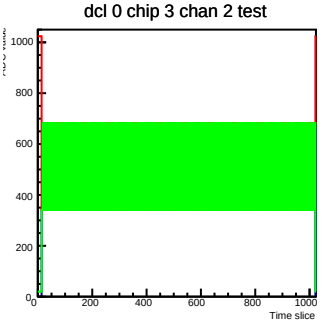

dcl 0 chip 2 chan 13 test
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Time slice

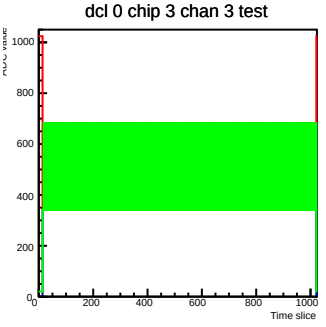

dcl 0 chip 2 chan 14 test
ADC value
Time slice

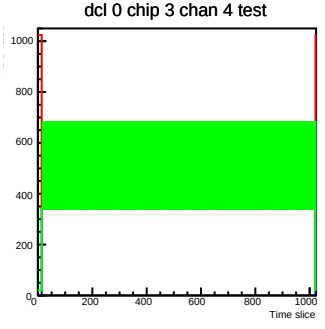

dcl 0 chip 2 chan 15 test
ADC value
Time slice

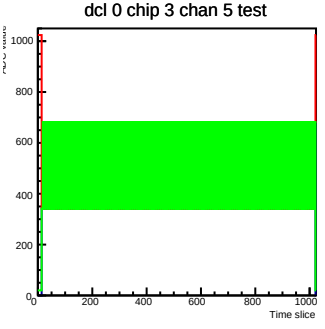

dcl 0 chip 3 chan 0 test
Time slice

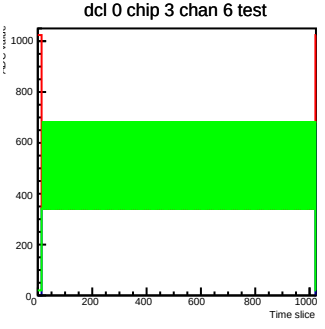

dcl 0 chip 3 chan 1 test
Time slice

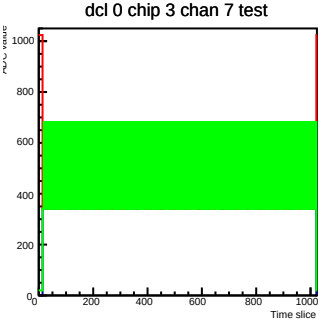

dcl 0 chip 3 chan 2 test
Time slice

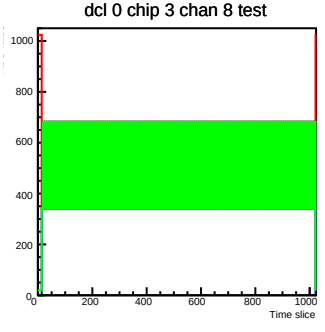

dcl 0 chip 3 chan 3 test
Time slice

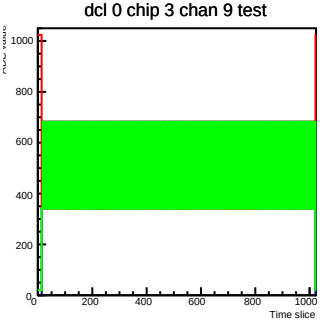

dcl 0 chip 3 chan 4 test
Time slice

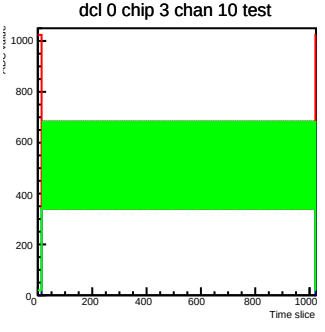

dcl 0 chip 3 chan 5 test
Time slice

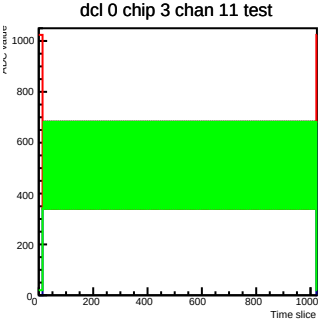

dcl 0 chip 3 chan 6 test
Time slice

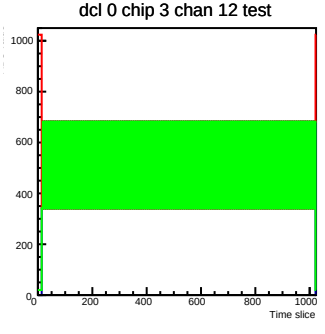

dcl 0 chip 3 chan 7 test
Time slice

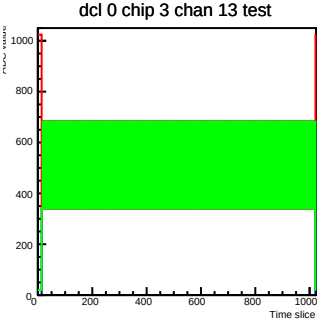

dcl 0 chip 3 chan 8 test
Time slice

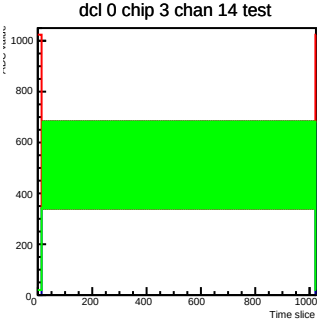

dcl 0 chip 3 chan 9 test
Time slice

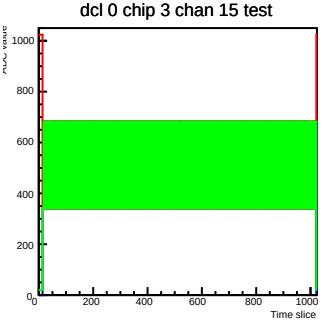

dcl 0 chip 3 chan 10 test
Time slice

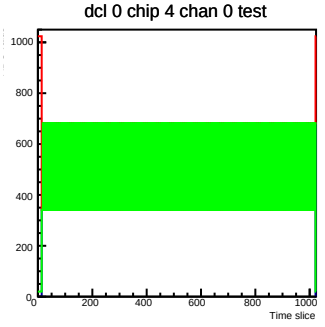

dcl 0 chip 3 chan 11 test
Time slice

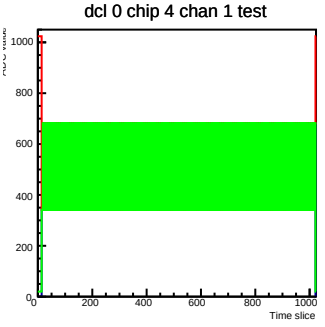

dcl 0 chip 3 chan 12 test
Time slice

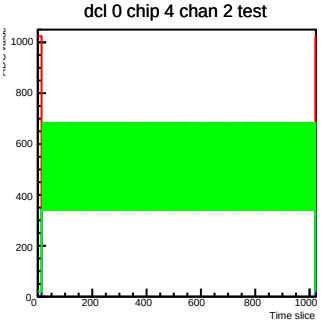

dcl 0 chip 3 chan 13 test
Time slice

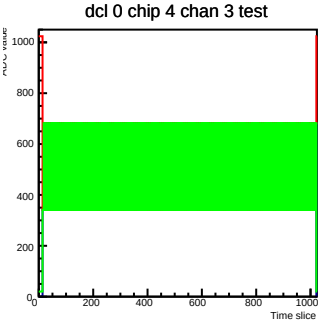

dcl 0 chip 3 chan 14 test
Time slice

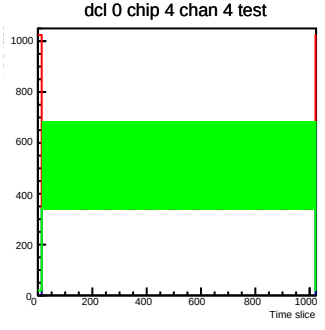

dcl 0 chip 3 chan 15 test
Time slice

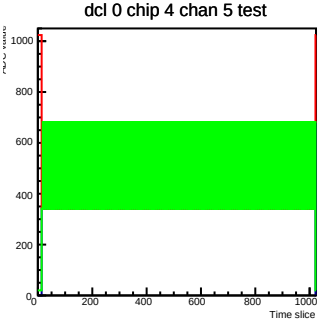

dcl 0 chip 4 chan 0 test
ADC value
Time slice

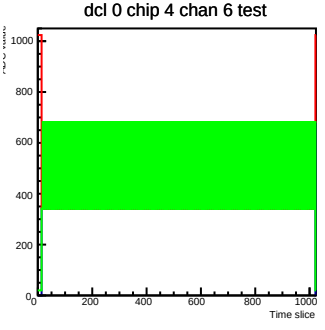

dcl 0 chip 4 chan 1 test
ADC value
Time slice

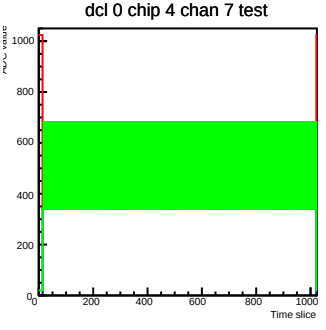

dcl 0 chip 4 chan 2 test
ADC value
Time slice

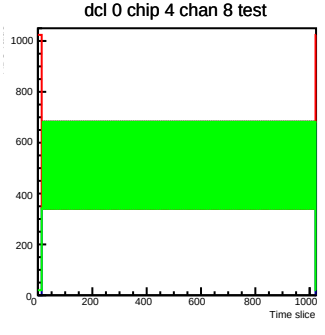

dcl 0 chip 4 chan 3 test
ADC value
Time slice

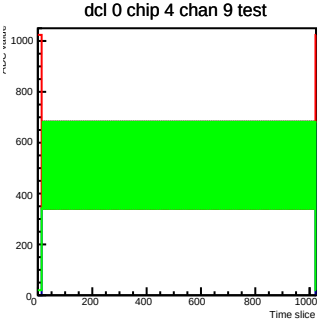

dcl 0 chip 4 chan 4 test
ADC value
Time slice

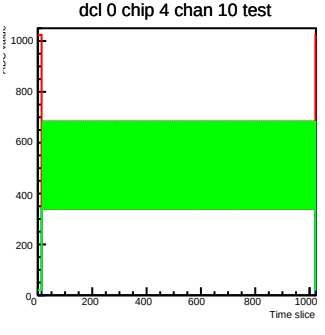

dcl 0 chip 4 chan 5 test
ADC value
Time slice

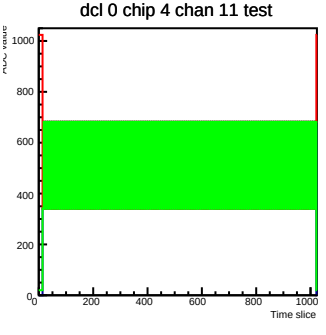

dcl 0 chip 4 chan 6 test
ADC value
Time slice

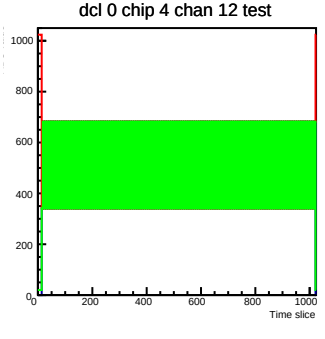

dcl 0 chip 4 chan 7 test
ADC value
Time slice

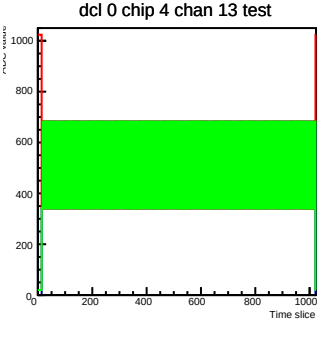

dcl 0 chip 4 chan 8 test
ADC value
Time slice

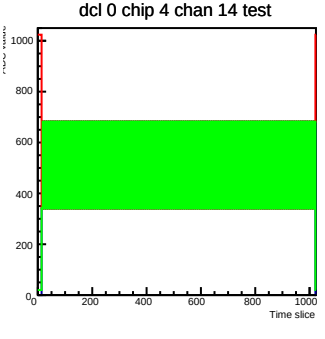

dcl 0 chip 4 chan 9 test
ADC value
Time slice

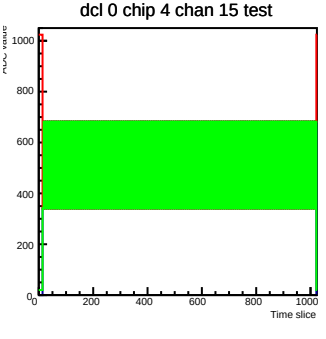

dcl 0 chip 4 chan 10 test
ADC value
Time slice

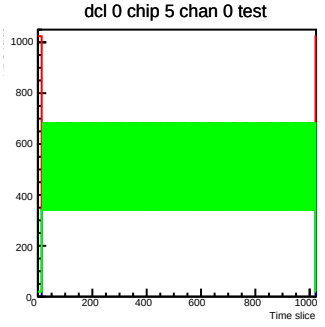

dcl 0 chip 4 chan 11 test
ADC value
Time slice

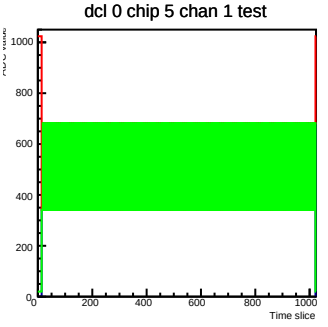

dcl 0 chip 4 chan 12 test
ADC value
Time slice

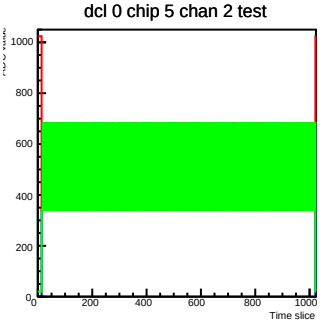

dcl 0 chip 4 chan 13 test
ADC value
Time slice

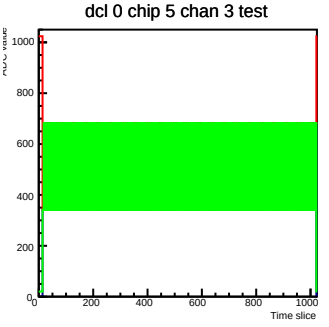

dcl 0 chip 4 chan 14 test
ADC value
Time slice

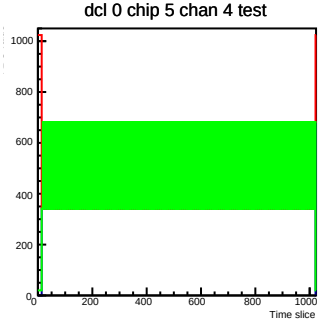

dcl 0 chip 4 chan 15 test
ADC value
Time slice

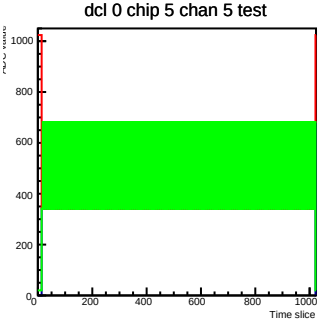

dcl 0 chip 5 chan 0 test
Time slice

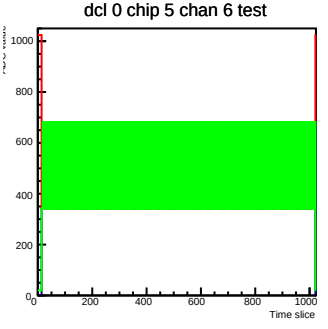

dcl 0 chip 5 chan 1 test
Time slice

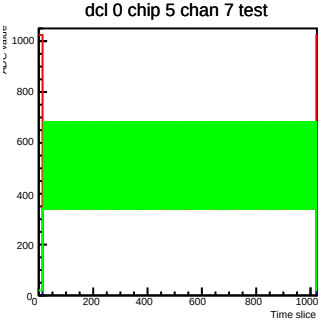

dcl 0 chip 5 chan 2 test
Time slice

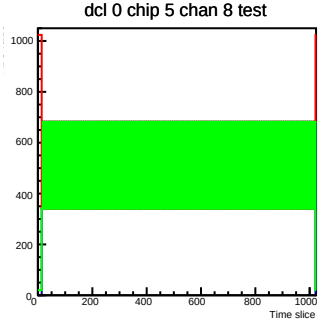

dcl 0 chip 5 chan 3 test
Time slice

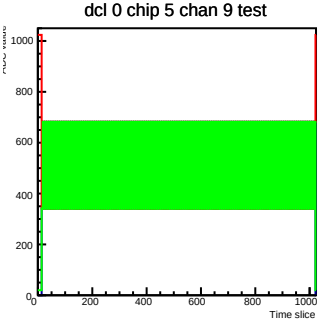

dcl 0 chip 5 chan 4 test
Time slice

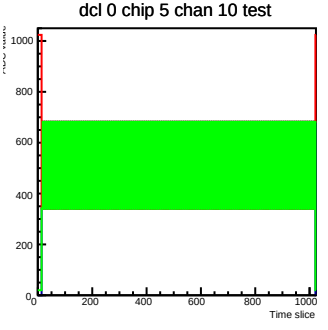

dcl 0 chip 5 chan 5 test
Time slice

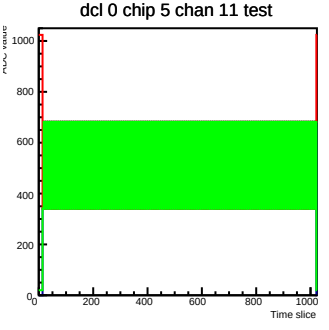

dcl 0 chip 5 chan 6 test
Time slice

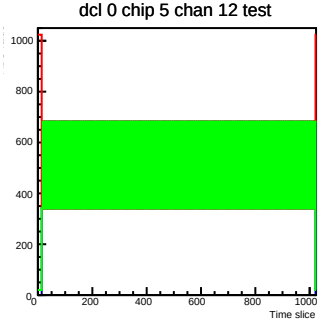

dcl 0 chip 5 chan 7 test
Time slice

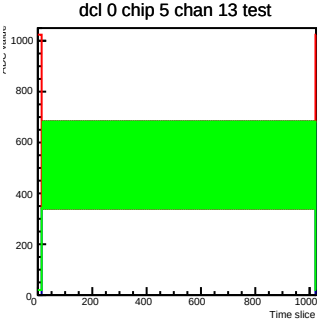

dcl 0 chip 5 chan 8 test
Time slice

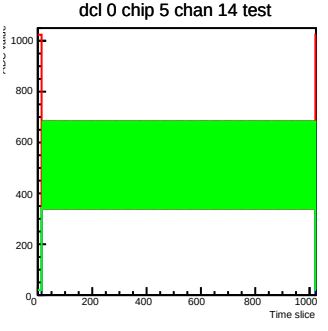

dcl 0 chip 5 chan 9 test
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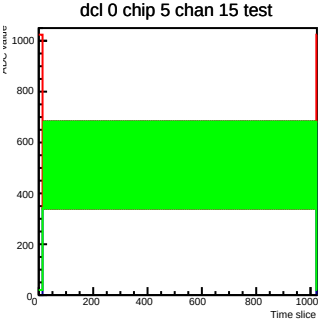

dcl 0 chip 5 chan 10 test
Time slice

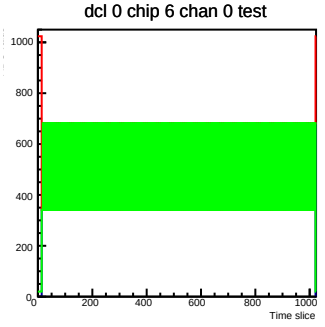

dcl 0 chip 5 chan 11 test
Time slice

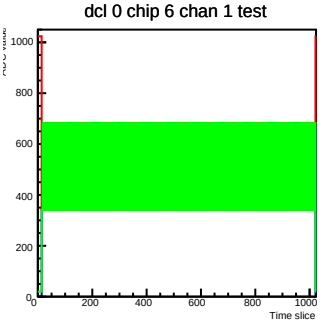

dcl 0 chip 5 chan 12 test
Time slice

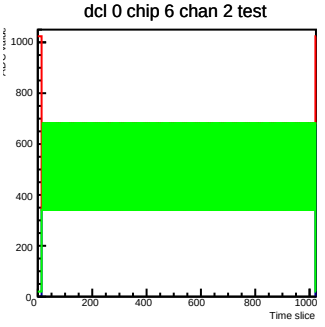

dcl 0 chip 5 chan 13 test
Time slice

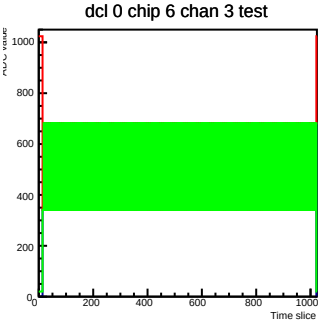

dcl 0 chip 5 chan 14 test
Time slice

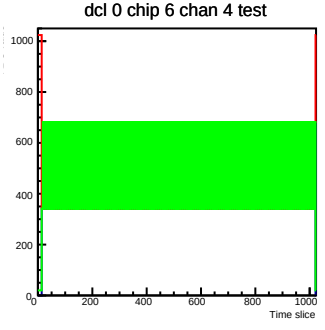

dcl 0 chip 5 chan 15 test
Time slice

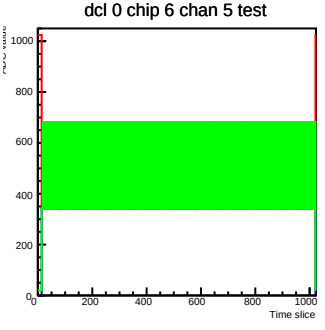

dcl 0 chip 6 chan 0 test
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Time slice

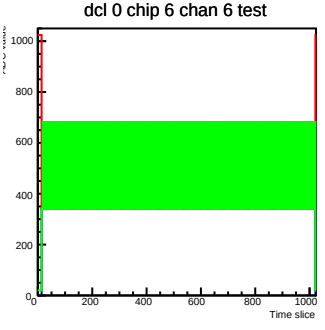

dcl 0 chip 6 chan 1 test
ADC value
Time slice

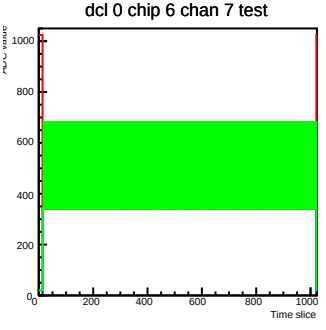

dcl 0 chip 6 chan 2 test
ADC value
Time slice

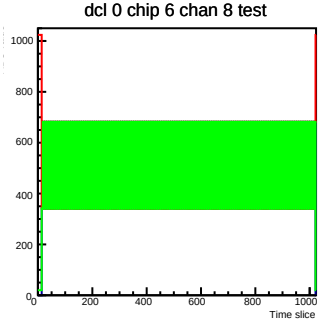

dcl 0 chip 6 chan 3 test
ADC value
Time slice

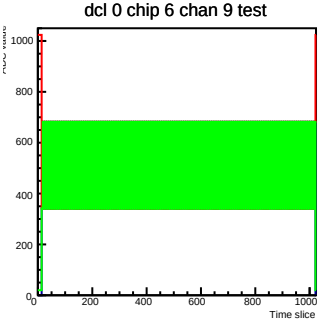

dcl 0 chip 6 chan 4 test
ADC value
Time slice

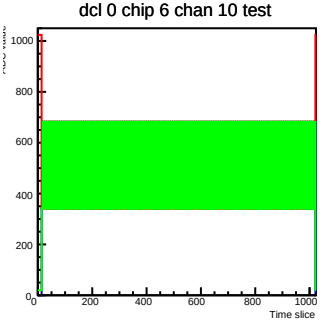

dcl 0 chip 6 chan 5 test
ADC value
Time slice

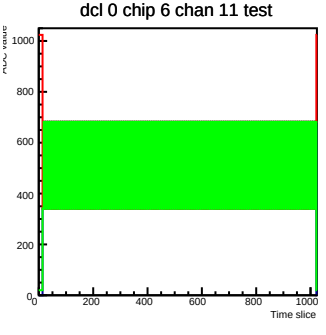

dcl 0 chip 6 chan 6 test
ADC value
Time slice

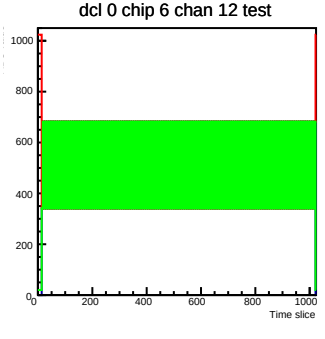

dcl 0 chip 6 chan 7 test
ADC value
Time slice

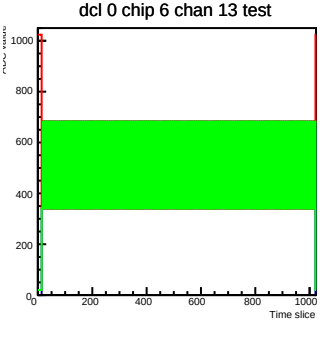

dcl 0 chip 6 chan 8 test
ADC value
Time slice

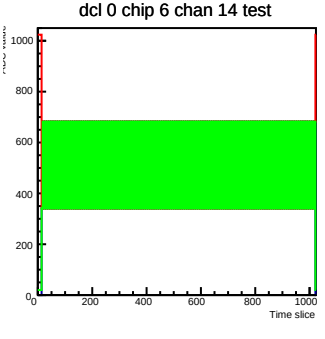

dcl 0 chip 6 chan 9 test
ADC value
Time slice

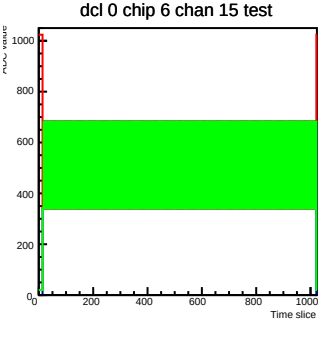

dcl 0 chip 6 chan 10 test
ADC value
Time slice

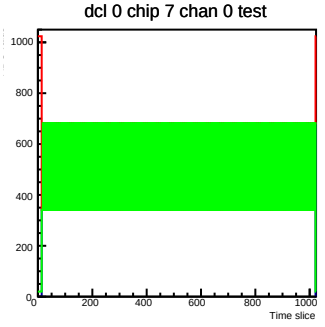

dcl 0 chip 6 chan 11 test
ADC value
Time slice

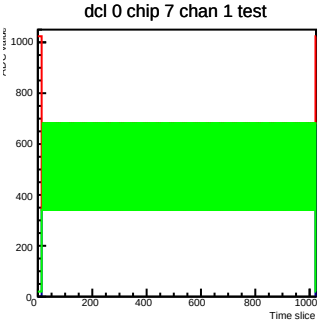

dcl 0 chip 6 chan 12 test
ADC value
Time slice

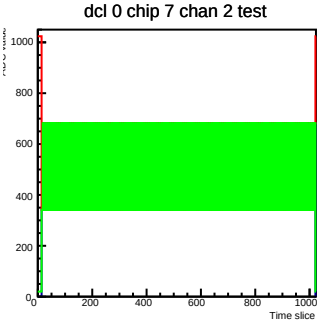

dcl 0 chip 6 chan 13 test
ADC value
Time slice

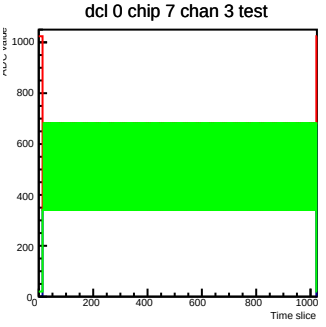

dcl 0 chip 6 chan 14 test
ADC value
Time slice

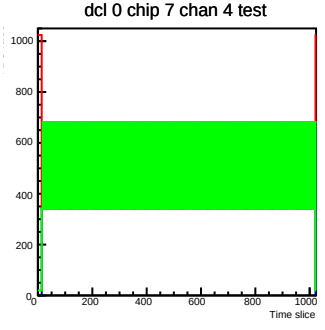

dcl 0 chip 6 chan 15 test
ADC value
Time slice

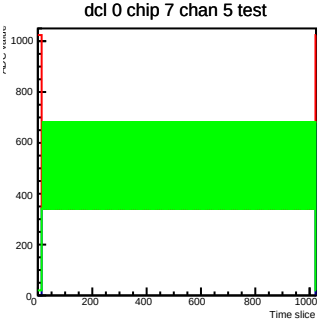

dcl 0 chip 7 chan 0 test
ADC value
Time slice

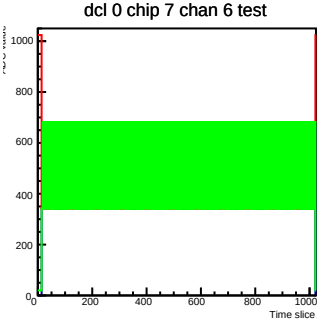

dcl 0 chip 7 chan 1 test
ADC value
Time slice

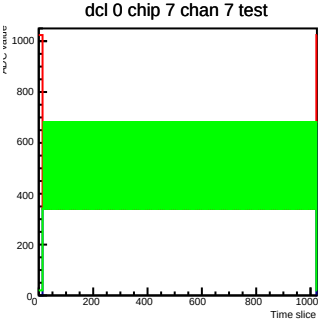

dcl 0 chip 7 chan 2 test
ADC value
Time slice

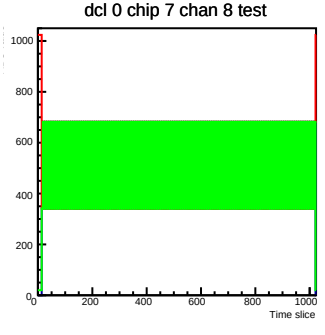

dcl 0 chip 7 chan 3 test
ADC value
Time slice

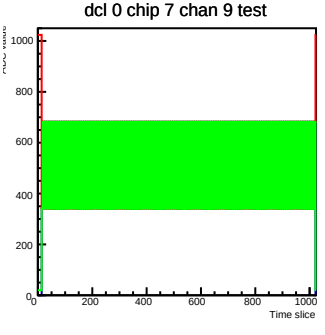

dcl 0 chip 7 chan 4 test
ADC value
Time slice

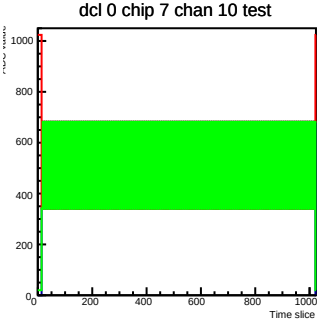

dcl 0 chip 7 chan 5 test
ADC value
Time slice

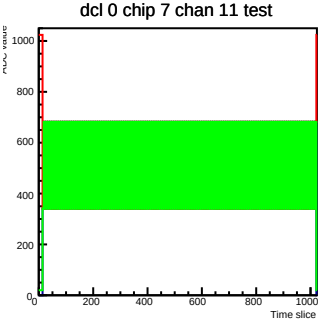

dcl 0 chip 7 chan 6 test
ADC value
Time slice

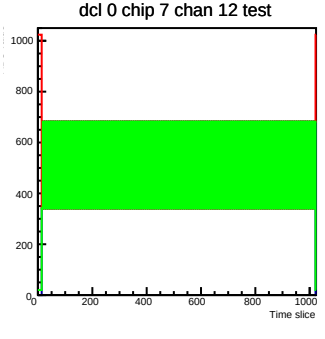

dcl 0 chip 7 chan 7 test
ADC value
Time slice

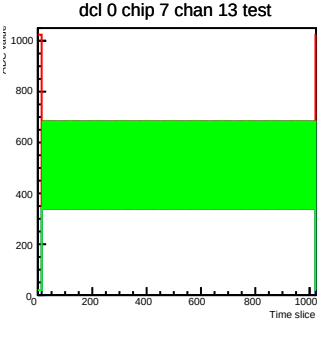

dcl 0 chip 7 chan 8 test
ADC value
Time slice

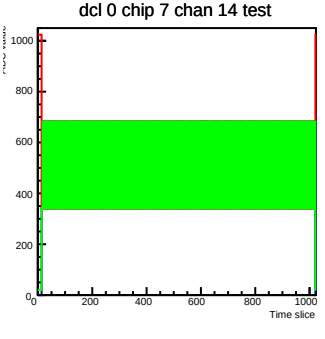

dcl 0 chip 7 chan 9 test
ADC value
Time slice

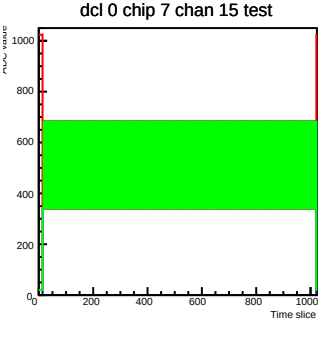

dcl 0 chip 7 chan 10 test
ADC value
Time slice

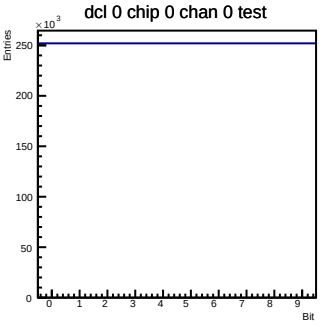

dcl 0 chip 7 chan 11 test
ADC value
Time slice

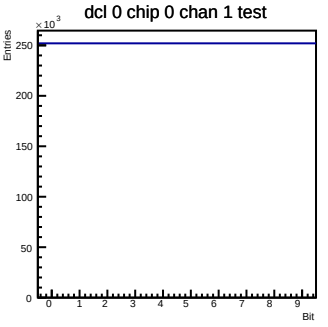

dcl 0 chip 7 chan 12 test
ADC value
Time slice

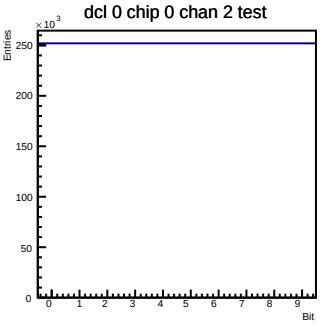

dcl 0 chip 7 chan 13 test
ADC value
Time slice

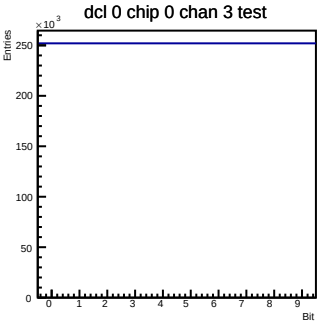

dcl 0 chip 7 chan 14 test
ADC value
Time slice

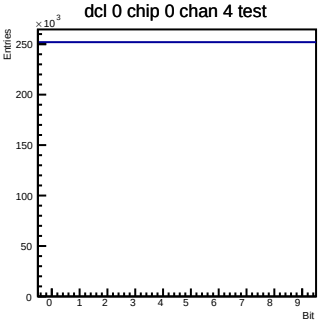

dcl 0 chip 7 chan 15 test
ADC value
Time slice

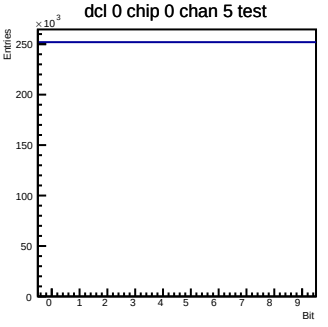

dcl 0 chip 0 chan 0 test
Entries
Bit

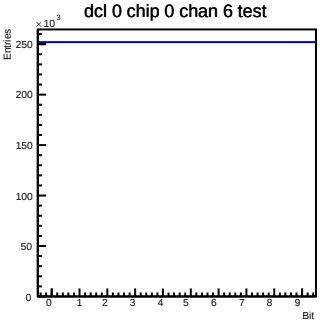

dcl 0 chip 0 chan 1 test
Entries
Bit

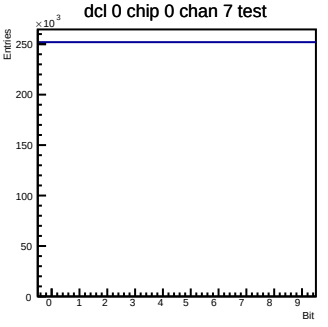

dcl 0 chip 0 chan 2 test
Entries
Bit

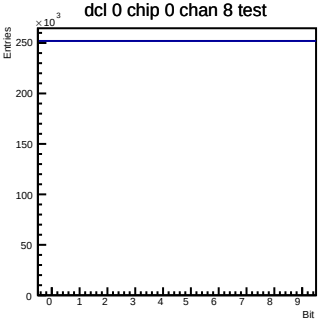

dcl 0 chip 0 chan 3 test
Entries
Bit

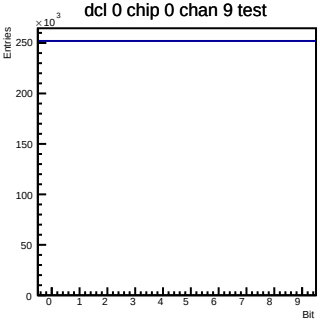

dcl 0 chip 0 chan 4 test
Entries
Bit

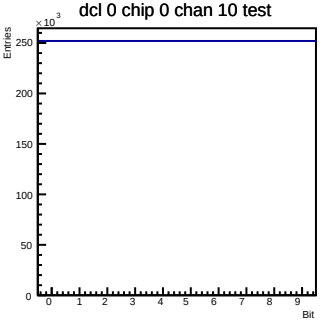

dcl 0 chip 0 chan 5 test
Entries
Bit

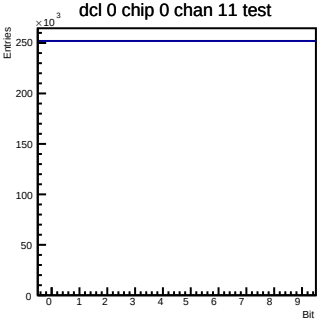

dcl 0 chip 0 chan 6 test
Entries
Bit

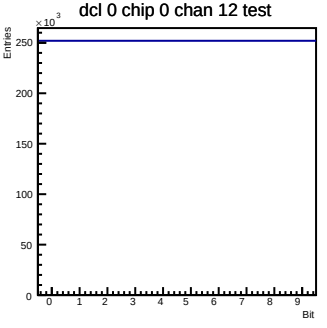

dcl 0 chip 0 chan 7 test
Entries
Bit

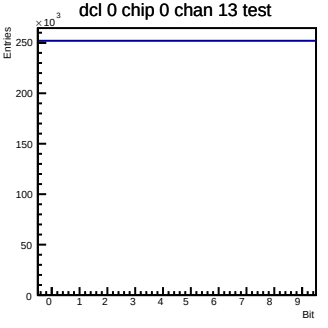

dcl 0 chip 0 chan 8 test
Entries
Bit

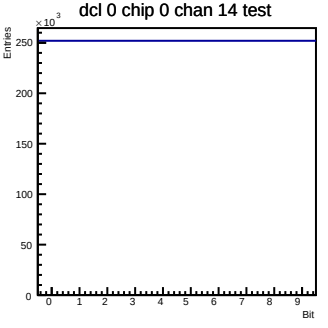

dcl 0 chip 0 chan 9 test
Entries
Bit

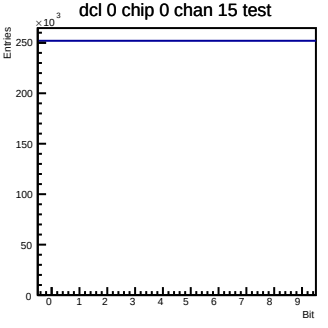

dcl 0 chip 0 chan 10 test
Entries
Bit

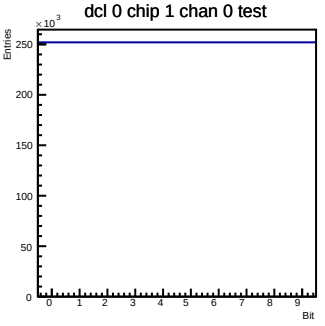

dcl 0 chip 0 chan 11 test
Entries
Bit

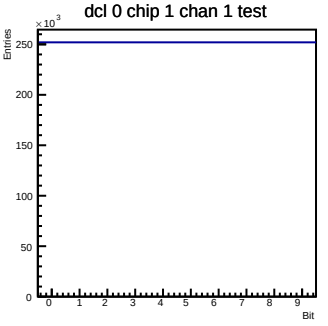

dcl 0 chip 0 chan 12 test
Entries
Bit

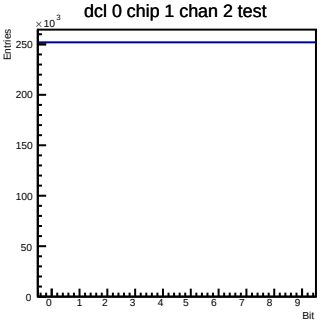

dcl 0 chip 0 chan 13 test
Entries
Bit

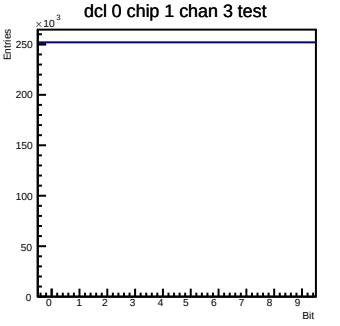

dcl 0 chip 0 chan 14 test
Entries
Bit

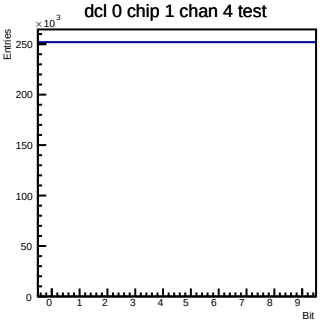

dcl 0 chip 0 chan 15 test
Entries
Bit

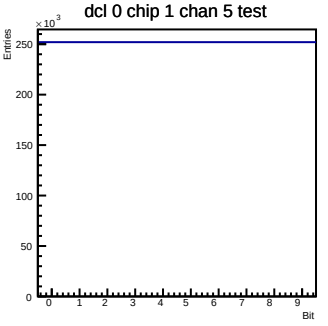

dcl 0 chip 1 chan 0 test
Entries
Bit

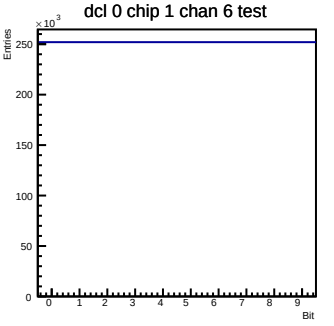

dcl 0 chip 1 chan 1 test
Entries
Bit

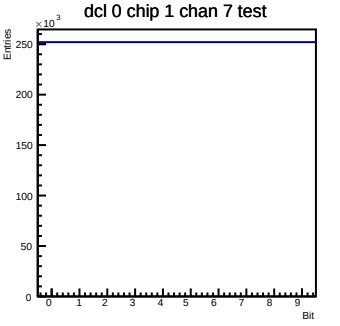

dcl 0 chip 1 chan 2 test
Entries
Bit

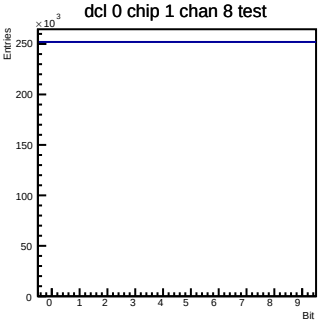

dcl 0 chip 1 chan 3 test
Entries
Bit

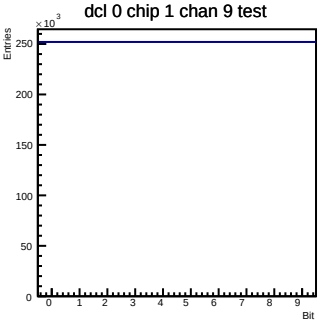

dcl 0 chip 1 chan 4 test
Entries
Bit

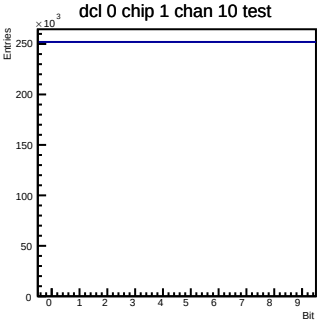

dcl 0 chip 1 chan 5 test
Entries
Bit

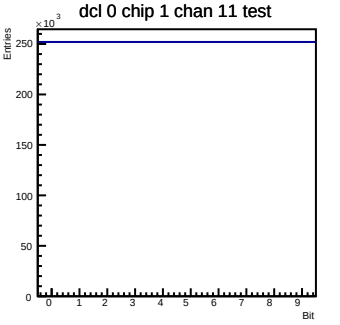

dcl 0 chip 1 chan 6 test
Entries
Bit

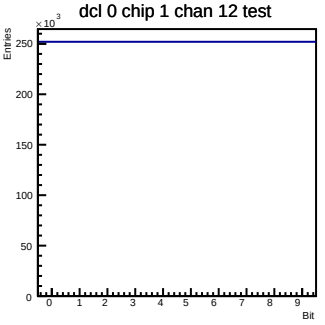

dcl 0 chip 1 chan 7 test
Entries
Bit

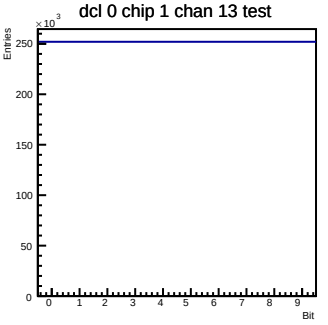

dcl 0 chip 1 chan 8 test
Entries
Bit

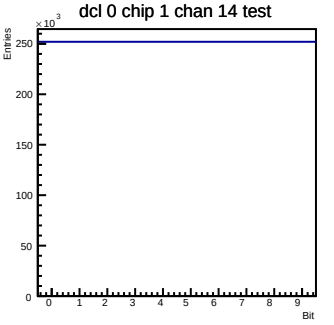

dcl 0 chip 1 chan 9 test
Entries
Bit

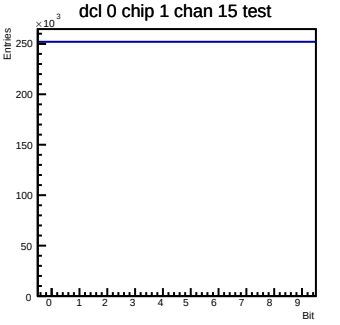

dcl 0 chip 1 chan 10 test
Entries
Bit

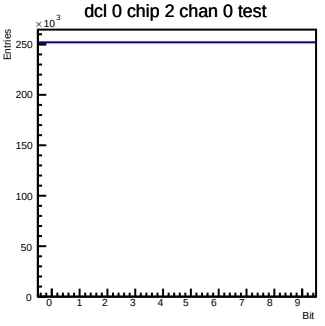

dcl 0 chip 1 chan 11 test
Entries
Bit

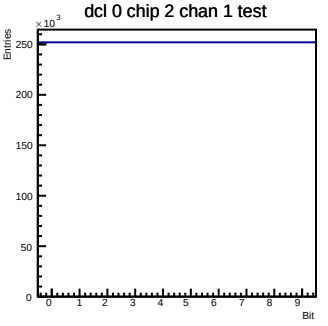

dcl 0 chip 1 chan 12 test
Entries
Bit

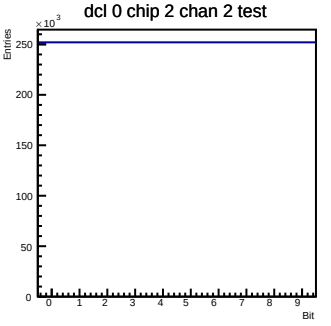

dcl 0 chip 1 chan 13 test
Entries
Bit

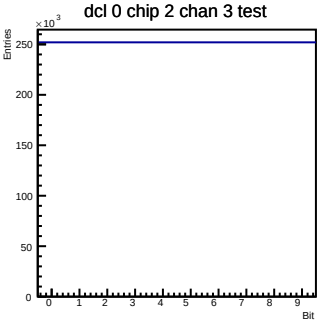

dcl 0 chip 1 chan 14 test
Entries
Bit

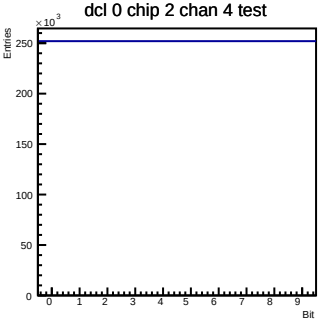

dcl 0 chip 1 chan 15 test
Entries
Bit

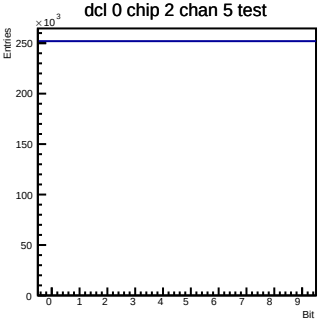

dcl 0 chip 2 chan 0 test
Entries
Bit

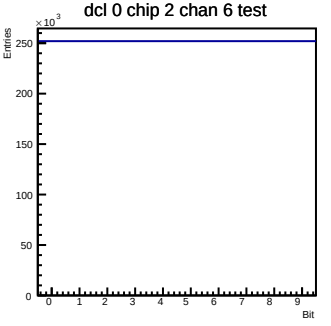

dcl 0 chip 2 chan 1 test
Entries
Bit

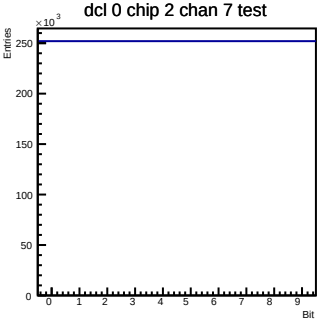

dcl 0 chip 2 chan 2 test
Entries
Bit

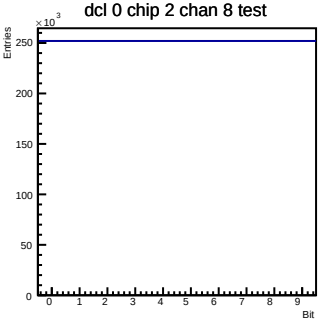

dcl 0 chip 2 chan 3 test
Entries
Bit

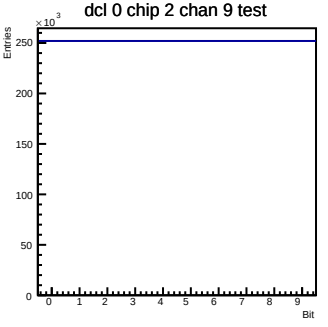

dcl 0 chip 2 chan 4 test
Entries
Bit

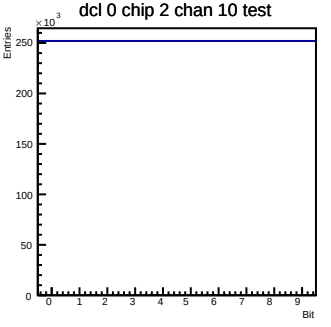

dcl 0 chip 2 chan 5 test
Entries
Bit

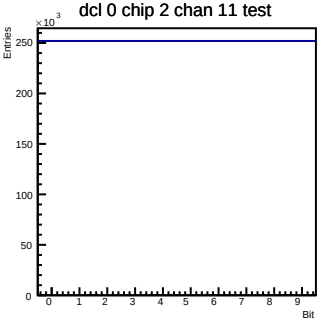

dcl 0 chip 2 chan 6 test
Entries
Bit

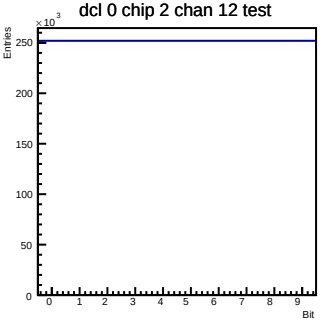

dcl 0 chip 2 chan 7 test
Entries
Bit

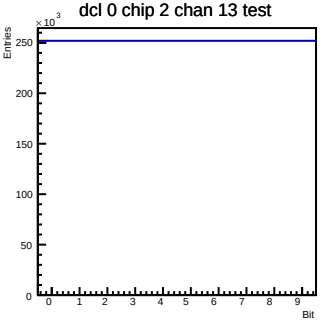

dcl 0 chip 2 chan 8 test
Entries
Bit

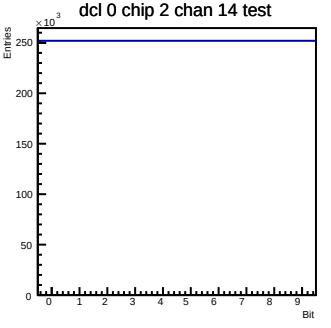

dcl 0 chip 2 chan 9 test
Entries
Bit

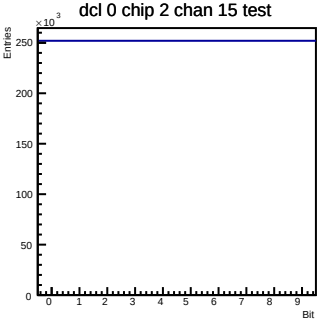

dcl 0 chip 2 chan 10 test
Entries
Bit

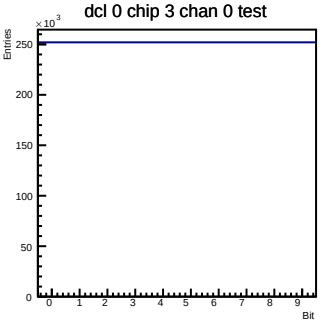

dcl 0 chip 2 chan 11 test
Entries
Bit

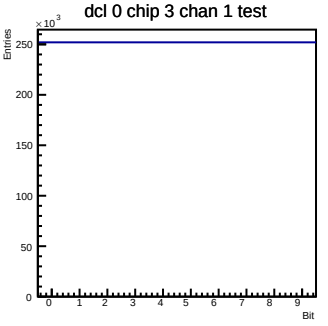

dcl 0 chip 2 chan 12 test
Entries
Bit

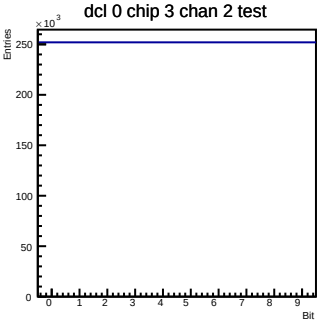

dcl 0 chip 2 chan 13 test
Entries
Bit

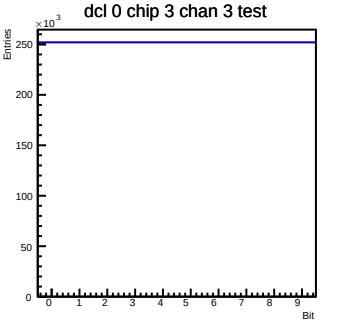

dcl 0 chip 2 chan 14 test
Entries
Bit

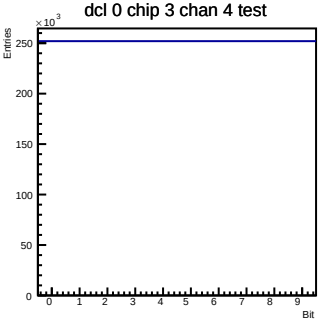

dcl 0 chip 2 chan 15 test
Entries
Bit

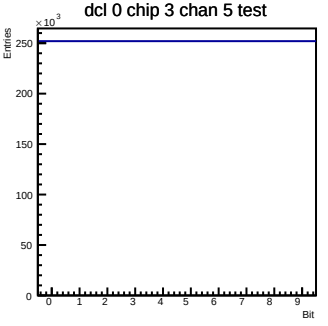

dcl 0 chip 3 chan 0 test
Entries
Bit

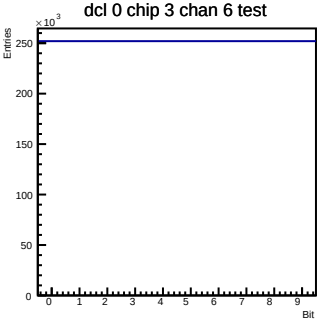

dcl 0 chip 3 chan 1 test
Entries
Bit

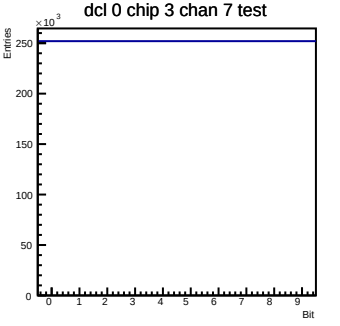

dcl 0 chip 3 chan 2 test
Entries
Bit

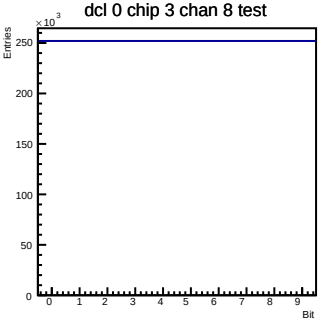

dcl 0 chip 3 chan 3 test
Entries
Bit

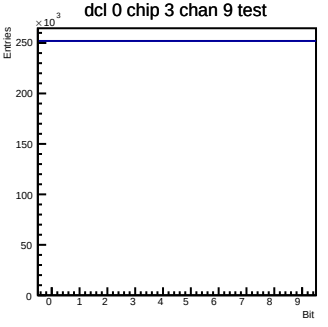

dcl 0 chip 3 chan 4 test
Entries
Bit

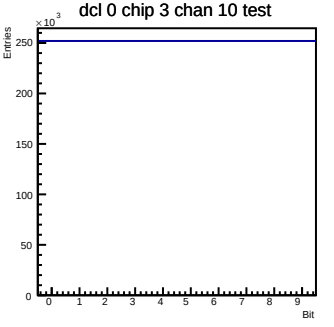

dcl 0 chip 3 chan 5 test
Entries
Bit

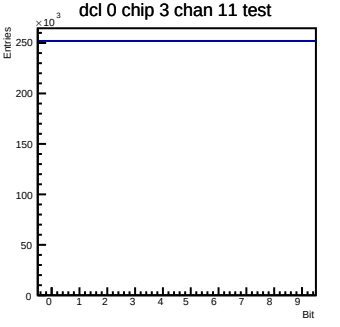

dcl 0 chip 3 chan 6 test
Entries
Bit

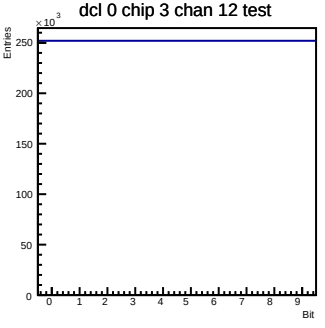

dcl 0 chip 3 chan 7 test
Entries
Bit

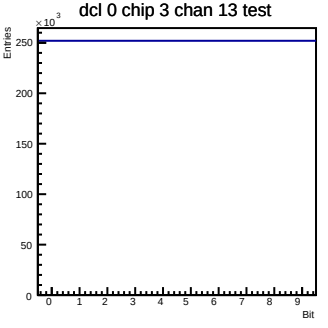

dcl 0 chip 3 chan 8 test
Entries
Bit

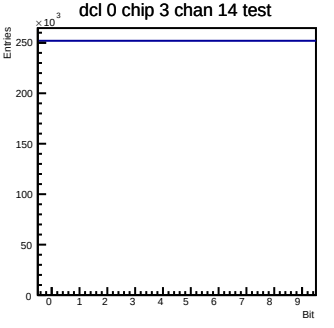

dcl 0 chip 3 chan 9 test
Entries
Bit

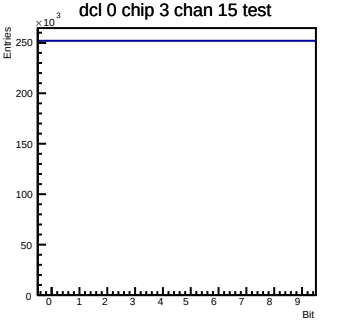

dcl 0 chip 3 chan 10 test
Entries
Bit

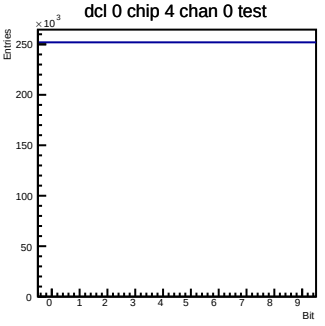

dcl 0 chip 3 chan 11 test
Entries
Bit

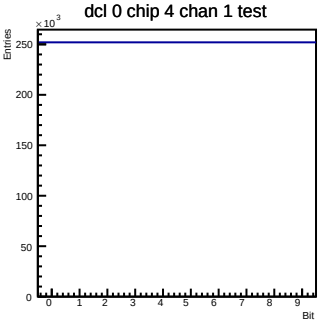

dcl 0 chip 3 chan 12 test
Entries
Bit

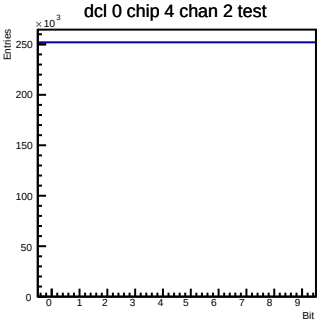

dcl 0 chip 3 chan 13 test
Entries
Bit

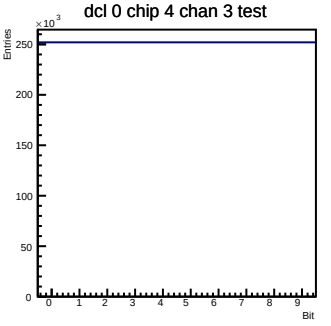

dcl 0 chip 3 chan 14 test
Entries
Bit

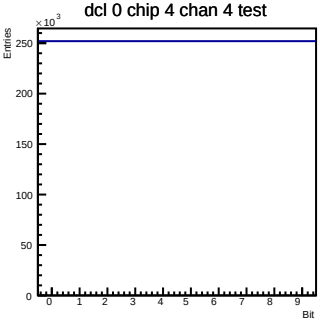

dcl 0 chip 3 chan 15 test
Entries
Bit

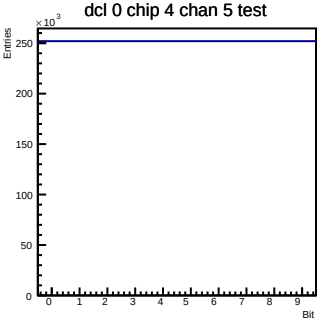

dcl 0 chip 4 chan 0 test
Entries
Bit

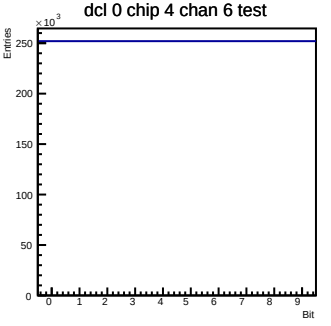

dcl 0 chip 4 chan 1 test
Entries
Bit

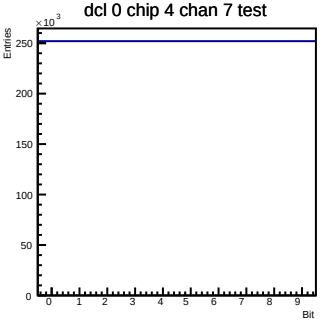

dcl 0 chip 4 chan 2 test
Entries
Bit

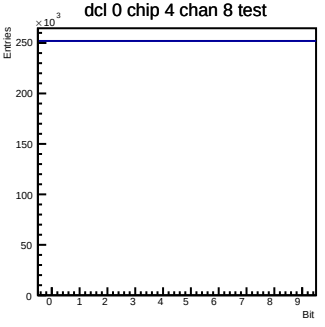

dcl 0 chip 4 chan 3 test
Entries
Bit

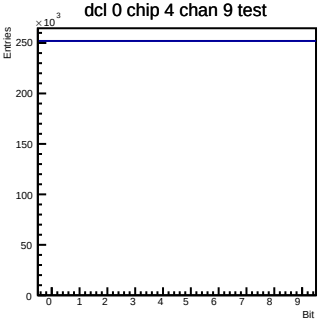

dcl 0 chip 4 chan 4 test
Entries
Bit

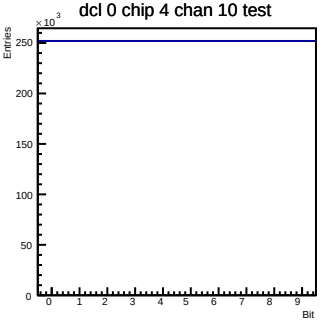

dcl 0 chip 4 chan 5 test
Entries
Bit

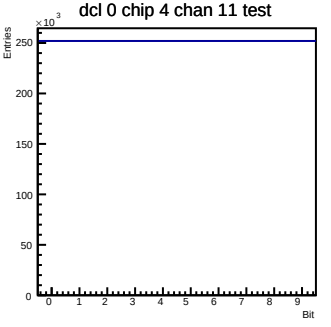

dcl 0 chip 4 chan 6 test
Entries
Bit

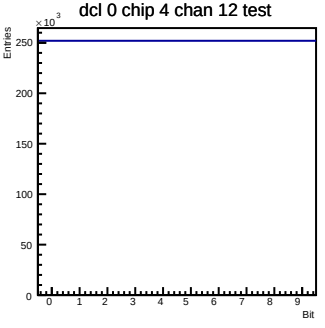

dcl 0 chip 4 chan 7 test
Entries
Bit

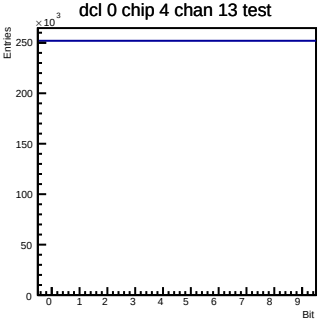

dcl 0 chip 4 chan 8 test
Entries
Bit

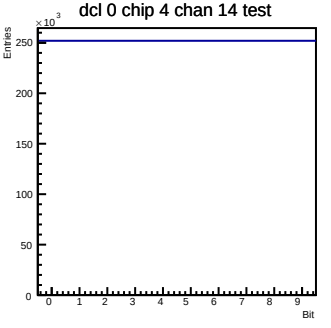

dcl 0 chip 4 chan 9 test
Entries
Bit

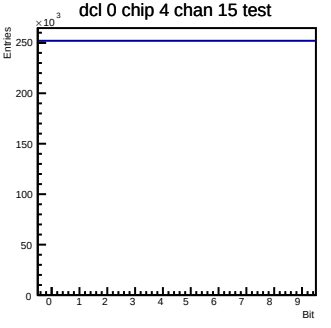

dcl 0 chip 4 chan 10 test
Entries
Bit

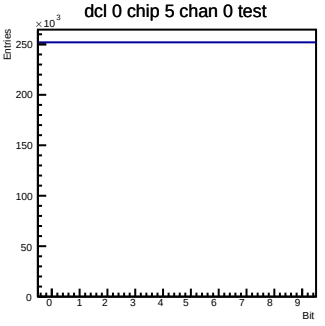

dcl 0 chip 4 chan 11 test
Entries
Bit

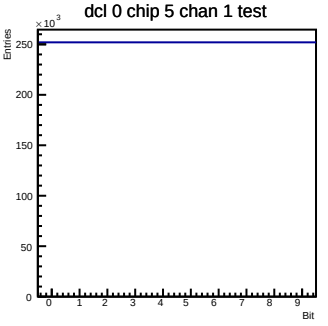

dcl 0 chip 4 chan 12 test
Entries
Bit

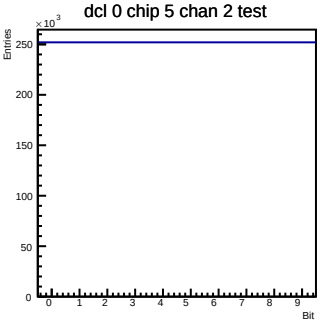

dcl 0 chip 4 chan 13 test
Entries
Bit

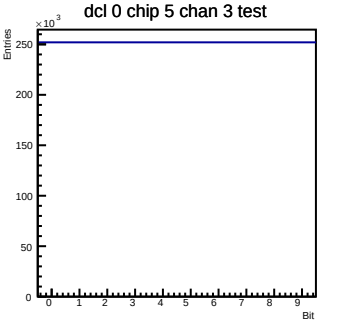

dcl 0 chip 4 chan 14 test
Entries
Bit

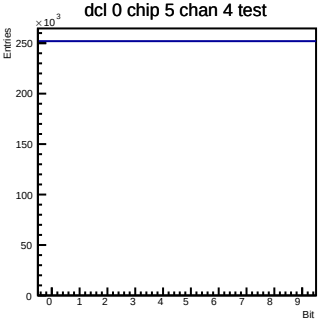

dcl 0 chip 4 chan 15 test
Entries
Bit

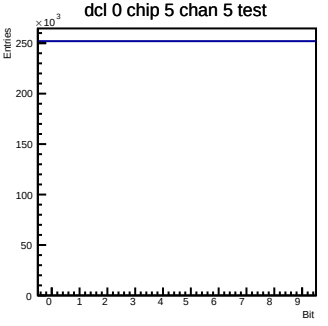

dcl 0 chip 5 chan 0 test
Entries
Bit

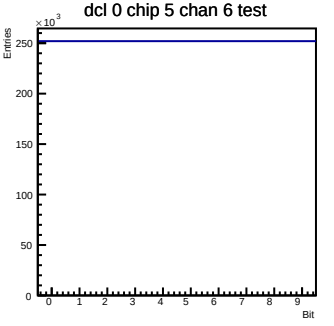

dcl 0 chip 5 chan 1 test
Entries
Bit

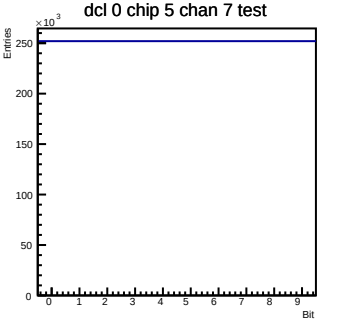

dcl 0 chip 5 chan 2 test
Entries
Bit

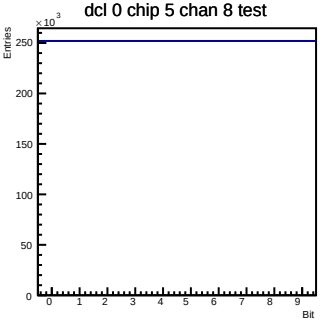

dcl 0 chip 5 chan 3 test
Entries
Bit

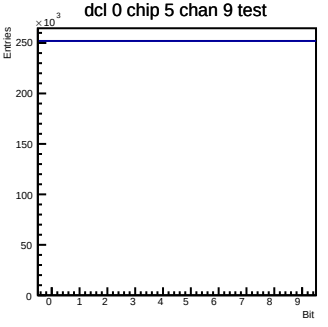

dcl 0 chip 5 chan 4 test
Entries
Bit

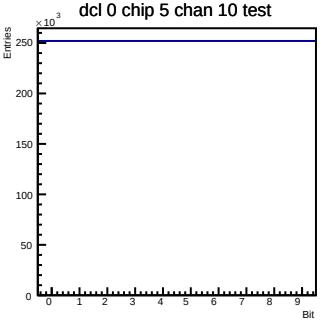

dcl 0 chip 5 chan 5 test
Entries
Bit

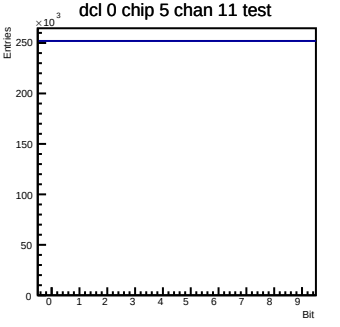

dcl 0 chip 5 chan 6 test
Entries
Bit

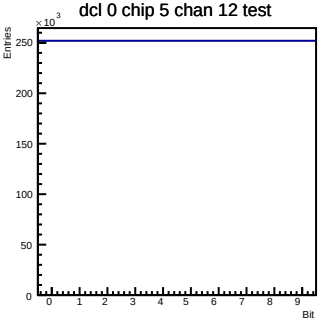

dcl 0 chip 5 chan 7 test
Entries
Bit

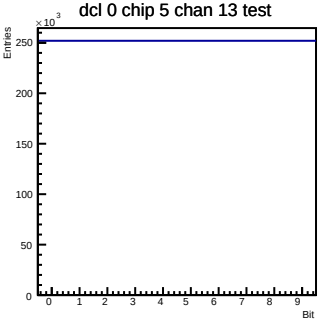

dcl 0 chip 5 chan 8 test
Entries
Bit

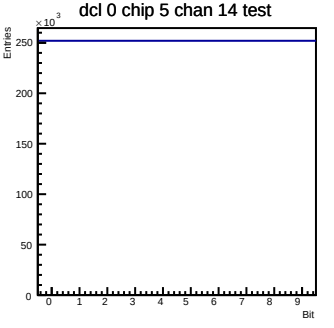

dcl 0 chip 5 chan 9 test
Entries
Bit

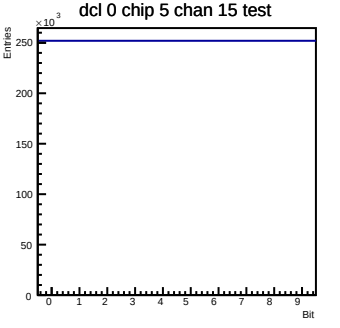

dcl 0 chip 5 chan 10 test
Entries
Bit

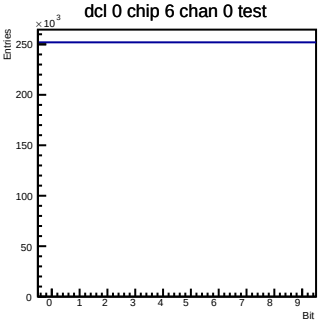

dcl 0 chip 5 chan 11 test
Entries
Bit

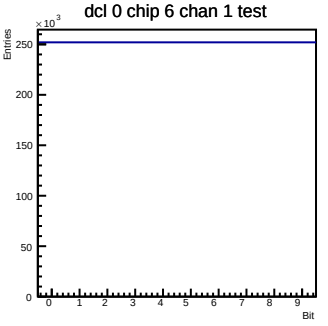

dcl 0 chip 5 chan 12 test
Entries
Bit

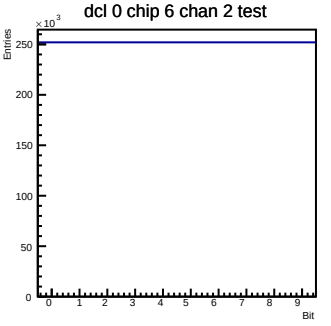

dcl 0 chip 5 chan 13 test
Entries
Bit

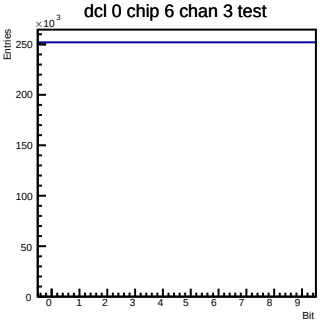

dcl 0 chip 5 chan 14 test
Entries
Bit

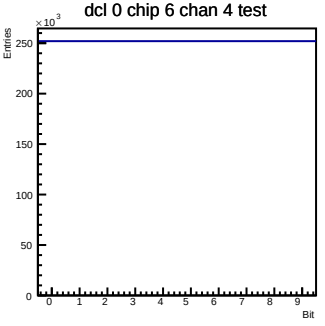

dcl 0 chip 5 chan 15 test
Entries
Bit

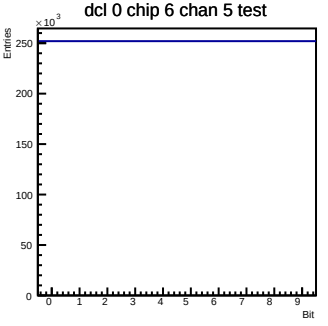

dcl 0 chip 6 chan 0 test
Entries
Bit

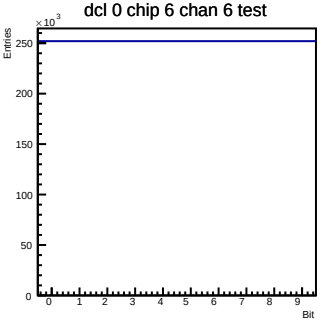

dcl 0 chip 6 chan 1 test
Entries
Bit

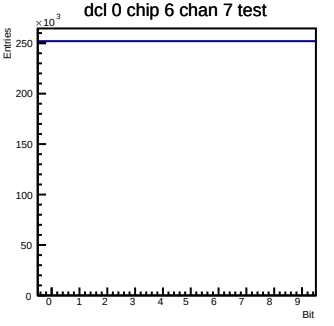

dcl 0 chip 6 chan 2 test
Entries
Bit

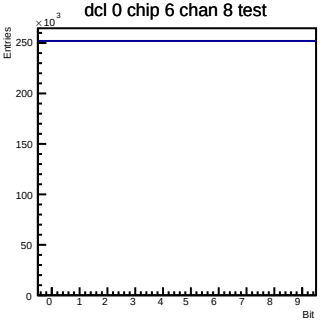

dcl 0 chip 6 chan 3 test
Entries
Bit

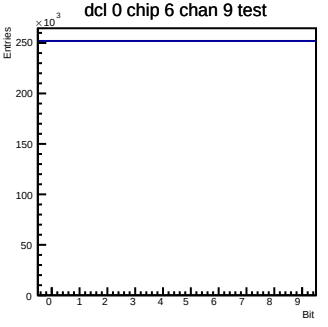

dcl 0 chip 6 chan 4 test
Entries
Bit

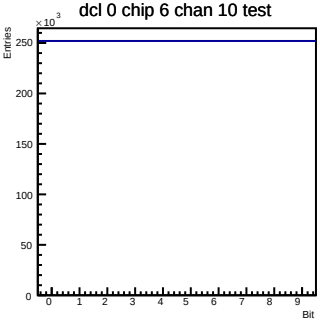

dcl 0 chip 6 chan 5 test
Entries
Bit

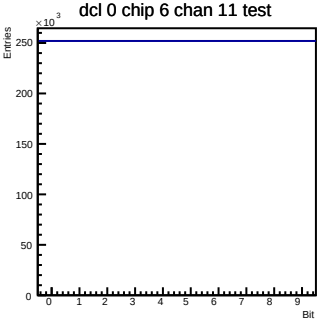

dcl 0 chip 6 chan 6 test
Entries
Bit

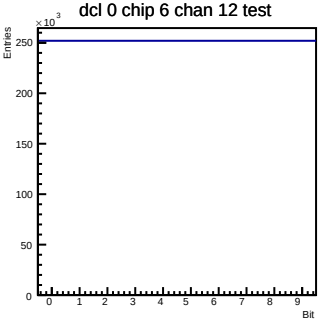

dcl 0 chip 6 chan 7 test
Entries
Bit

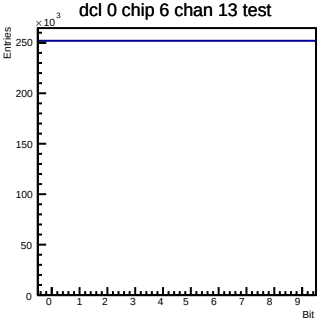

dcl 0 chip 6 chan 8 test
Entries
Bit

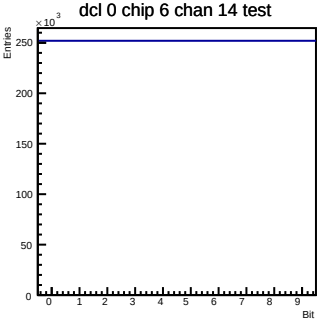

dcl 0 chip 6 chan 9 test
Entries
Bit

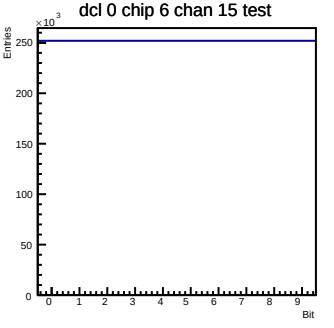

dcl 0 chip 6 chan 10 test
Entries
Bit

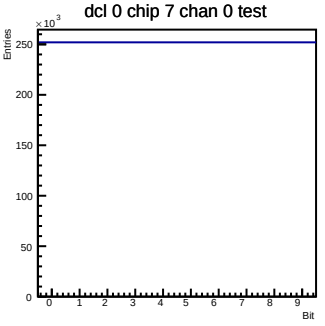

dcl 0 chip 6 chan 11 test
Entries
Bit

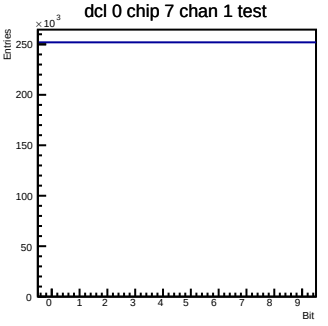

dcl 0 chip 6 chan 12 test
Entries
Bit

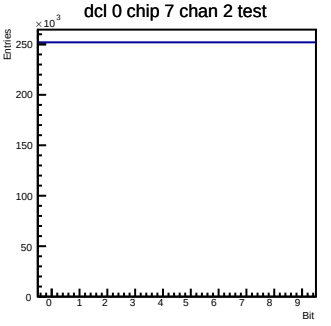

dcl 0 chip 6 chan 13 test
Entries
Bit

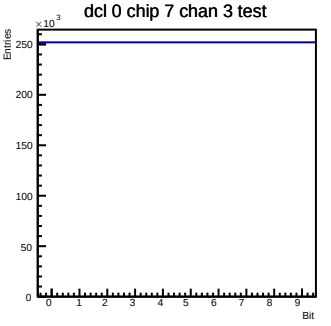

dcl 0 chip 6 chan 14 test
Entries
Bit

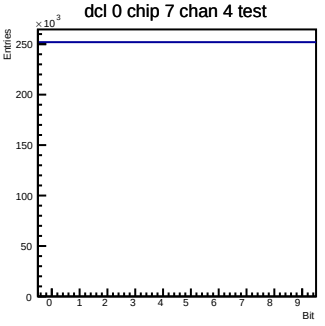

dcl 0 chip 6 chan 15 test
Entries
Bit

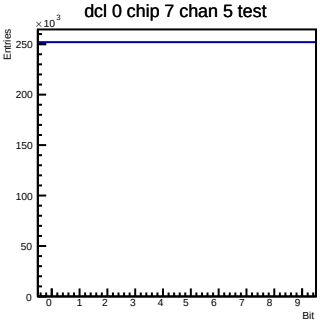

dcl 0 chip 7 chan 0 test
Entries
Bit

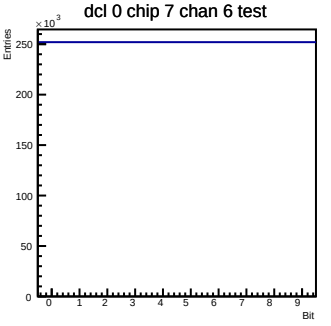

dcl 0 chip 7 chan 1 test
Entries
Bit

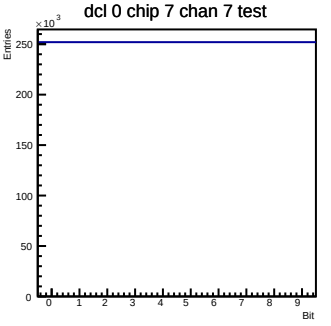

dcl 0 chip 7 chan 2 test
Entries
Bit

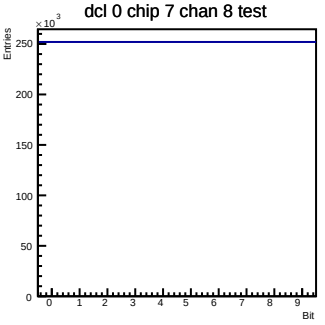

dcl 0 chip 7 chan 3 test
Entries
Bit

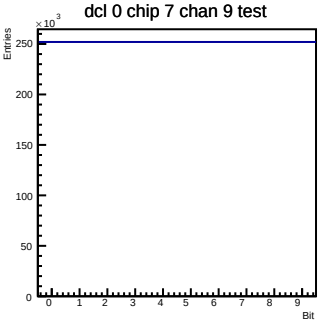

dcl 0 chip 7 chan 4 test
Entries
Bit

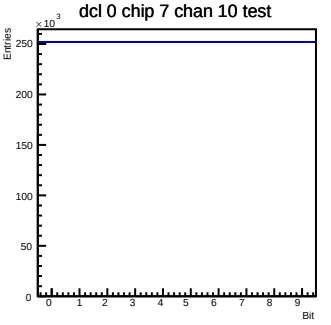

dcl 0 chip 7 chan 5 test
Entries
Bit

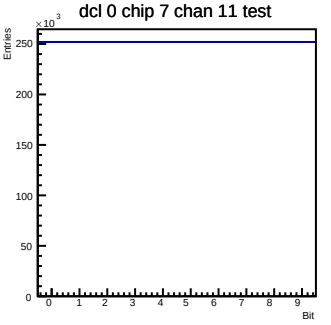

dcl 0 chip 7 chan 6 test
Entries
Bit

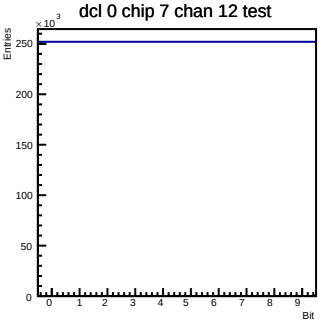

dcl 0 chip 7 chan 7 test
Entries
Bit

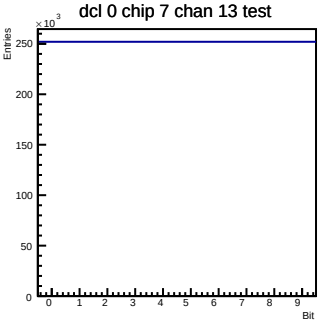

dcl 0 chip 7 chan 8 test
Entries
Bit

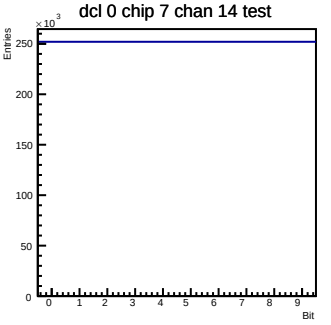

dcl 0 chip 7 chan 9 test
Entries
Bit

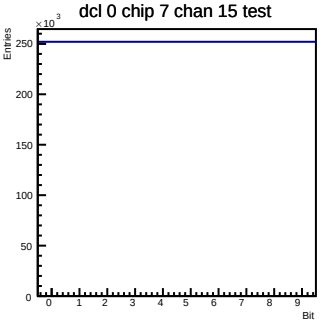

dcl 0 chip 7 chan 10 test
Entries
Bit

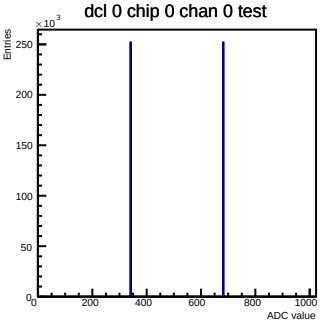

dcl 0 chip 7 chan 11 test
Entries
Bit

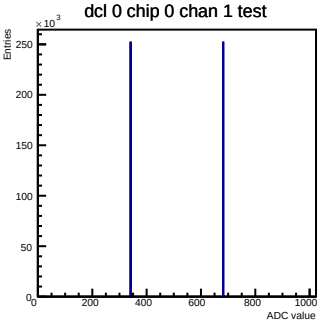

dcl 0 chip 7 chan 12 test
Entries
Bit

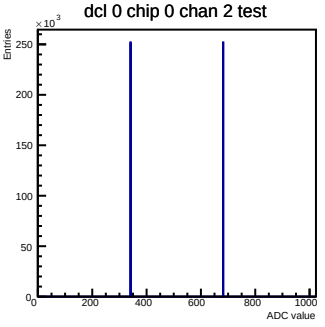

dcl 0 chip 7 chan 13 test
Entries
Bit

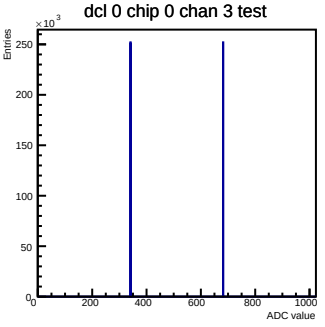

dcl 0 chip 7 chan 14 test
Entries
Bit

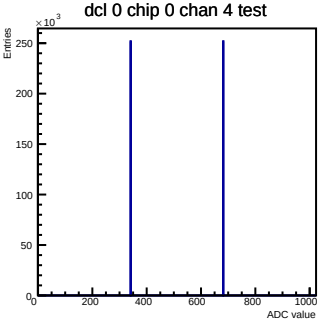

dcl 0 chip 7 chan 15 test
Entries
Bit

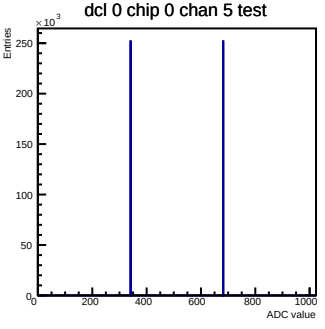

dcl 0 chip 0 chan 0 test
Entries
×10³
250
200
150
100
50
0
0
200
400
600
800
1000
ADC value

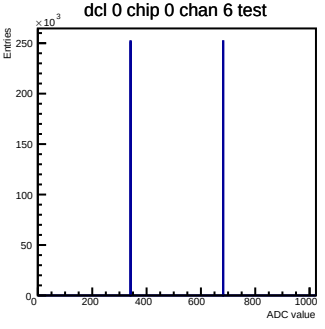

dcl 0 chip 0 chan 1 test
Entries
×10³
250
200
150
100
50
0
0
200
400
600
800
1000
ADC value

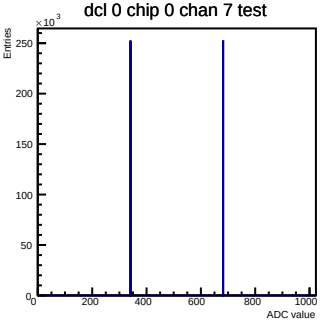

dcl 0 chip 0 chan 2 test
Entries
×10³
250
200
150
100
50
0
0
200
400
600
800
1000
ADC value

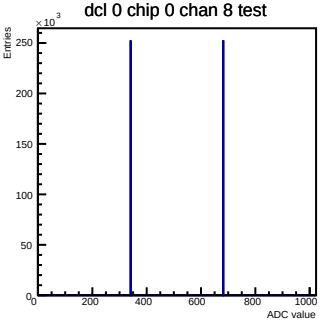

dcl 0 chip 0 chan 3 test
Entries
×10³
250
200
150
100
50
0
0
200
400
600
800
1000
ADC value

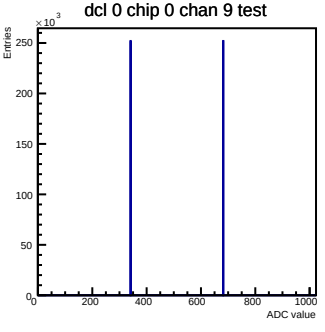

dcl 0 chip 0 chan 4 test
Entries
×10³
250
200
150
100
50
0
0
200
400
600
800
1000
ADC value

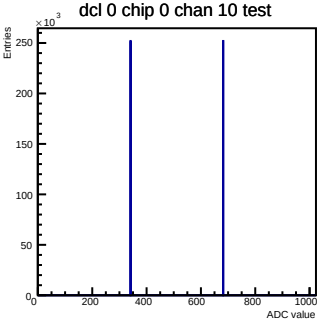

dcl 0 chip 0 chan 5 test
Entries
×10³
250
200
150
100
50
0
0
200
400
600
800
1000
ADC value

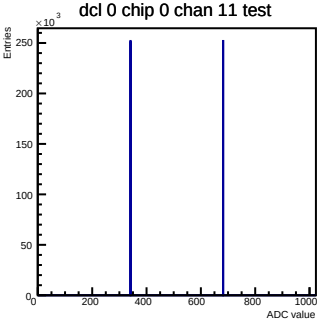

dcl 0 chip 0 chan 6 test
Entries
×10³
250
200
150
100
50
0
0
200
400
600
800
1000
ADC value

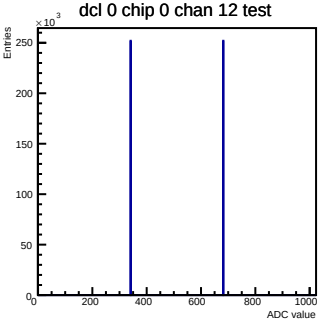

dcl 0 chip 0 chan 7 test
Entries
×10³
250
200
150
100
50
0
0
200
400
600
800
1000
ADC value

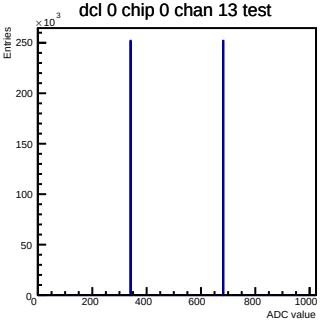

dcl 0 chip 0 chan 8 test
Entries
×10³
250
200
150
100
50
0
0
200
400
600
800
1000
ADC value

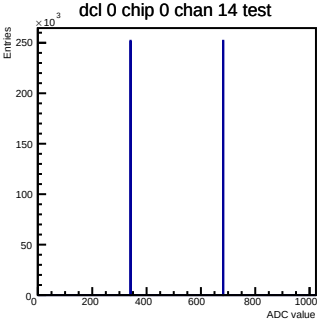

dcl 0 chip 0 chan 9 test
Entries
×10³
250
200
150
100
50
0
0
200
400
600
800
1000
ADC value

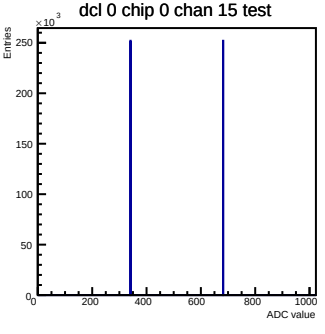

dcl 0 chip 0 chan 10 test
Entries
×10³
250
200
150
100
50
0
0
200
400
600
800
1000
ADC value

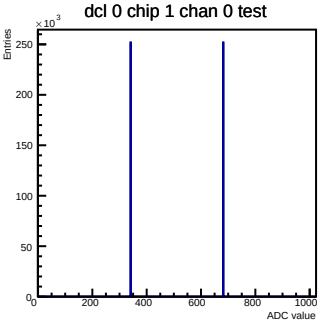

dcl 0 chip 0 chan 11 test
Entries
×10³
250
200
150
100
50
0
0
200
400
600
800
1000
ADC value

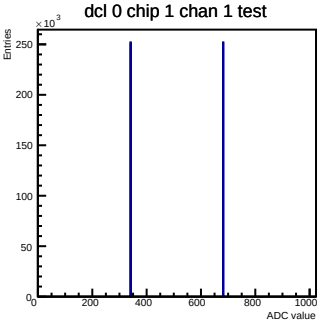

dcl 0 chip 0 chan 12 test
Entries
×10³
250
200
150
100
50
0
0
200
400
600
800
1000
ADC value

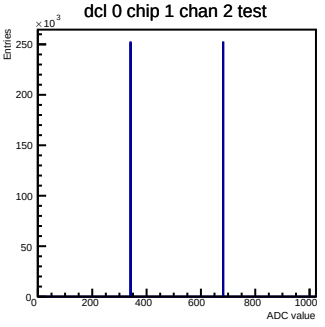

dcl 0 chip 0 chan 13 test
Entries
×10³
250
200
150
100
50
0
0
200
400
600
800
1000
ADC value

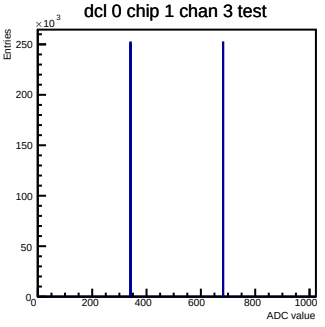

dcl 0 chip 0 chan 14 test
Entries
×10³
250
200
150
100
50
0
0
200
400
600
800
1000
ADC value

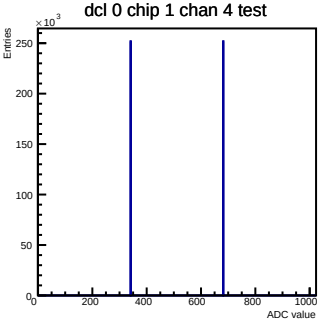

dcl 0 chip 0 chan 15 test
Entries
×10³
250
200
150
100
50
0
0
200
400
600
800
1000
ADC value

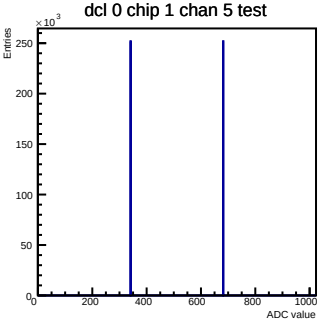

dcl 0 chip 1 chan 0 test
Entries
×10³
250
200
150
100
50
0
0
200
400
600
800
1000
ADC value

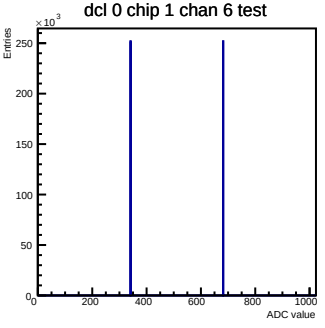

dcl 0 chip 1 chan 1 test
Entries
×10³
250
200
150
100
50
0
0
200
400
600
800
1000
ADC value

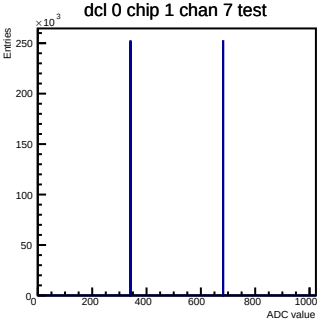

dcl 0 chip 1 chan 2 test
Entries
×10³
250
200
150
100
50
0
0
200
400
600
800
1000
ADC value

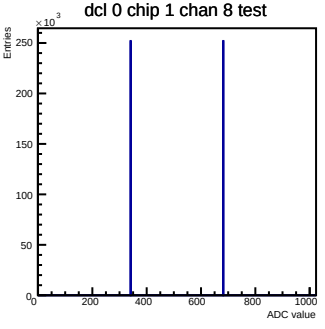

dcl 0 chip 1 chan 3 test
Entries
×10³
250
200
150
100
50
0
0
200
400
600
800
1000
ADC value

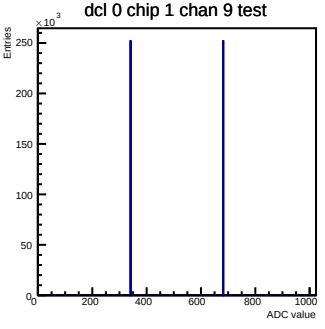

dcl 0 chip 1 chan 4 test
Entries
×10³
250
200
150
100
50
0
0
200
400
600
800
1000
ADC value

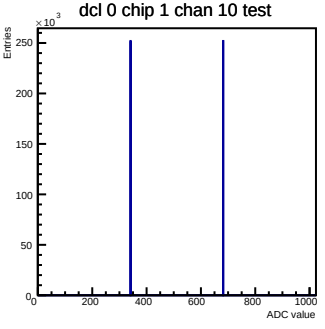

dcl 0 chip 1 chan 5 test
Entries
×10³
250
200
150
100
50
0
0
200
400
600
800
1000
ADC value

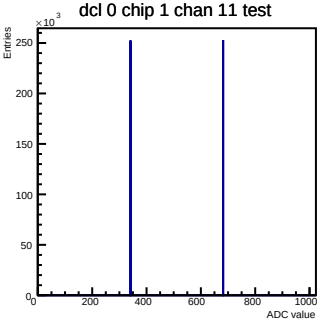

dcl 0 chip 1 chan 6 test
Entries
×10³
250
200
150
100
50
0
0
200
400
600
800
1000
ADC value

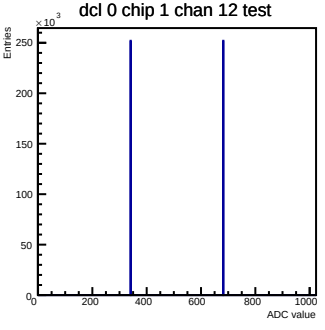

dcl 0 chip 1 chan 7 test
Entries
×10³
250
200
150
100
50
0
0
200
400
600
800
1000
ADC value

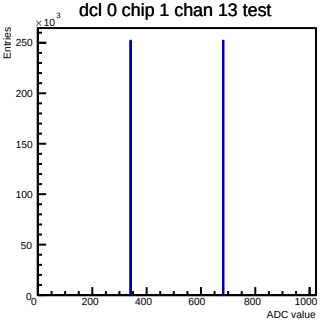

dcl 0 chip 1 chan 8 test
Entries
×10³
250
200
150
100
50
0
0
200
400
600
800
1000
ADC value

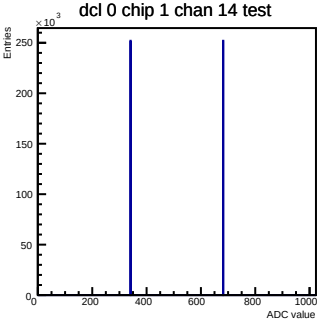

dcl 0 chip 1 chan 9 test
Entries
×10³
250
200
150
100
50
0
0
200
400
600
800
1000
ADC value

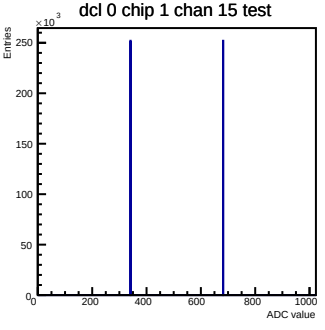

dcl 0 chip 1 chan 10 test
Entries
×10³
250
200
150
100
50
0
0
200
400
600
800
1000
ADC value

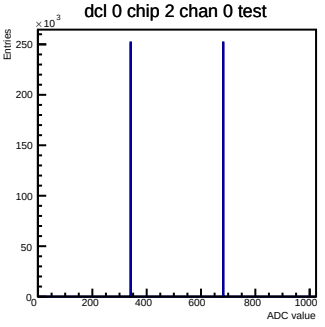

dcl 0 chip 1 chan 11 test
Entries
×10³
250
200
150
100
50
0
0
200
400
600
800
1000
ADC value

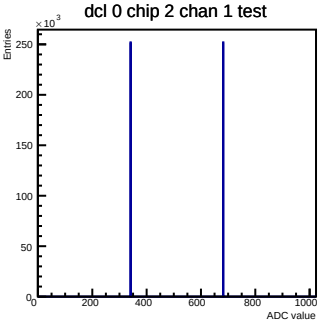

dcl 0 chip 1 chan 12 test
Entries
×10³
250
200
150
100
50
0
0
200
400
600
800
1000
ADC value

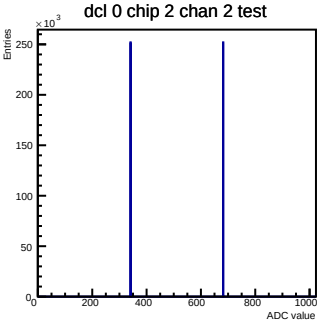

dcl 0 chip 1 chan 13 test
Entries
×10³
250
200
150
100
50
0
0
200
400
600
800
1000
ADC value

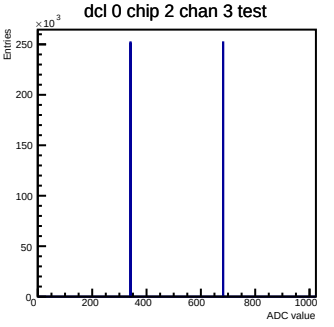

dcl 0 chip 1 chan 14 test
Entries
×10³
250
200
150
100
50
0
0
200
400
600
800
1000
ADC value

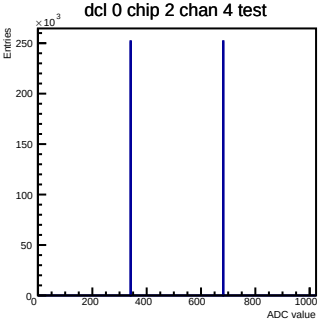

dcl 0 chip 1 chan 15 test
Entries
×10³
250
200
150
100
50
0
0
200
400
600
800
1000
ADC value

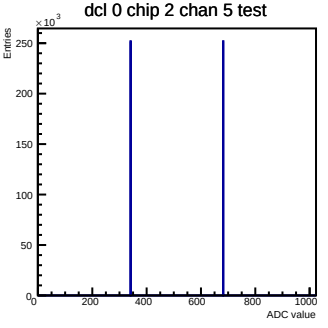

dcl 0 chip 2 chan 0 test
Entries
×10³
ADC value

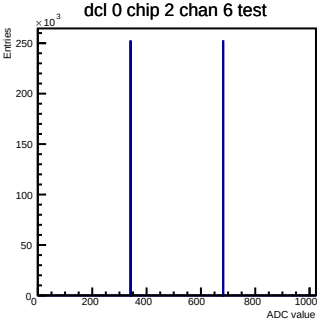

dcl 0 chip 2 chan 1 test
Entries
×10³
ADC value

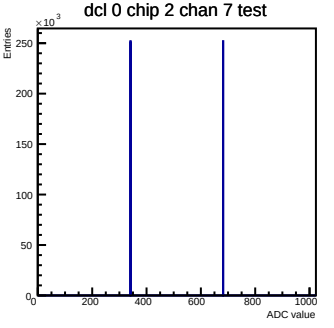

dcl 0 chip 2 chan 2 test
Entries
×10³
ADC value

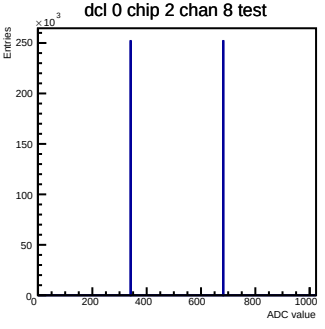

dcl 0 chip 2 chan 3 test
Entries
×10³
ADC value

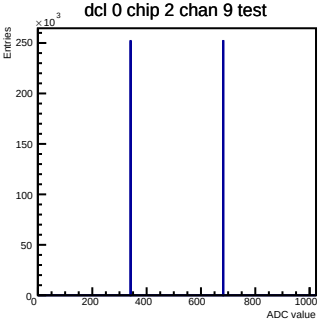

dcl 0 chip 2 chan 4 test
Entries
×10³
ADC value

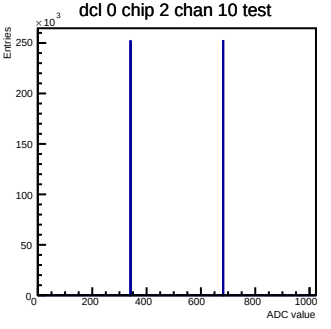

dcl 0 chip 2 chan 5 test
Entries
×10³
ADC value

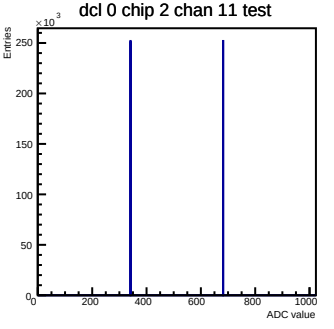

dcl 0 chip 2 chan 6 test
Entries
×10³
ADC value

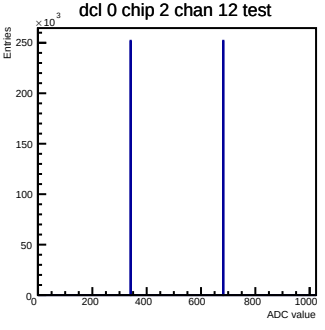

dcl 0 chip 2 chan 7 test
Entries
×10³
ADC value

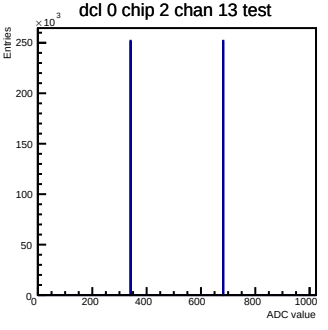

dcl 0 chip 2 chan 8 test
Entries
×10³
ADC value

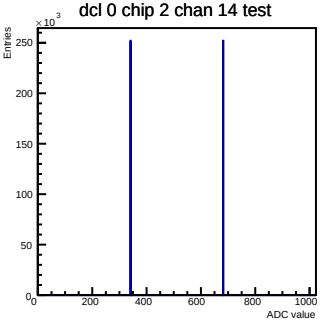

dcl 0 chip 2 chan 9 test
Entries
×10³
ADC value

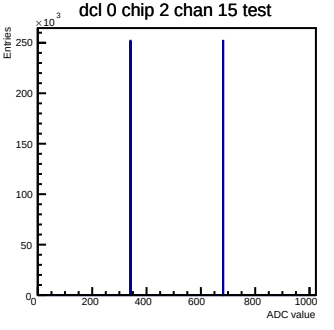

dcl 0 chip 2 chan 10 test
Entries
×10³
ADC value

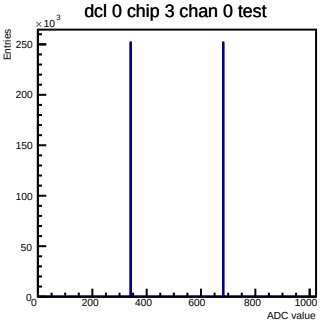

dcl 0 chip 2 chan 11 test
Entries
×10³
ADC value

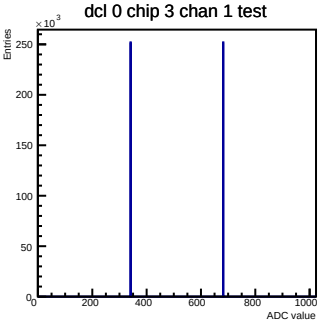

dcl 0 chip 2 chan 12 test
Entries
×10³
ADC value

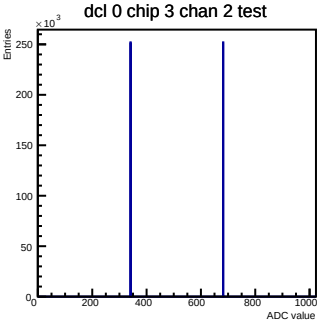

dcl 0 chip 2 chan 13 test
Entries
×10³
ADC value

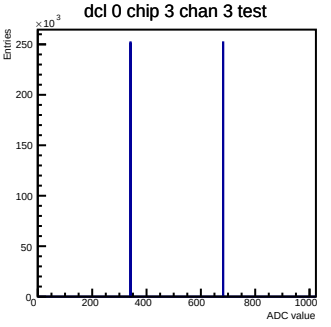

dcl 0 chip 2 chan 14 test
Entries
×10³
ADC value

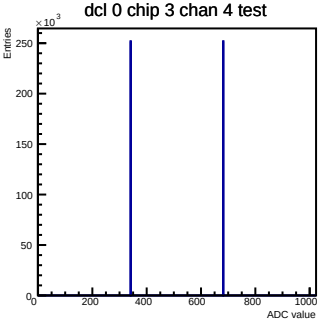

dcl 0 chip 2 chan 15 test
Entries
×10³
ADC value

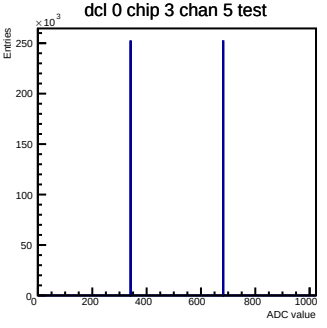

dcl 0 chip 3 chan 0 test
Entries
×10³
250
200
150
100
50
0
0
200
400
600
800
1000
ADC value

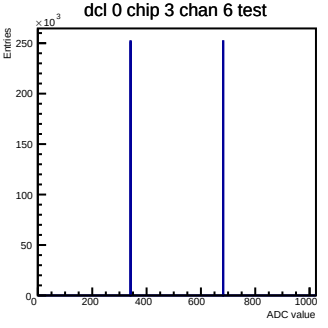

dcl 0 chip 3 chan 1 test
Entries
×10³
250
200
150
100
50
0
0
200
400
600
800
1000
ADC value

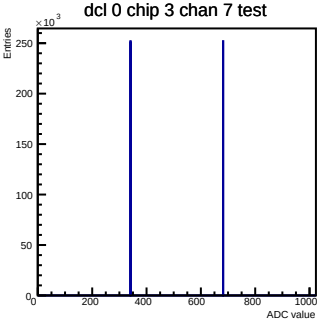

dcl 0 chip 3 chan 2 test
Entries
×10³
250
200
150
100
50
0
0
200
400
600
800
1000
ADC value

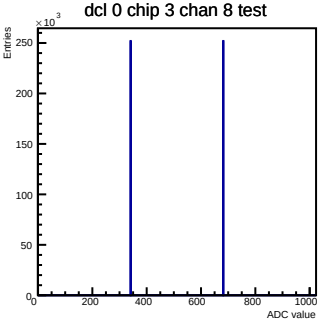

dcl 0 chip 3 chan 3 test
Entries
×10³
250
200
150
100
50
0
0
200
400
600
800
1000
ADC value

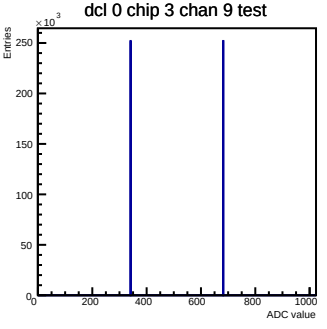

dcl 0 chip 3 chan 4 test
Entries
×10³
250
200
150
100
50
0
0
200
400
600
800
1000
ADC value

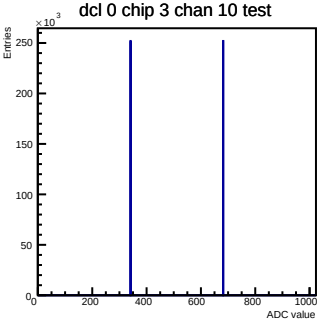

dcl 0 chip 3 chan 5 test
Entries
×10³
250
200
150
100
50
0
0
200
400
600
800
1000
ADC value

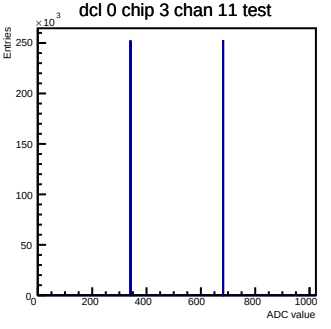

dcl 0 chip 3 chan 6 test
Entries
×10³
250
200
150
100
50
0
0
200
400
600
800
1000
ADC value

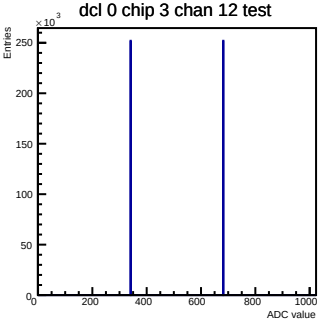

dcl 0 chip 3 chan 7 test
Entries
×10³
250
200
150
100
50
0
0
200
400
600
800
1000
ADC value

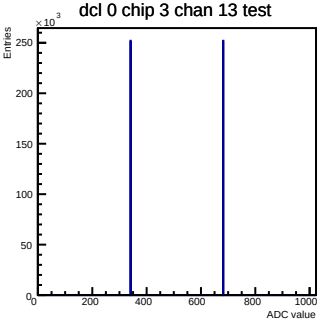

dcl 0 chip 3 chan 8 test
Entries
×10³
250
200
150
100
50
0
0
200
400
600
800
1000
ADC value

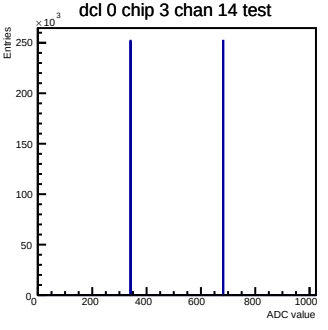

dcl 0 chip 3 chan 9 test
Entries
×10³
250
200
150
100
50
0
0
200
400
600
800
1000
ADC value

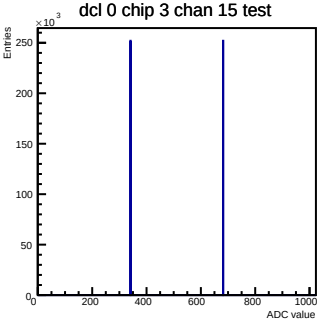

dcl 0 chip 3 chan 10 test
Entries
×10³
250
200
150
100
50
0
0
200
400
600
800
1000
ADC value

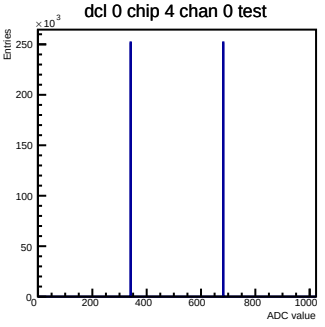

dcl 0 chip 3 chan 11 test
Entries
×10³
250
200
150
100
50
0
0
200
400
600
800
1000
ADC value

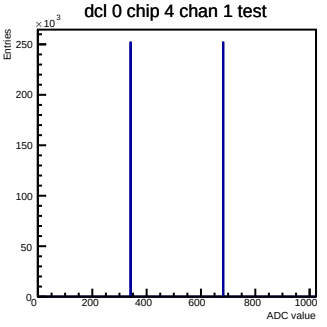

dcl 0 chip 3 chan 12 test
Entries
×10³
250
200
150
100
50
0
0
200
400
600
800
1000
ADC value

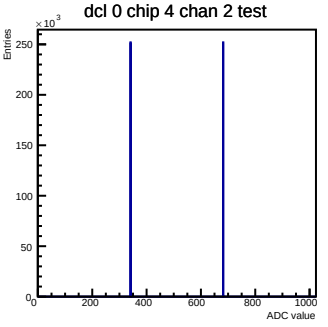

dcl 0 chip 3 chan 13 test
Entries
×10³
250
200
150
100
50
0
0
200
400
600
800
1000
ADC value

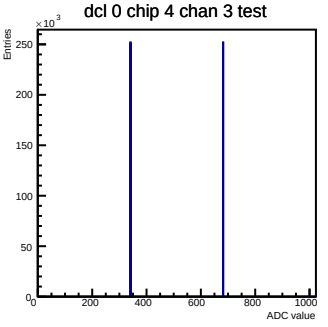

dcl 0 chip 3 chan 14 test
Entries
×10³
250
200
150
100
50
0
0
200
400
600
800
1000
ADC value

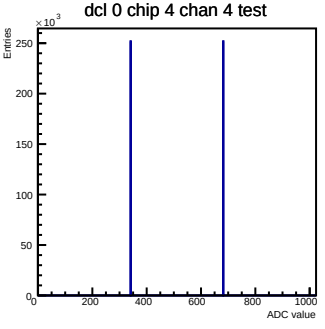

dcl 0 chip 3 chan 15 test
Entries
×10³
250
200
150
100
50
0
0
200
400
600
800
1000
ADC value

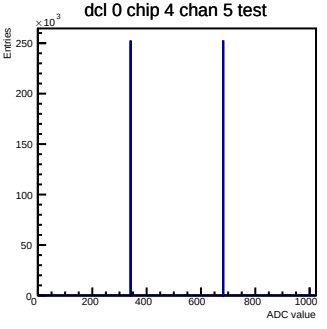

dcl 0 chip 4 chan 0 test
Entries
×10³
ADC value

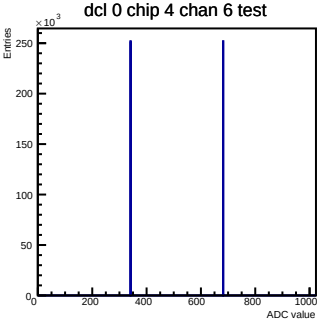

dcl 0 chip 4 chan 1 test
Entries
×10³
ADC value

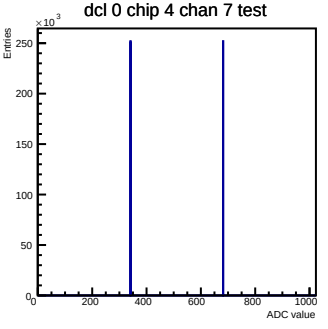

dcl 0 chip 4 chan 2 test
Entries
×10³
ADC value

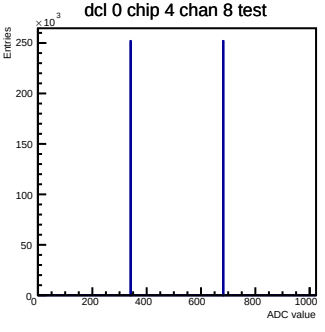

dcl 0 chip 4 chan 3 test
Entries
×10³
ADC value

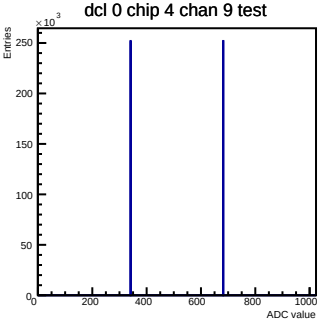

dcl 0 chip 4 chan 4 test
Entries
×10³
ADC value

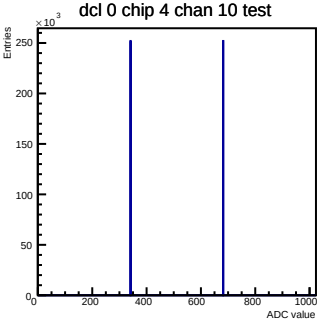

dcl 0 chip 4 chan 5 test
Entries
×10³
ADC value

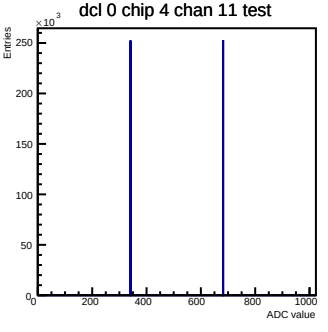

dcl 0 chip 4 chan 6 test
Entries
×10³
ADC value

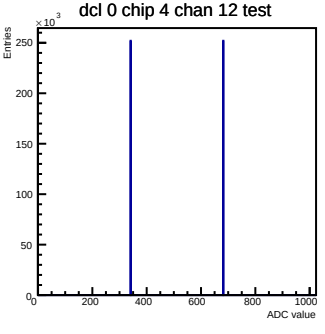

dcl 0 chip 4 chan 7 test
Entries
×10³
ADC value

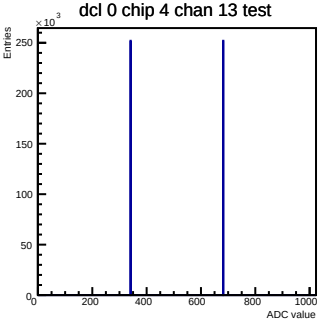

dcl 0 chip 4 chan 8 test
Entries
×10³
ADC value

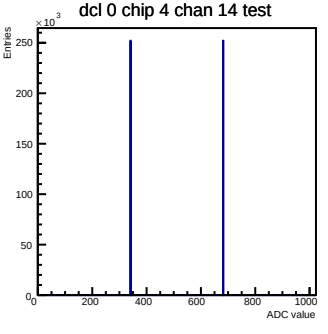

dcl 0 chip 4 chan 9 test
Entries
×10³
ADC value

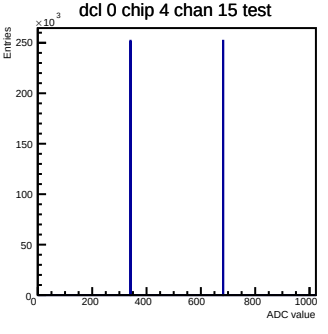

dcl 0 chip 4 chan 10 test
Entries
×10³
ADC value

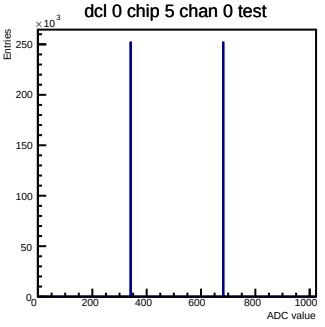

dcl 0 chip 4 chan 11 test
Entries
×10³
ADC value

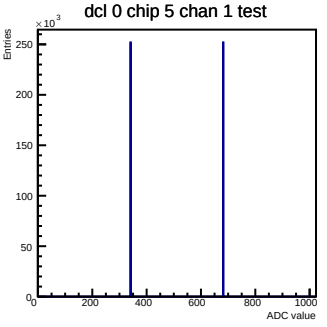

dcl 0 chip 4 chan 12 test
Entries
×10³
ADC value

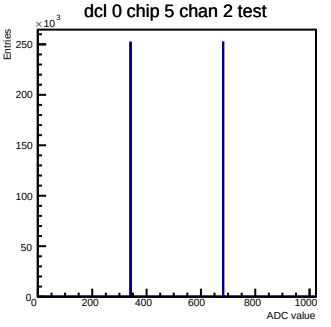

dcl 0 chip 4 chan 13 test
Entries
×10³
ADC value

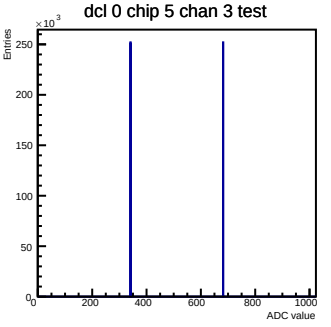

dcl 0 chip 4 chan 14 test
Entries
×10³
ADC value

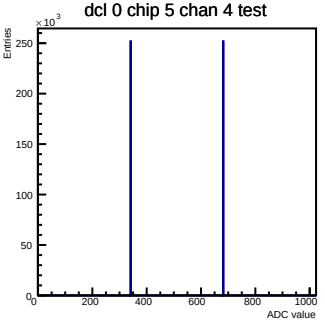

dcl 0 chip 4 chan 15 test
Entries
×10³
ADC value

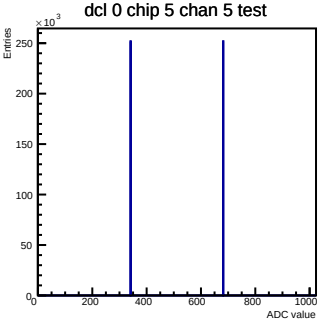

dcl 0 chip 5 chan 0 test
Entries
×10³
ADC value

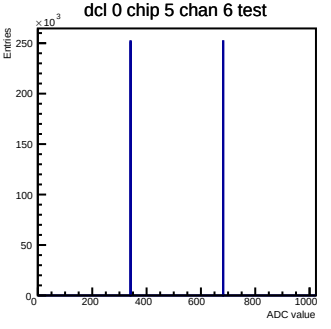

dcl 0 chip 5 chan 1 test
Entries
×10³
ADC value

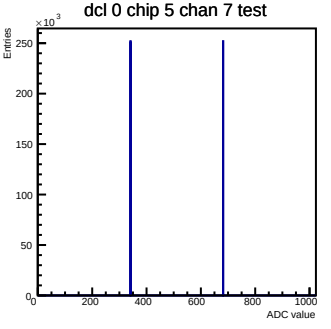

dcl 0 chip 5 chan 2 test
Entries
×10³
ADC value

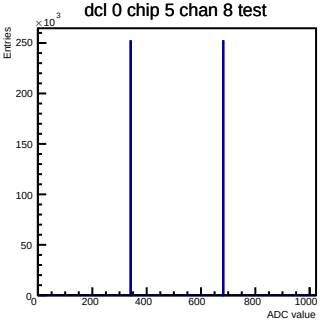

dcl 0 chip 5 chan 3 test
Entries
×10³
ADC value

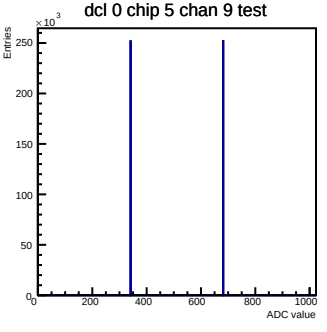

dcl 0 chip 5 chan 4 test
Entries
×10³
ADC value

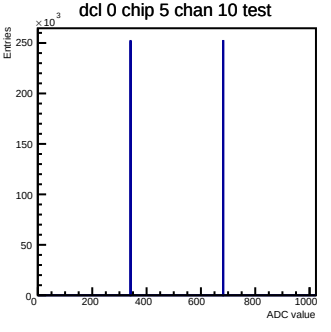

dcl 0 chip 5 chan 5 test
Entries
×10³
ADC value

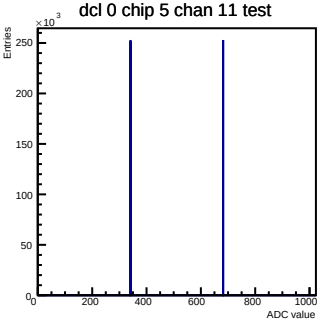

dcl 0 chip 5 chan 6 test
Entries
×10³
ADC value

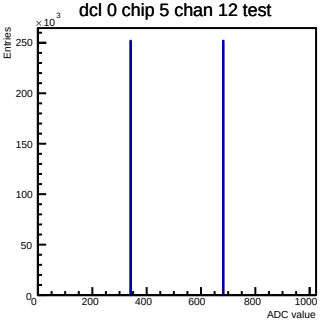

dcl 0 chip 5 chan 7 test
Entries
×10³
ADC value

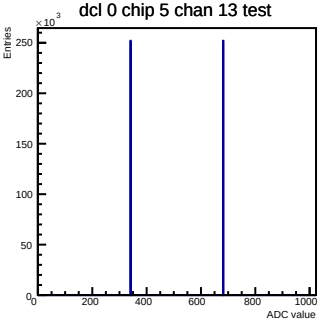

dcl 0 chip 5 chan 8 test
Entries
×10³
ADC value

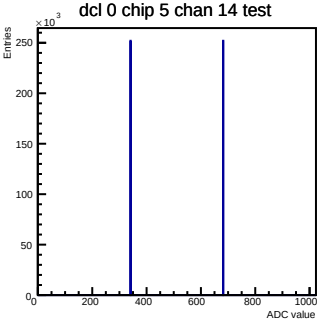

dcl 0 chip 5 chan 9 test
Entries
×10³
ADC value

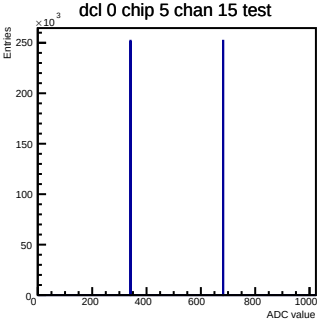

dcl 0 chip 5 chan 10 test
Entries
×10³
ADC value

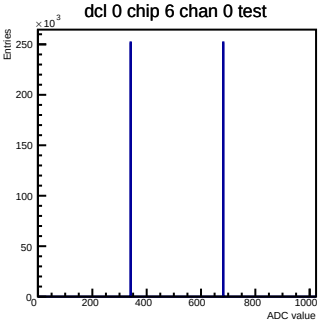

dcl 0 chip 5 chan 11 test
Entries
×10³
ADC value

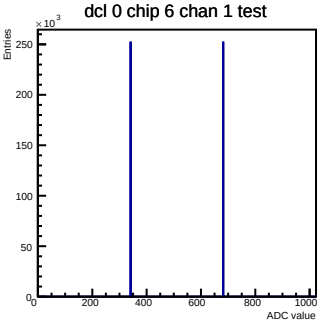

dcl 0 chip 5 chan 12 test
Entries
×10³
ADC value

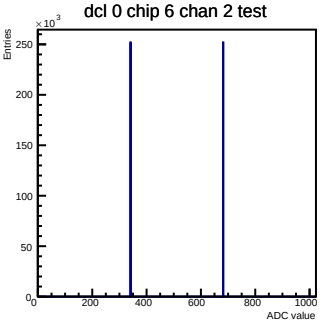

dcl 0 chip 5 chan 13 test
Entries
×10³
ADC value

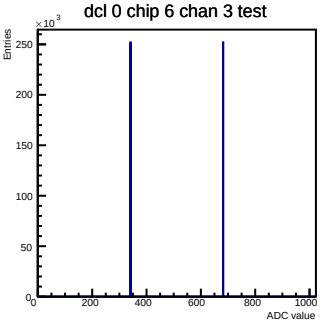

dcl 0 chip 5 chan 14 test
Entries
×10³
ADC value

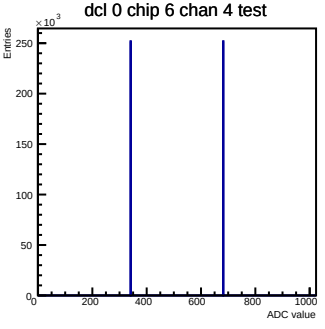

dcl 0 chip 5 chan 15 test
Entries
×10³
ADC value

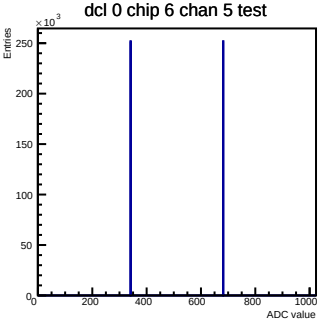

dcl 0 chip 6 chan 0 test
Entries
×10³
ADC value

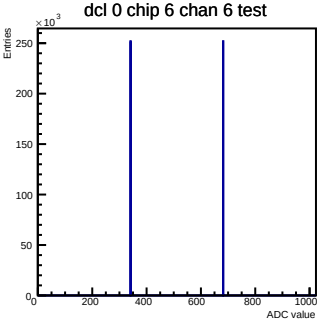

dcl 0 chip 6 chan 1 test
Entries
×10³
ADC value

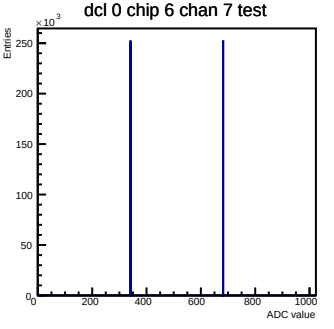

dcl 0 chip 6 chan 2 test
Entries
×10³
ADC value

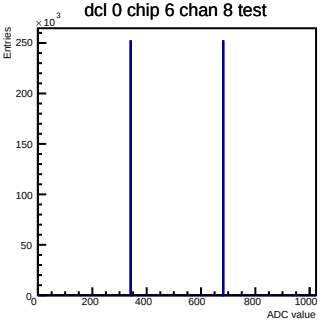

dcl 0 chip 6 chan 3 test
Entries
×10³
ADC value

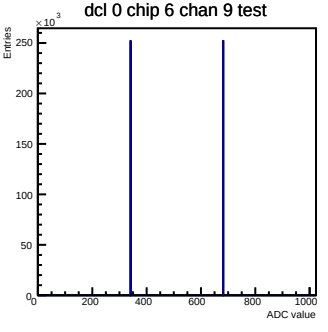

dcl 0 chip 6 chan 4 test
Entries
×10³
ADC value

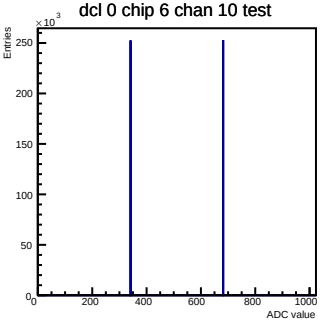

dcl 0 chip 6 chan 5 test
Entries
×10³
ADC value

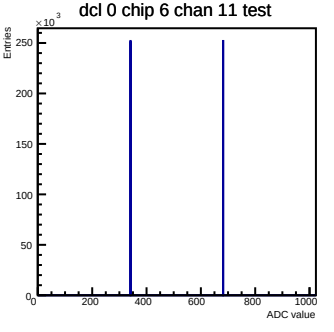

dcl 0 chip 6 chan 6 test
Entries
×10³
ADC value

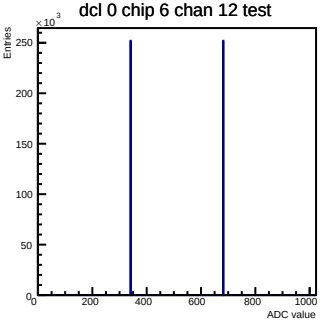

dcl 0 chip 6 chan 7 test
Entries
×10³
ADC value

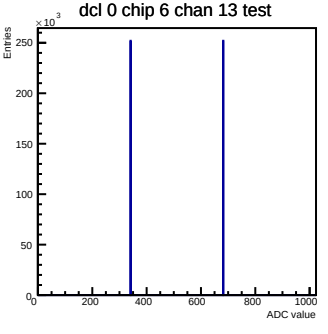

dcl 0 chip 6 chan 8 test
Entries
×10³
ADC value

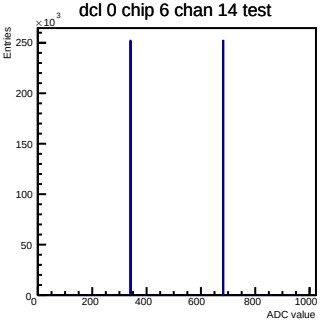

dcl 0 chip 6 chan 9 test
Entries
×10³
ADC value

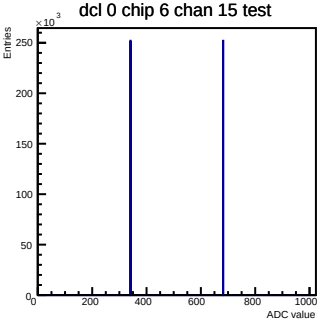

dcl 0 chip 6 chan 10 test
Entries
×10³
ADC value

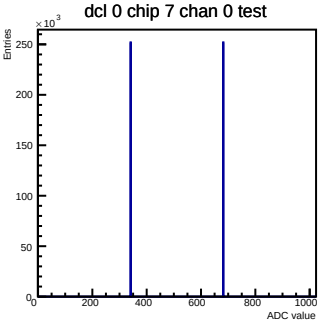

dcl 0 chip 6 chan 11 test
Entries
×10³
ADC value

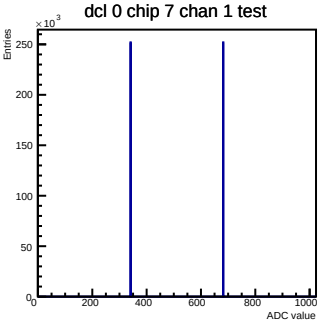

dcl 0 chip 6 chan 12 test
Entries
×10³
ADC value

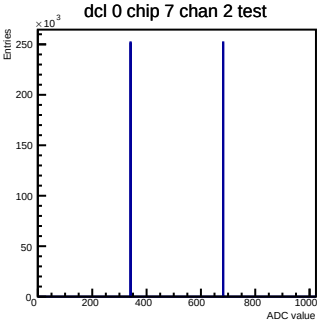

dcl 0 chip 6 chan 13 test
Entries
×10³
ADC value

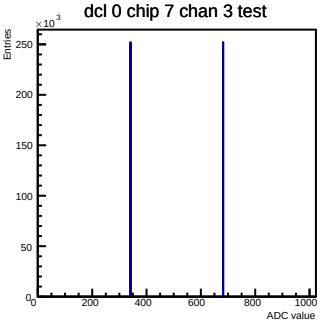

dcl 0 chip 6 chan 14 test
Entries
×10³
ADC value

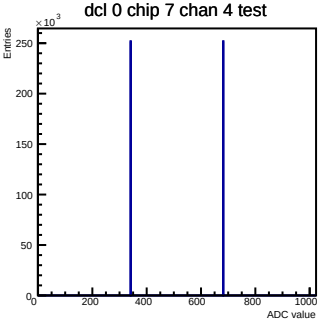

dcl 0 chip 6 chan 15 test
Entries
×10³
ADC value

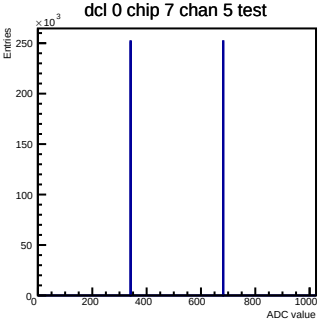

dcl 0 chip 7 chan 0 test
Entries
×10³
ADC value

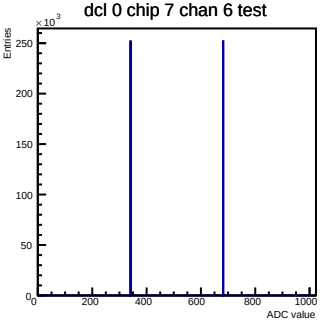

dcl 0 chip 7 chan 1 test
Entries
×10³
ADC value

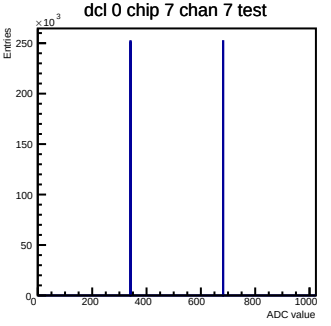

dcl 0 chip 7 chan 2 test
Entries
×10³
ADC value

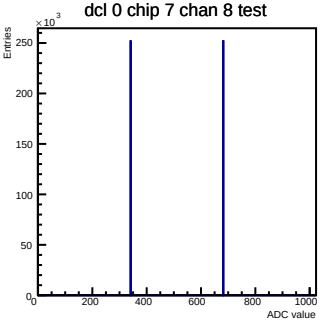

dcl 0 chip 7 chan 3 test
Entries
×10³
ADC value

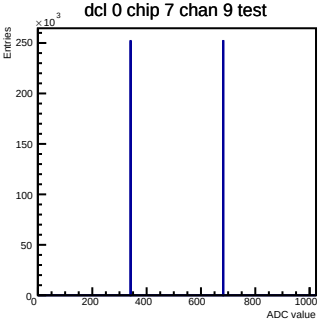

dcl 0 chip 7 chan 4 test
Entries
×10³
ADC value

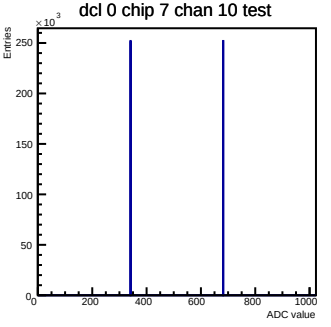

dcl 0 chip 7 chan 5 test
Entries
×10³
ADC value

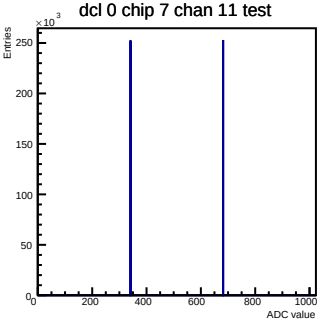

dcl 0 chip 7 chan 6 test
Entries
×10³
ADC value

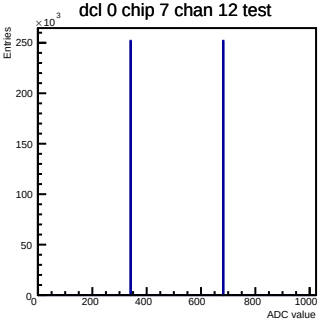

dcl 0 chip 7 chan 7 test
Entries
×10³
ADC value

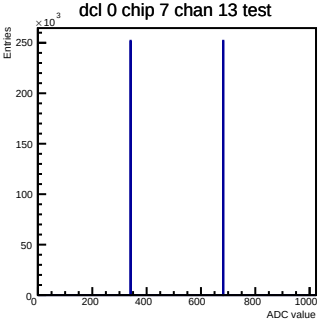

dcl 0 chip 7 chan 8 test
Entries
×10³
ADC value

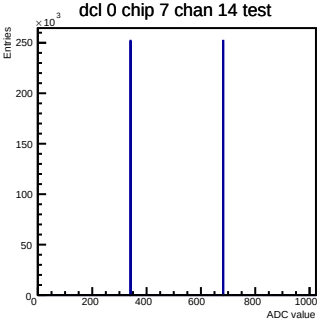

dcl 0 chip 7 chan 9 test
Entries
×10³
ADC value

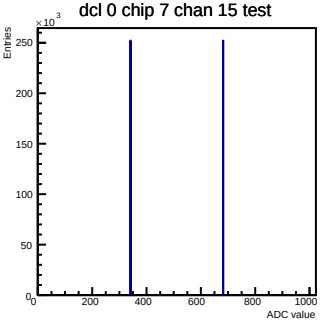

dcl 0 chip 7 chan 10 test
Entries
×10³
ADC value


dcl 0 chip 7 chan 11 test
Entries
×10³
ADC value


dcl 0 chip 7 chan 12 test
Entries
×10³
ADC value


dcl 0 chip 7 chan 13 test
Entries
×10³
ADC value


dcl 0 chip 7 chan 14 test
Entries
×10³
ADC value


dcl 0 chip 7 chan 15 test
Entries
×10³
ADC value