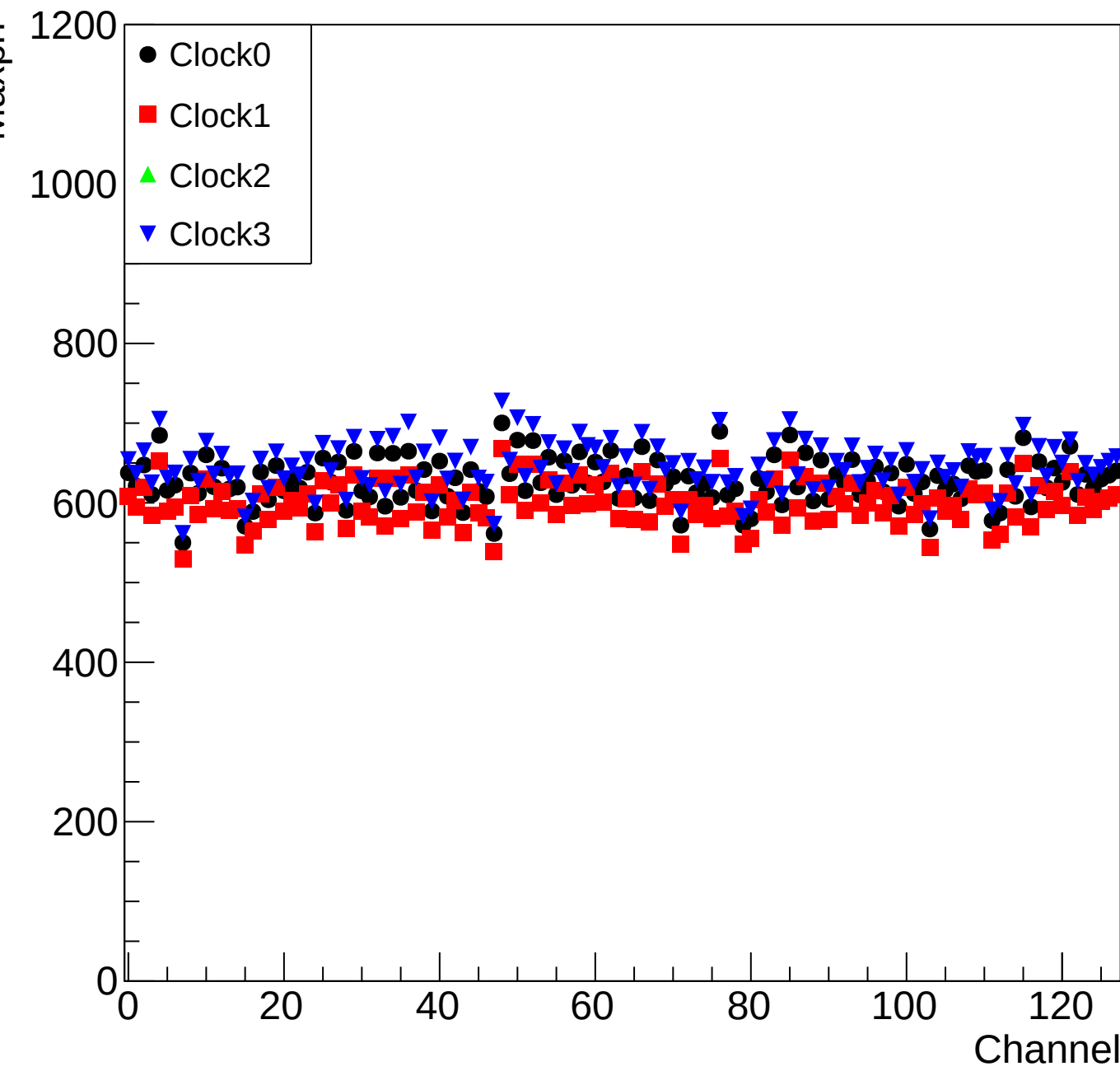


Maxph clocks 0-3



Maxph all clocks 0-3

Entries

14

12

10

8

6

4

2

0

— Clock0

— Clock1

— Clock2

— Clock3

Entries 128

Mean 627

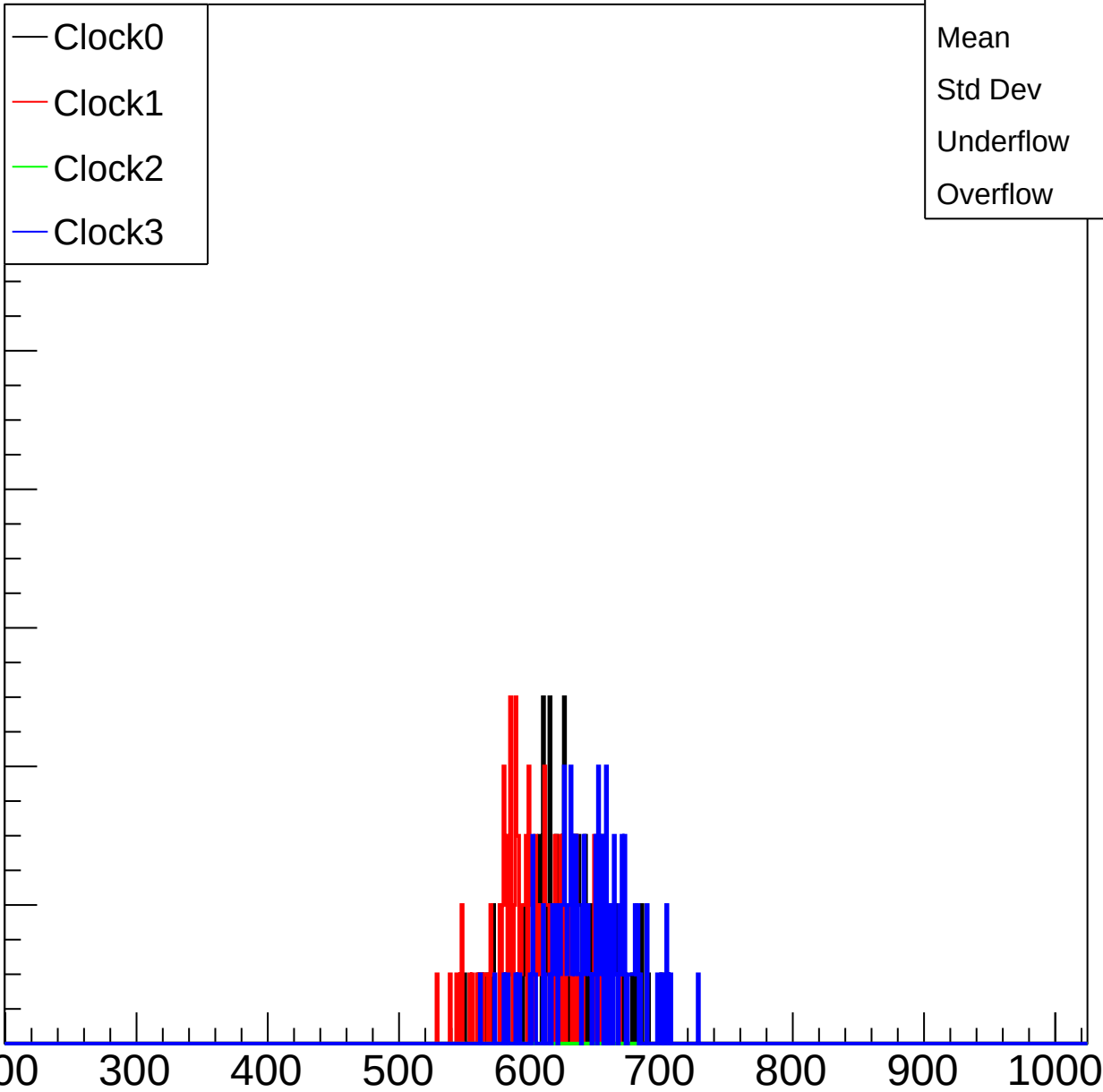
Std Dev 28.25

Underflow 0

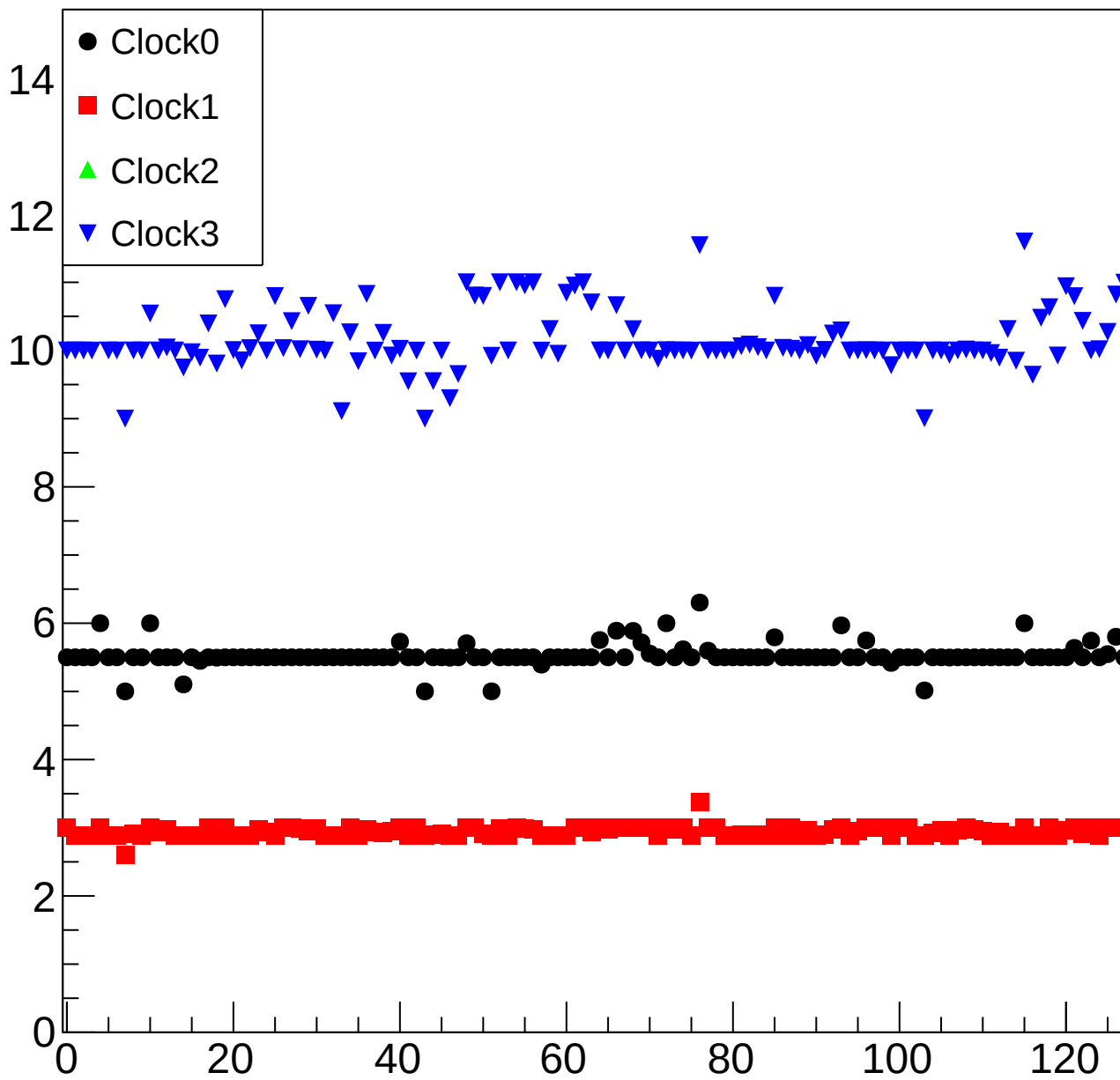
Overflow 0

200 300 400 500 600 700 800 900 1000

ADC



Clocks width 0-3



Clocks width all 0-3

