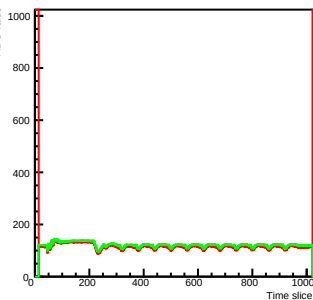
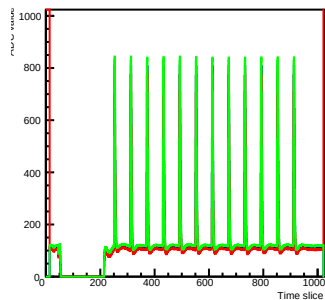


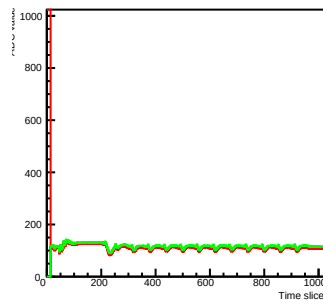
Time mcm 0 chip 0 chan 0 test1



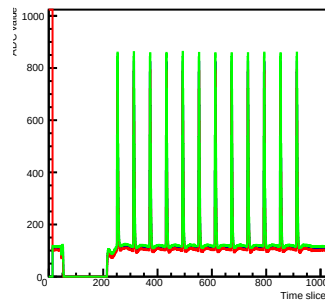
Time mcm 0 chip 0 chan 1 test1



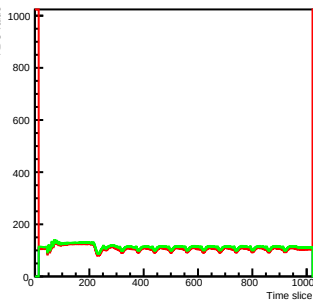
Time mcm 0 chip 0 chan 2 test1



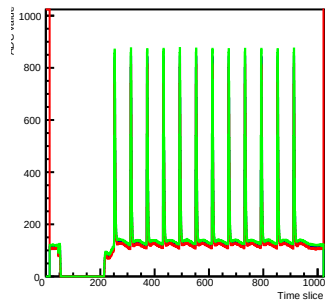
Time mcm 0 chip 0 chan 3 test1



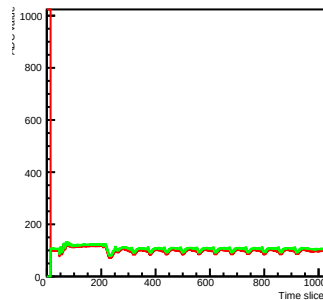
Time mcm 0 chip 0 chan 4 test1



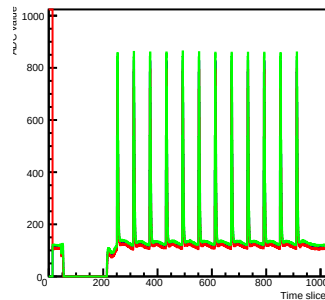
Time mcm 0 chip 0 chan 5 test1



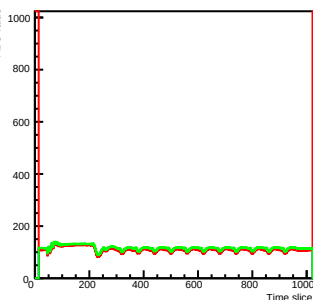
Time mcm 0 chip 0 chan 6 test1



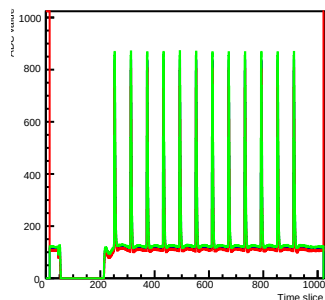
Time mcm 0 chip 0 chan 7 test1



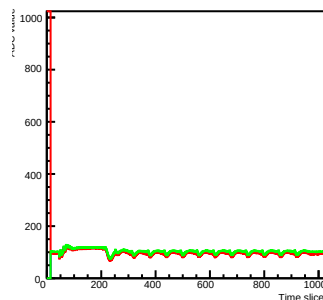
Time mcm 0 chip 0 chan 8 test1



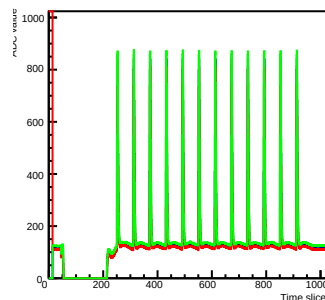
Time mcm 0 chip 0 chan 9 test1



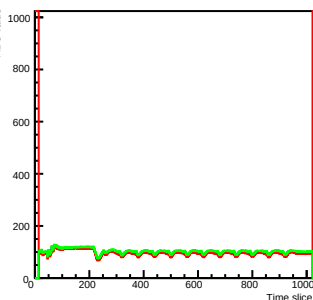
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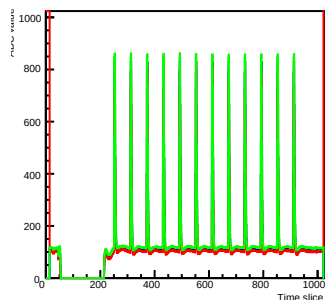
Time mcm 0 chip 0 chan 11 test1



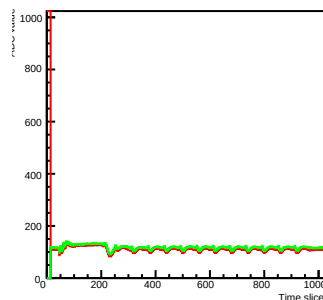
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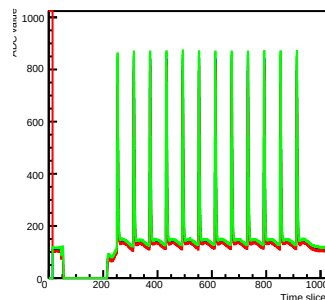
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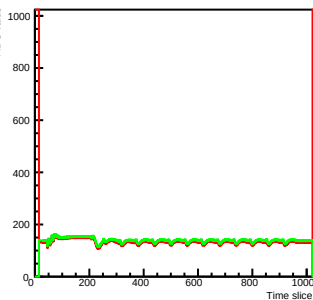
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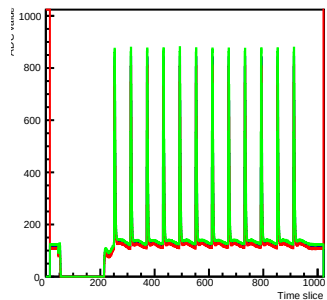
Time mcm 0 chip 0 chan 15 test1



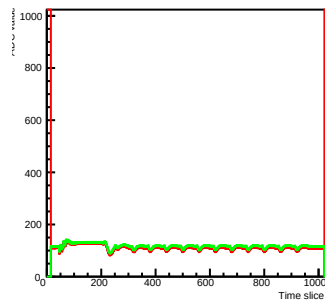
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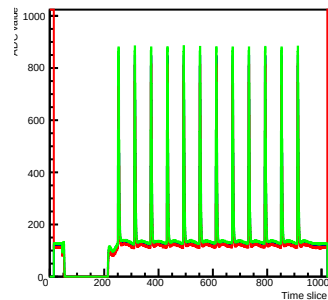
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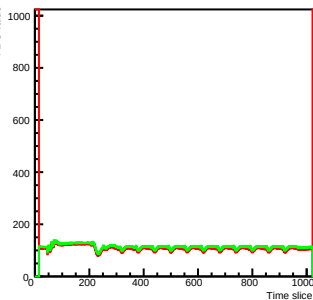
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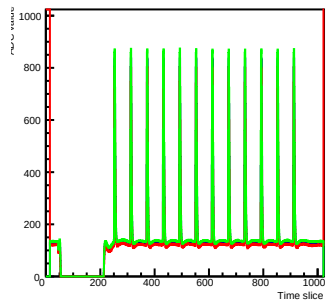
Time mcm 0 chip 1 chan 3 test1



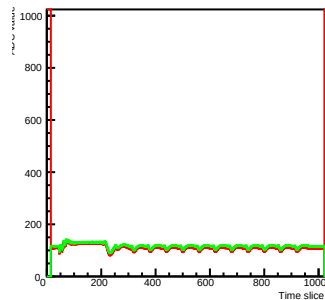
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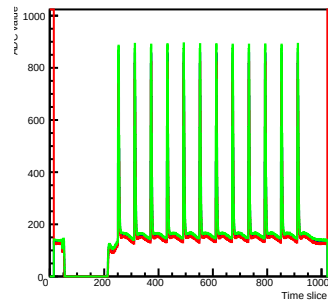
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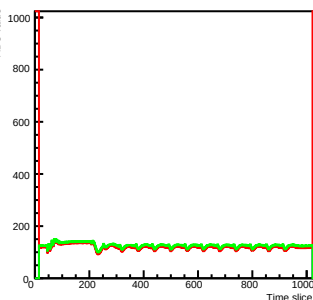
Time mcm 0 chip 1 chan 6 test1



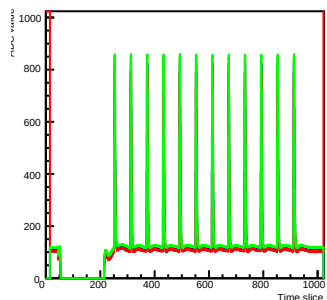
Time mcm 0 chip 1 chan 7 test1



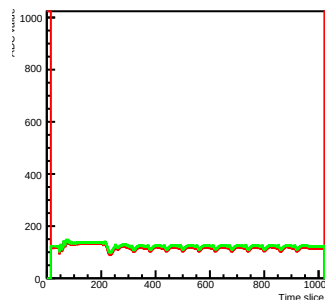
Time mcm 0 chip 1 chan 8 test1



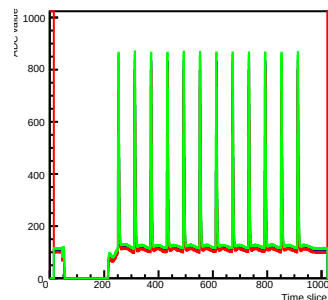
Time mcm 0 chip 1 chan 9 test1



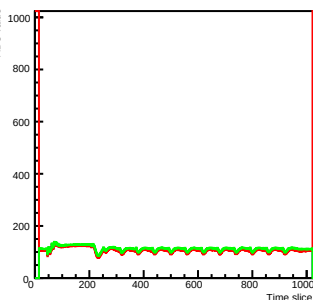
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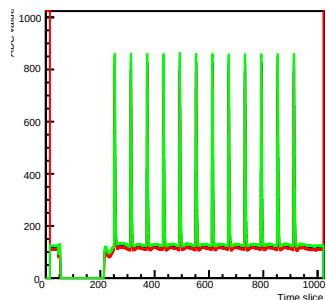
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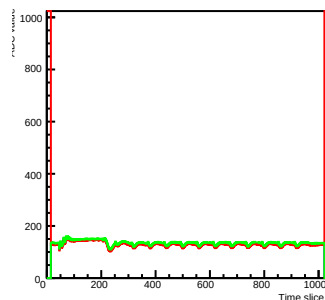
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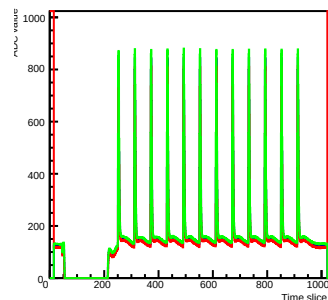
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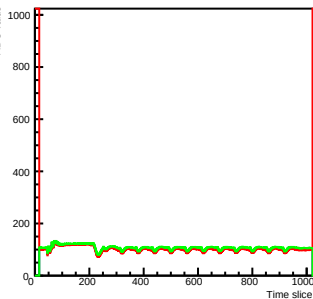
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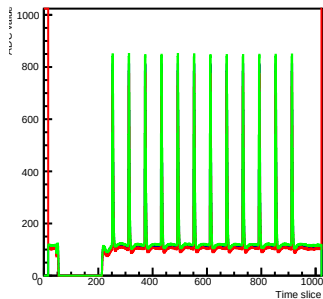
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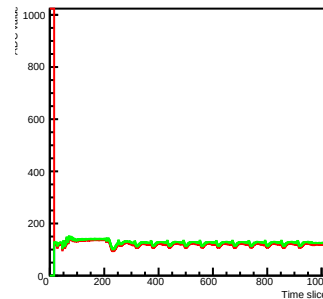
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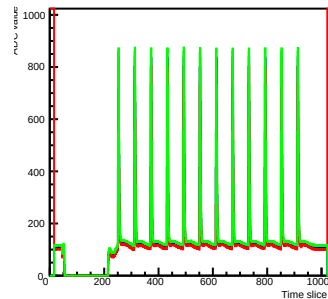
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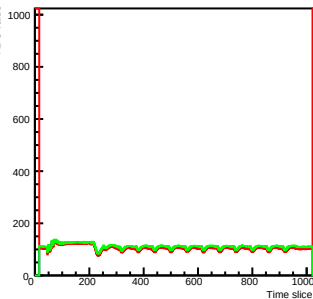
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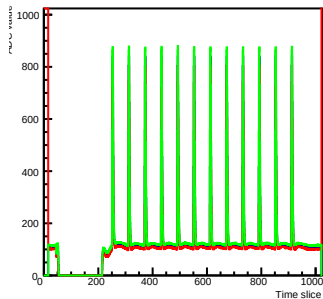
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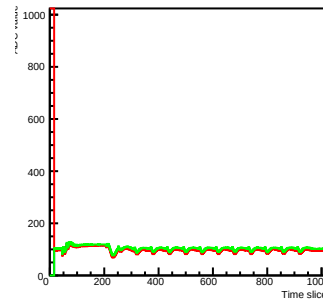
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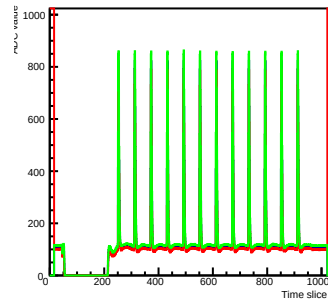
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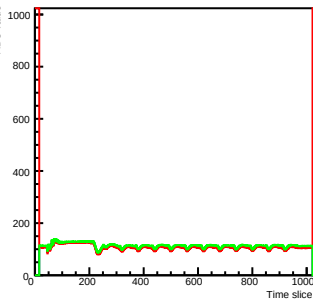
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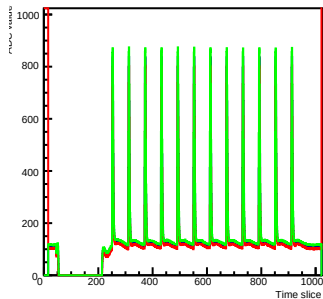
Time mcm 0 chip 2 chan 7 test1



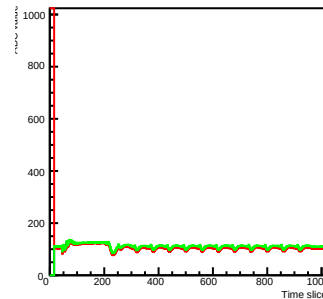
Time mcm 0 chip 2 chan 8 test1



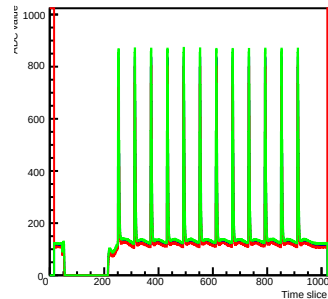
Time mcm 0 chip 2 chan 9 test1



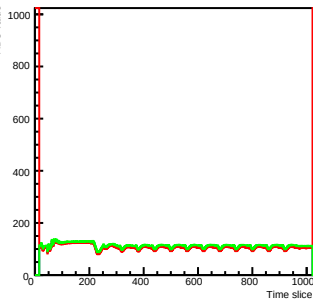
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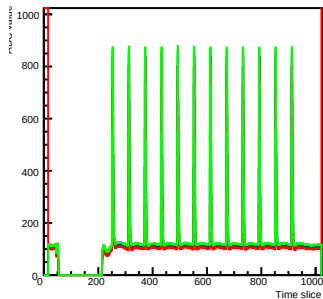
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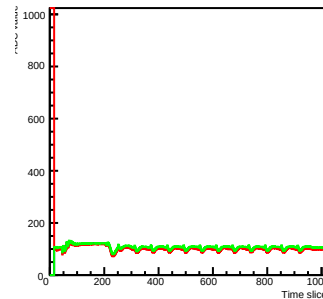
Time mcm 0 chip 2 chan 12 test1



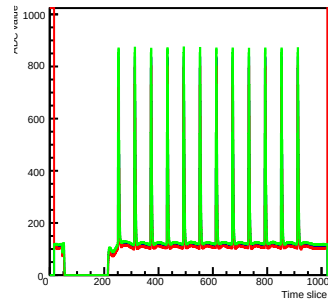
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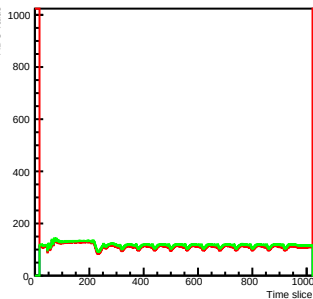
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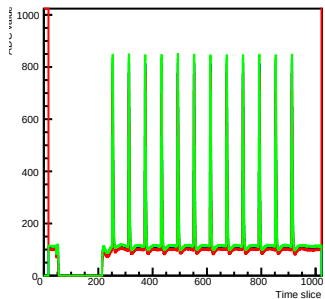
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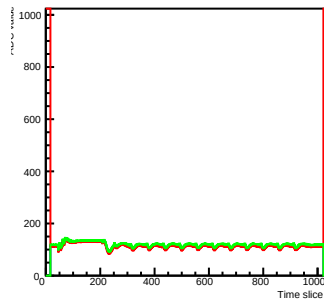
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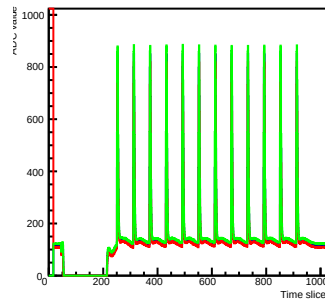
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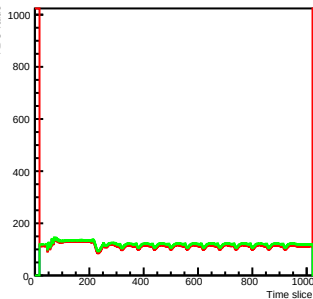
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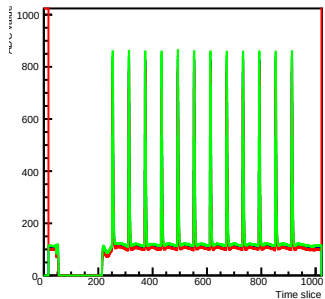
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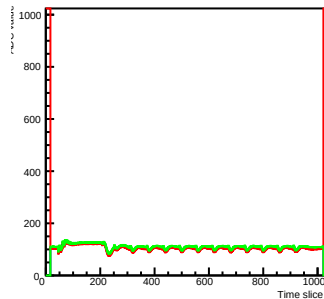
Time mcm 0 chip 3 chan 4 test1



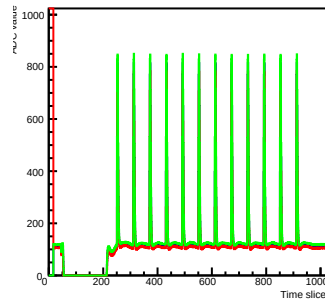
Time mcm 0 chip 3 chan 5 test1



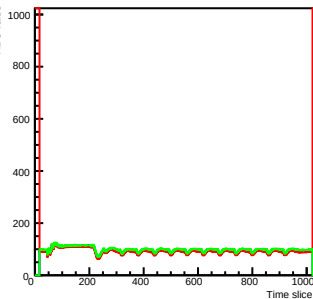
Time mcm 0 chip 3 chan 6 test1



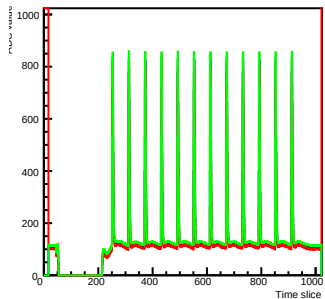
Time mcm 0 chip 3 chan 7 test1



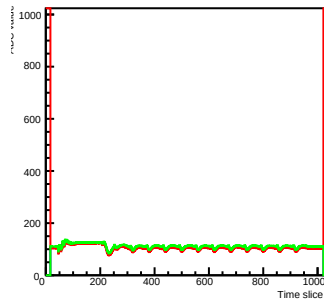
Time mcm 0 chip 3 chan 8 test1



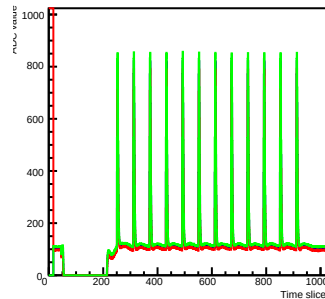
Time mcm 0 chip 3 chan 9 test1



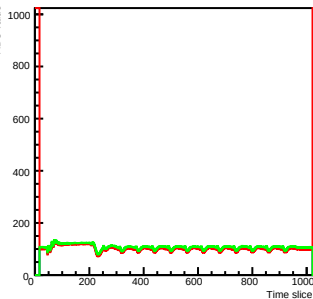
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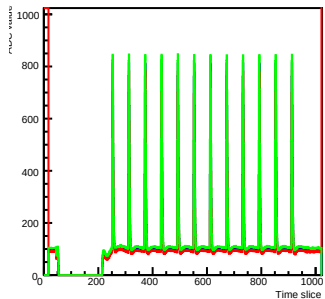
Time mcm 0 chip 3 chan 11 test1



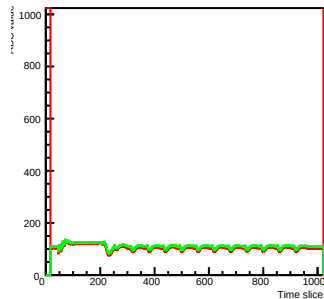
Time mcm 0 chip 3 chan 12 test1



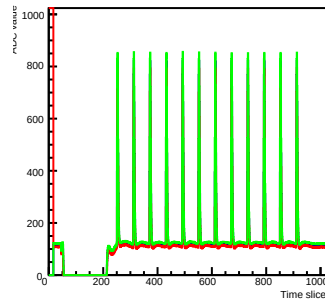
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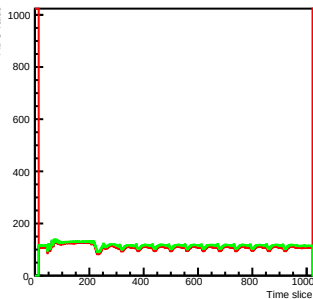
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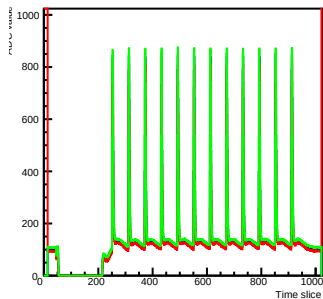
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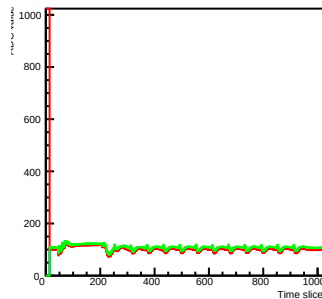
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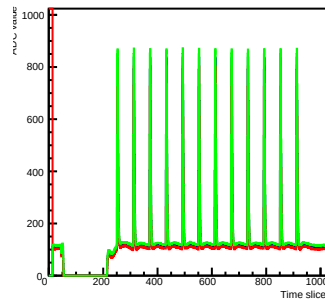
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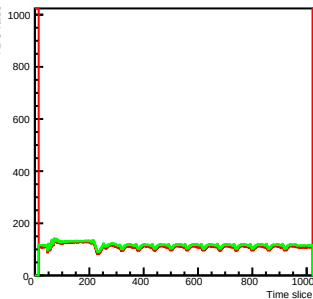
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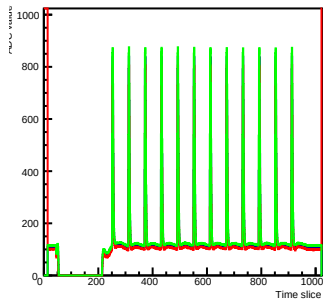
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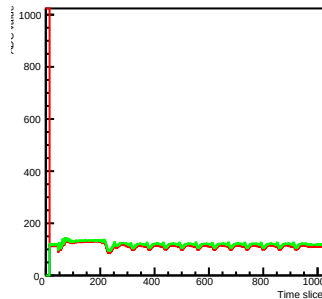
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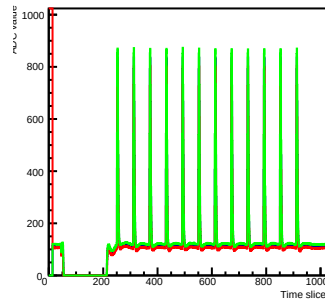
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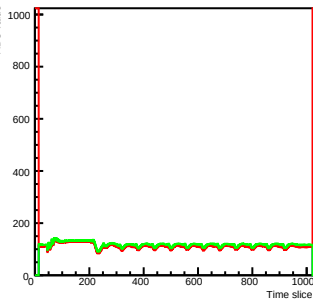
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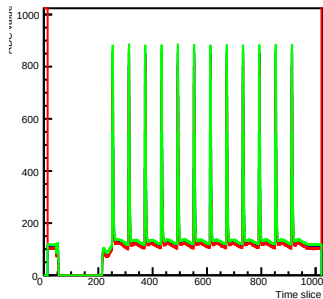
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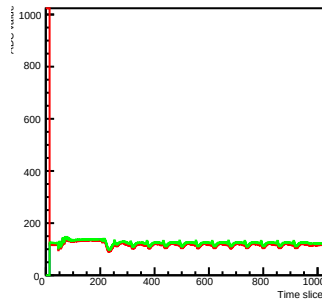
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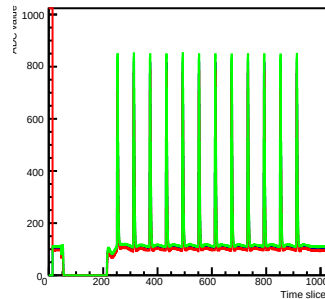
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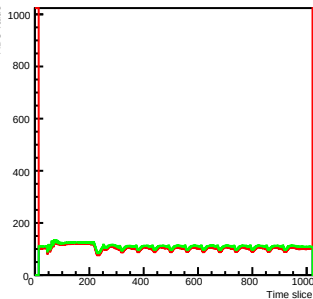
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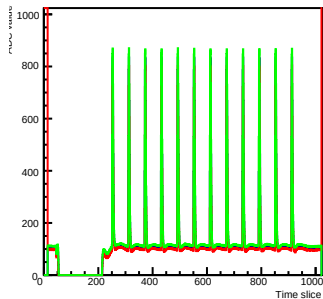
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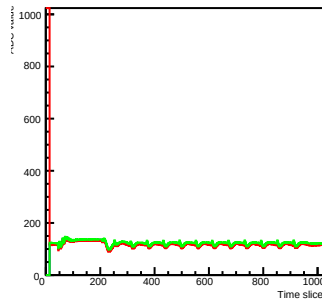
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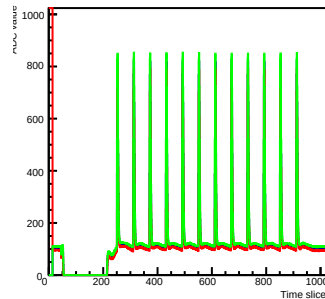
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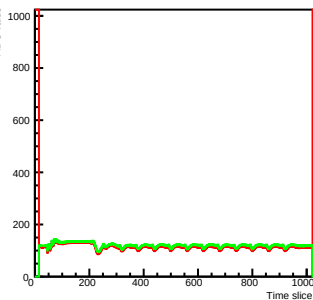
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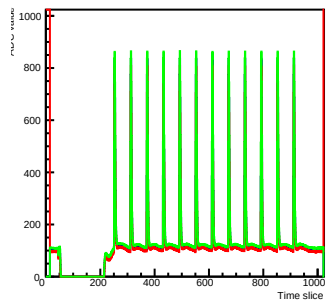
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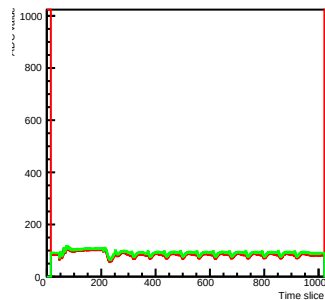
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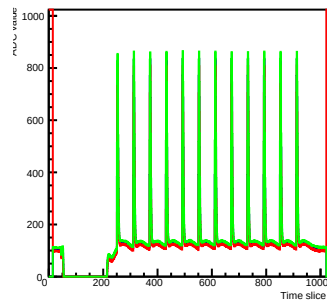
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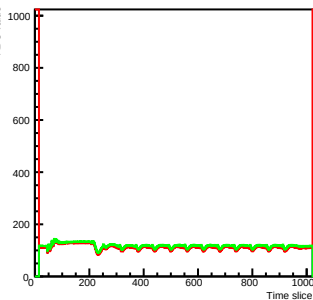
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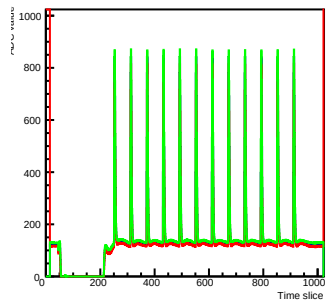
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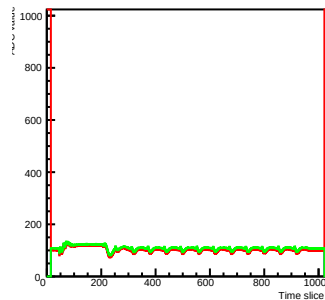
Time mcm 0 chip 5 chan 4 test1



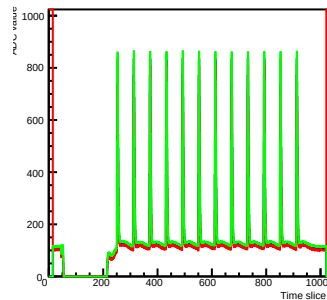
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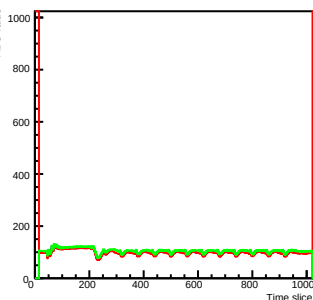
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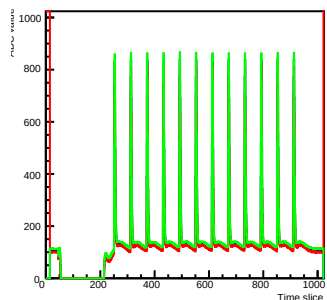
Time mcm 0 chip 5 chan 7 test1



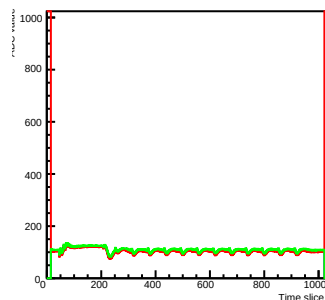
Time mcm 0 chip 5 chan 8 test1



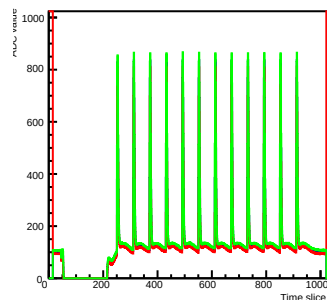
Time mcm 0 chip 5 chan 9 test1



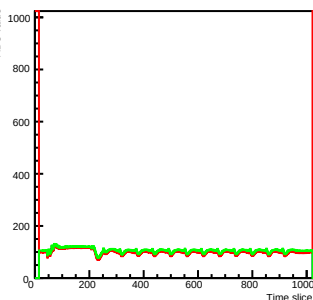
Time mcm 0 chip 5 chan 10 test1



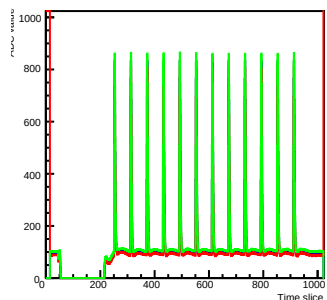
Time mcm 0 chip 5 chan 11 test1



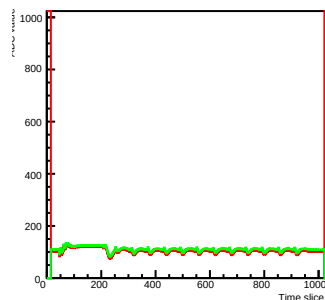
Time mcm 0 chip 5 chan 12 test1



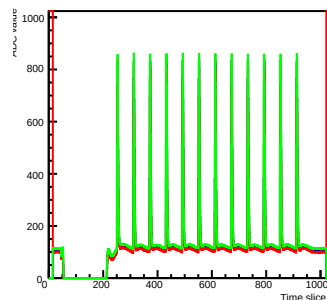
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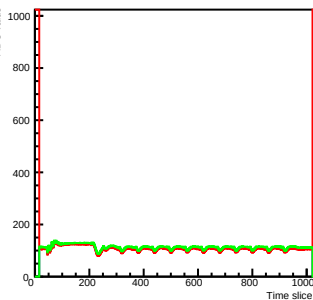
Time mcm 0 chip 5 chan 14 test1



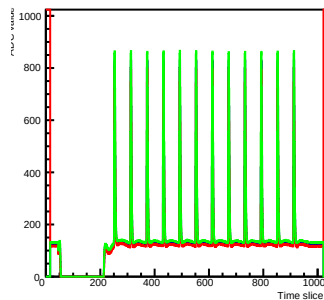
Time mcm 0 chip 5 chan 15 test1



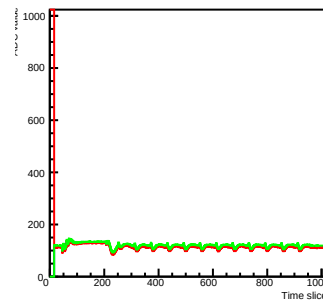
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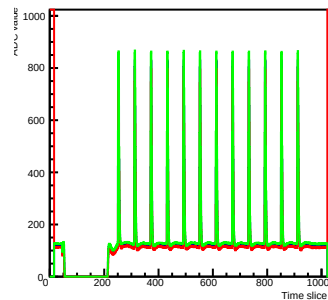
Time mcm 0 chip 6 chan 1 test1



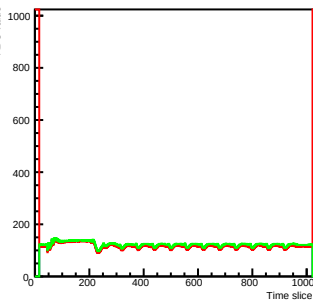
Time mcm 0 chip 6 chan 2 test1



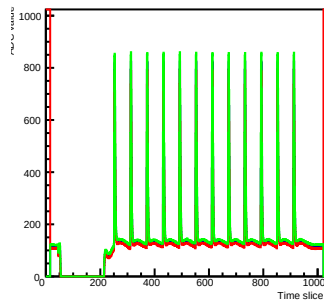
Time mcm 0 chip 6 chan 3 test1



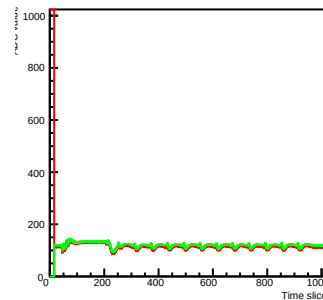
Time mcm 0 chip 6 chan 4 test1



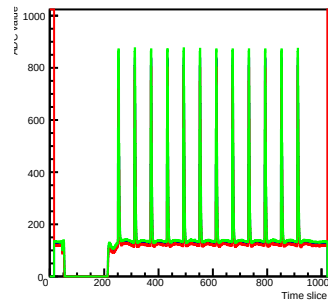
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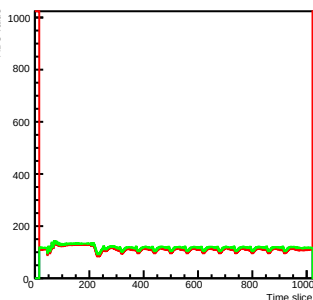
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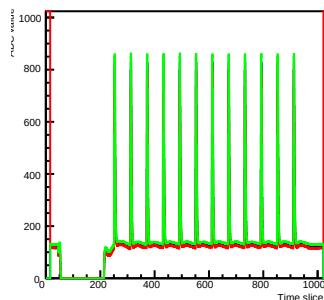
Time mcm 0 chip 6 chan 7 test1



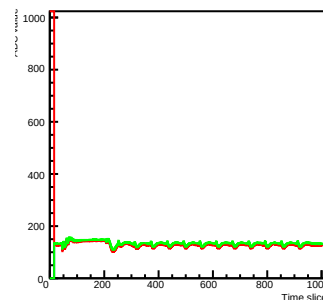
Time mcm 0 chip 6 chan 8 test1



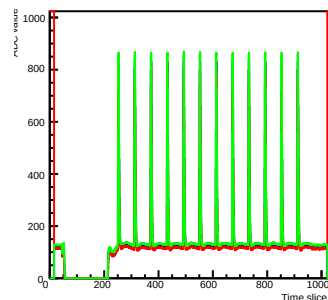
Time mcm 0 chip 6 chan 9 test1



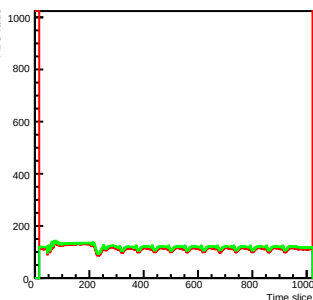
Time mcm 0 chip 6 chan 10 test1



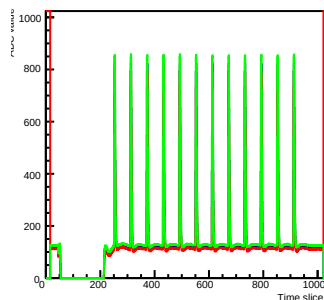
Time mcm 0 chip 6 chan 11 test1



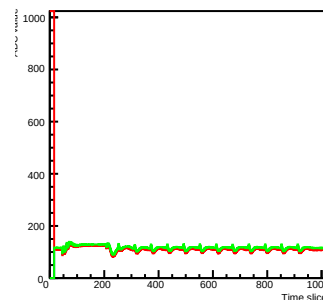
Time mcm 0 chip 6 chan 12 test1



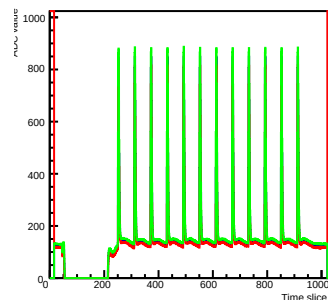
Time mcm 0 chip 6 chan 13 test1



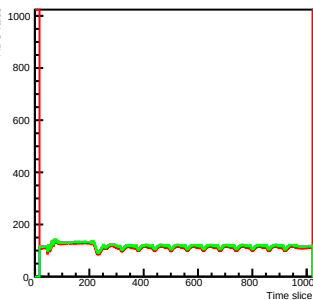
Time mcm 0 chip 6 chan 14 test1



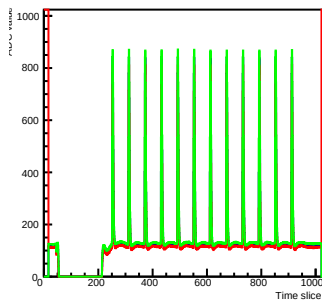
Time mcm 0 chip 6 chan 15 test1



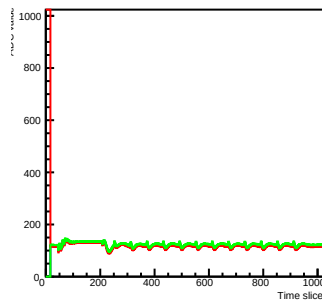
Time mcm 0 chip 7 chan 0 test1



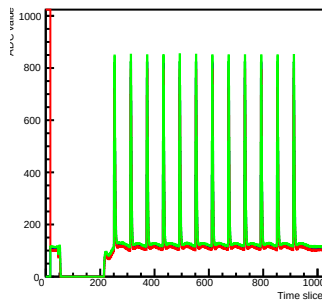
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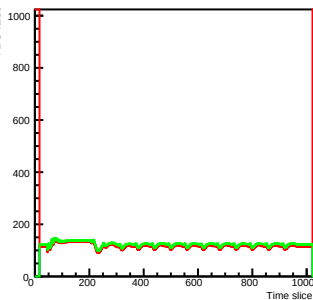
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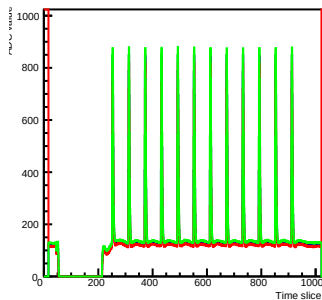
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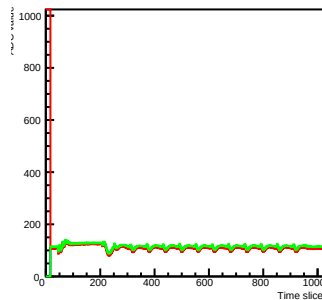
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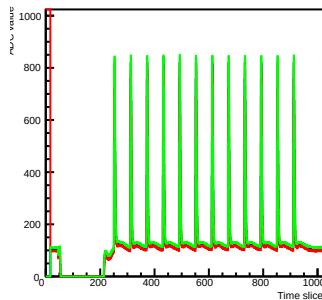
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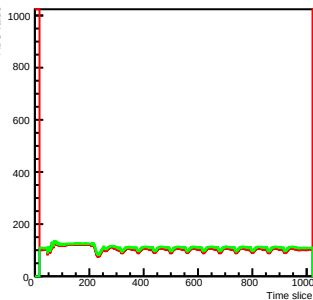
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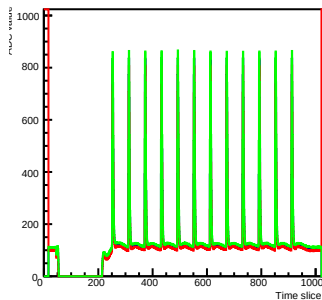
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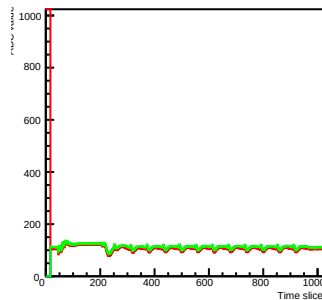
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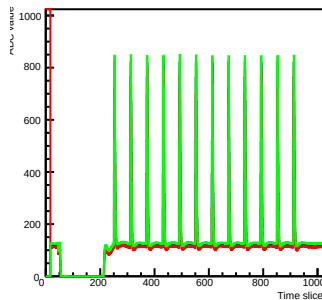
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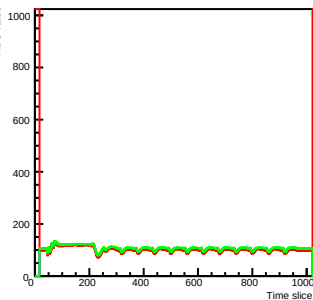
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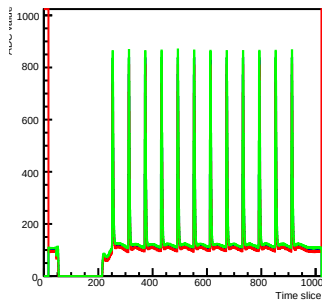
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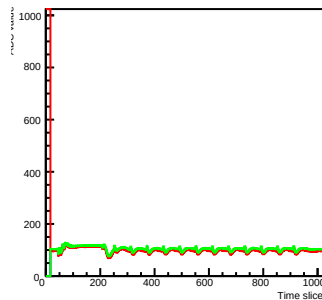
Time mcm 0 chip 7 chan 12 test1



Time mcm 0 chip 7 chan 13 test1



Time mcm 0 chip 7 chan 14 test1



Time mcm 0 chip 7 chan 15 test1

