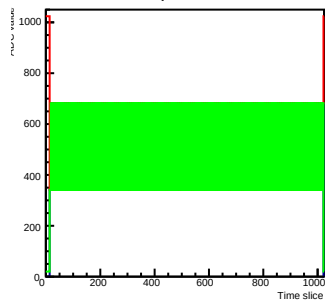


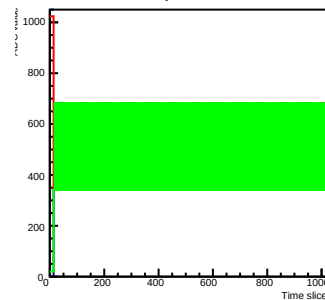
mcm 0 chip 0 chan 0 test1



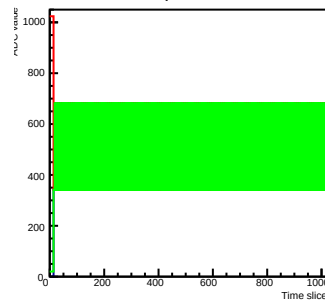
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mcm 0 chip 0 chan 2 test1



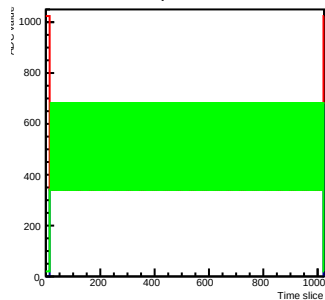
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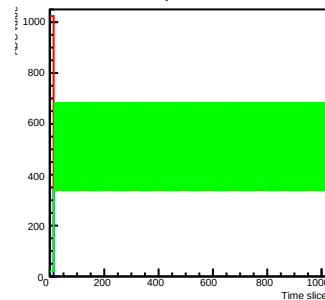
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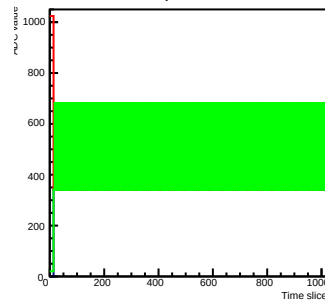
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mcm 0 chip 0 chan 6 test1



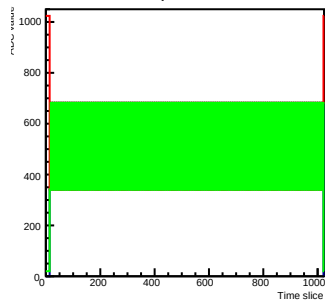
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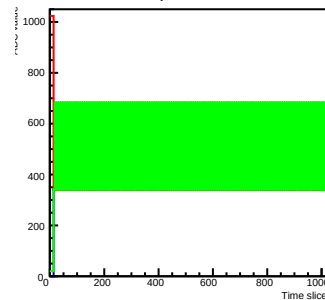
mcm 0 chip 0 chan 8 test1



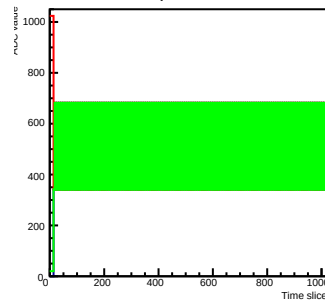
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mcm 0 chip 0 chan 10 test1



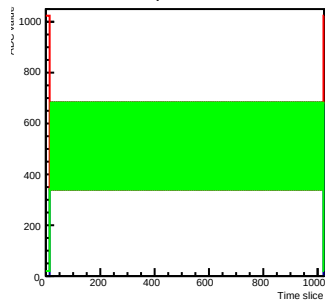
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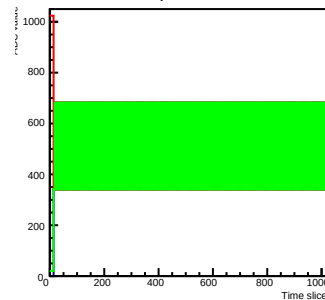
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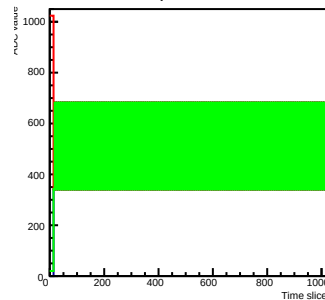
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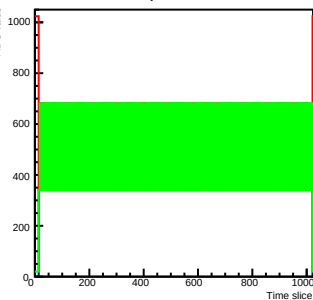
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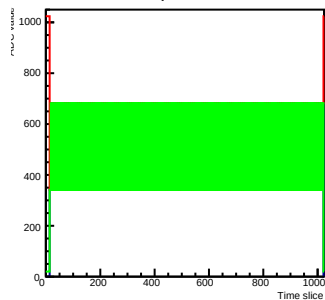
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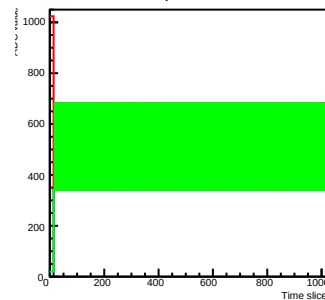
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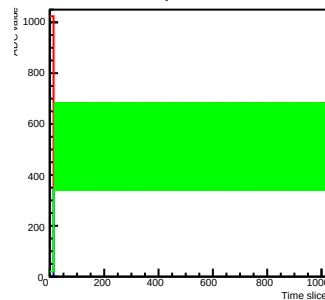
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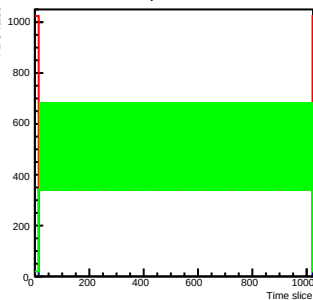
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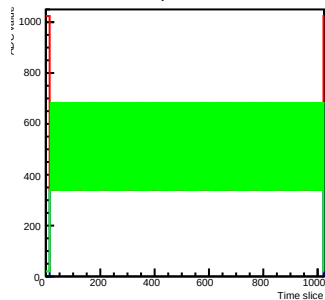
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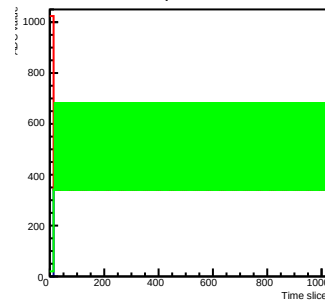
mcm 0 chip 1 chan 4 test1



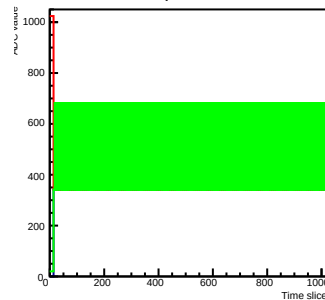
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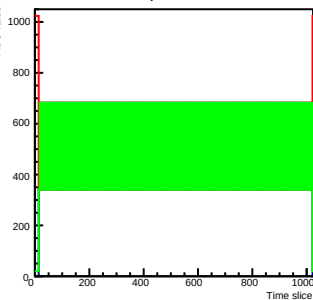
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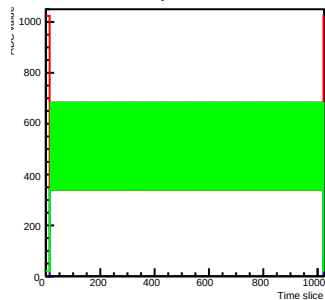
mcm 0 chip 1 chan 7 test1



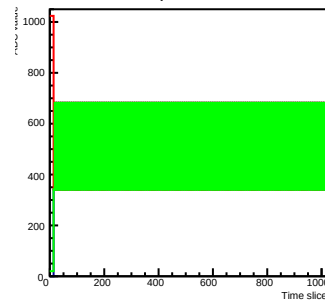
mcm 0 chip 1 chan 8 test1



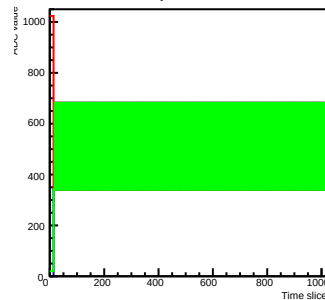
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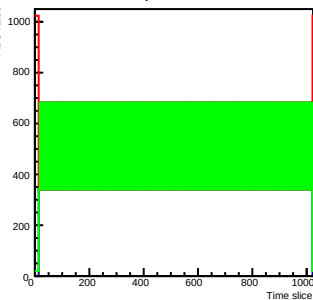
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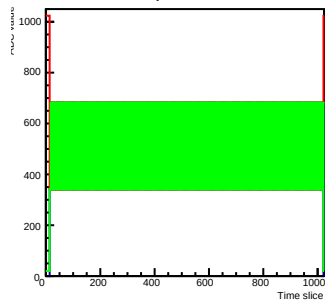
mcm 0 chip 1 chan 11 test1



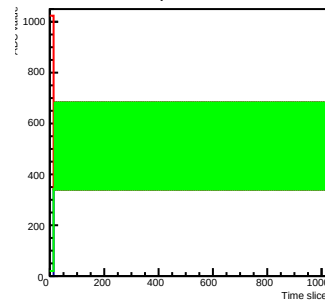
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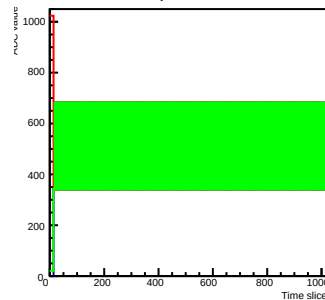
mcm 0 chip 1 chan 13 test1



mcm 0 chip 1 chan 14 test1



mcm 0 chip 1 chan 15 test1



mcm 0 chip 2 chan 0 test1



mcm 0 chip 2 chan 1 test1



mcm 0 chip 2 chan 2 test1



mcm 0 chip 2 chan 3 test1



mcm 0 chip 2 chan 4 test1



mcm 0 chip 2 chan 5 test1



mcm 0 chip 2 chan 6 test1



mcm 0 chip 2 chan 7 test1



mcm 0 chip 2 chan 8 test1



mcm 0 chip 2 chan 9 test1



mcm 0 chip 2 chan 10 test1



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mcm 0 chip 2 chan 12 test1



mcm 0 chip 2 chan 13 test1



mcm 0 chip 2 chan 14 test1



mcm 0 chip 2 chan 15 test1



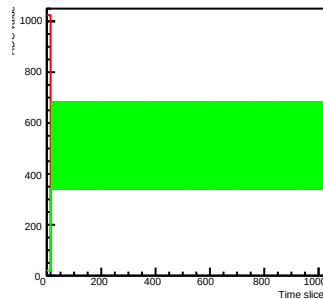
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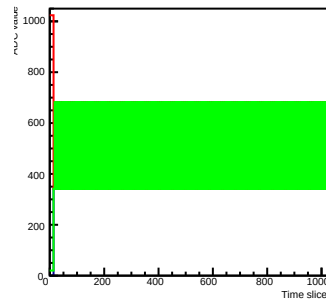
mcm 0 chip 3 chan 1 test1



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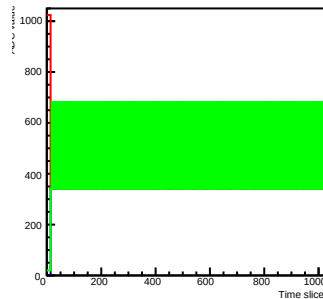
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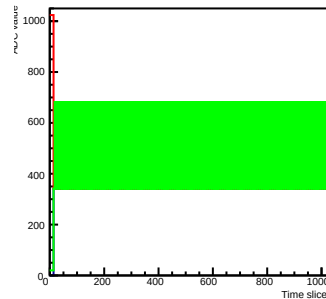
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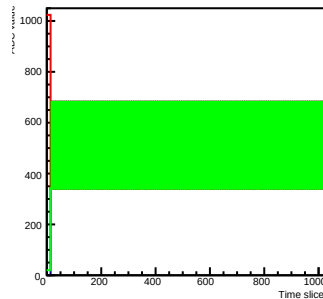
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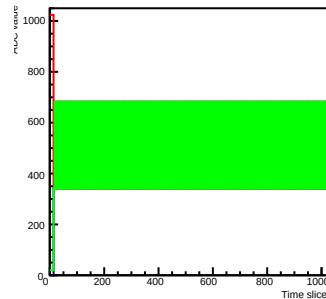
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mcm 0 chip 3 chan 10 test1



mcm 0 chip 3 chan 11 test1



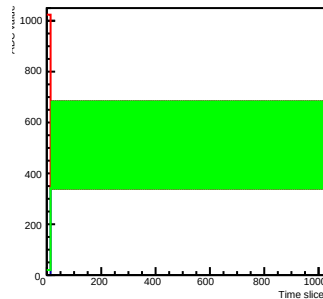
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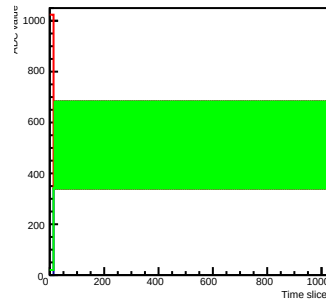
mcm 0 chip 3 chan 13 test1



mcm 0 chip 3 chan 14 test1



mcm 0 chip 3 chan 15 test1



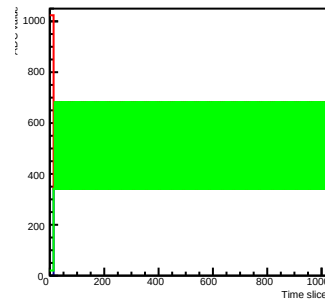
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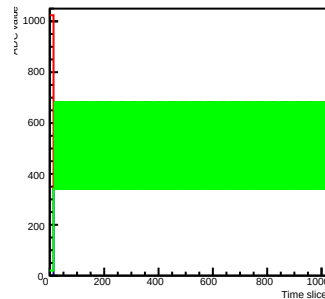
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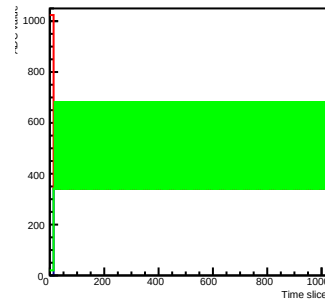
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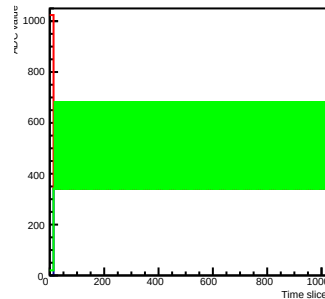
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mcm 0 chip 4 chan 6 test1



mcm 0 chip 4 chan 7 test1



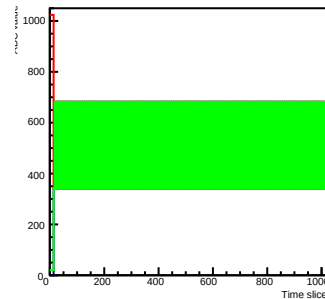
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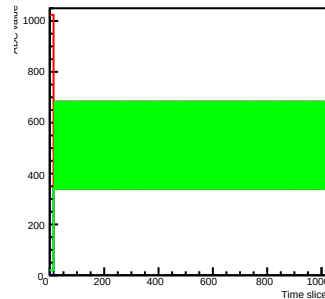
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mcm 0 chip 4 chan 10 test1



mcm 0 chip 4 chan 11 test1



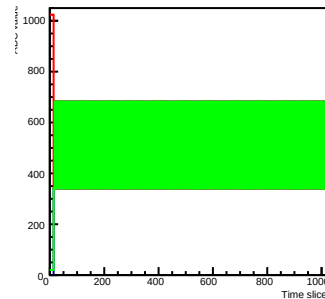
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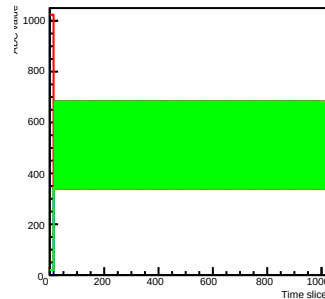
mcm 0 chip 4 chan 13 test1



mcm 0 chip 4 chan 14 test1



mcm 0 chip 4 chan 15 test1



mcm 0 chip 5 chan 0 test1



mcm 0 chip 5 chan 1 test1



mcm 0 chip 5 chan 2 test1



mcm 0 chip 5 chan 3 test1



mcm 0 chip 5 chan 4 test1



mcm 0 chip 5 chan 5 test1



mcm 0 chip 5 chan 6 test1



mcm 0 chip 5 chan 7 test1



mcm 0 chip 5 chan 8 test1



mcm 0 chip 5 chan 9 test1



mcm 0 chip 5 chan 10 test1



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mcm 0 chip 5 chan 12 test1



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mcm 0 chip 5 chan 15 test1



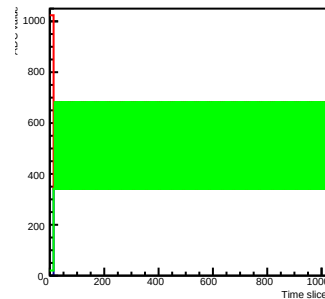
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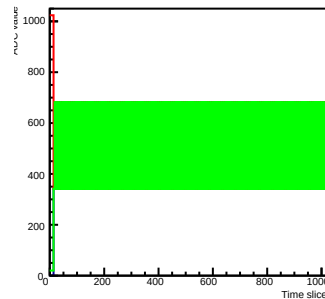
mcm 0 chip 6 chan 1 test1



mcm 0 chip 6 chan 2 test1



mcm 0 chip 6 chan 3 test1



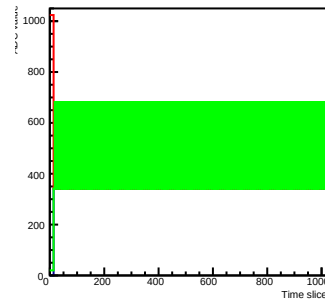
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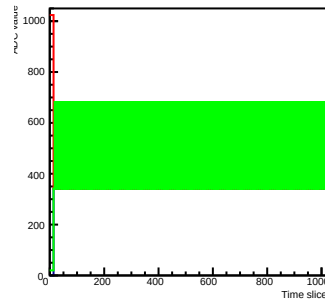
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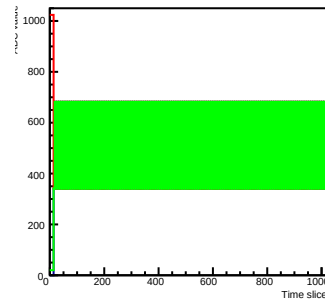
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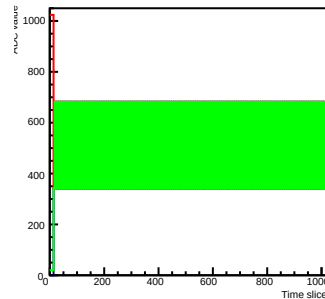
mcm 0 chip 6 chan 9 test1



mcm 0 chip 6 chan 10 test1



mcm 0 chip 6 chan 11 test1



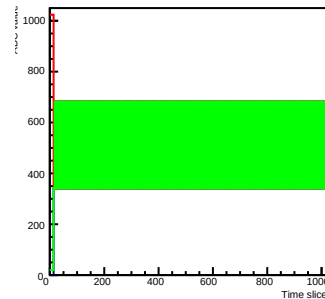
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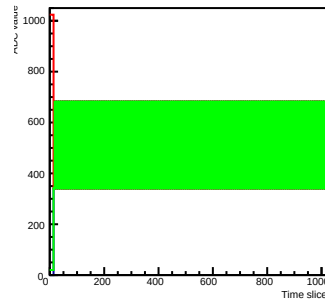
mcm 0 chip 6 chan 13 test1



mcm 0 chip 6 chan 14 test1



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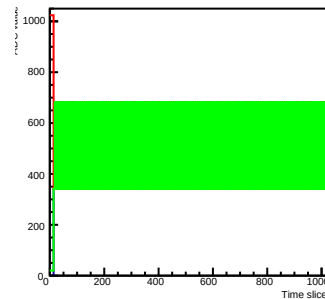
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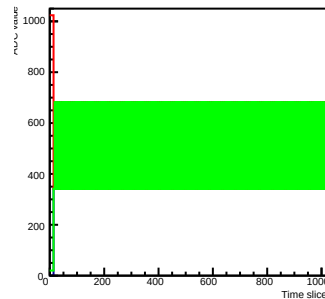
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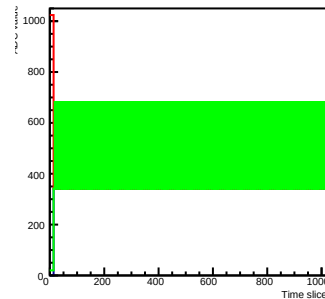
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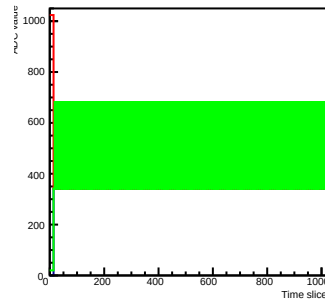
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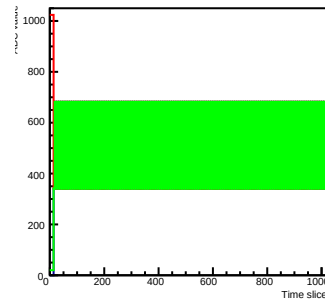
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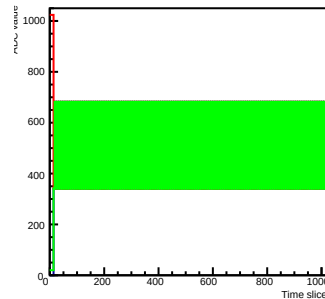
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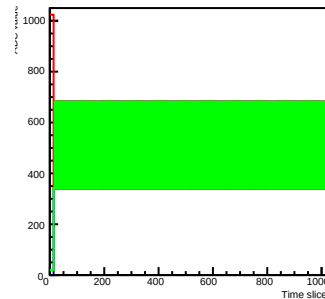
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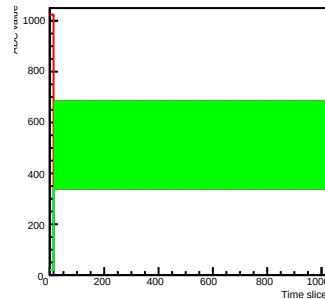
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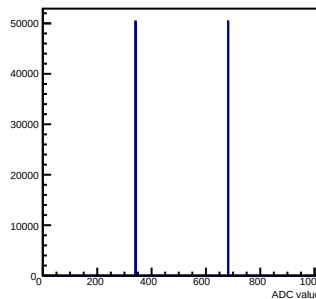
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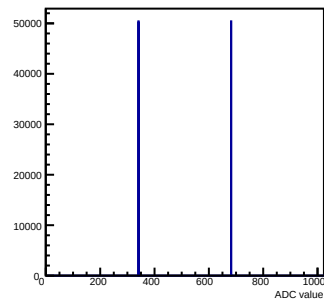
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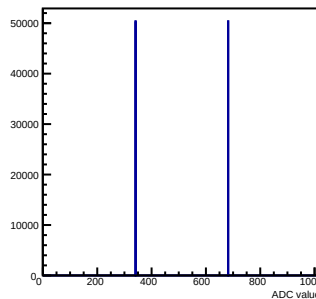
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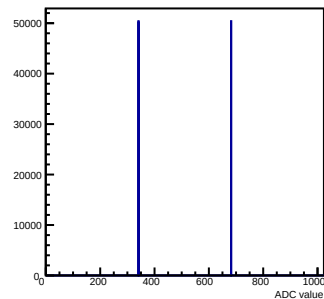
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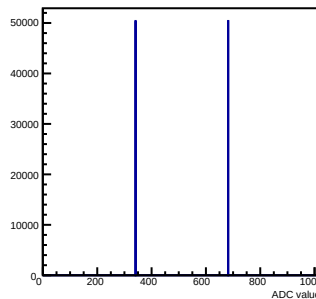
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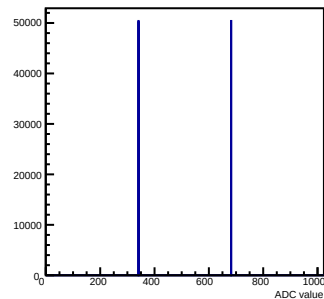
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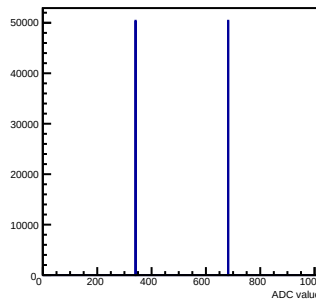
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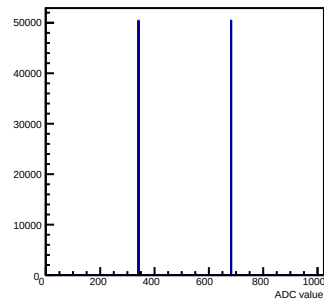
mcm 0 chip 0 chan 13 test1



mcm 0 chip 0 chan 14 test1



mcm 0 chip 0 chan 15 test1



mcm 0 chip 1 chan 0 test1



mcm 0 chip 1 chan 1 test1



mcm 0 chip 1 chan 2 test1



mcm 0 chip 1 chan 3 test1



mcm 0 chip 1 chan 4 test1



mcm 0 chip 1 chan 5 test1



mcm 0 chip 1 chan 6 test1



mcm 0 chip 1 chan 7 test1



mcm 0 chip 1 chan 8 test1



mcm 0 chip 1 chan 9 test1



mcm 0 chip 1 chan 10 test1



mcm 0 chip 1 chan 11 test1



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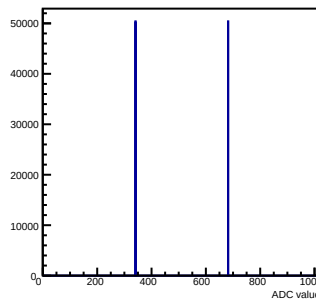
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mcm 0 chip 2 chan 2 test1



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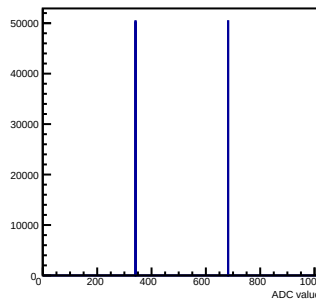
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mcm 0 chip 2 chan 6 test1



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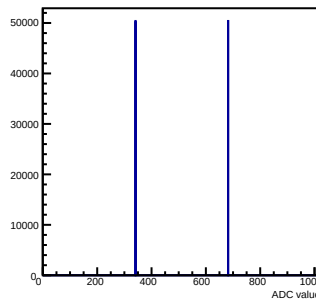
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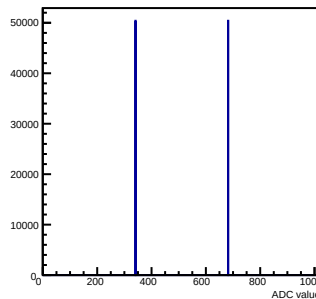
mcm 0 chip 2 chan 13 test1



mcm 0 chip 2 chan 14 test1



mcm 0 chip 2 chan 15 test1



The ADC histogram displays two sharp, narrow peaks. The first peak is located at approximately 350 ADC units, and the second peak is at approximately 700 ADC units. The x-axis is labeled 'ADC value' and ranges from 200 to 1000 with major ticks every 200 units. The y-axis represents frequency, with a maximum value of 1000 indicated by a horizontal line at the top of the plot area.

[illegible][illegible]

mcm 0 chip 4 chan 0 test1



mcm 0 chip 4 chan 1 test1



mcm 0 chip 4 chan 2 test1



mcm 0 chip 4 chan 3 test1



mcm 0 chip 4 chan 4 test1



mcm 0 chip 4 chan 5 test1



mcm 0 chip 4 chan 6 test1



mcm 0 chip 4 chan 7 test1



mcm 0 chip 4 chan 8 test1



mcm 0 chip 4 chan 9 test1



mcm 0 chip 4 chan 10 test1



mcm 0 chip 4 chan 11 test1



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mcm 0 chip 4 chan 13 test1



mcm 0 chip 4 chan 14 test1



mcm 0 chip 4 chan 15 test1



mcm 0 chip 5 chan 0 test1



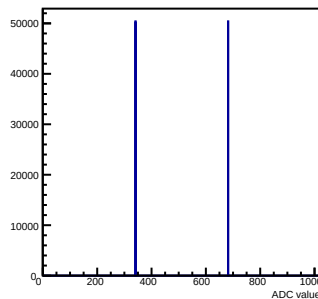
mcm 0 chip 5 chan 1 test1



mcm 0 chip 5 chan 2 test1



mcm 0 chip 5 chan 3 test1



mcm 0 chip 5 chan 4 test1



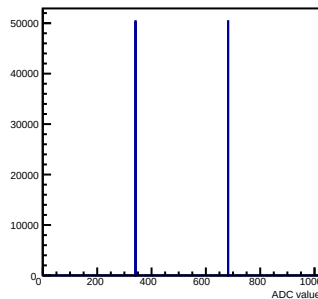
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mcm 0 chip 5 chan 6 test1



mcm 0 chip 5 chan 7 test1



mcm 0 chip 5 chan 8 test1



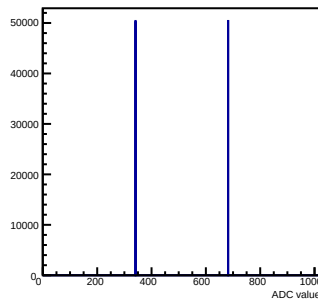
mcm 0 chip 5 chan 9 test1



mcm 0 chip 5 chan 10 test1



mcm 0 chip 5 chan 11 test1



mcm 0 chip 5 chan 12 test1



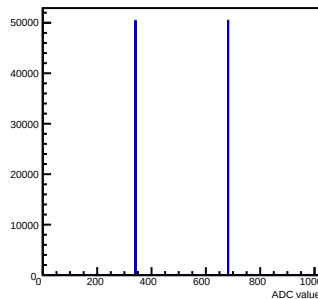
mcm 0 chip 5 chan 13 test1



mcm 0 chip 5 chan 14 test1



mcm 0 chip 5 chan 15 test1



mcm 0 chip 6 chan 0 test1



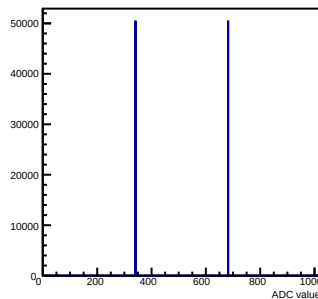
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mcm 0 chip 6 chan 2 test1



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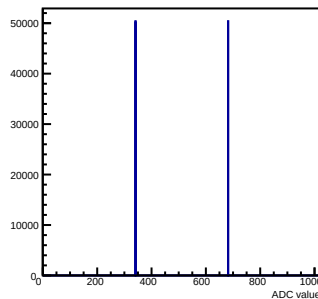
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mcm 0 chip 6 chan 6 test1



mcm 0 chip 6 chan 7 test1



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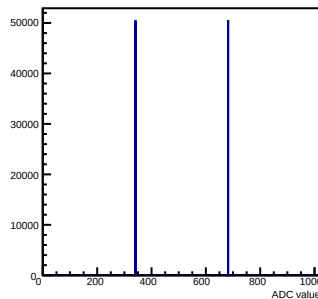
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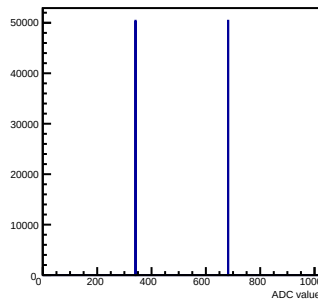
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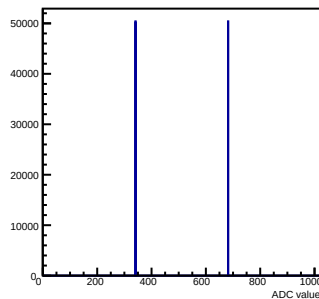
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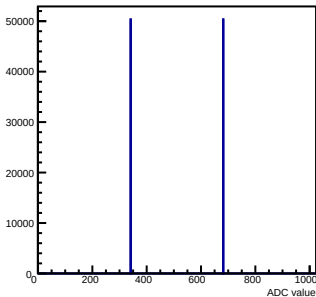
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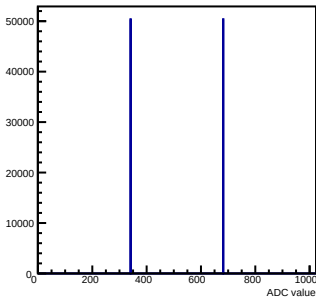
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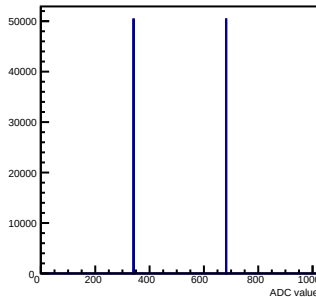
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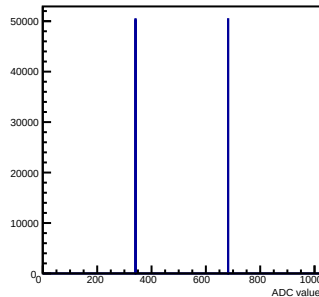
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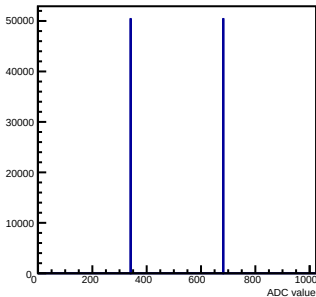
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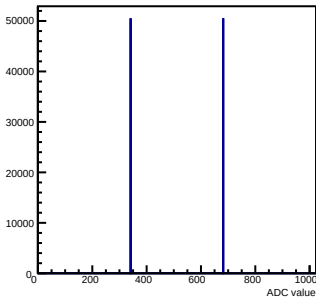
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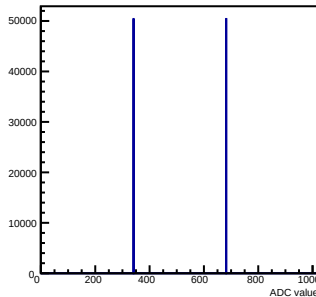
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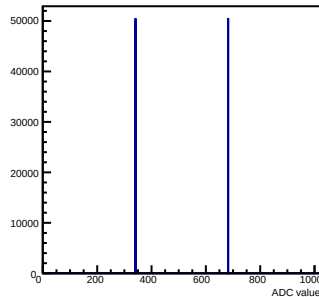
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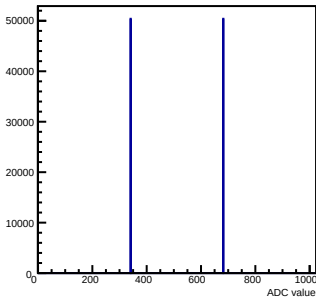
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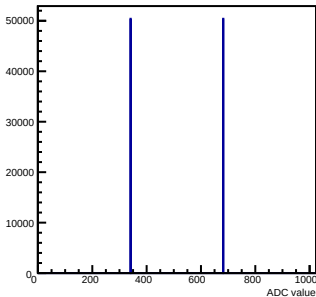
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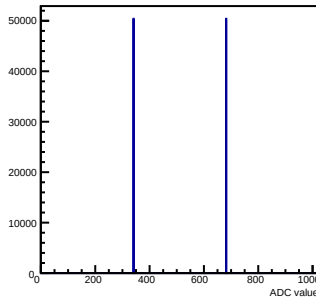
mcm 0 chip 7 chan 12 test1



mcm 0 chip 7 chan 13 test1



mcm 0 chip 7 chan 14 test1



mcm 0 chip 7 chan 15 test1

