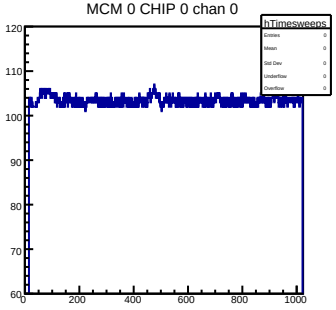
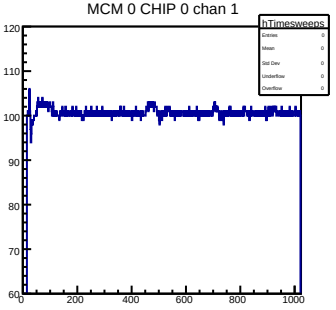
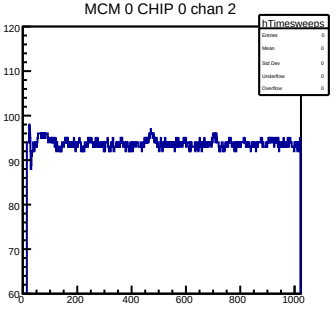
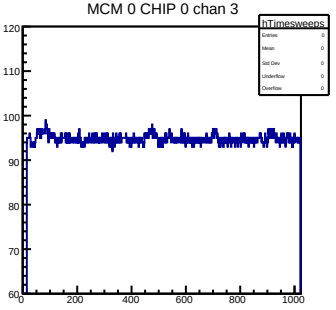
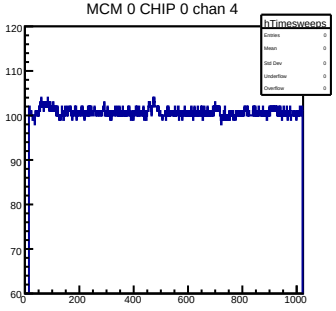
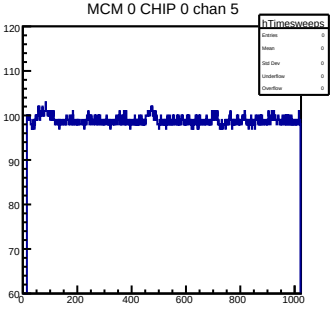

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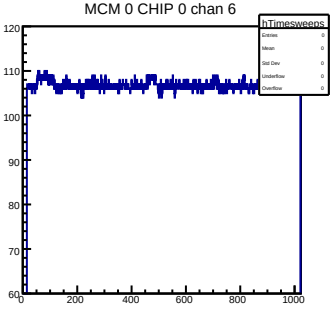

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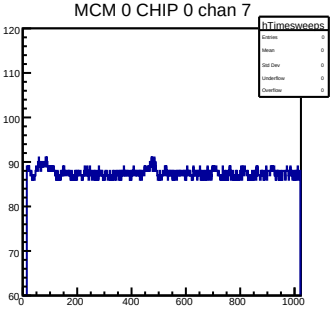

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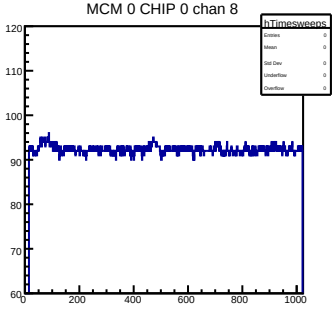

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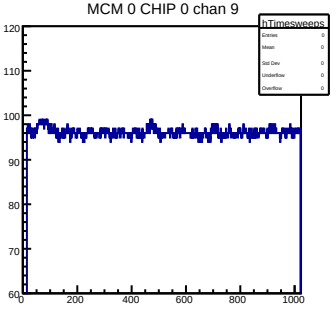

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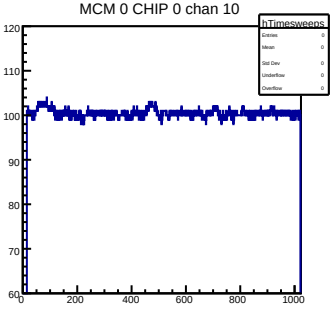

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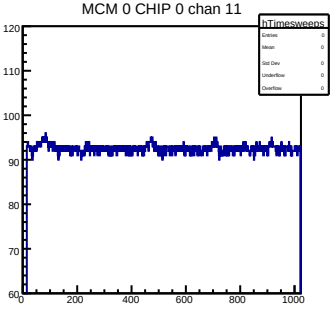

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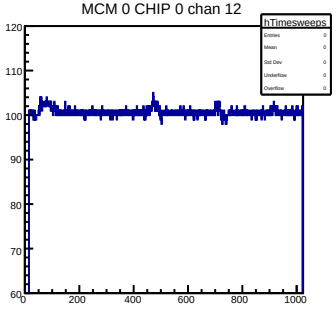

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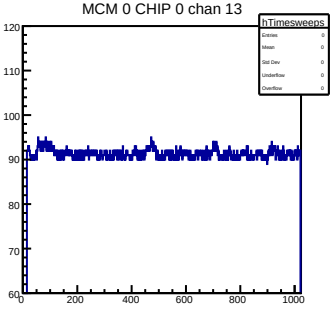

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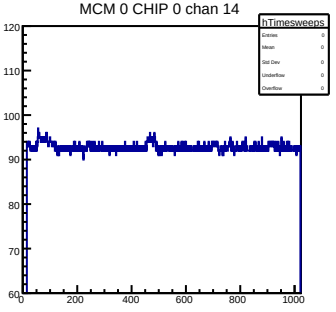

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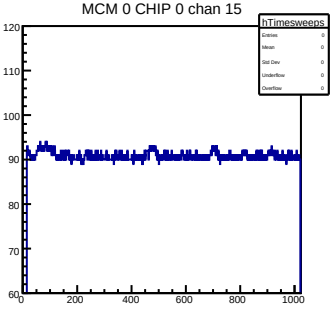

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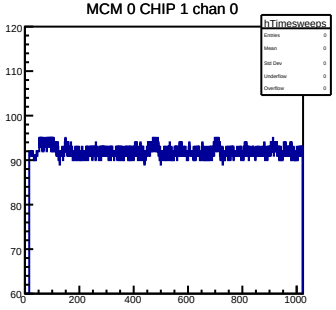

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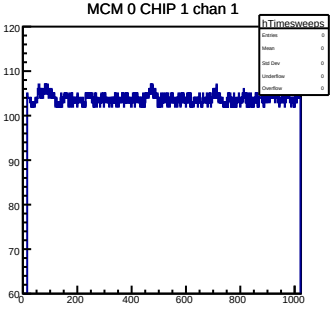

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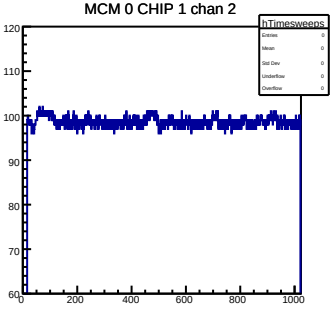

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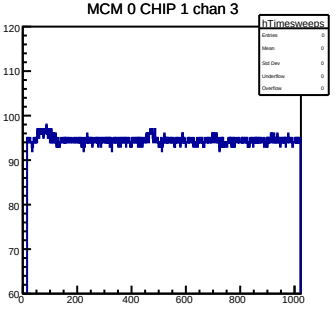

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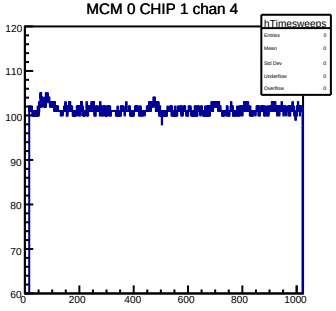

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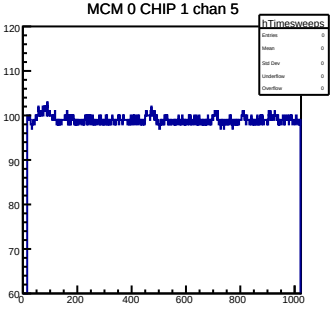

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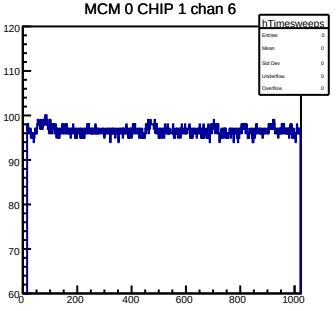

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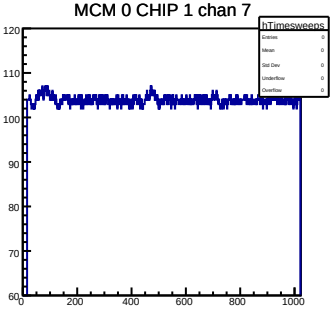

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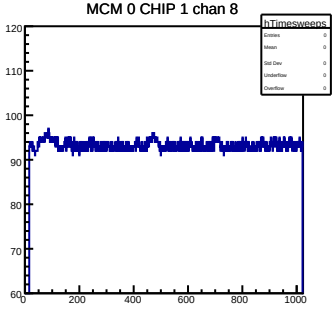

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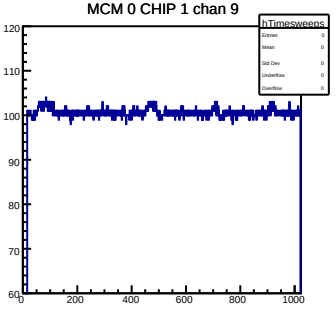

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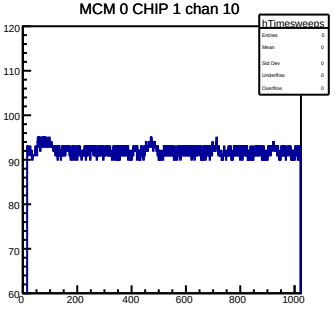

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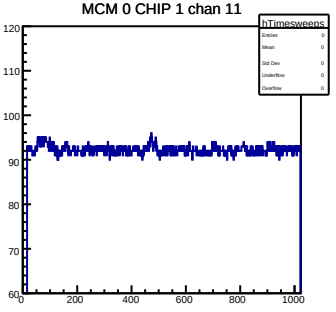

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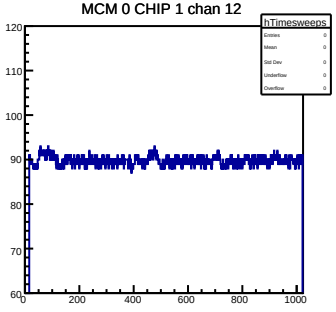

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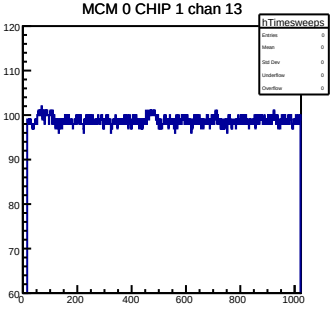

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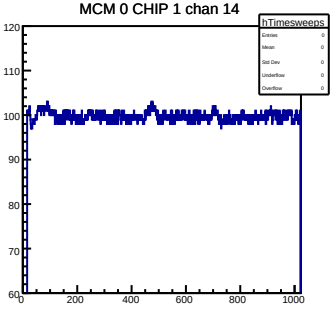

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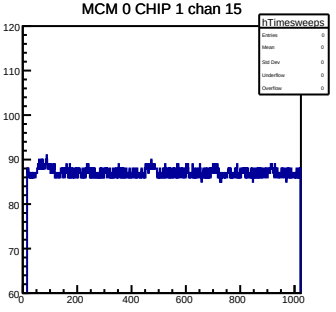

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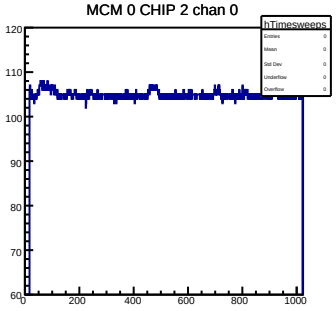

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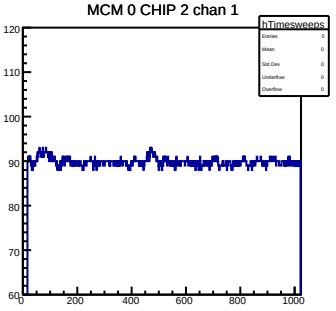

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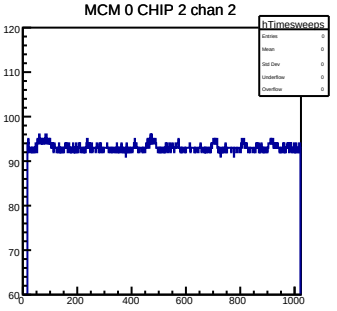

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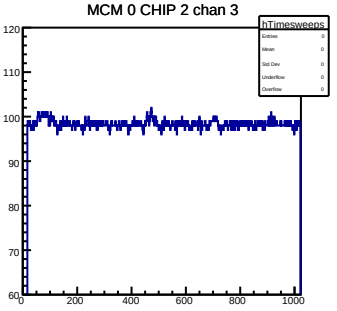

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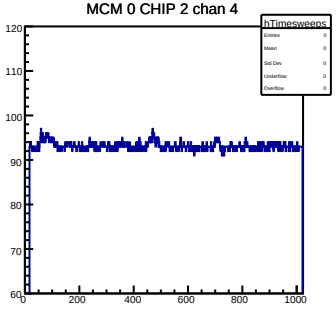

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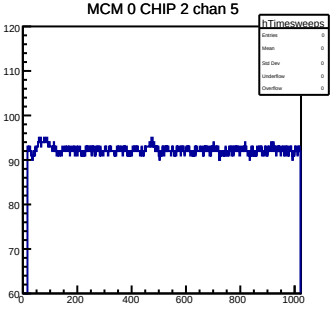

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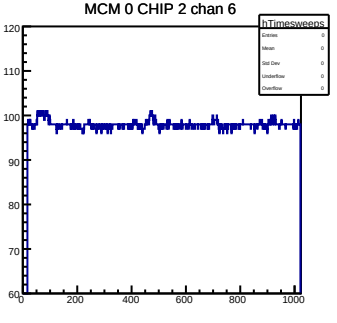

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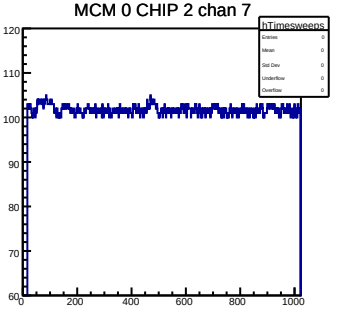

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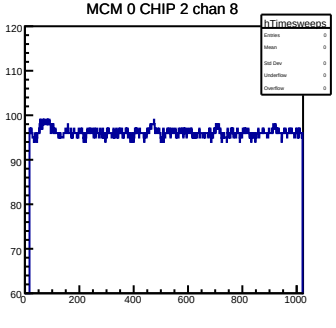

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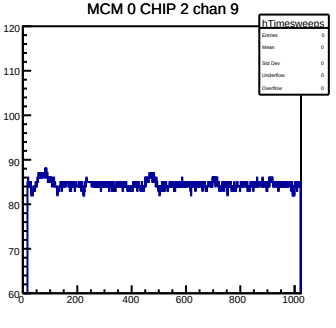

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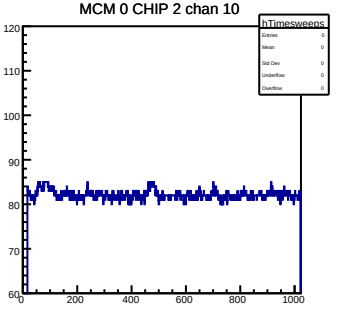

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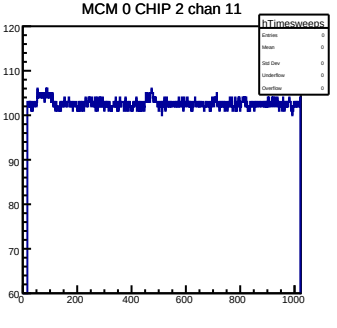

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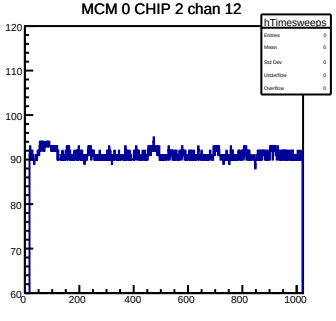

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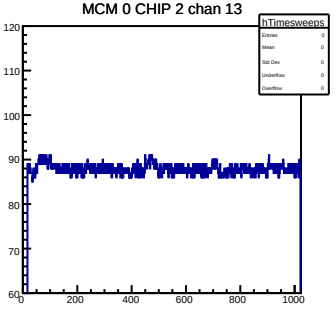

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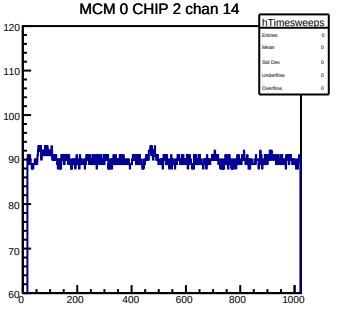

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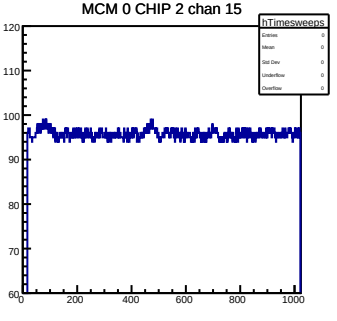

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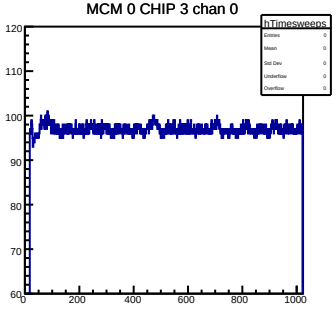

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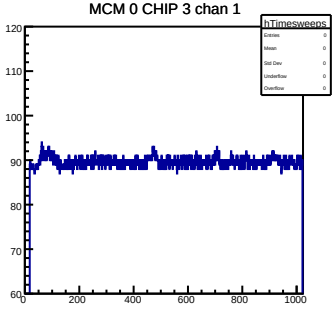

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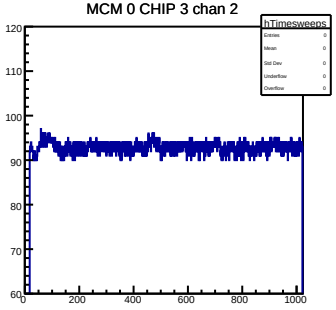

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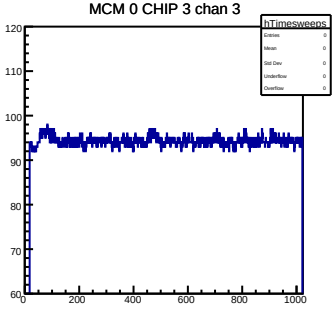

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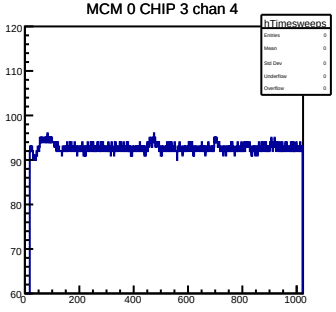

MCM 0 CHIP 2 chan 15
hTimesweeps

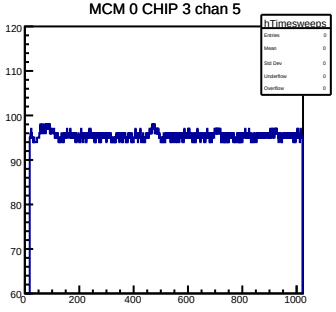

MCM 0 CHIP 3 chan 0
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

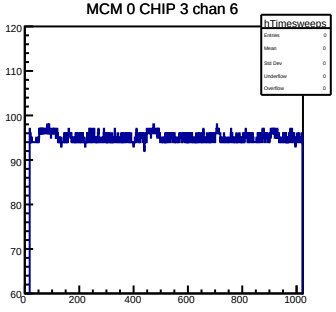

MCM 0 CHIP 3 chan 1
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

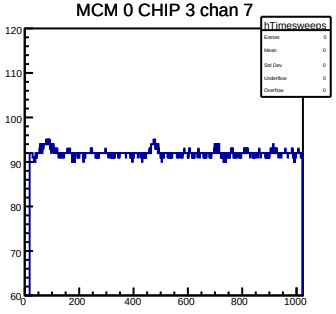

MCM 0 CHIP 3 chan 2
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

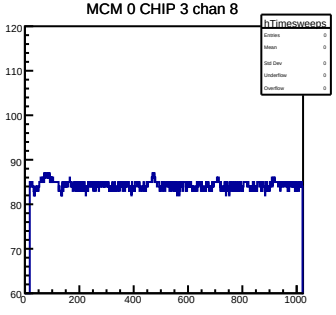

MCM 0 CHIP 3 chan 3
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

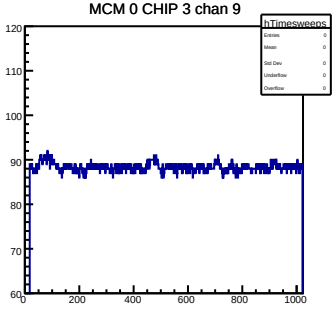

MCM 0 CHIP 3 chan 4
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

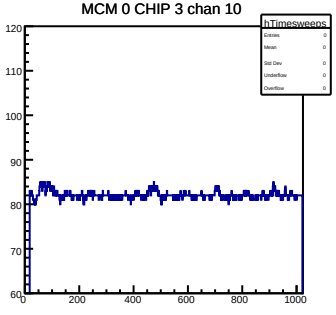

MCM 0 CHIP 3 chan 5
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

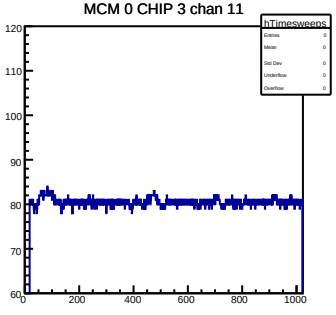

MCM 0 CHIP 3 chan 6
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

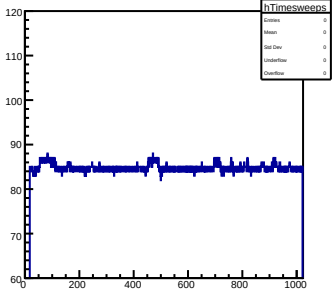

MCM 0 CHIP 3 chan 7
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

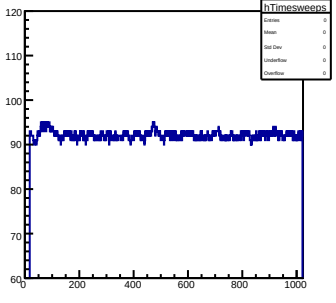

MCM 0 CHIP 3 chan 8
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

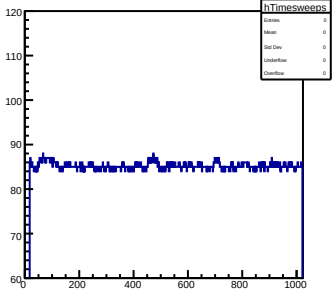

MCM 0 CHIP 3 chan 9
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

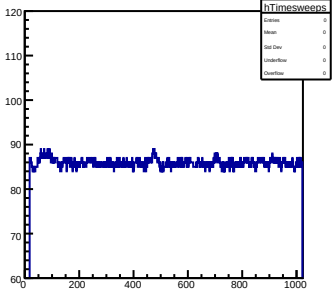

MCM 0 CHIP 3 chan 10
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

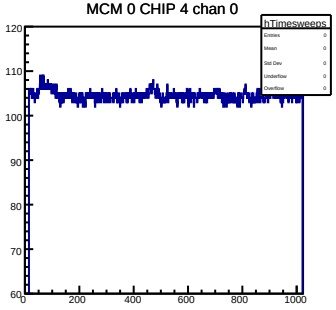

MCM 0 CHIP 3 chan 11
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

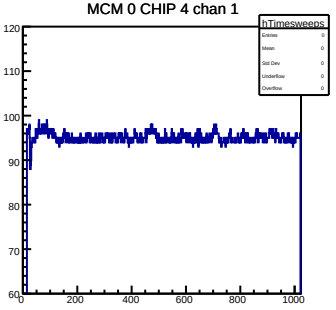

MCM 0 CHIP 3 chan 12
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

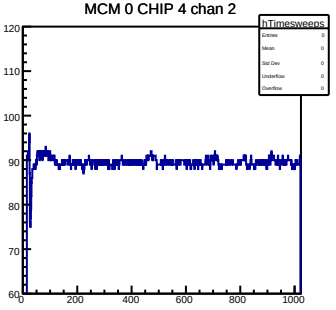

MCM 0 CHIP 3 chan 13
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

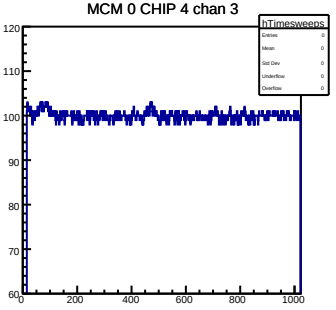

MCM 0 CHIP 3 chan 14
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

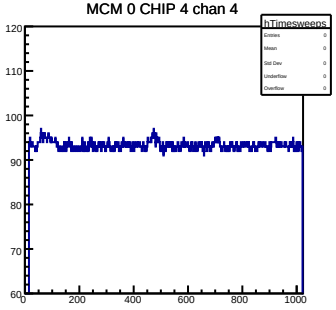

MCM 0 CHIP 3 chan 15
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

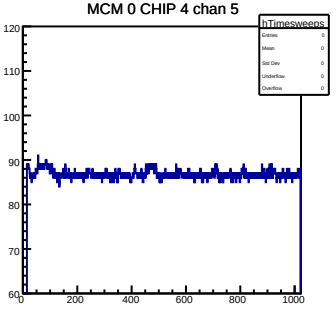

MCM 0 CHIP 4 chan 0
hTimesweeps

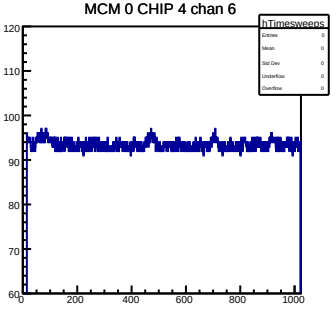

MCM 0 CHIP 4 chan 1
hTimesweeps

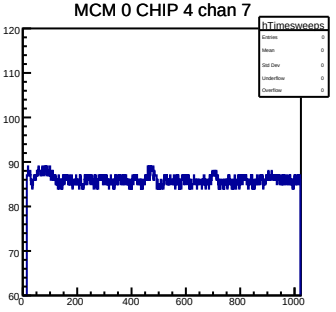

MCM 0 CHIP 4 chan 2
hTimesweeps

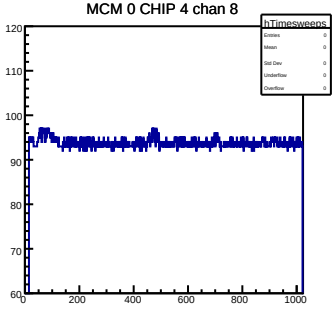

MCM 0 CHIP 4 chan 3
hTimesweeps

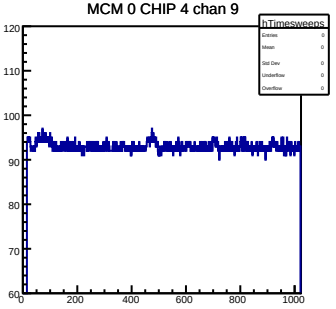

MCM 0 CHIP 4 chan 4
hTimesweeps

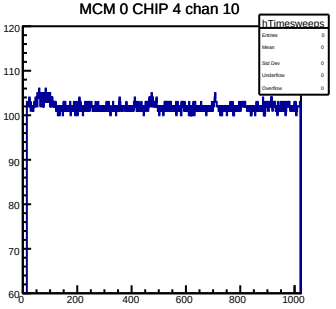

MCM 0 CHIP 4 chan 5
hTimesweeps

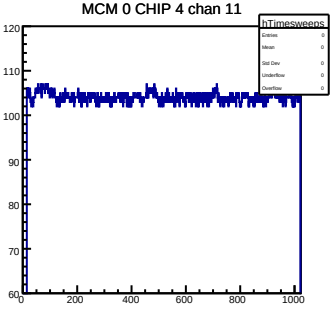

MCM 0 CHIP 4 chan 6
hTimesweeps

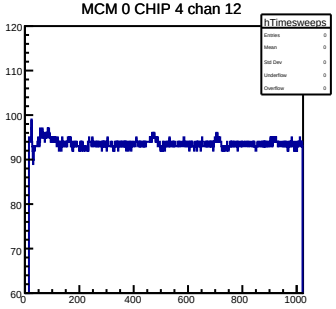

MCM 0 CHIP 4 chan 7
hTimesweeps

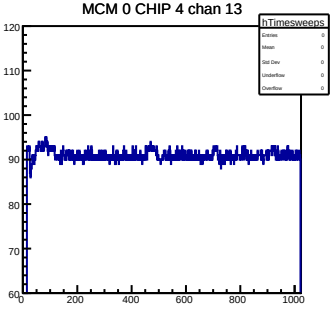

MCM 0 CHIP 4 chan 8
hTimesweeps

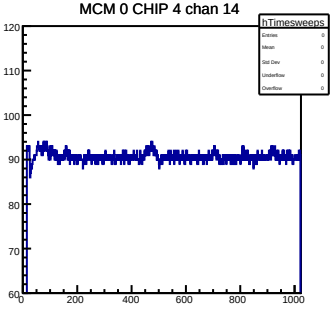

MCM 0 CHIP 4 chan 9
hTimesweeps

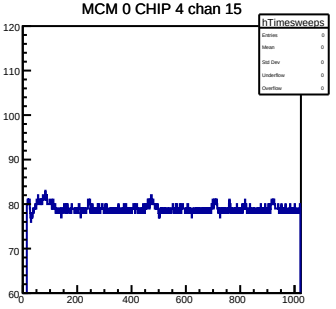

MCM 0 CHIP 4 chan 10
hTimesweeps

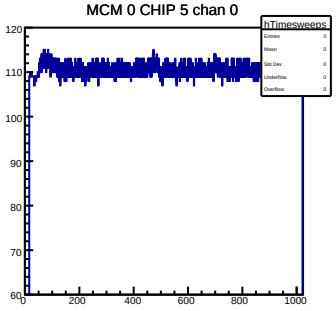

MCM 0 CHIP 4 chan 11
hTimesweeps

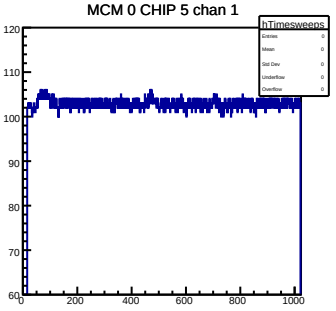

MCM 0 CHIP 4 chan 12
hTimesweeps

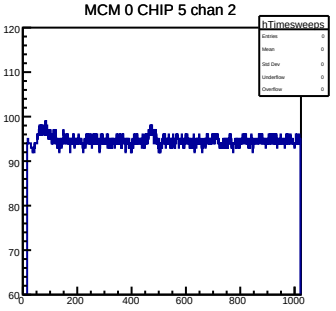

MCM 0 CHIP 4 chan 13
hTimesweeps

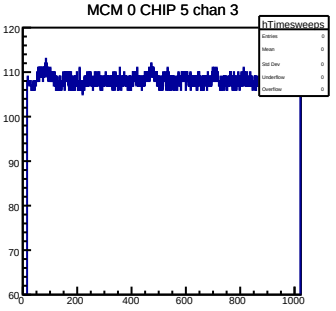

MCM 0 CHIP 4 chan 14
hTimesweeps

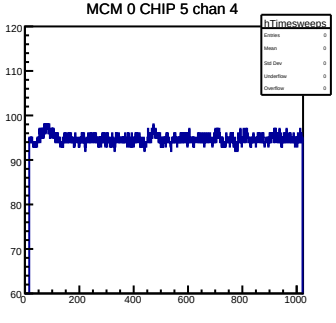

MCM 0 CHIP 4 chan 15
hTimesweeps

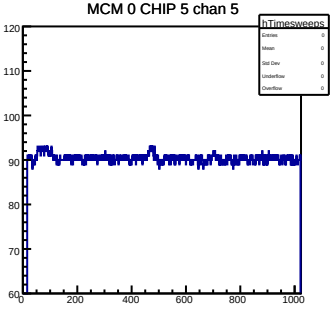

MCM 0 CHIP 5 chan 0
hTimesweeps

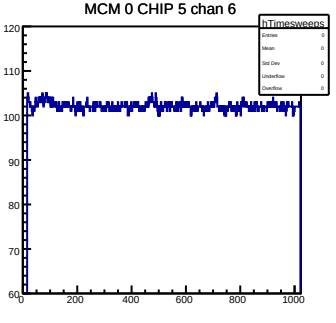

MCM 0 CHIP 5 chan 1
hTimesweeps

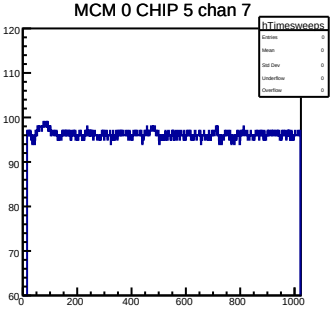

MCM 0 CHIP 5 chan 2
hTimesweeps

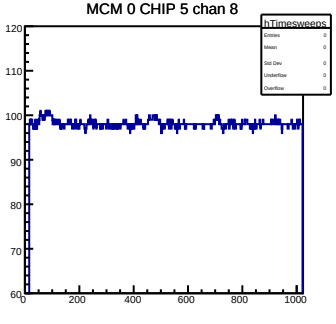

MCM 0 CHIP 5 chan 3
hTimesweeps

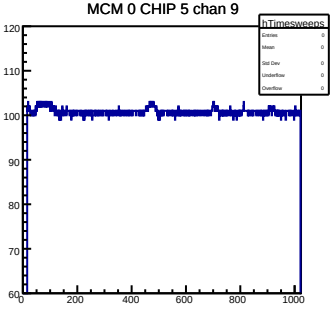

MCM 0 CHIP 5 chan 4
hTimesweeps

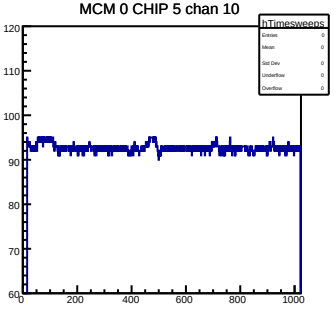

MCM 0 CHIP 5 chan 5
hTimesweeps

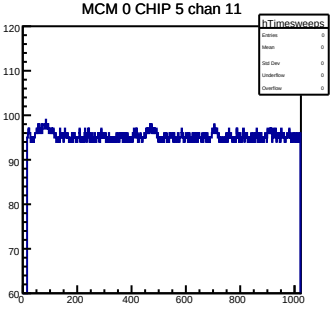

MCM 0 CHIP 5 chan 6
hTimesweeps

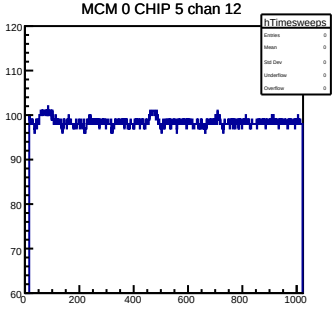

MCM 0 CHIP 5 chan 7
hTimesweeps

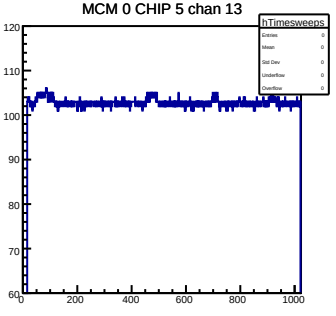

MCM 0 CHIP 5 chan 8
hTimesweeps

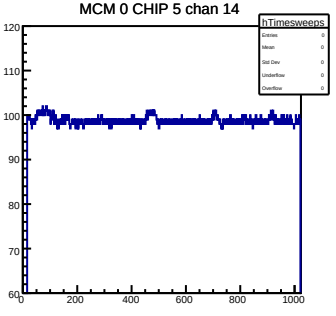

MCM 0 CHIP 5 chan 9
hTimesweeps

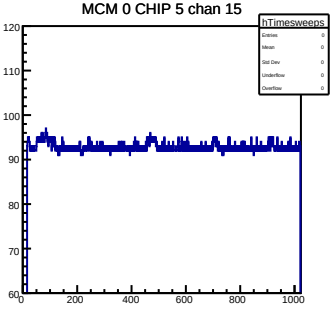

MCM 0 CHIP 5 chan 10
hTimesweeps

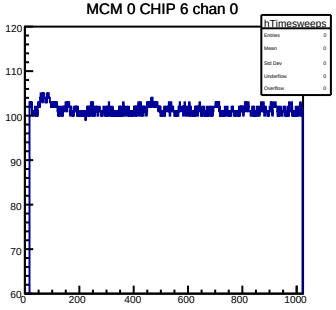

MCM 0 CHIP 5 chan 11
hTimesweeps

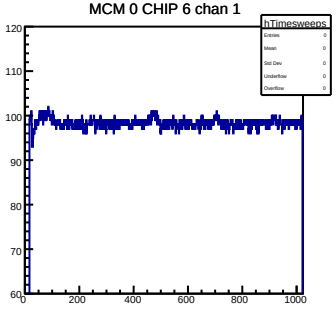

MCM 0 CHIP 5 chan 12
hTimesweeps

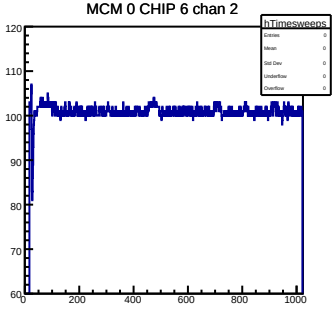

MCM 0 CHIP 5 chan 13
hTimesweeps

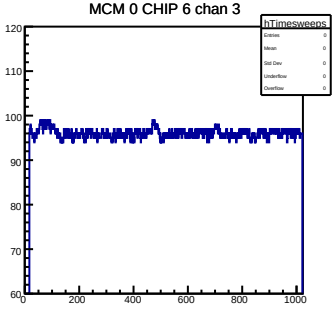

MCM 0 CHIP 5 chan 14
hTimesweeps

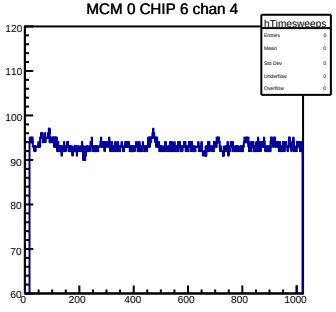

MCM 0 CHIP 5 chan 15
hTimesweeps

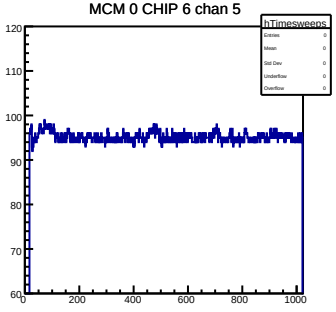

MCM 0 CHIP 6 chan 0
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

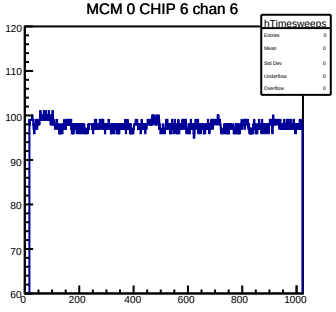

MCM 0 CHIP 6 chan 1
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

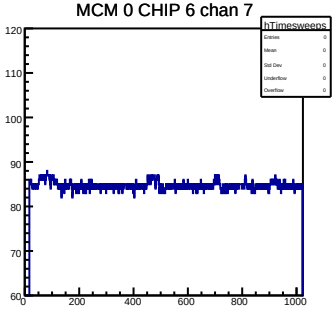

MCM 0 CHIP 6 chan 2
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

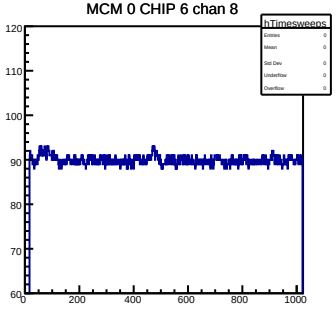

MCM 0 CHIP 6 chan 3
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

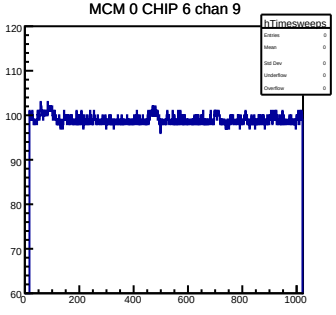

MCM 0 CHIP 6 chan 4
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

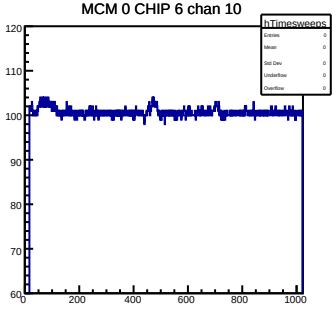

MCM 0 CHIP 6 chan 5
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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200
400
600
800
1000

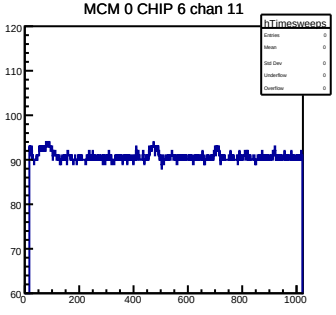

MCM 0 CHIP 6 chan 6
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

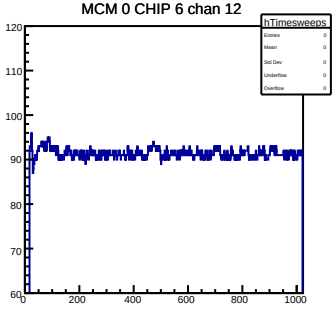

MCM 0 CHIP 6 chan 7
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

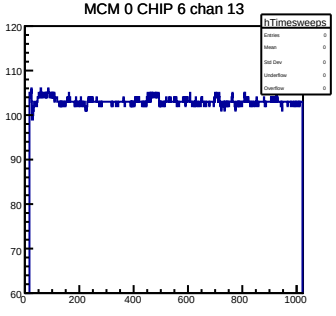

MCM 0 CHIP 6 chan 8
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

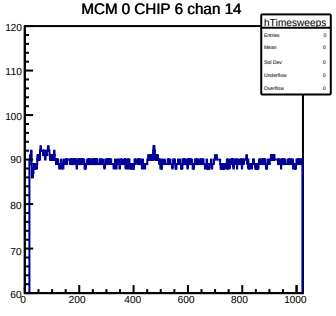

MCM 0 CHIP 6 chan 9
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

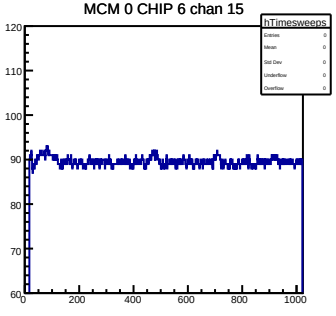

MCM 0 CHIP 6 chan 10
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

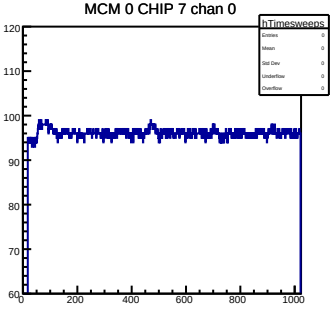

MCM 0 CHIP 6 chan 11
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

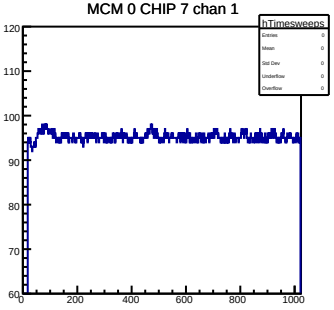

MCM 0 CHIP 6 chan 12
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

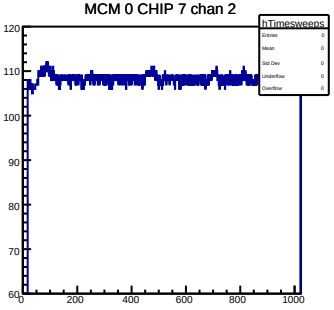

MCM 0 CHIP 6 chan 13
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

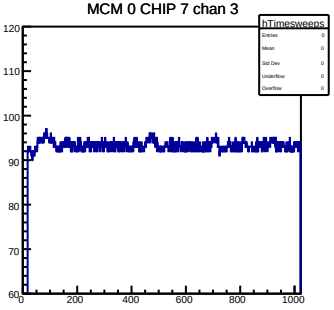

MCM 0 CHIP 6 chan 14
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

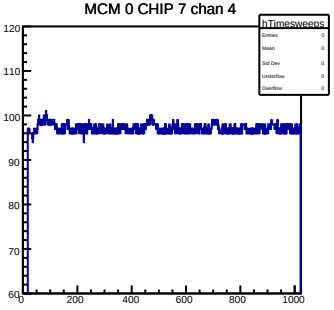

MCM 0 CHIP 6 chan 15
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

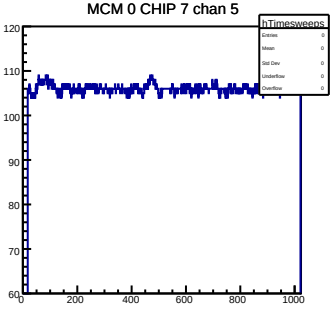

MCM 0 CHIP 7 chan 0
hTimesweeps

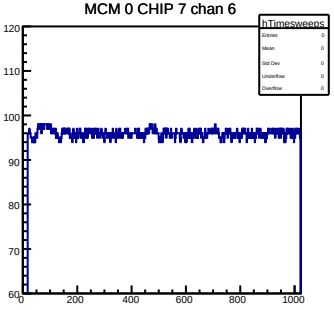

MCM 0 CHIP 7 chan 1
hTimesweeps

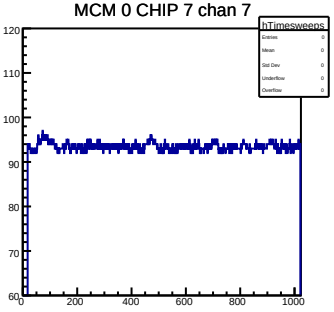

MCM 0 CHIP 7 chan 2
hTimesweeps

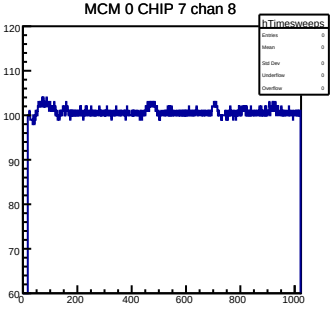

MCM 0 CHIP 7 chan 3
hTimesweeps

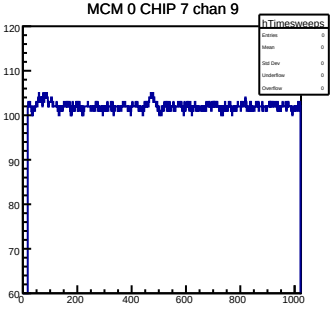

MCM 0 CHIP 7 chan 4
hTimesweeps

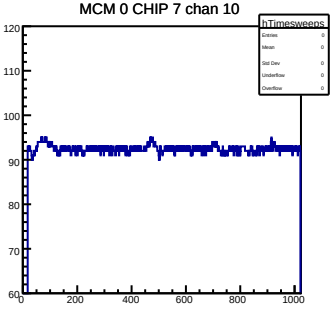

MCM 0 CHIP 7 chan 5
hTimesweeps

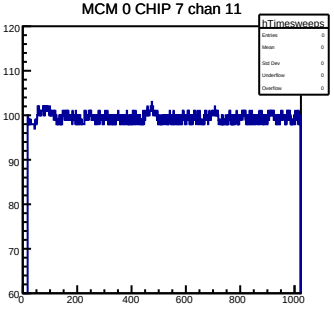

MCM 0 CHIP 7 chan 6
hTimesweeps

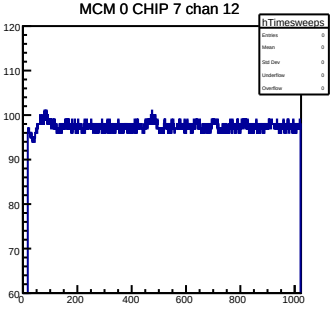

MCM 0 CHIP 7 chan 7
hTimesweeps

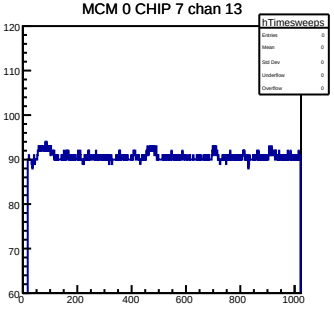

MCM 0 CHIP 7 chan 8
hTimesweeps

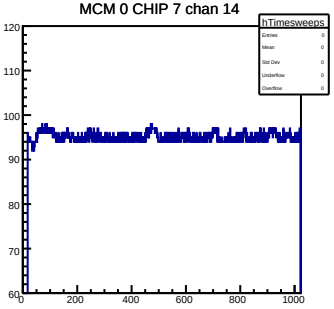

MCM 0 CHIP 7 chan 9
hTimesweeps

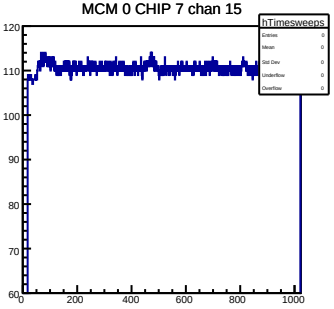

MCM 0 CHIP 7 chan 10
hTimesweeps

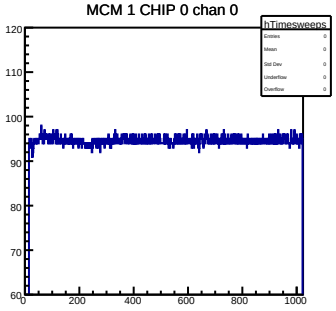

MCM 0 CHIP 7 chan 11
hTimesweeps

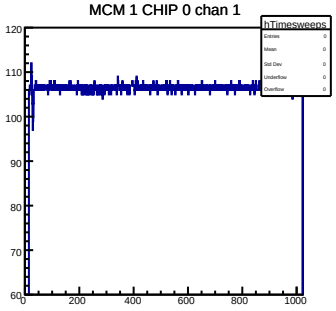

MCM 0 CHIP 7 chan 12
hTimesweeps

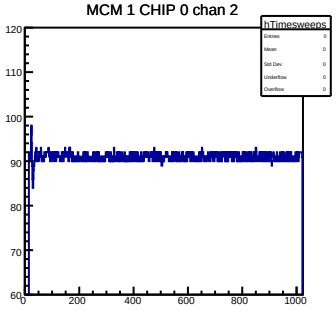

MCM 0 CHIP 7 chan 13
hTimesweeps

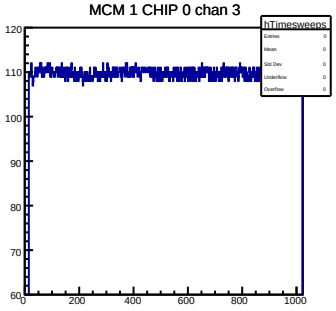

MCM 0 CHIP 7 chan 14
hTimesweeps

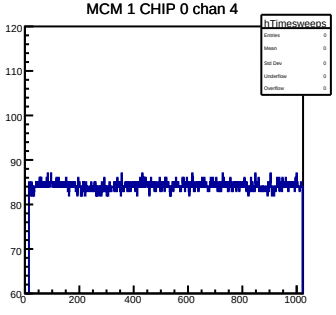

MCM 0 CHIP 7 chan 15
hTimesweeps

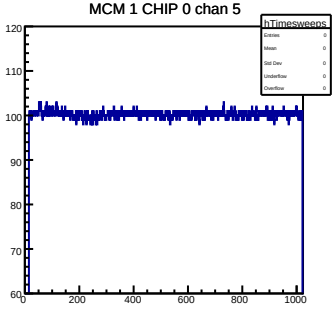

MCM 1 CHIP 0 chan 0
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
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600
800
1000

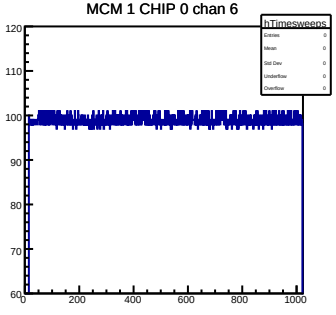

MCM 1 CHIP 0 chan 1
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

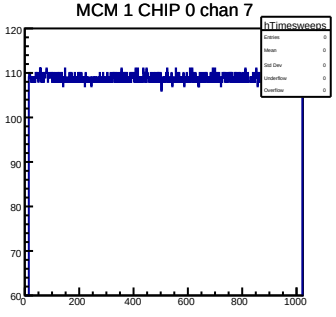

MCM 1 CHIP 0 chan 2
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

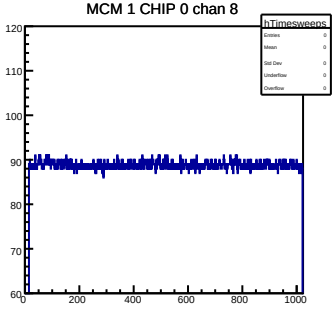

MCM 1 CHIP 0 chan 3
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

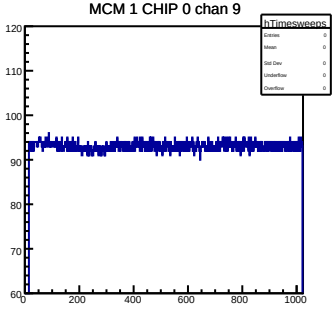

MCM 1 CHIP 0 chan 4
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

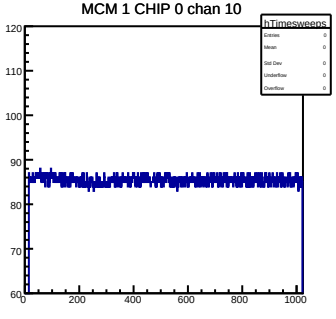

MCM 1 CHIP 0 chan 5
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

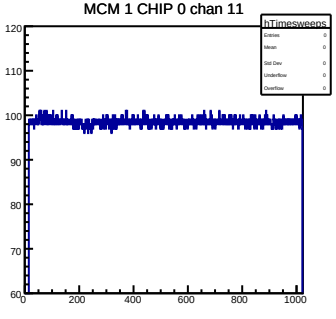

MCM 1 CHIP 0 chan 6
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

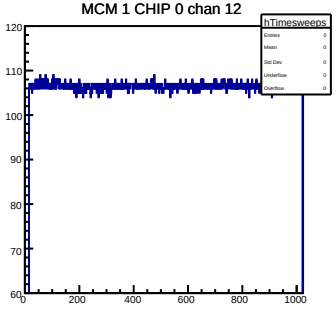

MCM 1 CHIP 0 chan 7
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

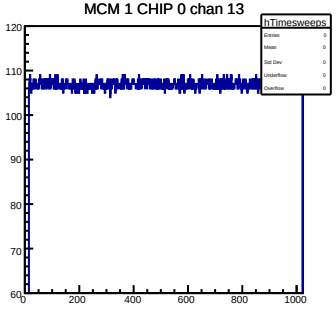

MCM 1 CHIP 0 chan 8
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

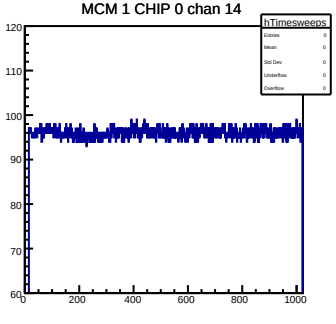

MCM 1 CHIP 0 chan 9
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
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400
600
800
1000

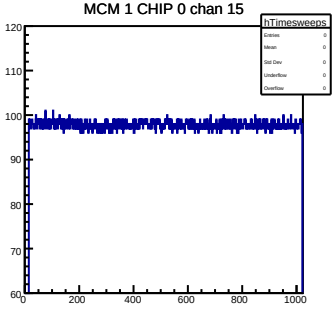

MCM 1 CHIP 0 chan 10
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
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70
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800
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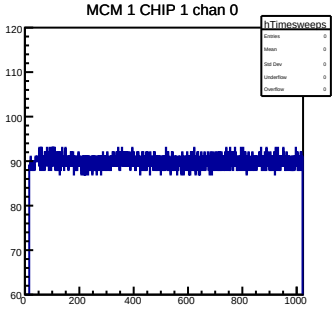

MCM 1 CHIP 0 chan 11
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
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70
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0
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400
600
800
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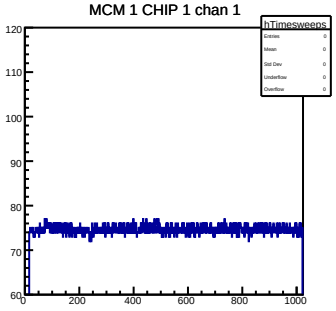

MCM 1 CHIP 0 chan 12
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
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110
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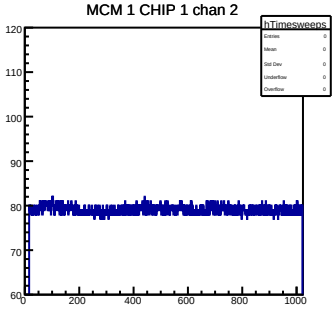

MCM 1 CHIP 0 chan 13
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
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70
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800
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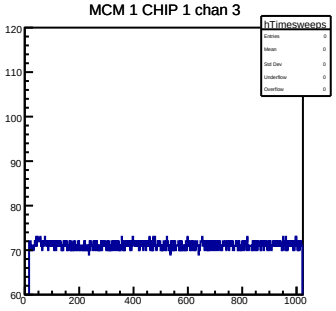

MCM 1 CHIP 0 chan 14
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
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70
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200
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800
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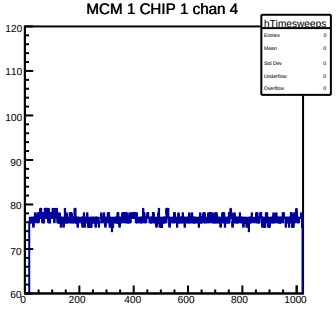

MCM 1 CHIP 0 chan 15
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

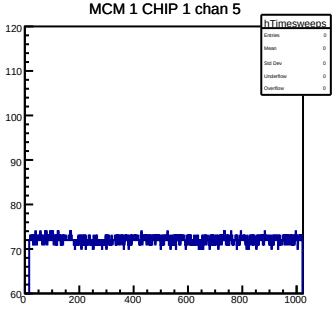

MCM 1 CHIP 1 chan 0
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
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110
100
90
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70
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0
200
400
600
800
1000

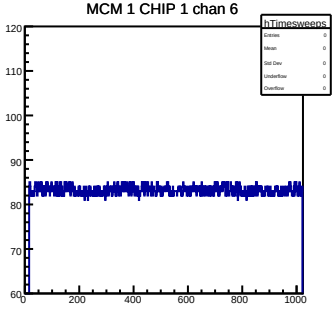

MCM 1 CHIP 1 chan 1
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
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70
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0
200
400
600
800
1000

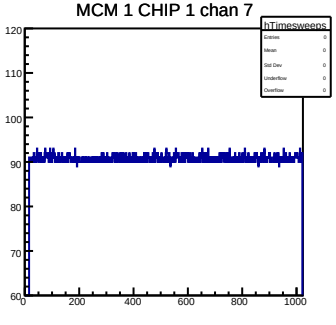

MCM 1 CHIP 1 chan 2
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

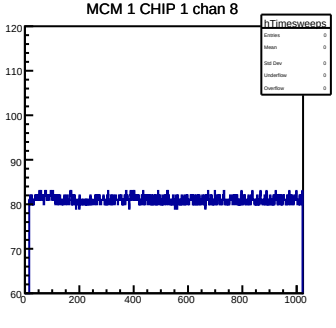

MCM 1 CHIP 1 chan 3
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

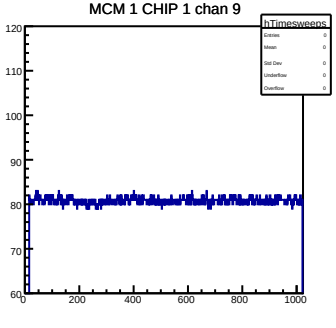

MCM 1 CHIP 1 chan 4
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

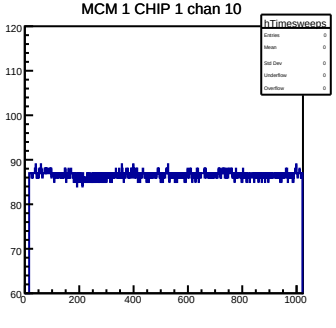

MCM 1 CHIP 1 chan 5
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

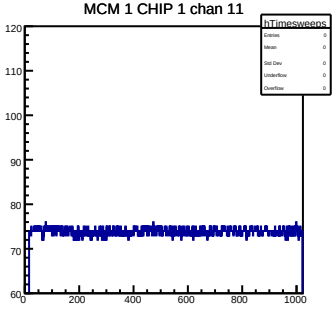

MCM 1 CHIP 1 chan 6
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

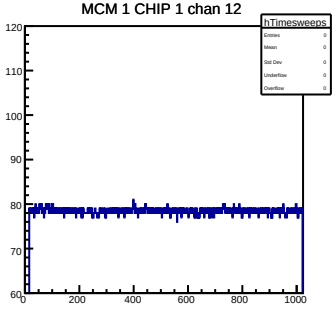

MCM 1 CHIP 1 chan 7
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

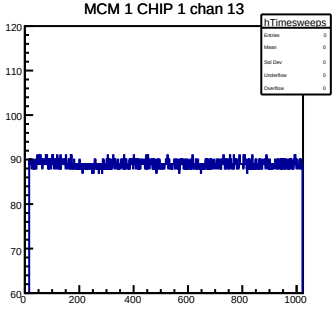

MCM 1 CHIP 1 chan 8
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

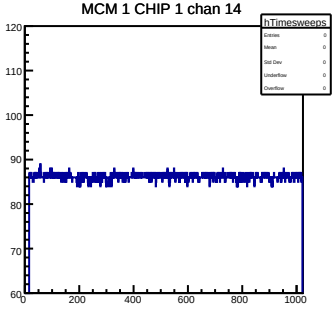

MCM 1 CHIP 1 chan 9
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
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70
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0
200
400
600
800
1000

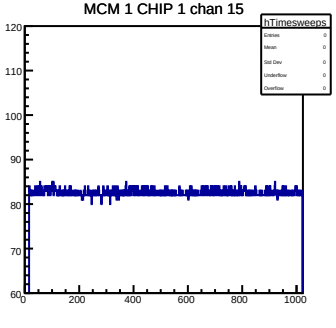

MCM 1 CHIP 1 chan 10
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

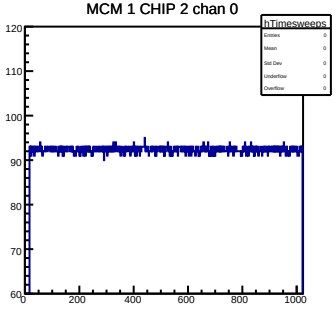

MCM 1 CHIP 1 chan 11
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
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70
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0
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600
800
1000

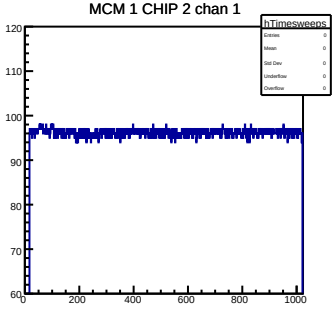

MCM 1 CHIP 1 chan 12
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
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70
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0
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400
600
800
1000

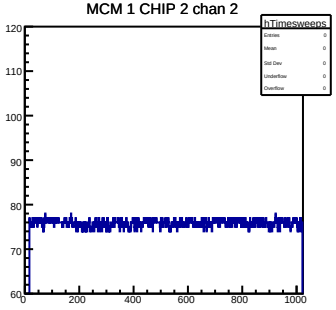

MCM 1 CHIP 1 chan 13
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
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70
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0
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600
800
1000

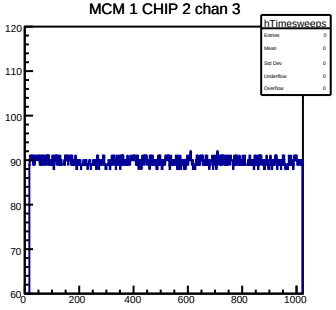

MCM 1 CHIP 1 chan 14
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
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110
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70
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400
600
800
1000

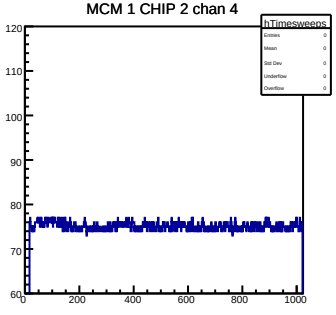

MCM 1 CHIP 1 chan 15
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
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70
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0
200
400
600
800
1000

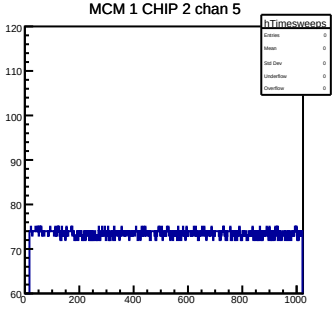

MCM 1 CHIP 2 chan 0
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
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110
100
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70
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600
800
1000

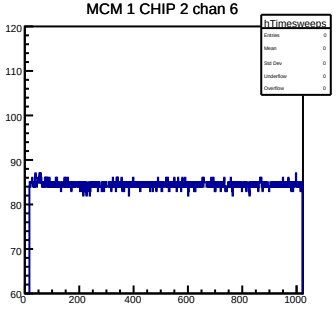

MCM 1 CHIP 2 chan 1
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
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90
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800
1000

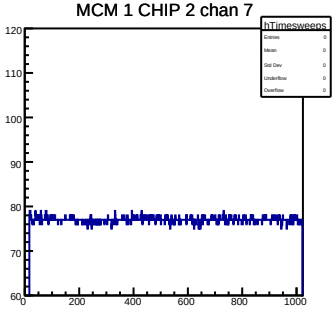

MCM 1 CHIP 2 chan 2
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

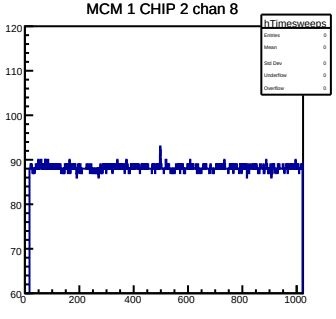

MCM 1 CHIP 2 chan 3
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
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100
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600
800
1000

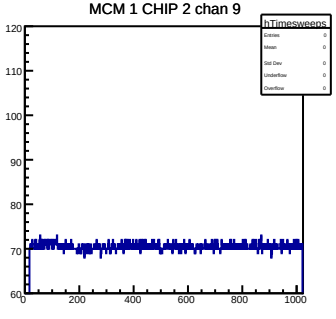

MCM 1 CHIP 2 chan 4
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

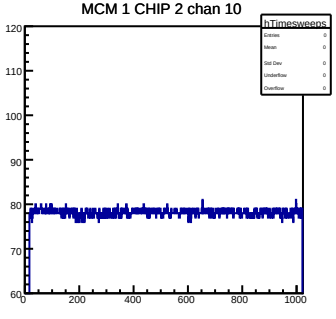

MCM 1 CHIP 2 chan 5
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
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70
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0
200
400
600
800
1000

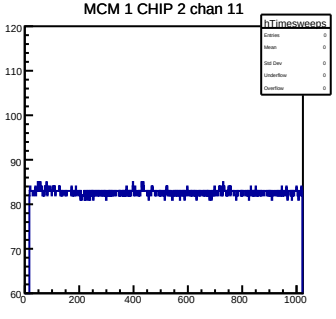

MCM 1 CHIP 2 chan 6
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

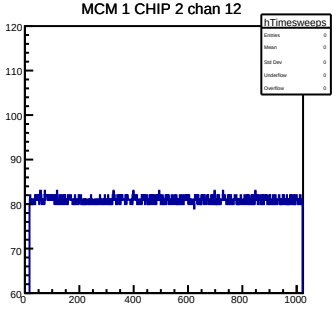

MCM 1 CHIP 2 chan 7
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

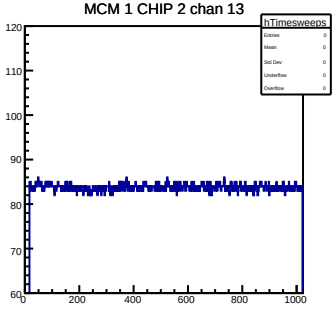

MCM 1 CHIP 2 chan 8
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
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70
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0
200
400
600
800
1000

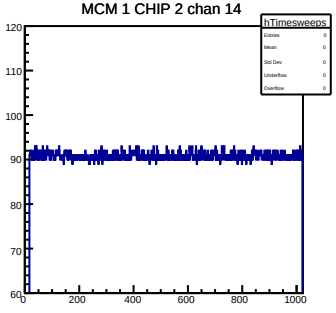

MCM 1 CHIP 2 chan 9
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

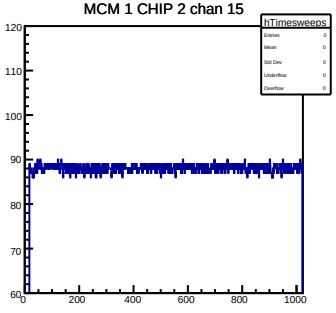

MCM 1 CHIP 2 chan 10
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

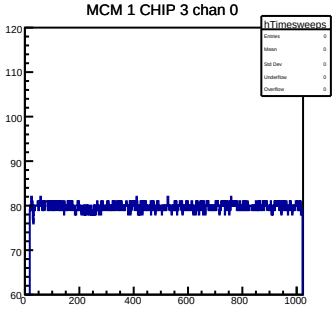

MCM 1 CHIP 2 chan 11
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

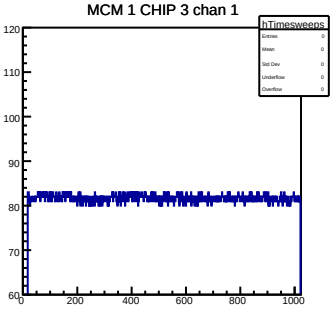

MCM 1 CHIP 2 chan 12
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

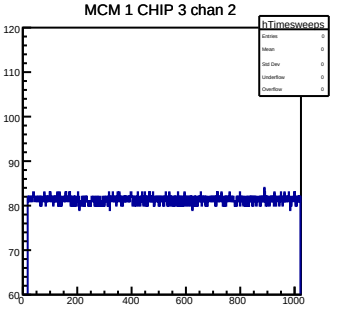

MCM 1 CHIP 2 chan 13
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
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100
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80
70
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400
600
800
1000

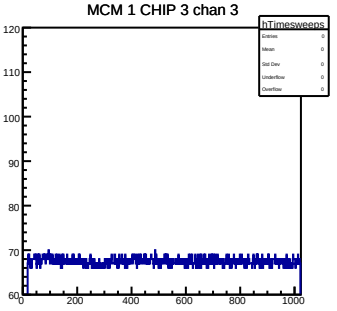

MCM 1 CHIP 2 chan 14
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

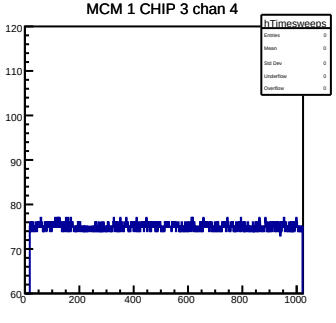

MCM 1 CHIP 2 chan 15
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

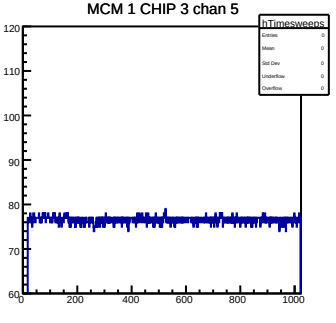

MCM 1 CHIP 3 chan 0
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

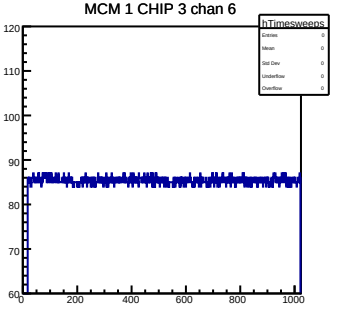

MCM 1 CHIP 3 chan 1
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

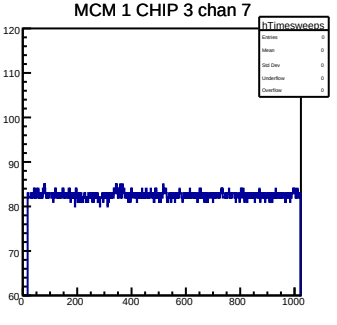

MCM 1 CHIP 3 chan 2
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

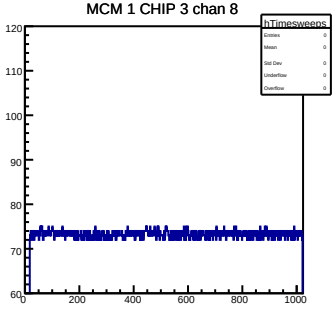

MCM 1 CHIP 3 chan 3
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

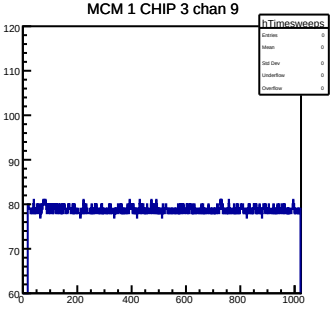

MCM 1 CHIP 3 chan 4
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

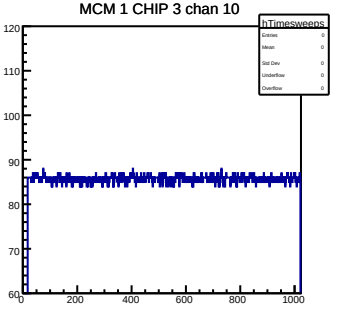

MCM 1 CHIP 3 chan 5
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

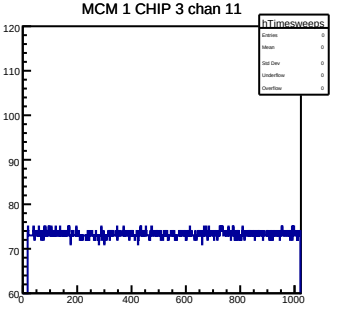

MCM 1 CHIP 3 chan 6
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

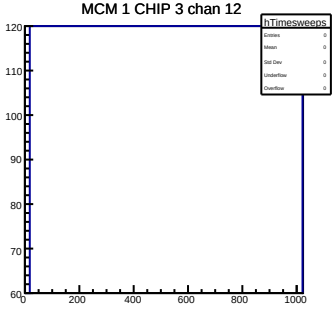

MCM 1 CHIP 3 chan 7
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

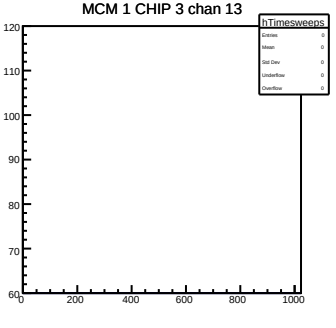

MCM 1 CHIP 3 chan 8
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

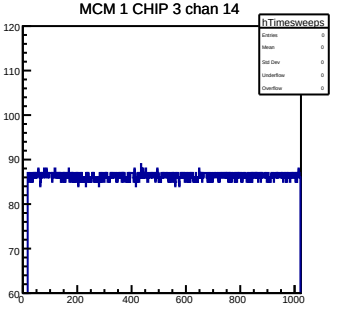

MCM 1 CHIP 3 chan 9
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

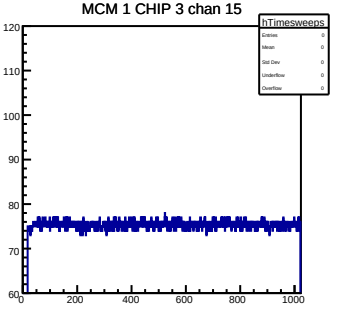

MCM 1 CHIP 3 chan 10
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

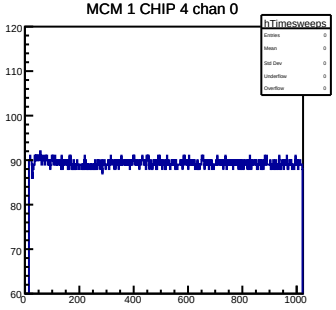

MCM 1 CHIP 3 chan 11
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

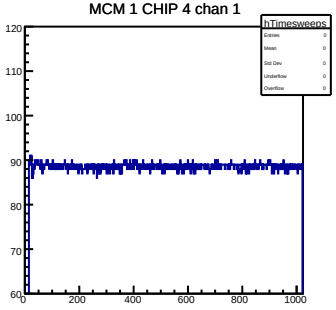

MCM 1 CHIP 3 chan 12
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

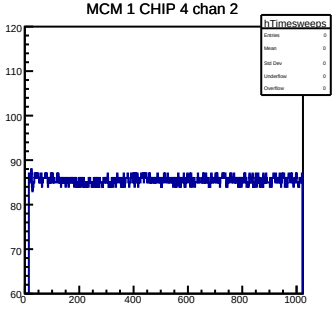

MCM 1 CHIP 3 chan 13
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

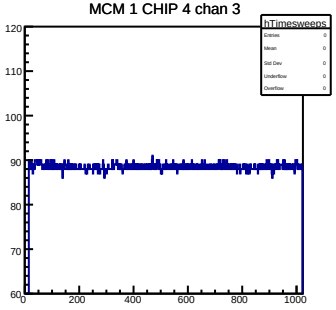

MCM 1 CHIP 3 chan 14
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

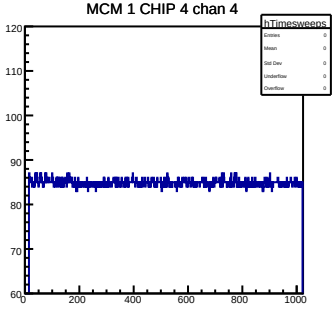

MCM 1 CHIP 3 chan 15
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

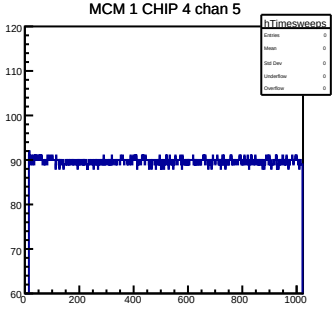

MCM 1 CHIP 4 chan 0
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

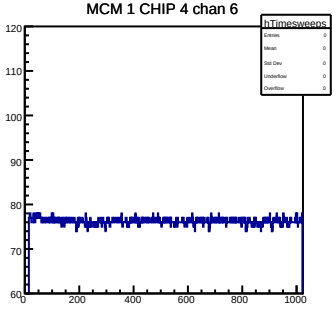

MCM 1 CHIP 4 chan 1
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

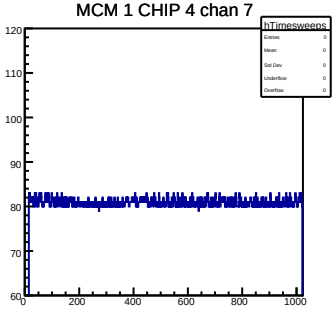

MCM 1 CHIP 4 chan 2
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

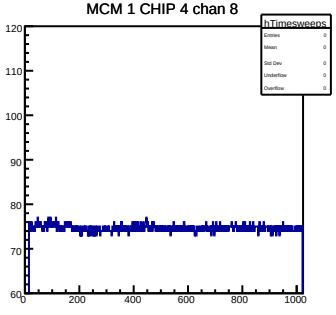

MCM 1 CHIP 4 chan 3
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

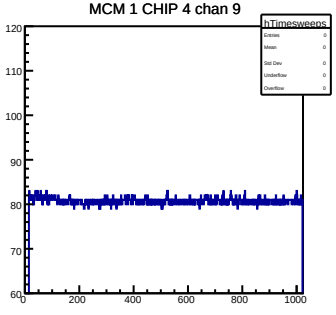

MCM 1 CHIP 4 chan 4
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

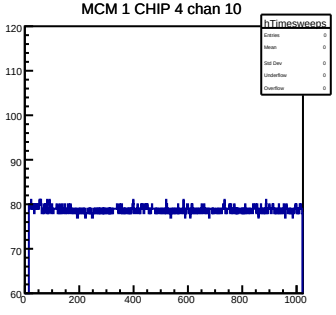

MCM 1 CHIP 4 chan 5
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

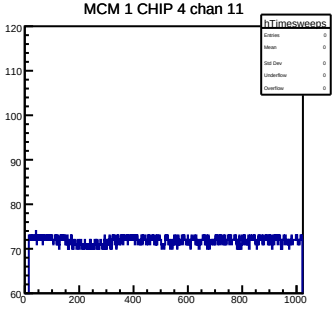

MCM 1 CHIP 4 chan 6
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

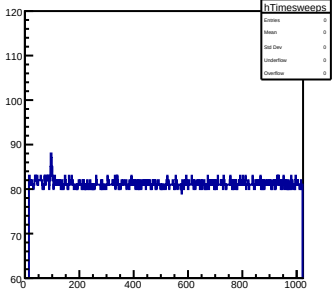

MCM 1 CHIP 4 chan 7
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

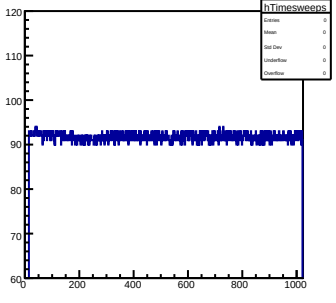

MCM 1 CHIP 4 chan 8
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

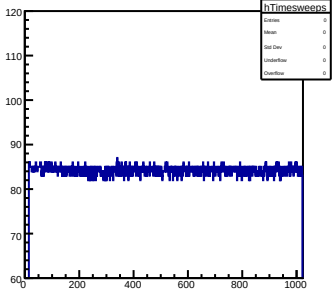

MCM 1 CHIP 4 chan 9
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

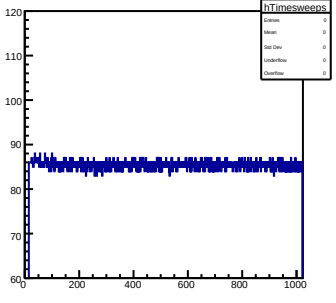

MCM 1 CHIP 4 chan 10
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

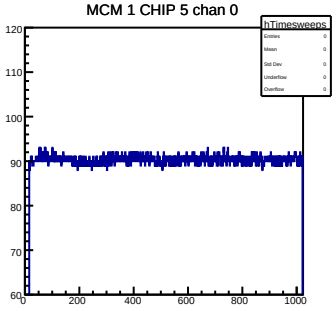

MCM 1 CHIP 4 chan 11
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

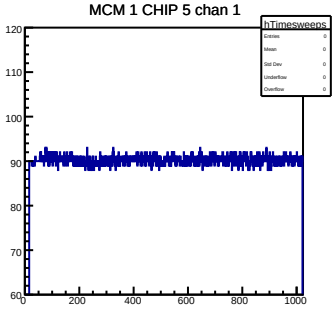

MCM 1 CHIP 4 chan 12
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

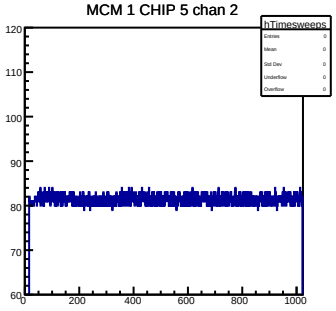

MCM 1 CHIP 4 chan 13
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

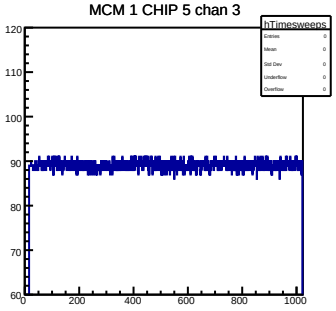

MCM 1 CHIP 4 chan 14
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

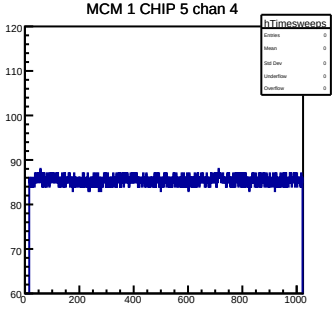

MCM 1 CHIP 4 chan 15
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

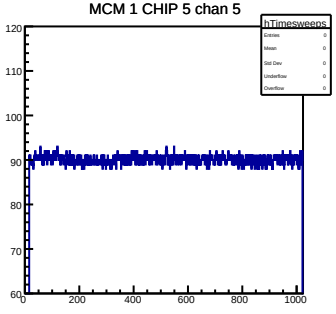

MCM 1 CHIP 5 chan 0
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

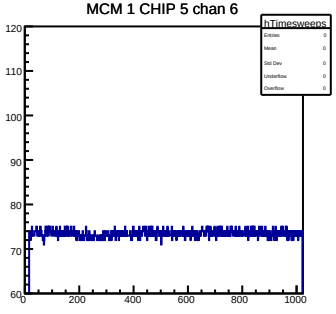

MCM 1 CHIP 5 chan 1
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

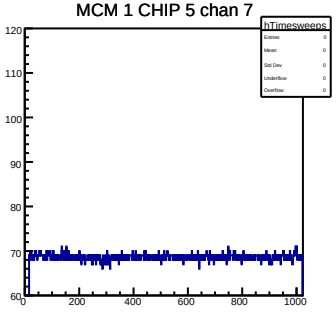

MCM 1 CHIP 5 chan 2
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

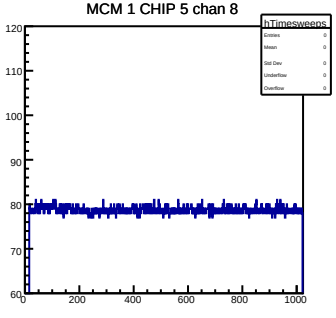

MCM 1 CHIP 5 chan 3
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

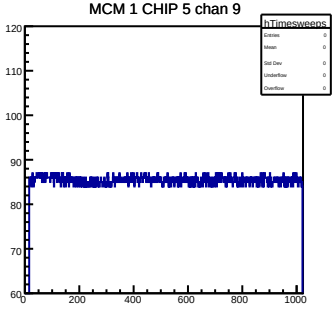

MCM 1 CHIP 5 chan 4
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

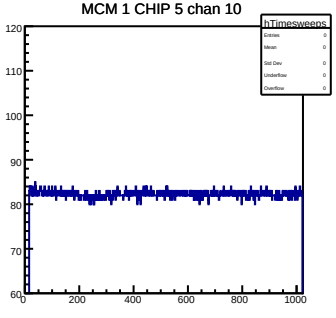

MCM 1 CHIP 5 chan 5
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

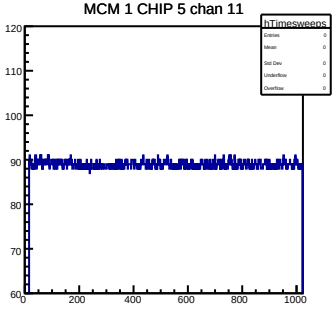

MCM 1 CHIP 5 chan 6
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

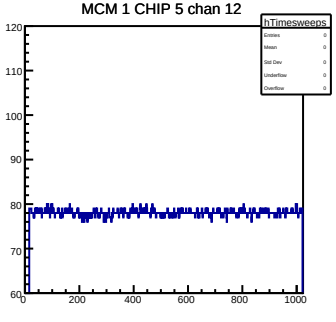

MCM 1 CHIP 5 chan 7
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

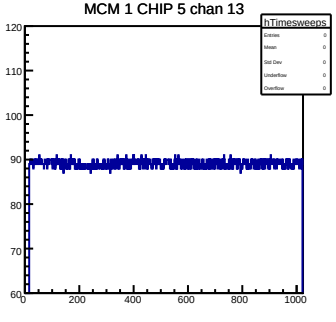

MCM 1 CHIP 5 chan 8
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
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70
60
0
200
400
600
800
1000

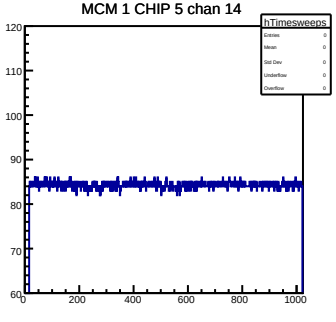

MCM 1 CHIP 5 chan 9
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

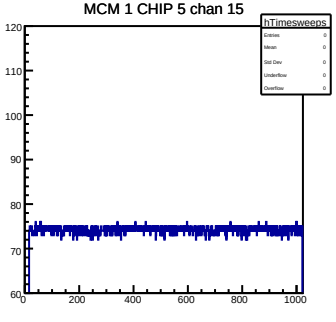

MCM 1 CHIP 5 chan 10
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

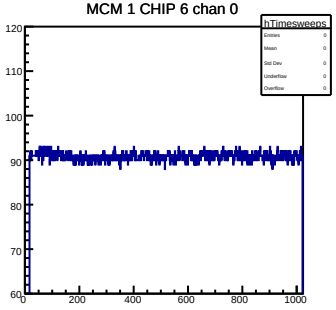

MCM 1 CHIP 5 chan 11
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

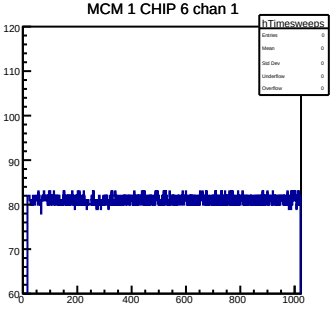

MCM 1 CHIP 5 chan 12
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

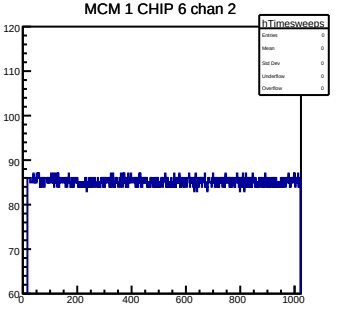

MCM 1 CHIP 5 chan 13
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

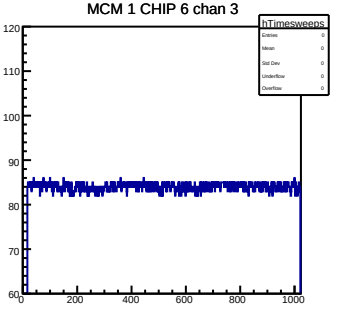

MCM 1 CHIP 5 chan 14
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

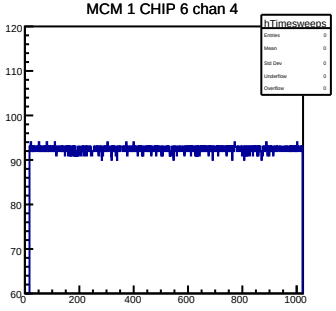

MCM 1 CHIP 5 chan 15
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

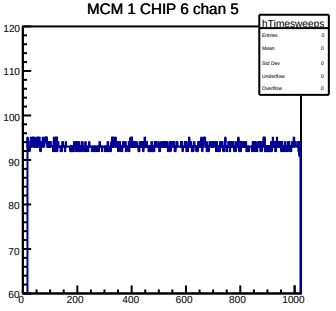

MCM 1 CHIP 6 chan 0
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

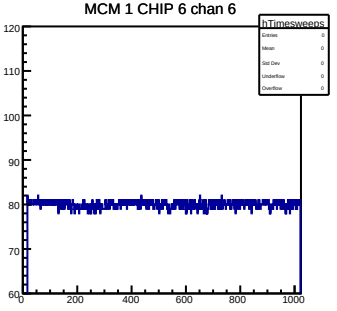

MCM 1 CHIP 6 chan 1
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

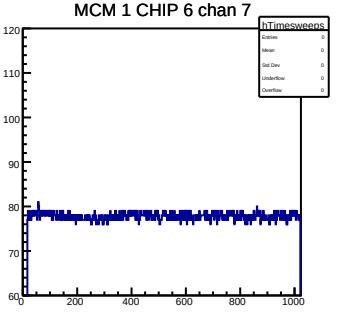

MCM 1 CHIP 6 chan 2
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

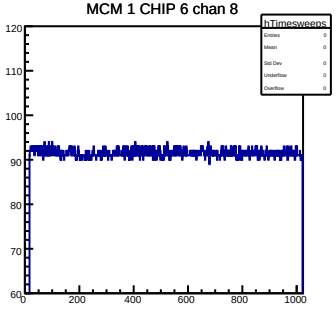

MCM 1 CHIP 6 chan 3
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

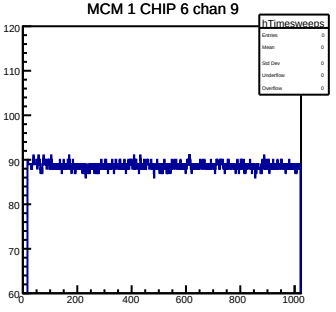

MCM 1 CHIP 6 chan 4
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

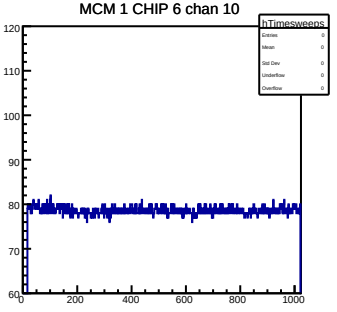

MCM 1 CHIP 6 chan 5
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

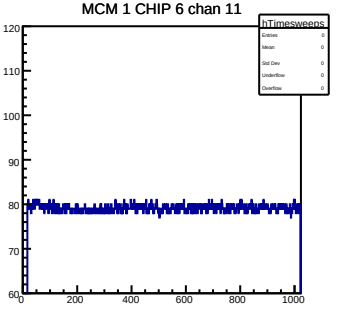

MCM 1 CHIP 6 chan 6
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

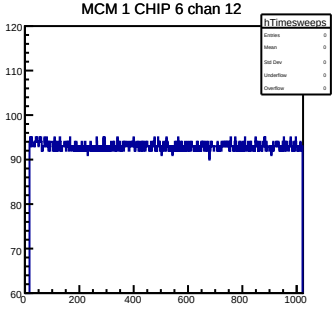

MCM 1 CHIP 6 chan 7
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

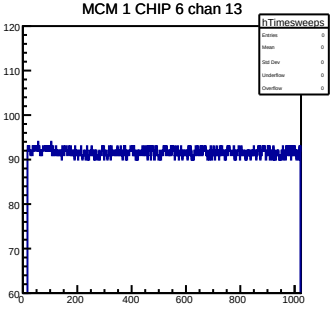

MCM 1 CHIP 6 chan 8
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

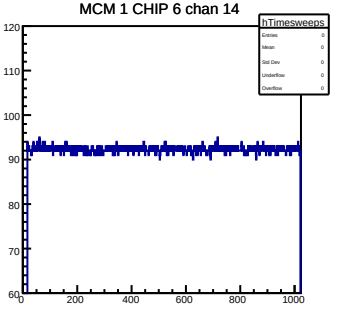

MCM 1 CHIP 6 chan 9
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

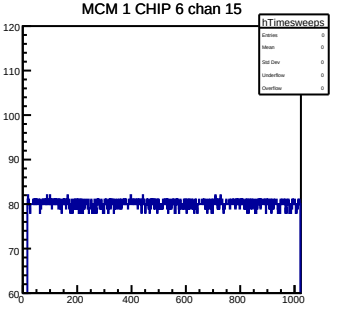

MCM 1 CHIP 6 chan 10
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

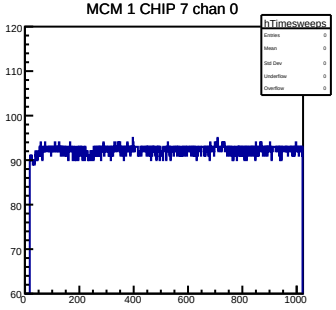

MCM 1 CHIP 6 chan 11
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

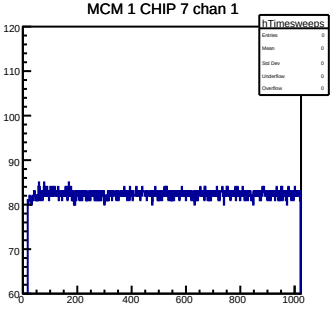

MCM 1 CHIP 6 chan 12
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

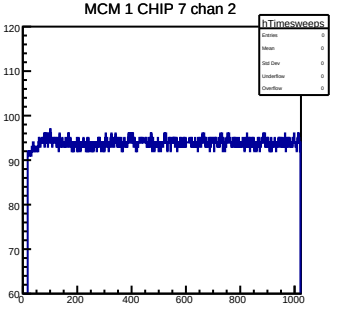

MCM 1 CHIP 6 chan 13
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
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70
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0
200
400
600
800
1000

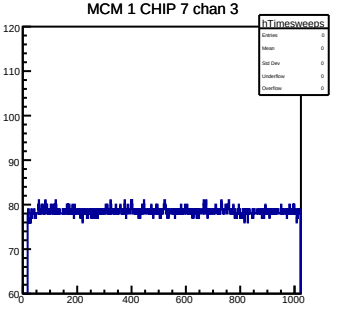

MCM 1 CHIP 6 chan 14
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

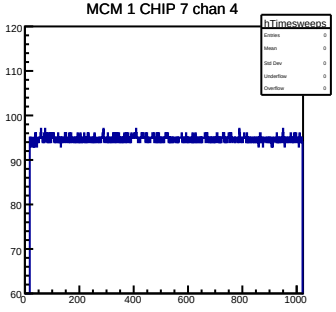

MCM 1 CHIP 6 chan 15
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

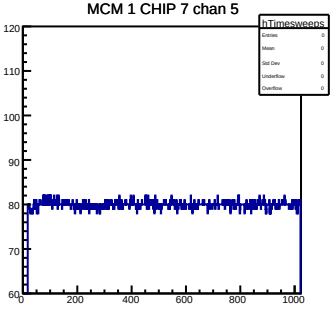

MCM 1 CHIP 7 chan 0
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

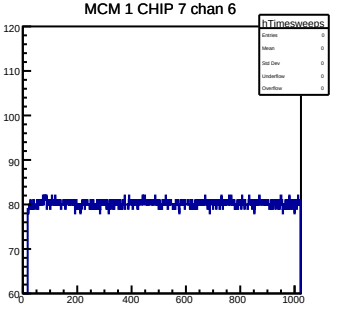

MCM 1 CHIP 7 chan 1
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

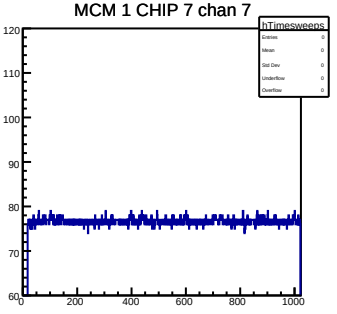

MCM 1 CHIP 7 chan 2
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

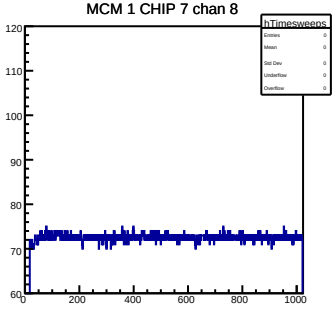

MCM 1 CHIP 7 chan 3
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

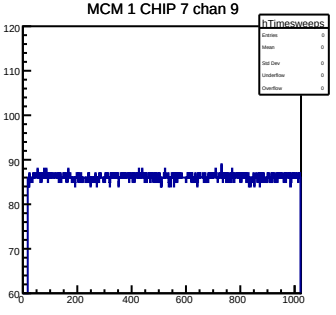

MCM 1 CHIP 7 chan 4
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

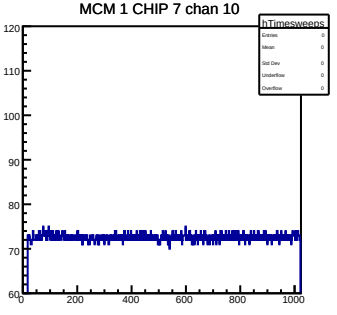

MCM 1 CHIP 7 chan 5
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

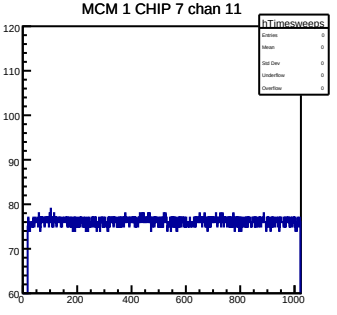

MCM 1 CHIP 7 chan 6
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

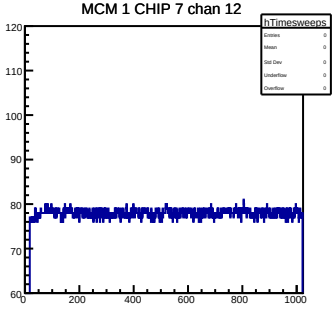

MCM 1 CHIP 7 chan 7
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
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0
200
400
600
800
1000

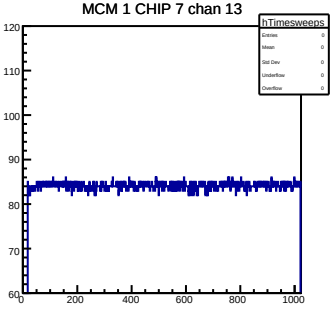

MCM 1 CHIP 7 chan 8
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

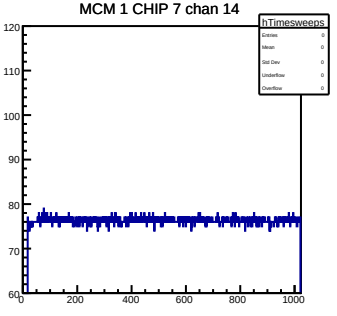

MCM 1 CHIP 7 chan 9
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000

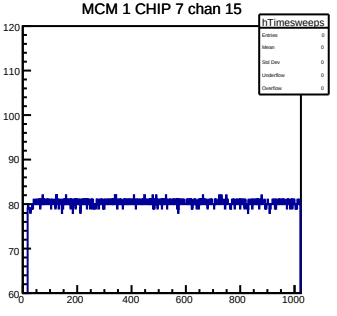

MCM 1 CHIP 7 chan 10
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000


MCM 1 CHIP 7 chan 11
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000


MCM 1 CHIP 7 chan 12
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000


MCM 1 CHIP 7 chan 13
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000


MCM 1 CHIP 7 chan 14
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000


MCM 1 CHIP 7 chan 15
hTimesweeps
Entries 0
Mean 0
Std Dev 0
Underflow 0
Overflow 0
120
110
100
90
80
70
60
0
200
400
600
800
1000