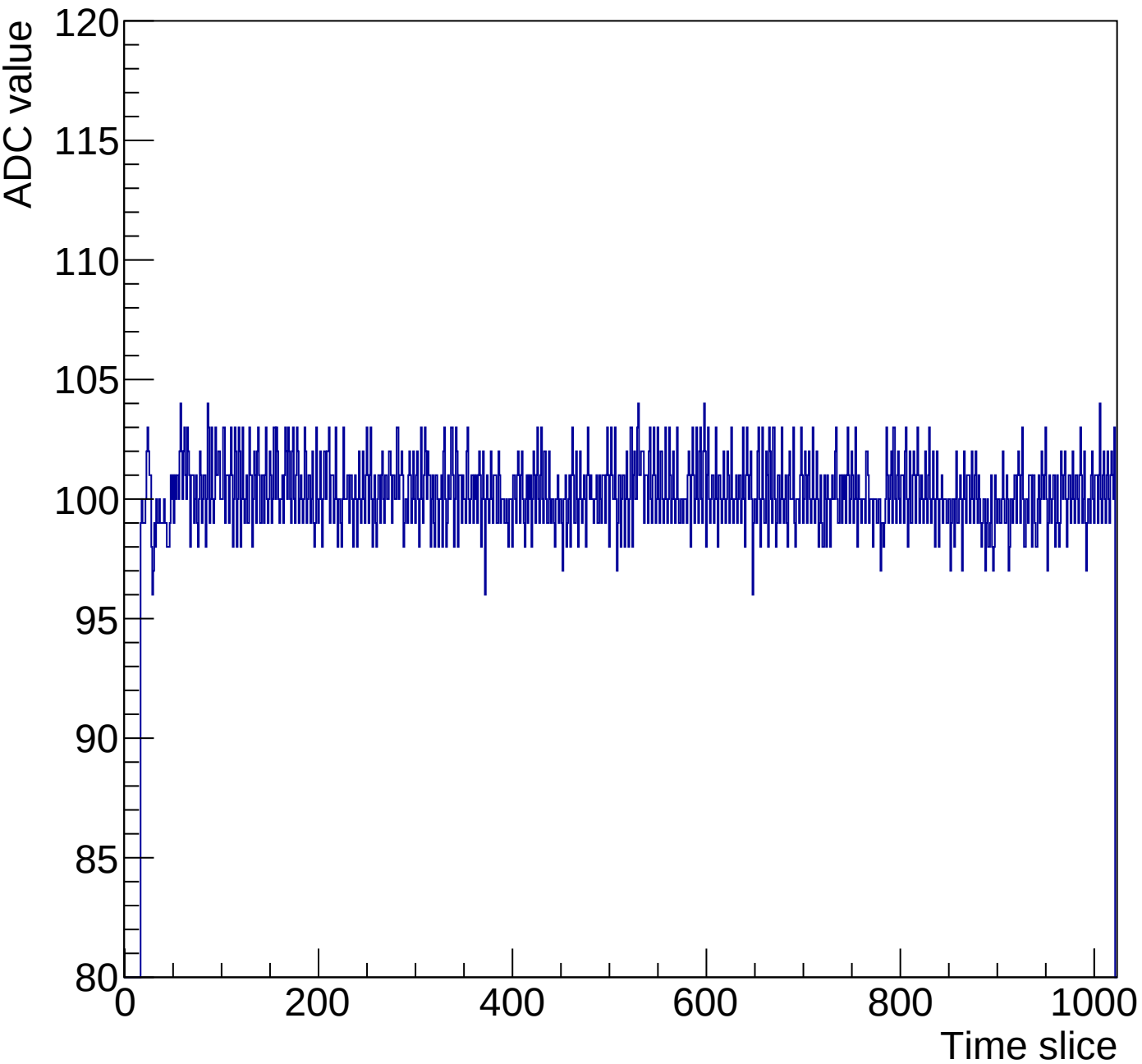
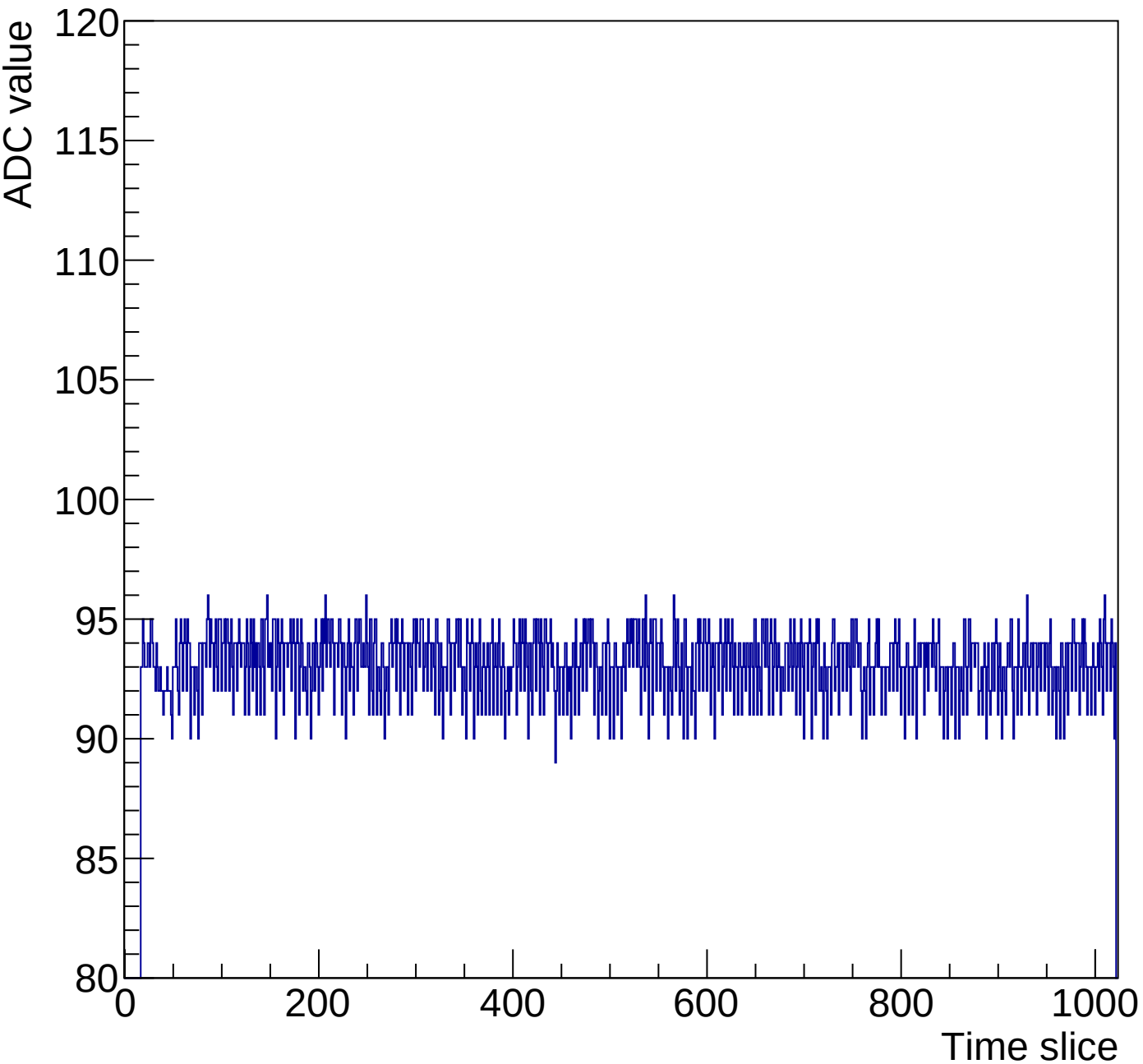


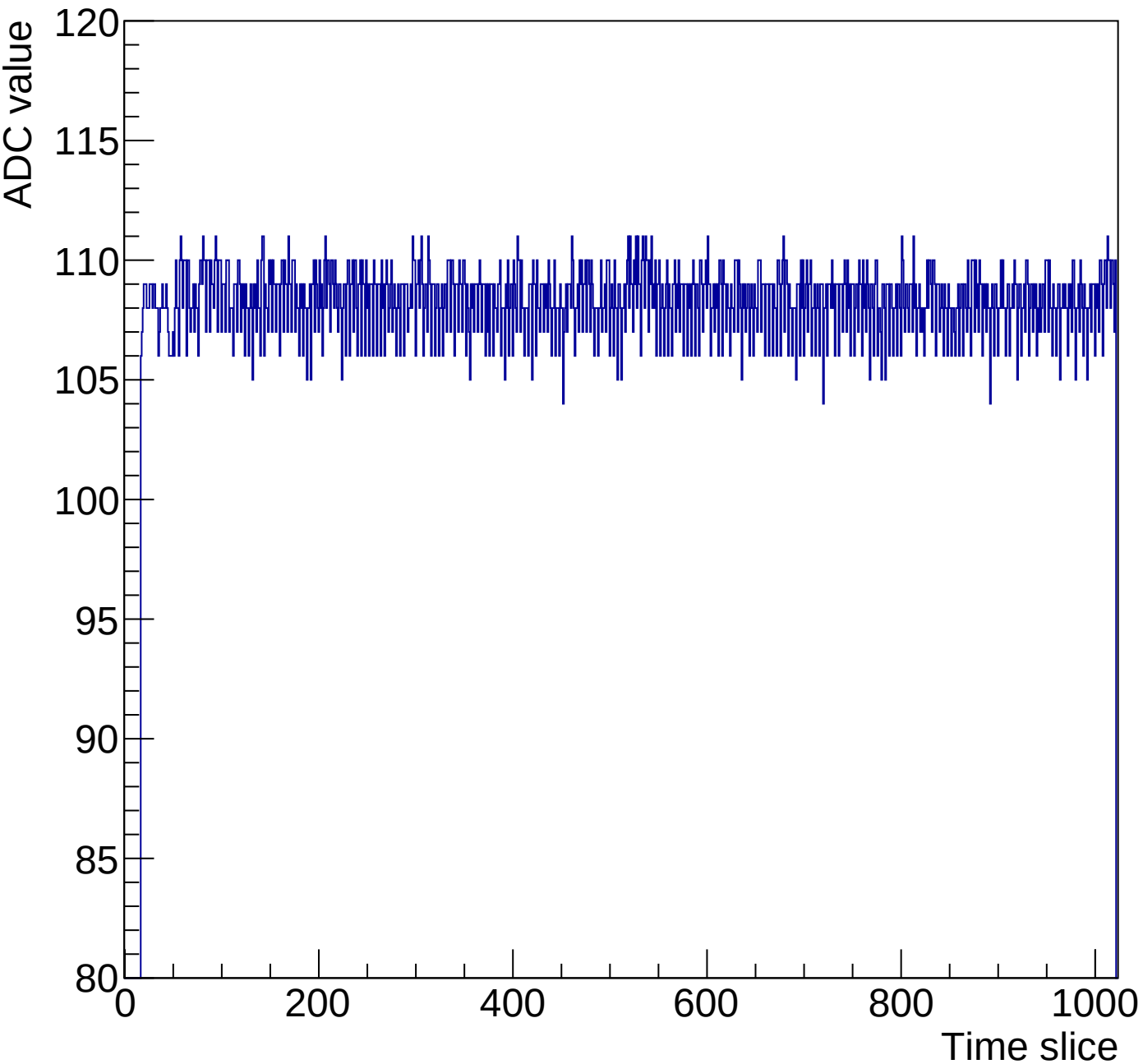
Run 1 event 100 mcm 0 chip 3 channel 0 full



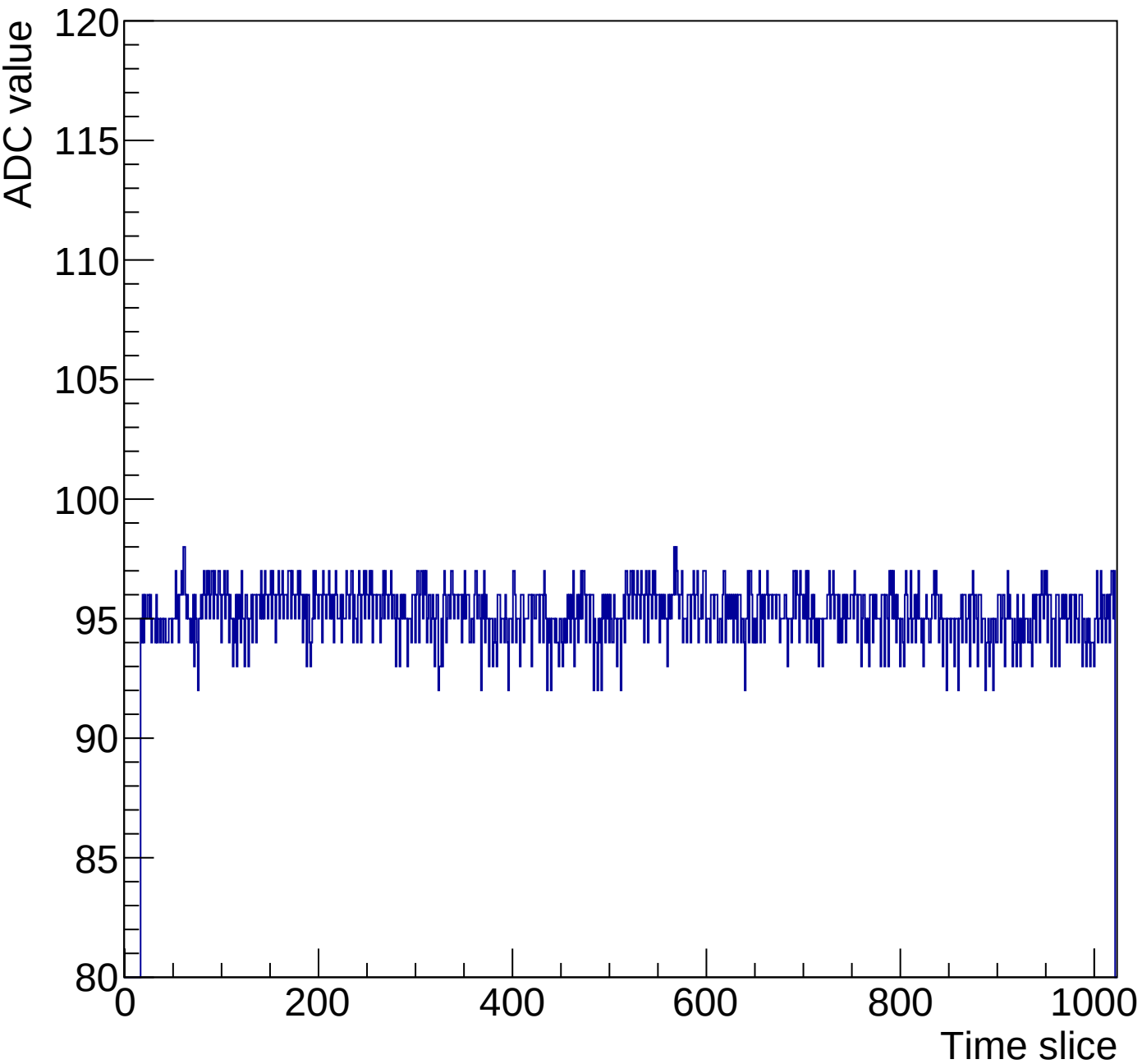
Run 1 event 100 mcm 0 chip 3 channel 1 full



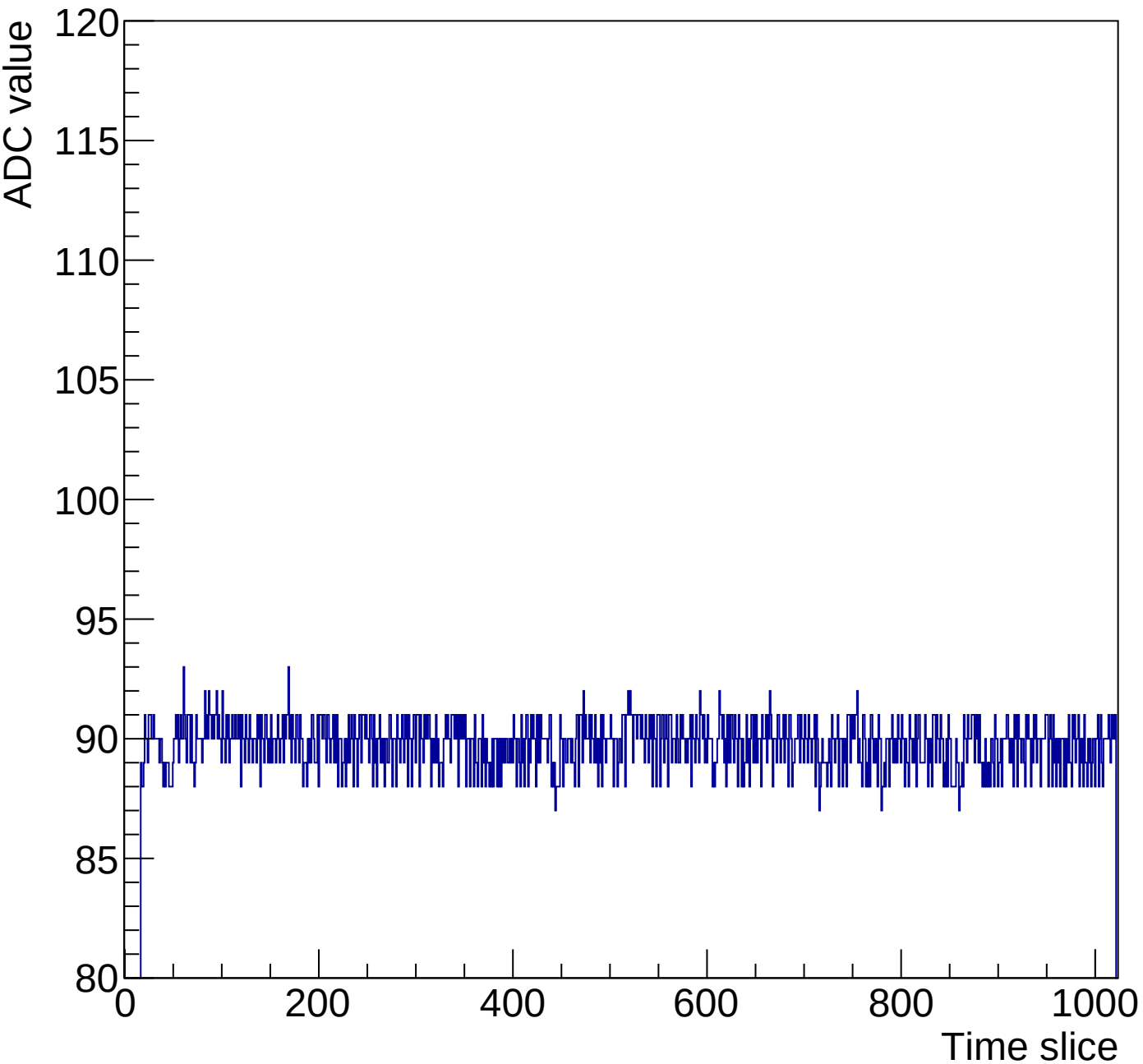
Run 1 event 100 mcm 0 chip 3 channel 2 full



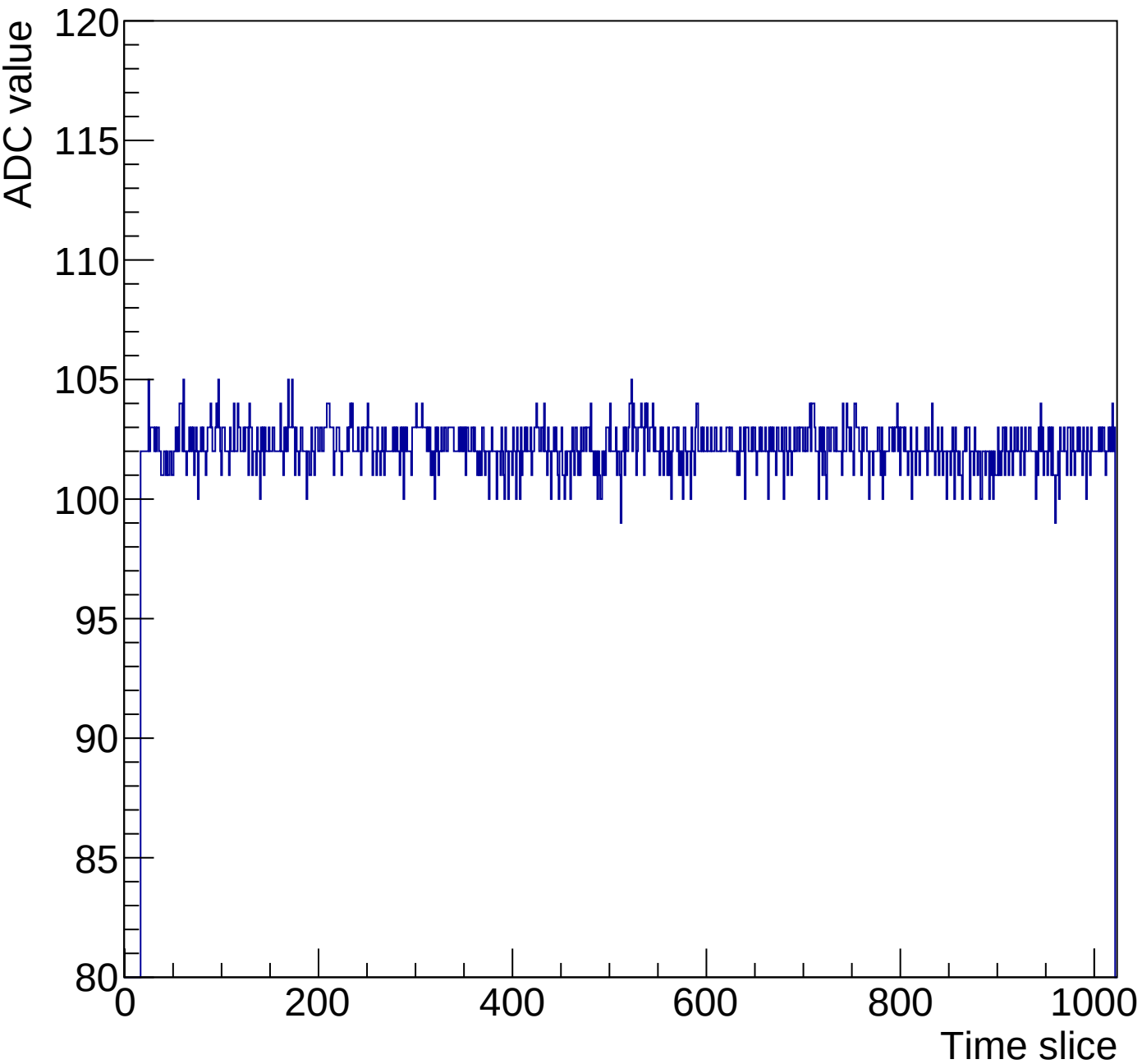
Run 1 event 100 mcm 0 chip 3 channel 3 full



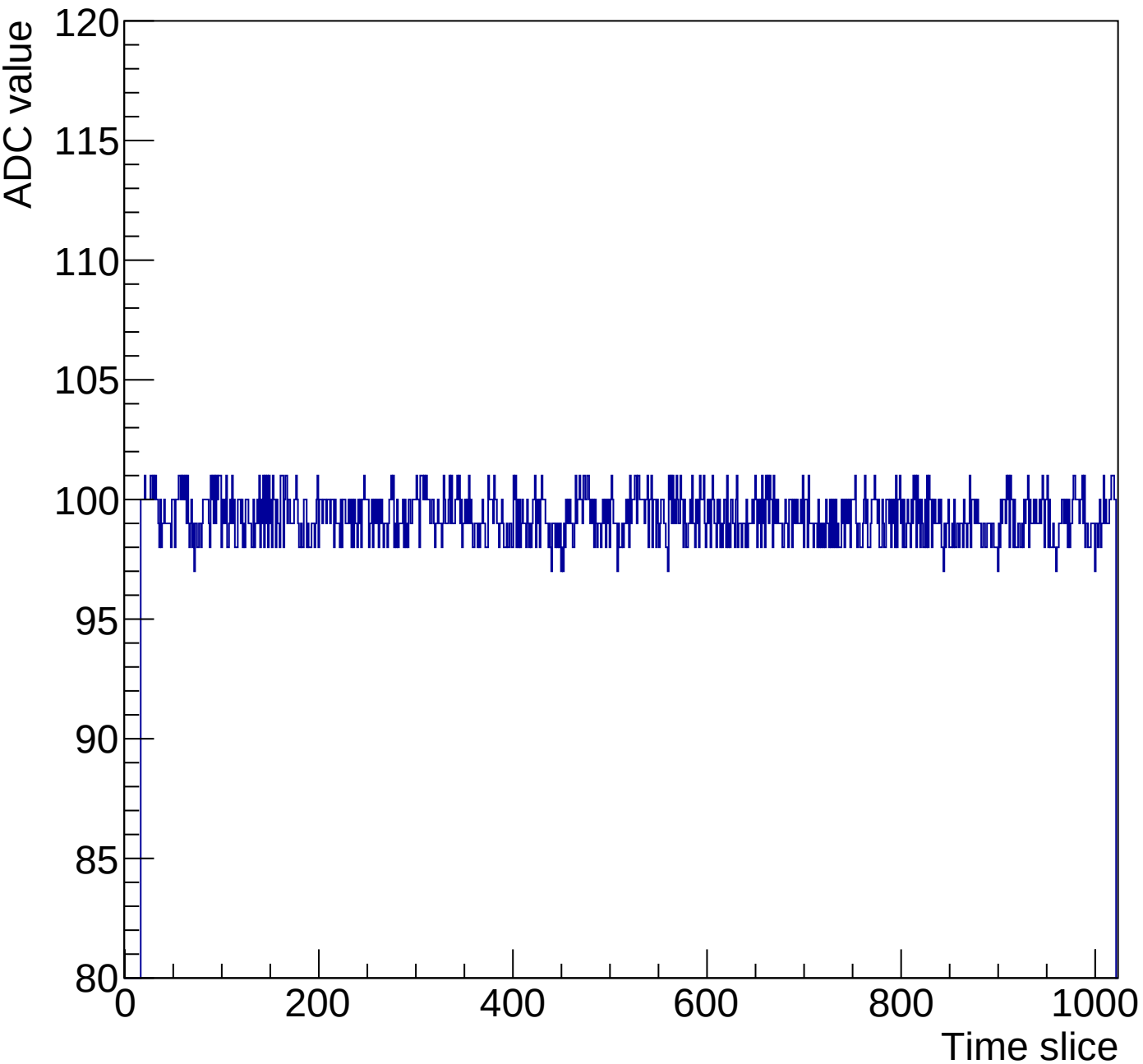
Run 1 event 100 mcm 0 chip 3 channel 4 full



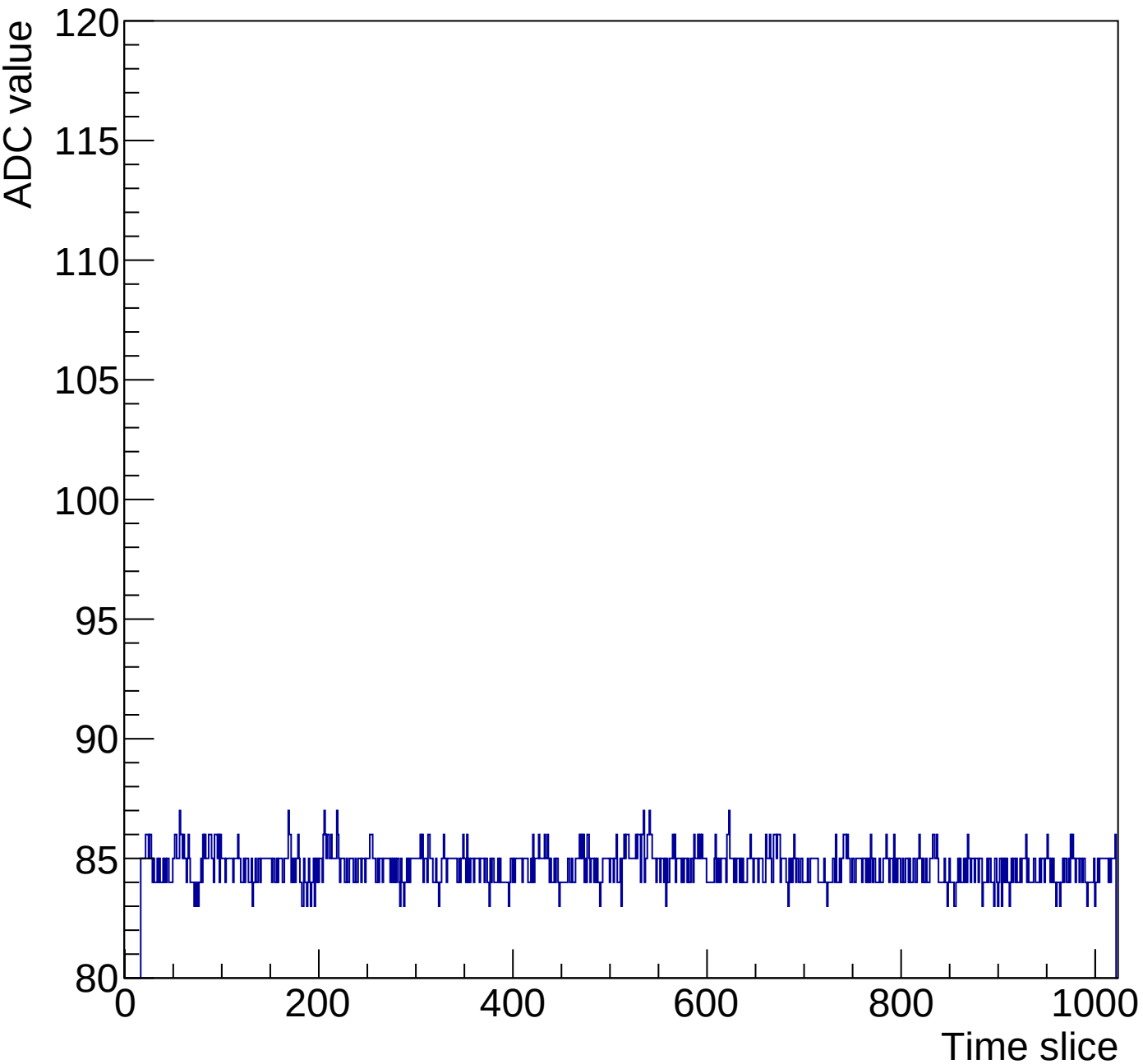
Run 1 event 100 mcm 0 chip 3 channel 5 full



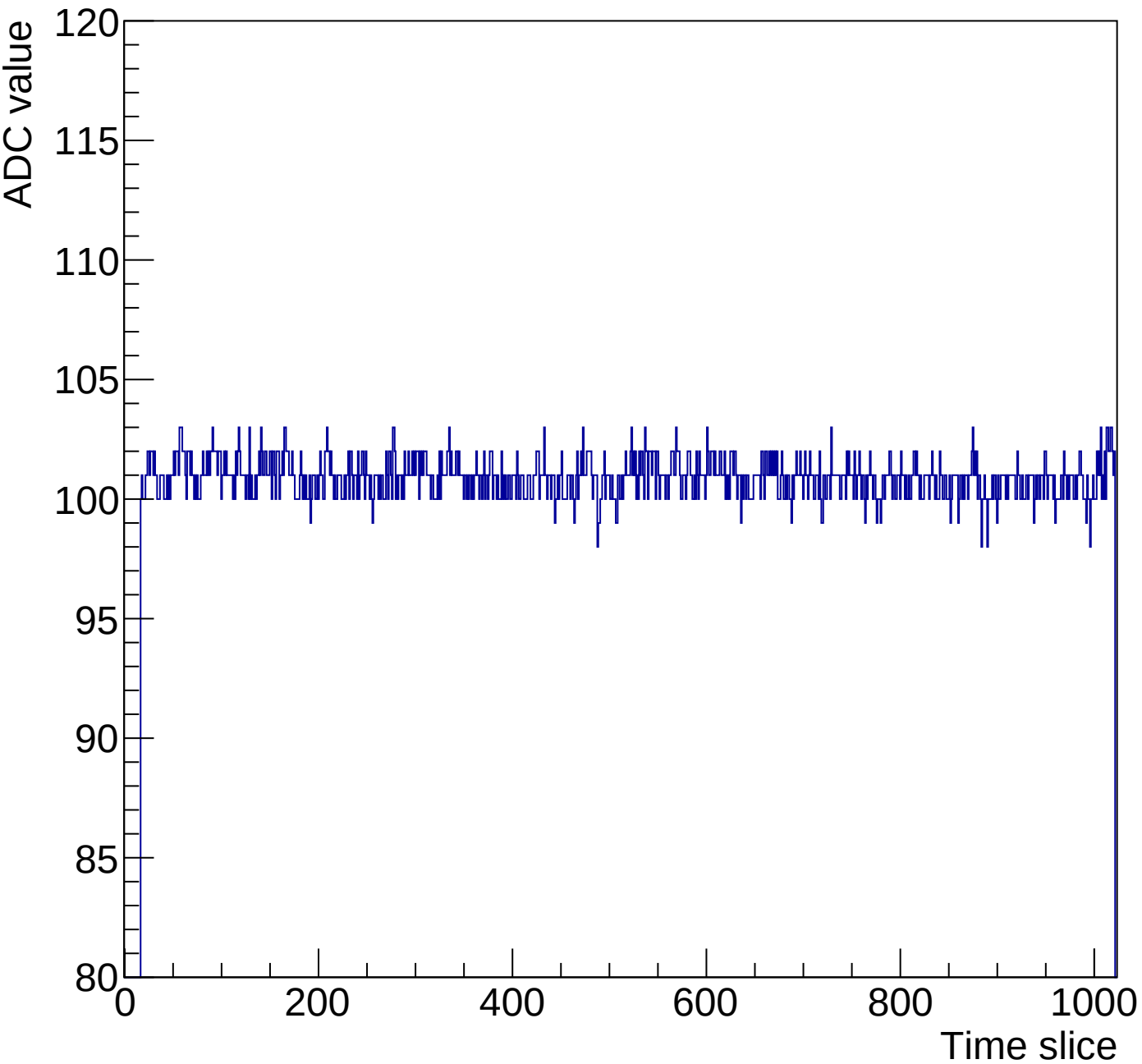
Run 1 event 100 mcm 0 chip 3 channel 6 full



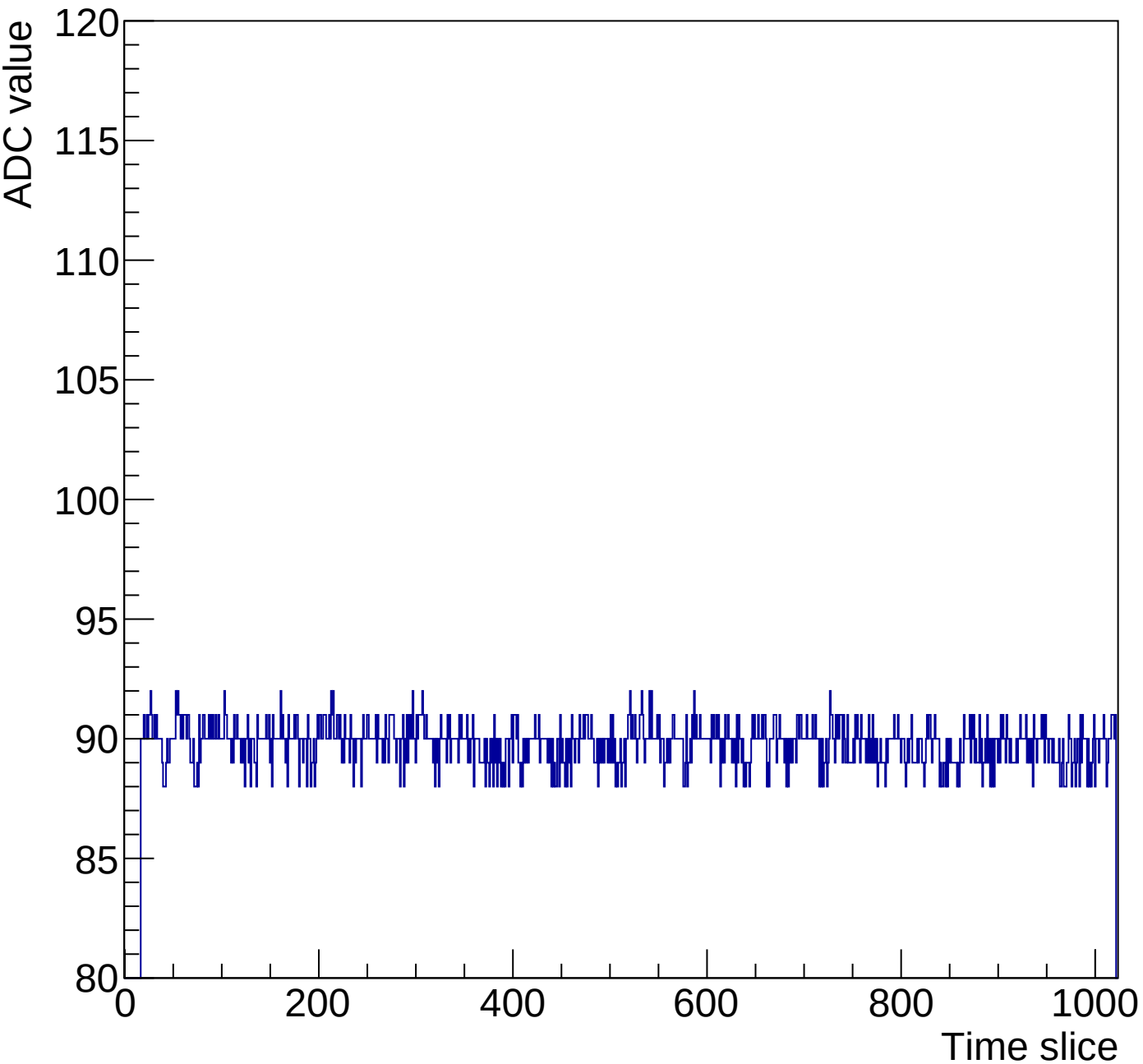
Run 1 event 100 mcm 0 chip 3 channel 7 full



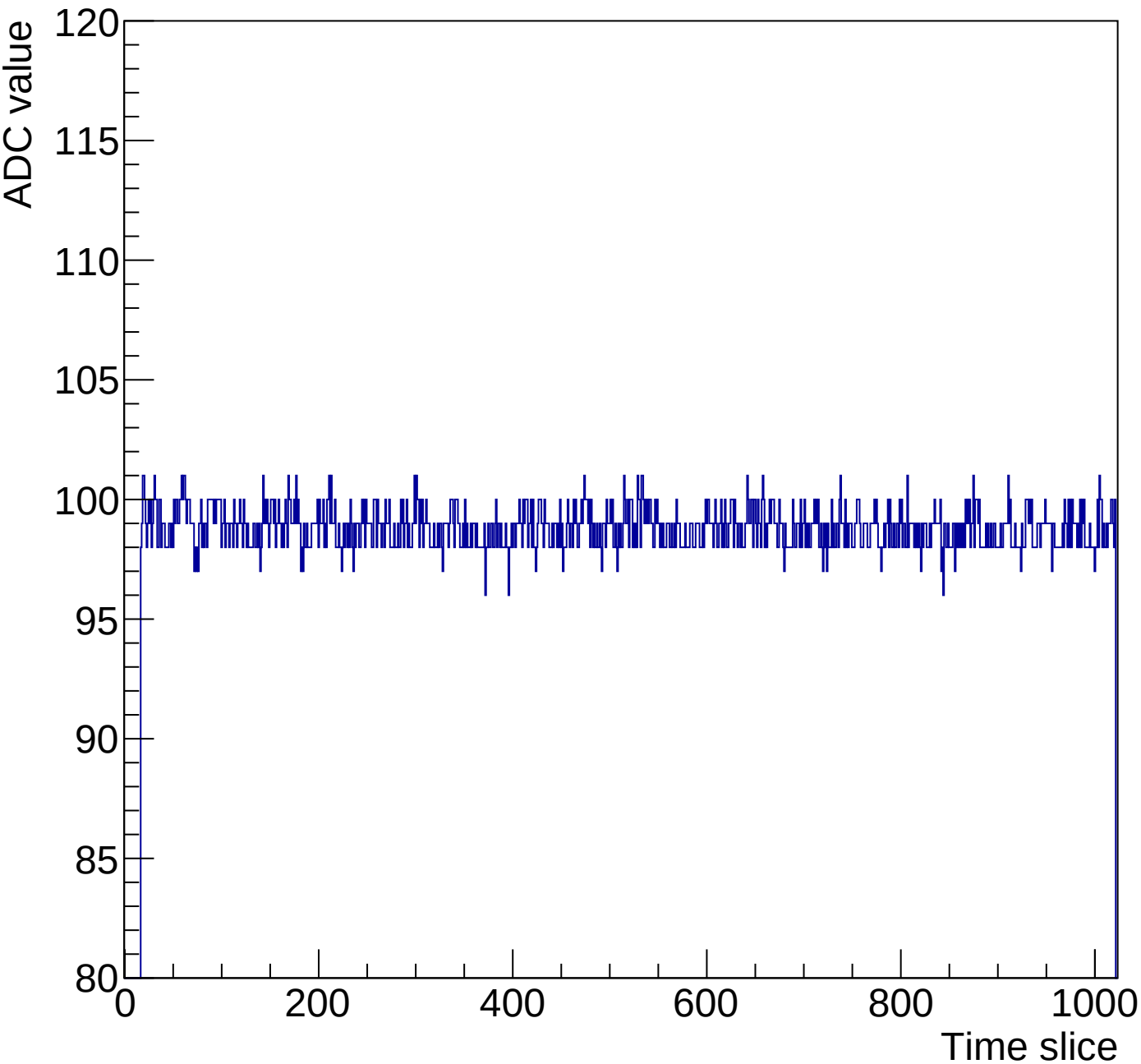
Run 1 event 100 mcm 0 chip 3 channel 8 full



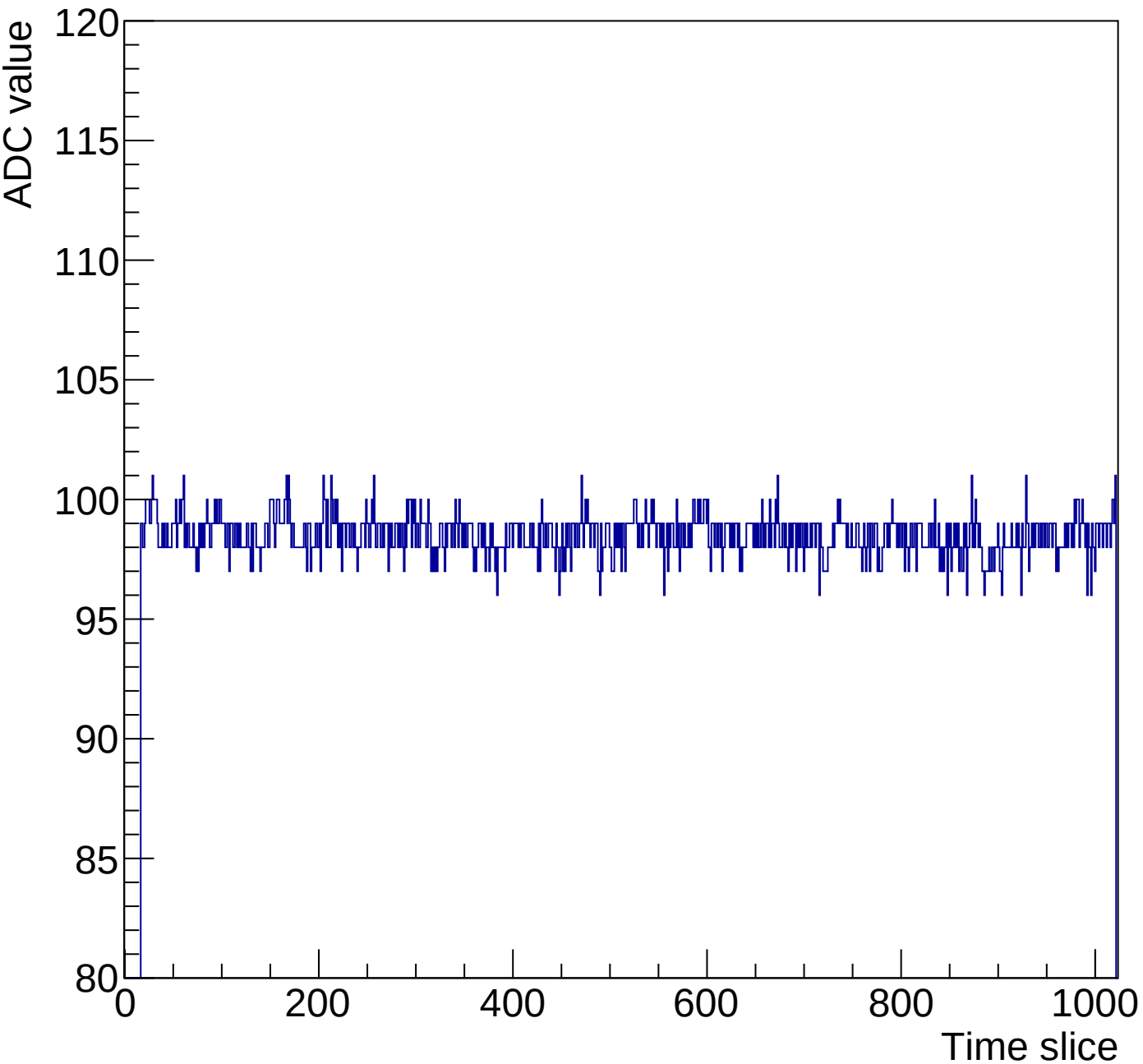
Run 1 event 100 mcm 0 chip 3 channel 9 full



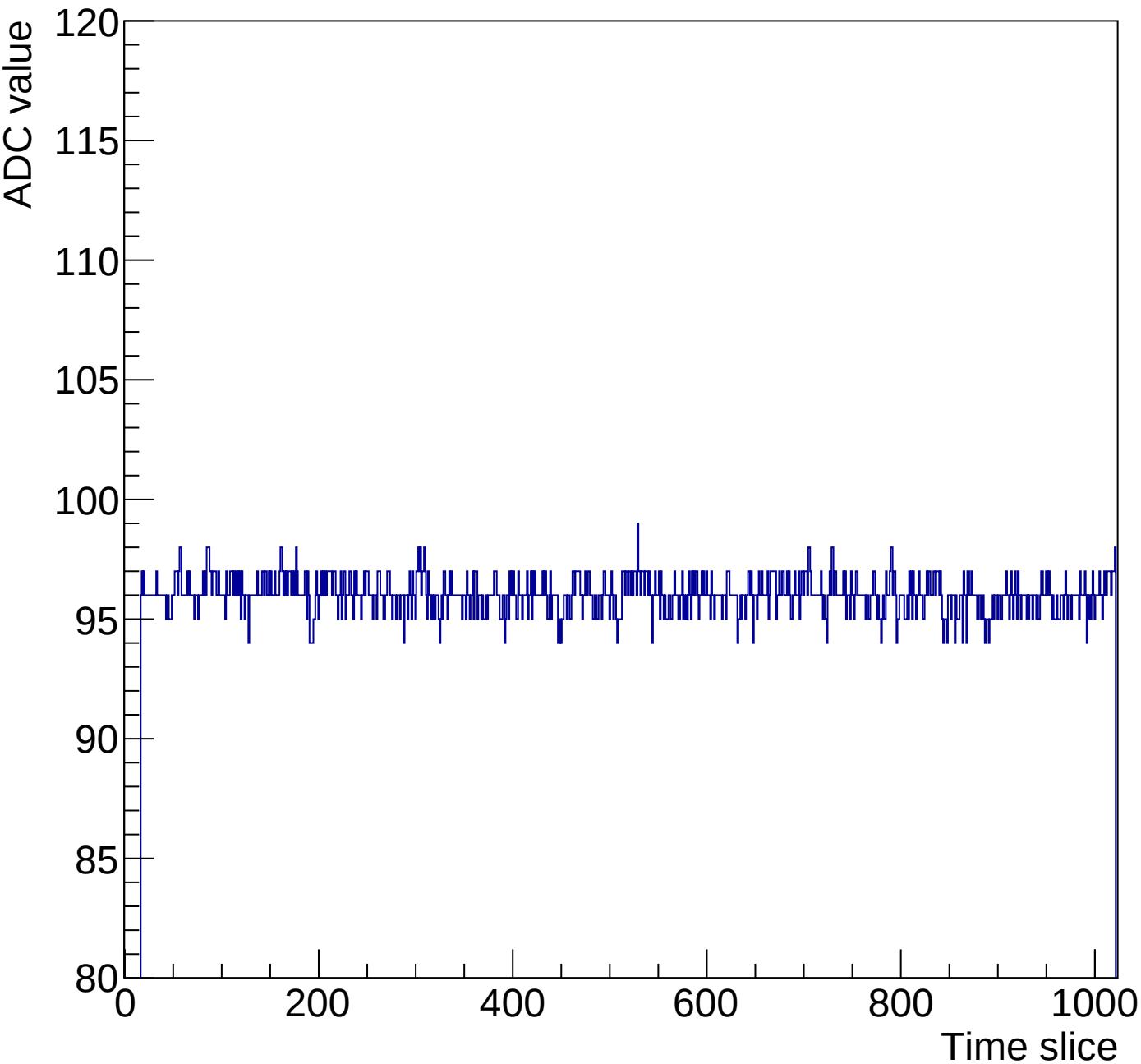
Run 1 event 100 mcm 0 chip 3 channel 10 full



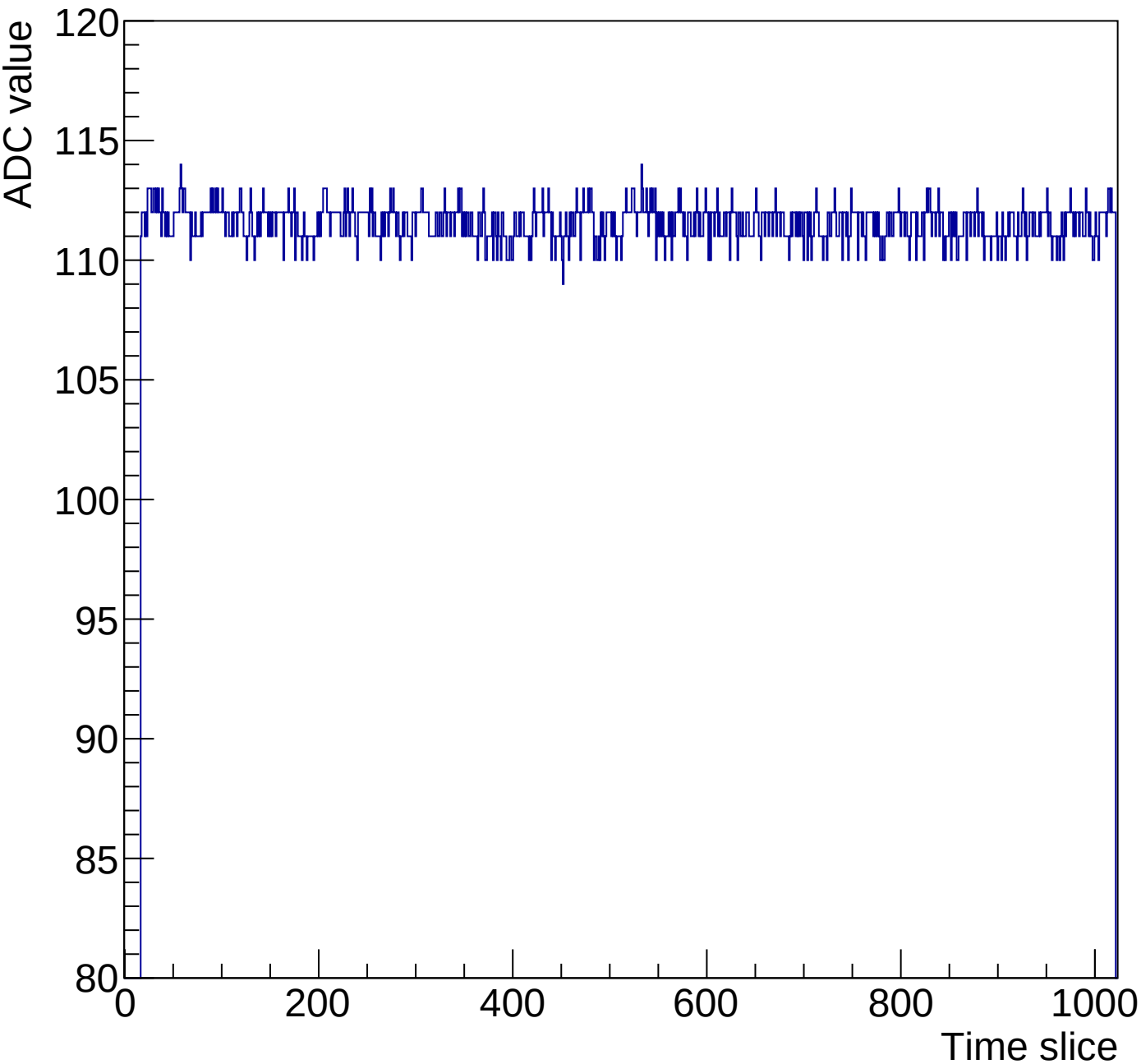
Run 1 event 100 mcm 0 chip 3 channel 11 full



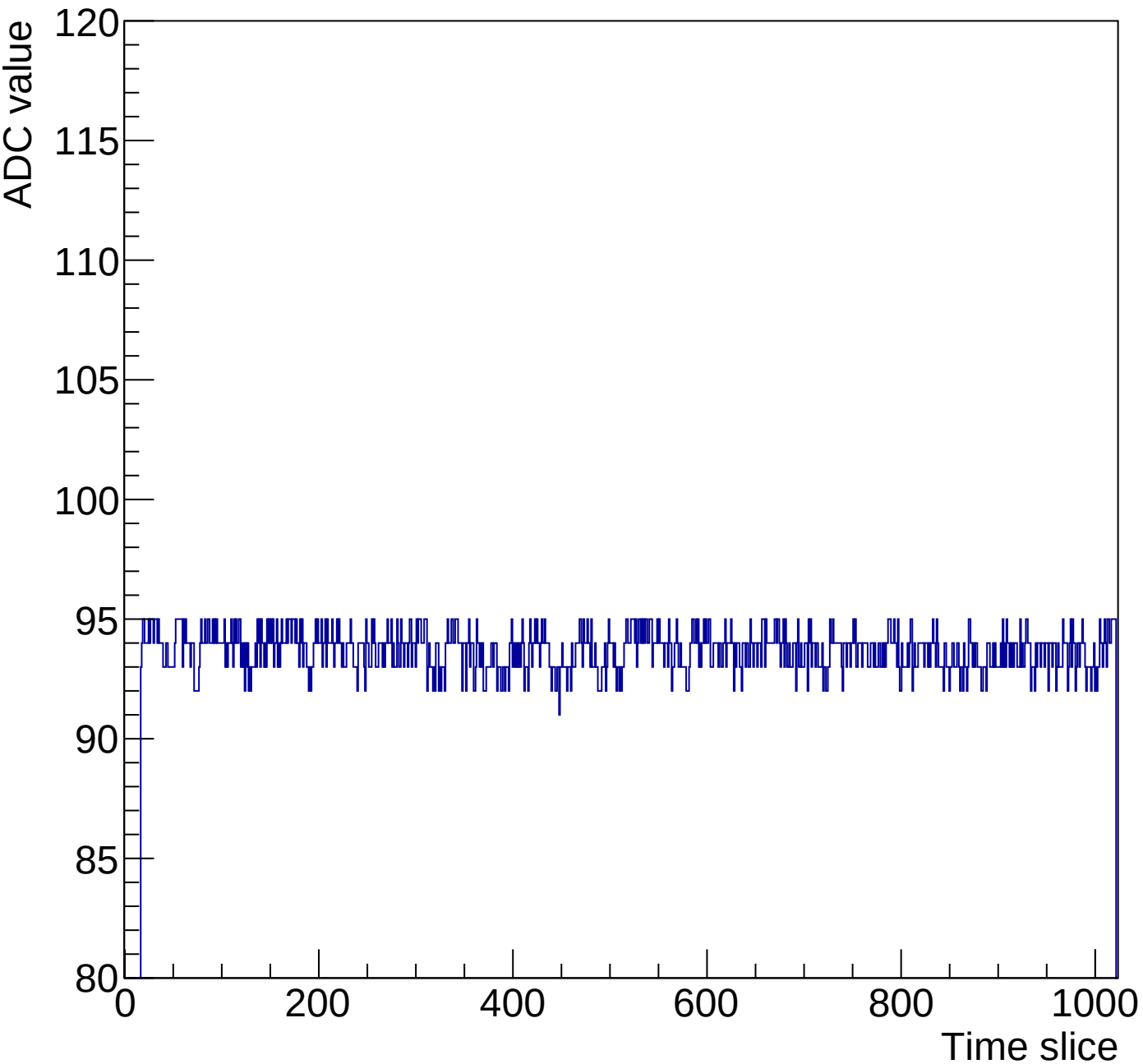
Run 1 event 100 mcm 0 chip 3 channel 12 full



Run 1 event 100 mcm 0 chip 3 channel 13 full



Run 1 event 100 mcm 0 chip 3 channel 14 full



Run 1 event 100 mcm 0 chip 3 channel 15 full

