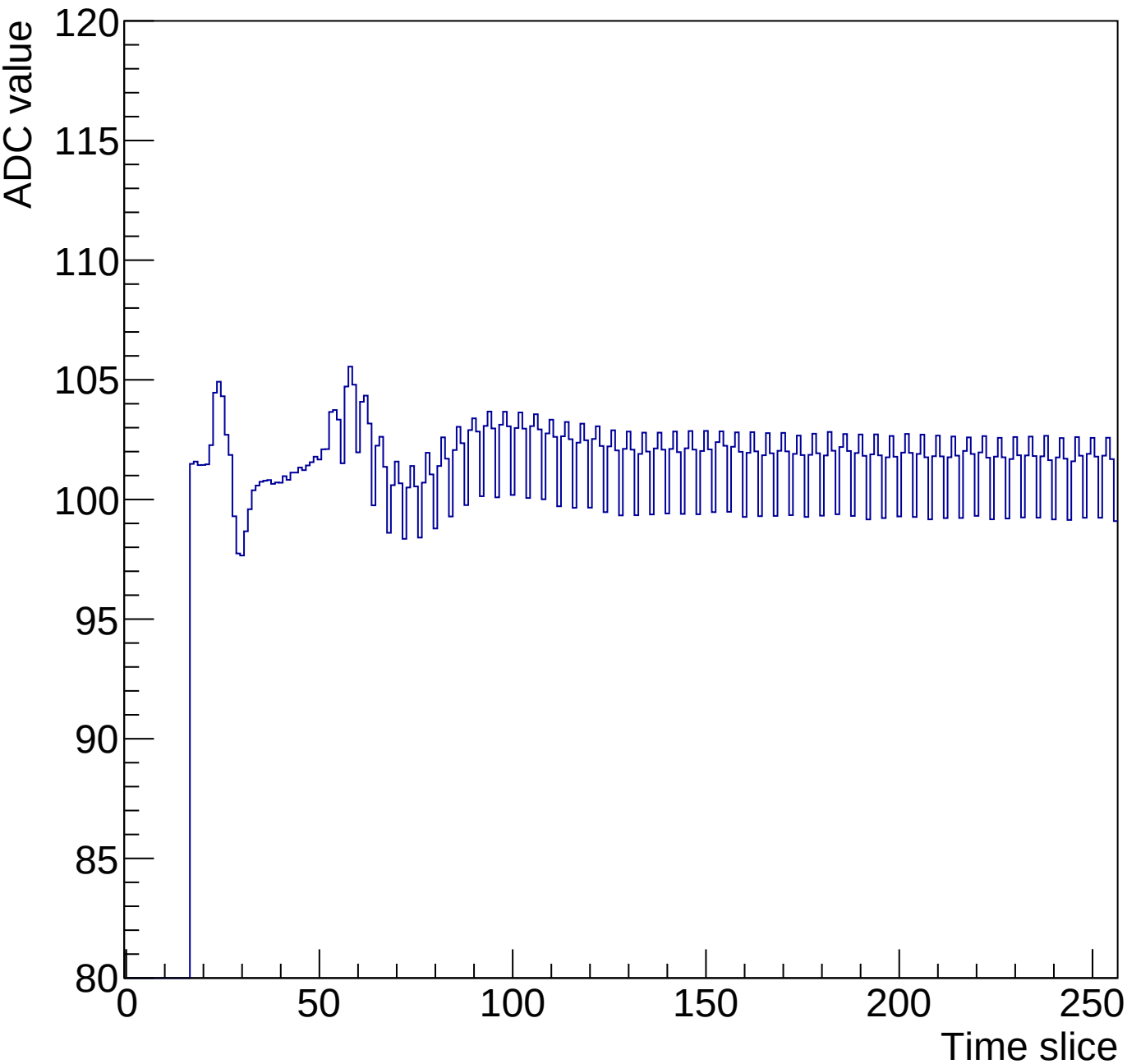
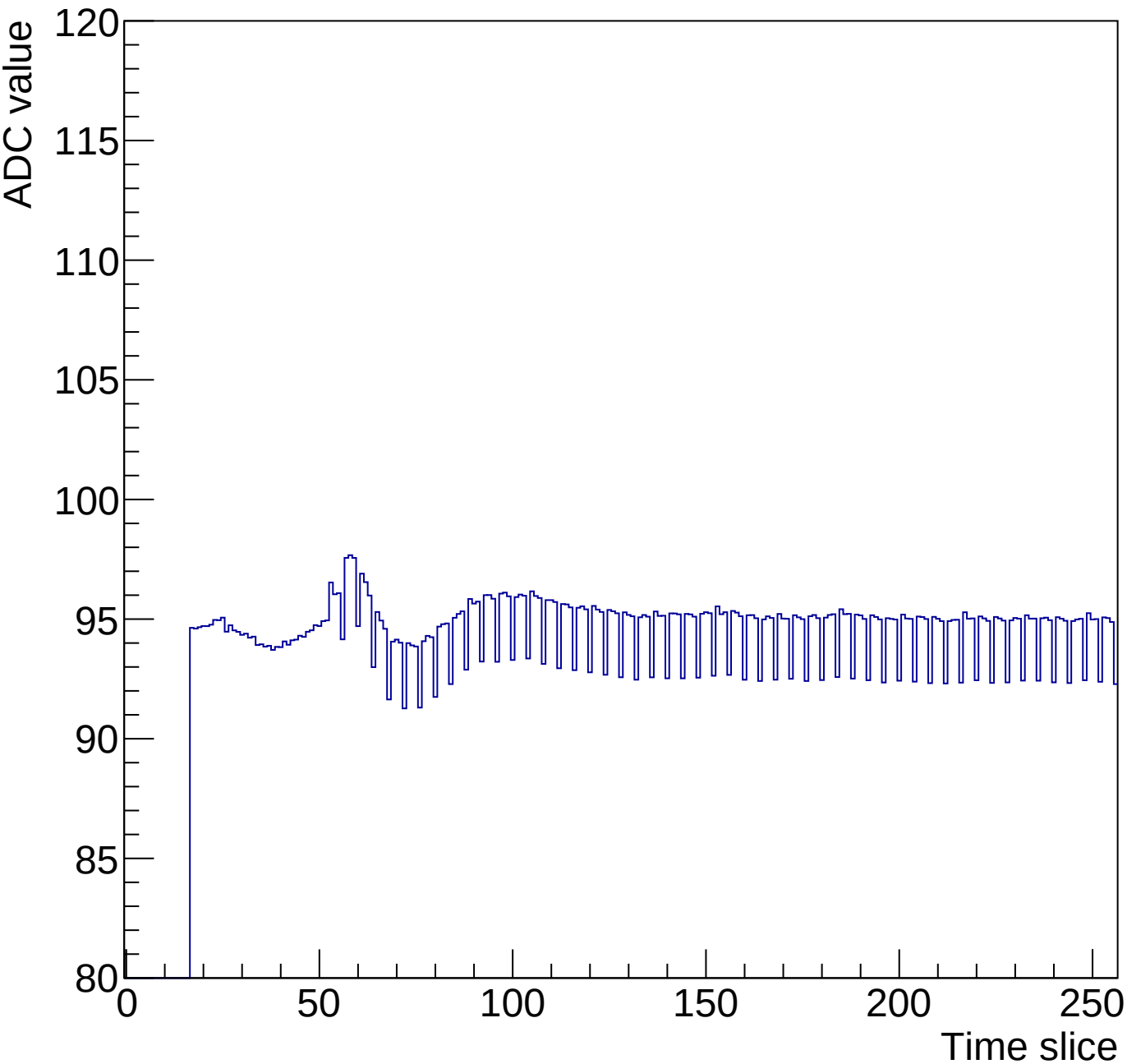


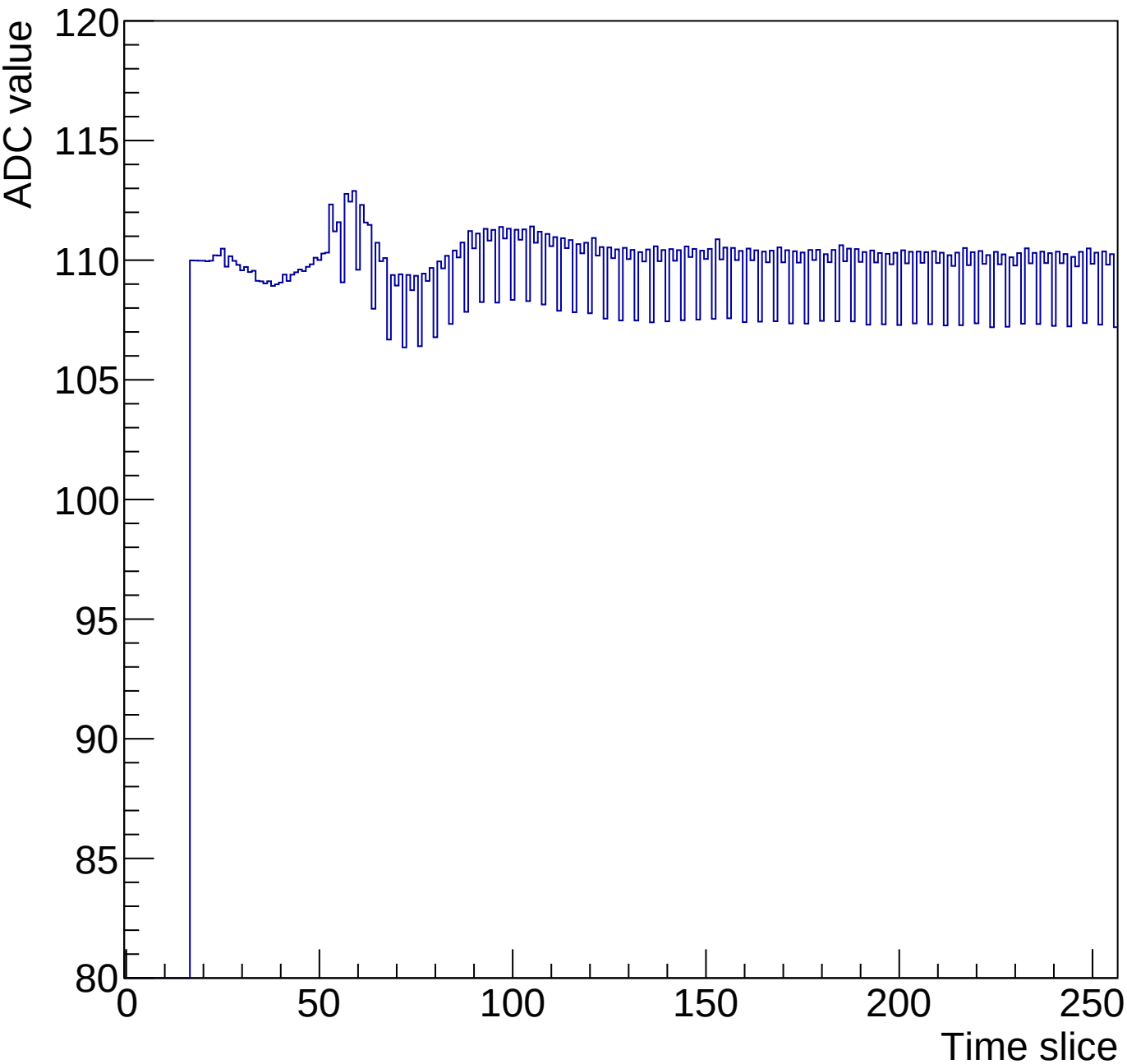
Run 0 Time mcm 0 chip 3 chan 0 256-120ns



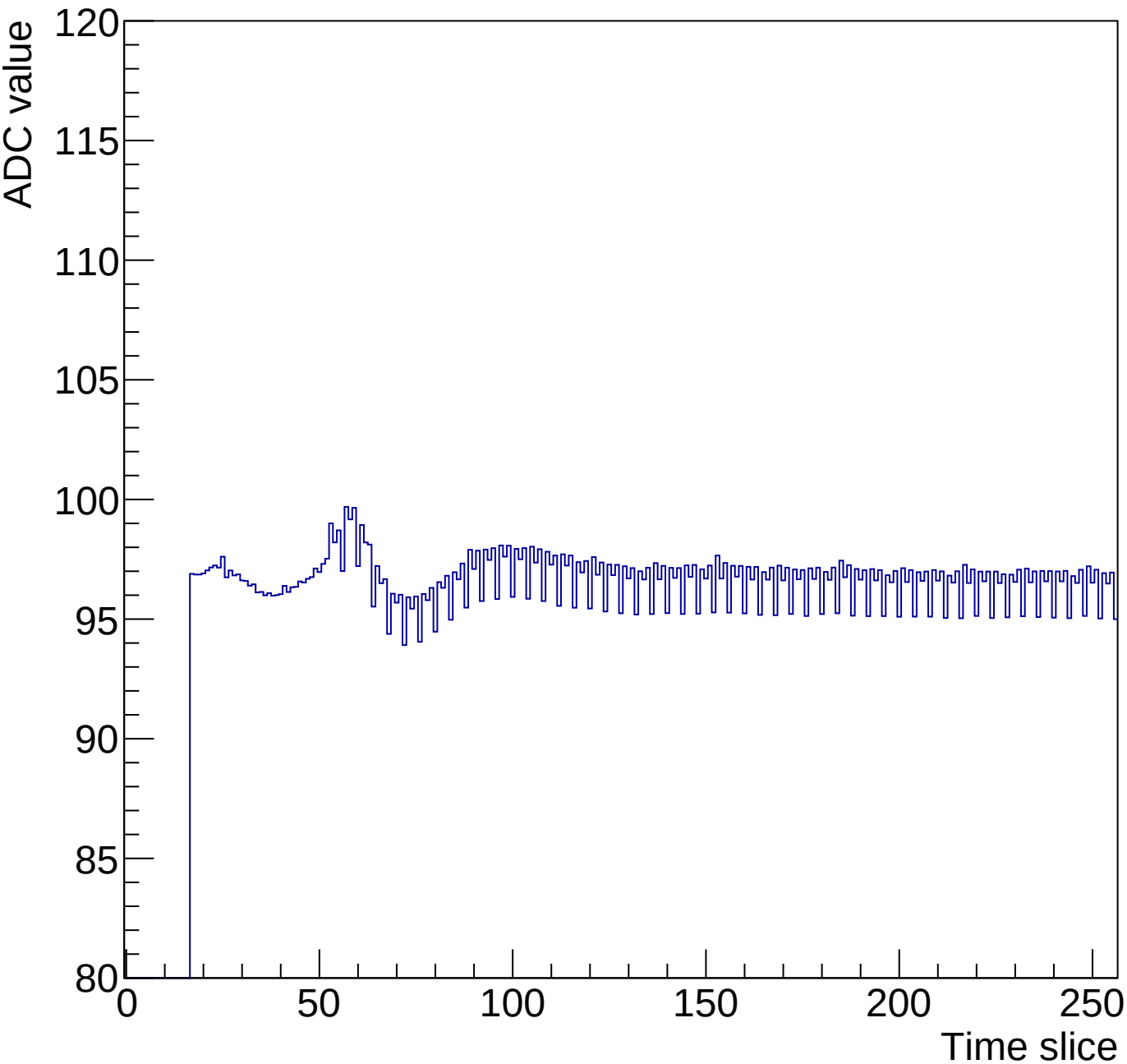
Run 0 Time mcm 0 chip 3 chan 1 256-120ns



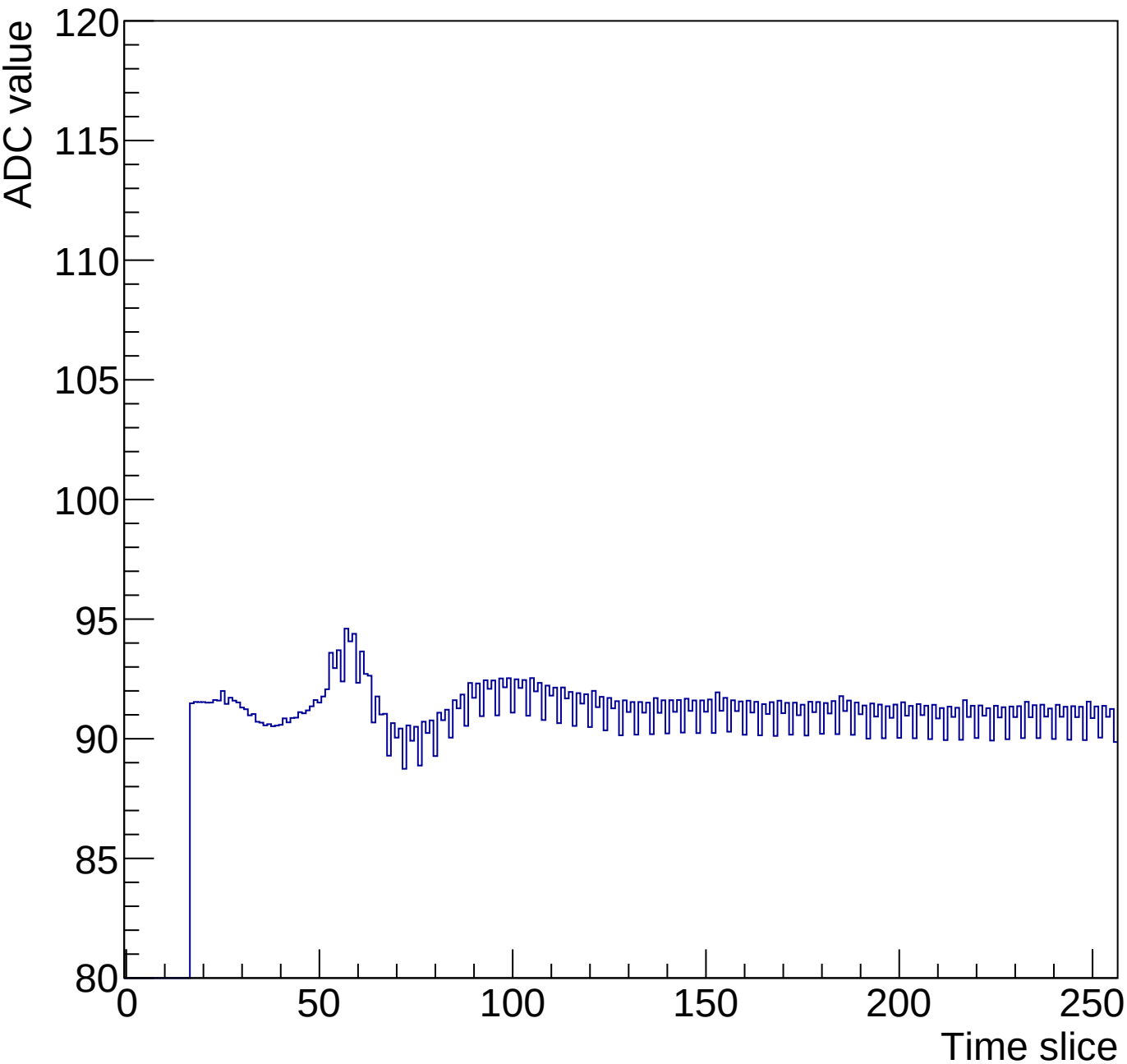
Run 0 Time mcm 0 chip 3 chan 2 256-120ns



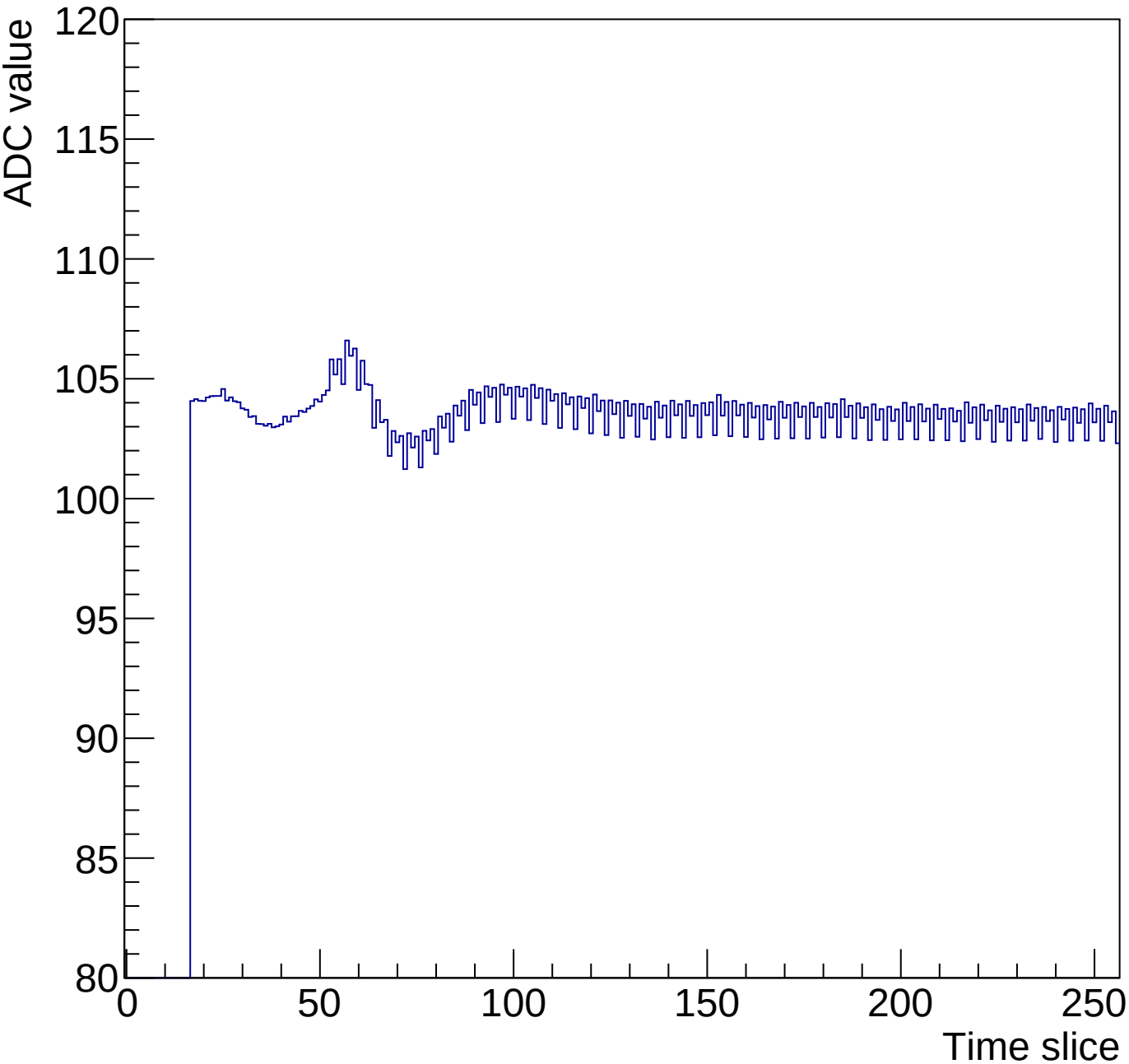
Run 0 Time mcm 0 chip 3 chan 3 256-120ns



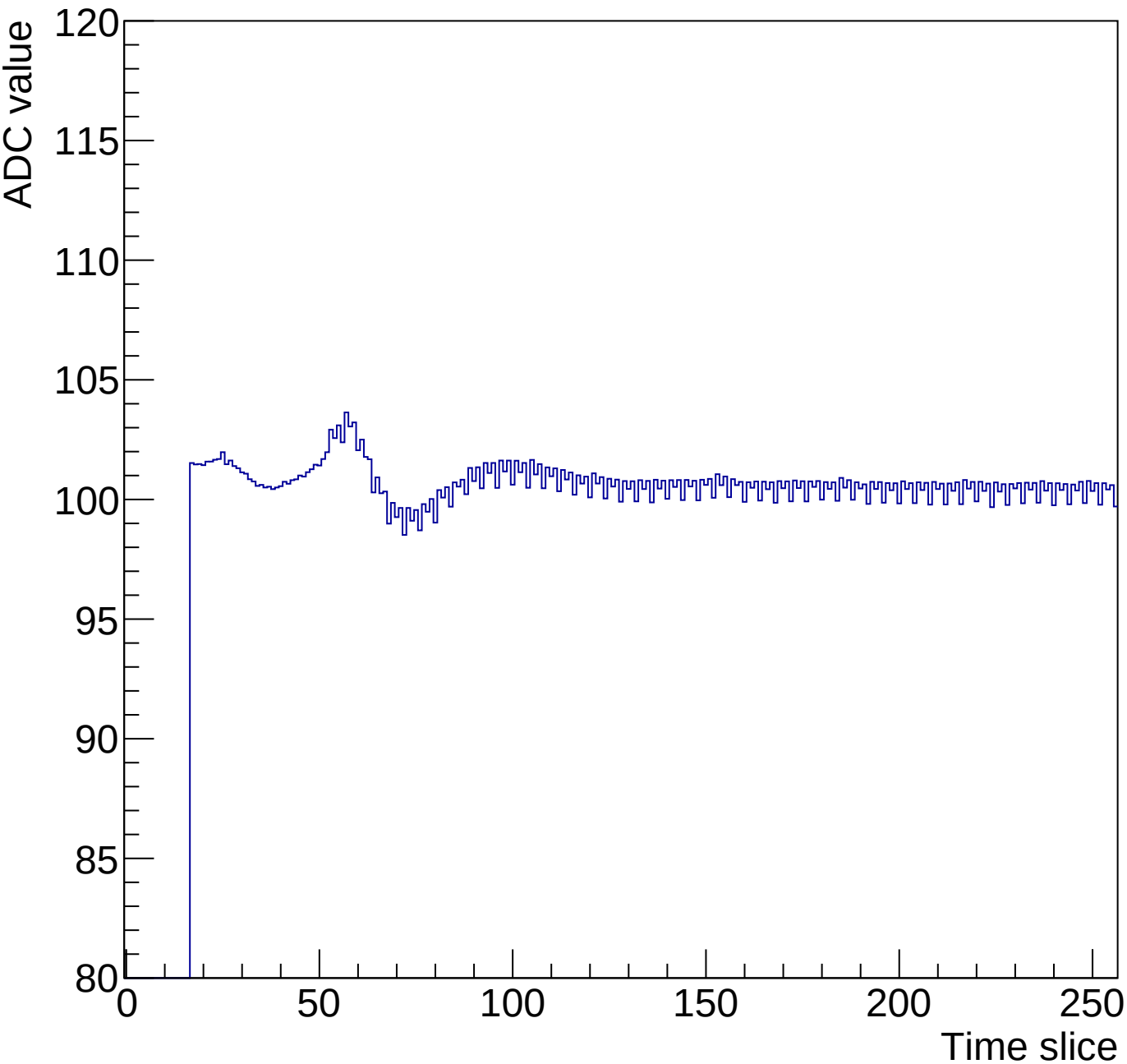
Run 0 Time mcm 0 chip 3 chan 4 256-120ns



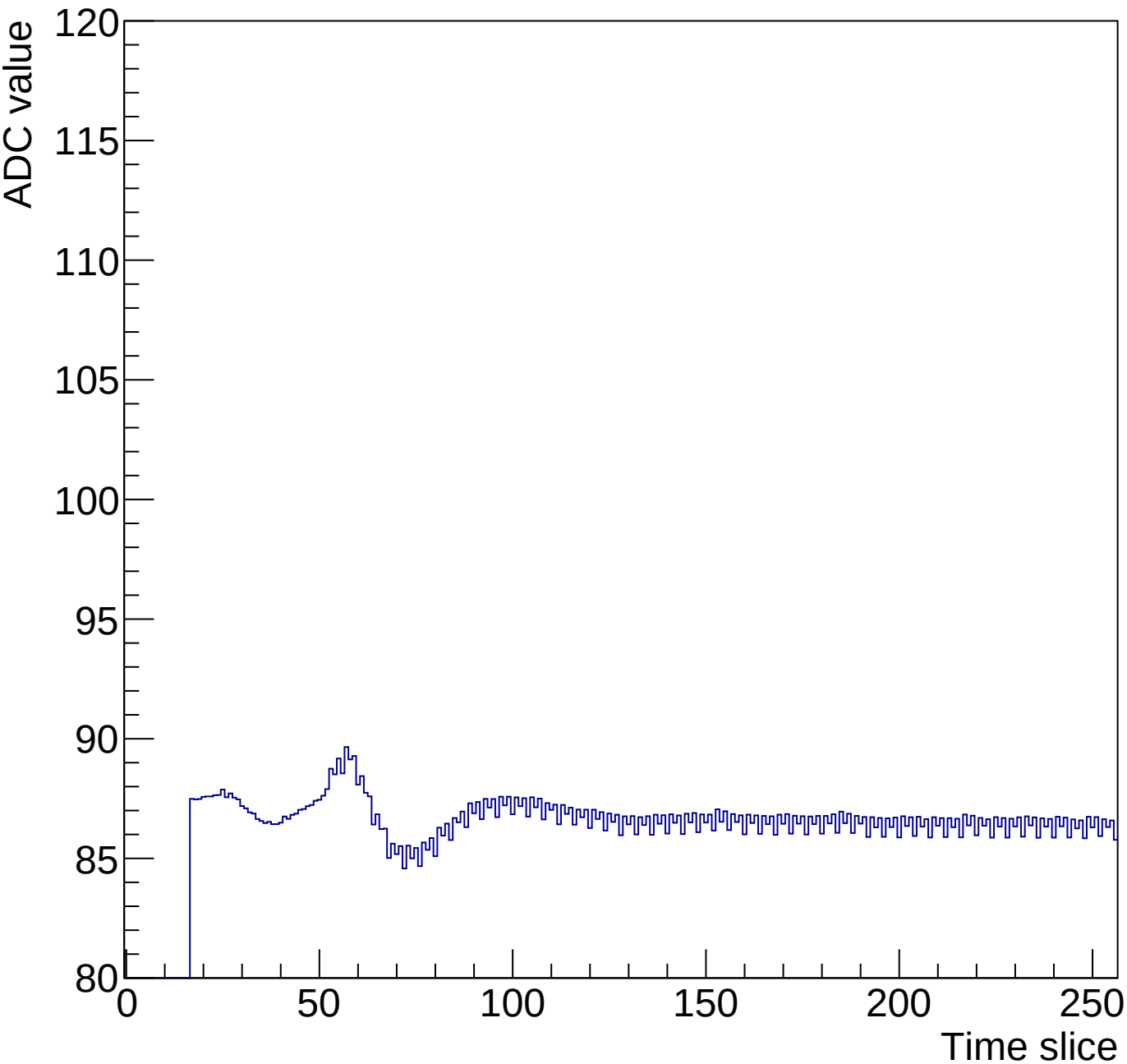
Run 0 Time mcm 0 chip 3 chan 5 256-120ns



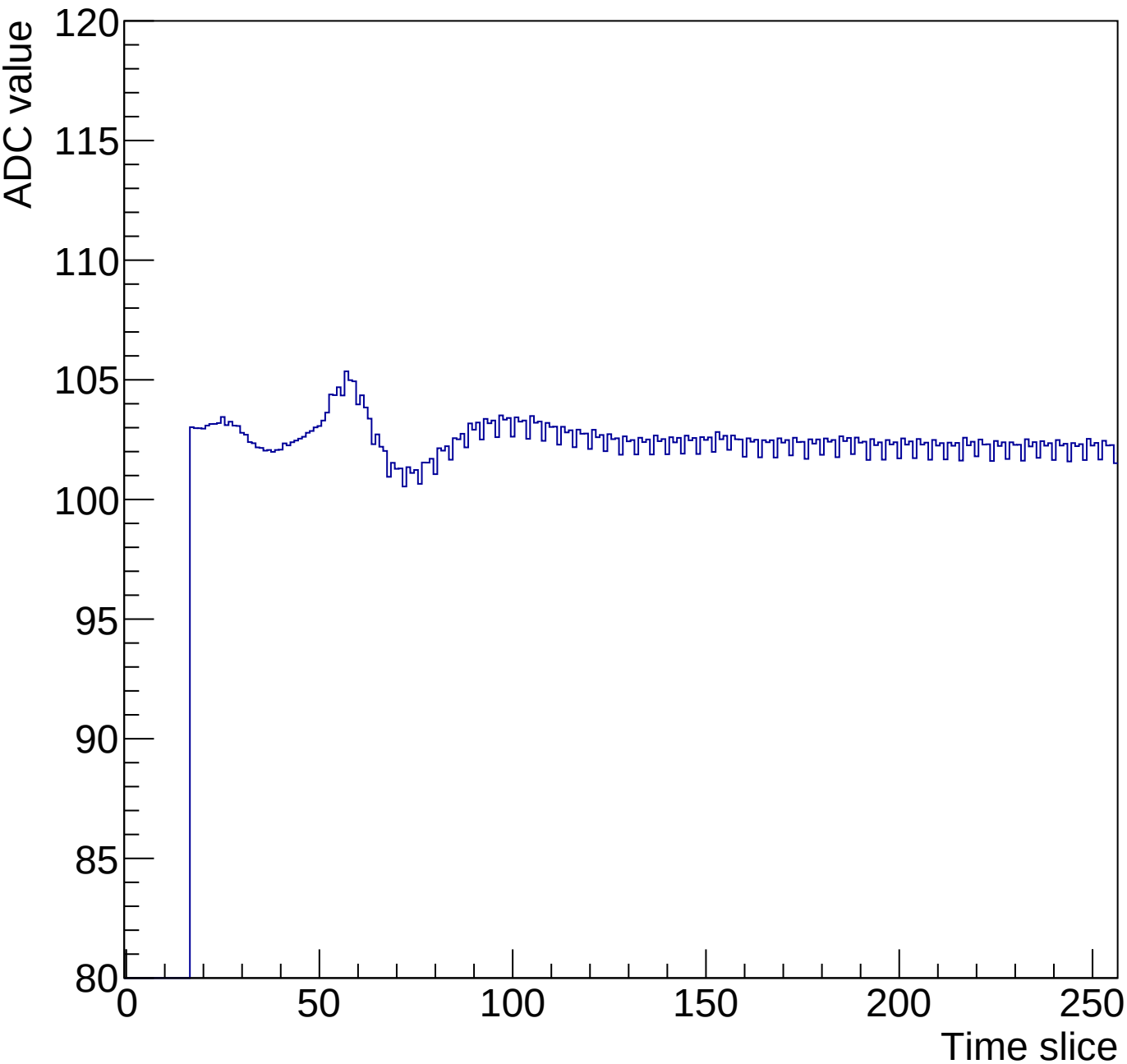
Run 0 Time mcm 0 chip 3 chan 6 256-120ns



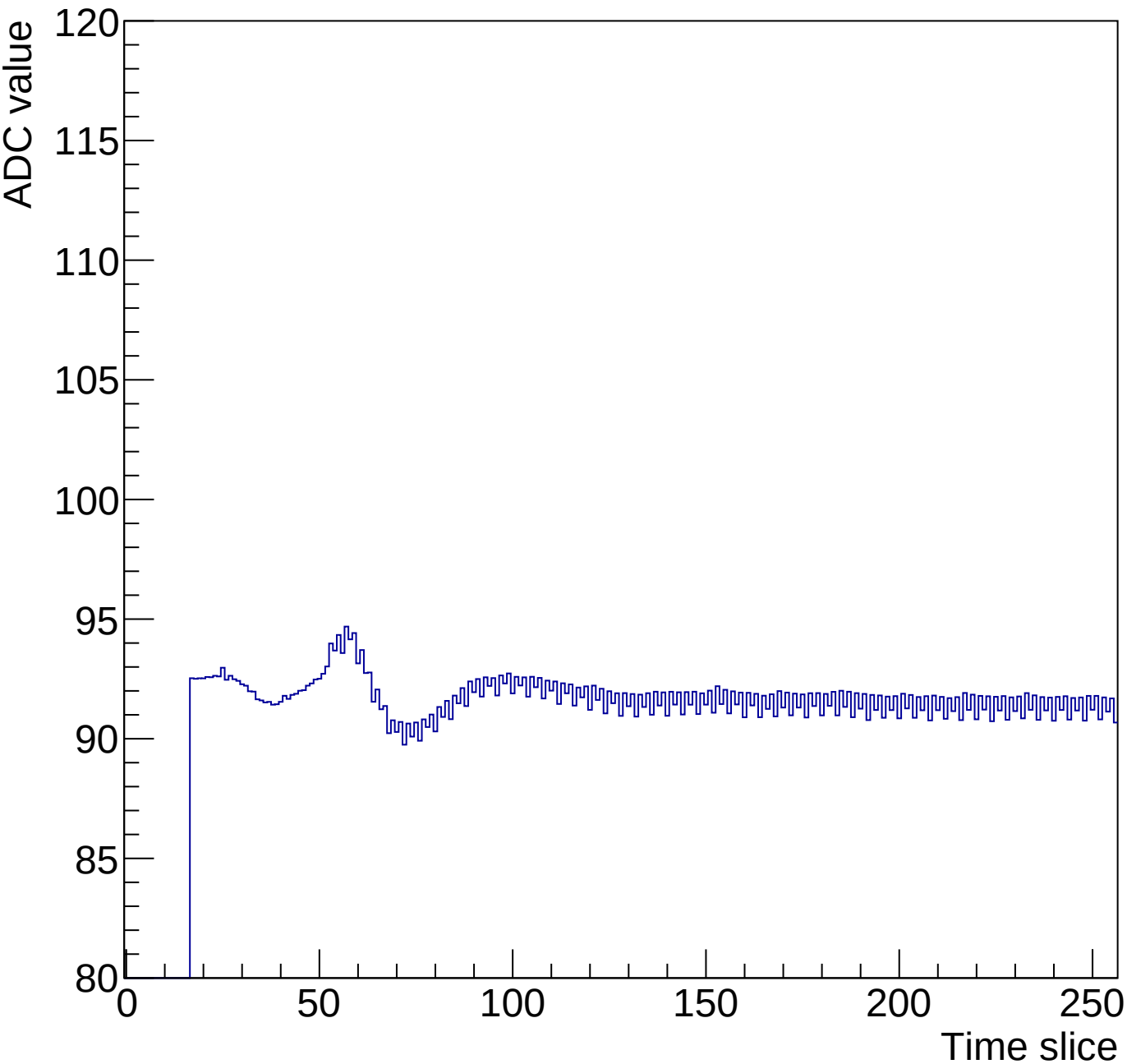
Run 0 Time mcm 0 chip 3 chan 7 256-120ns



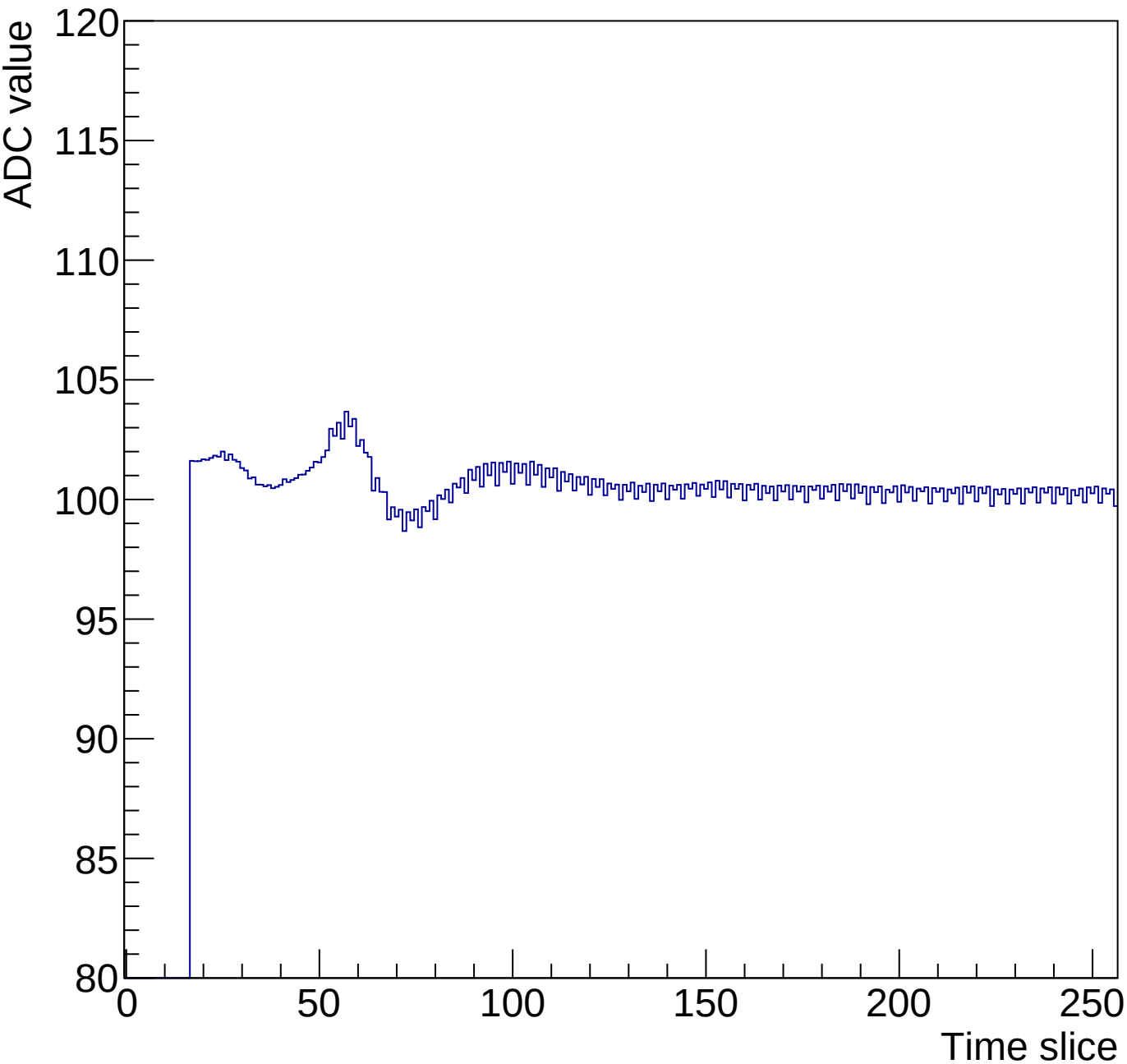
Run 0 Time mcm 0 chip 3 chan 8 256-120ns



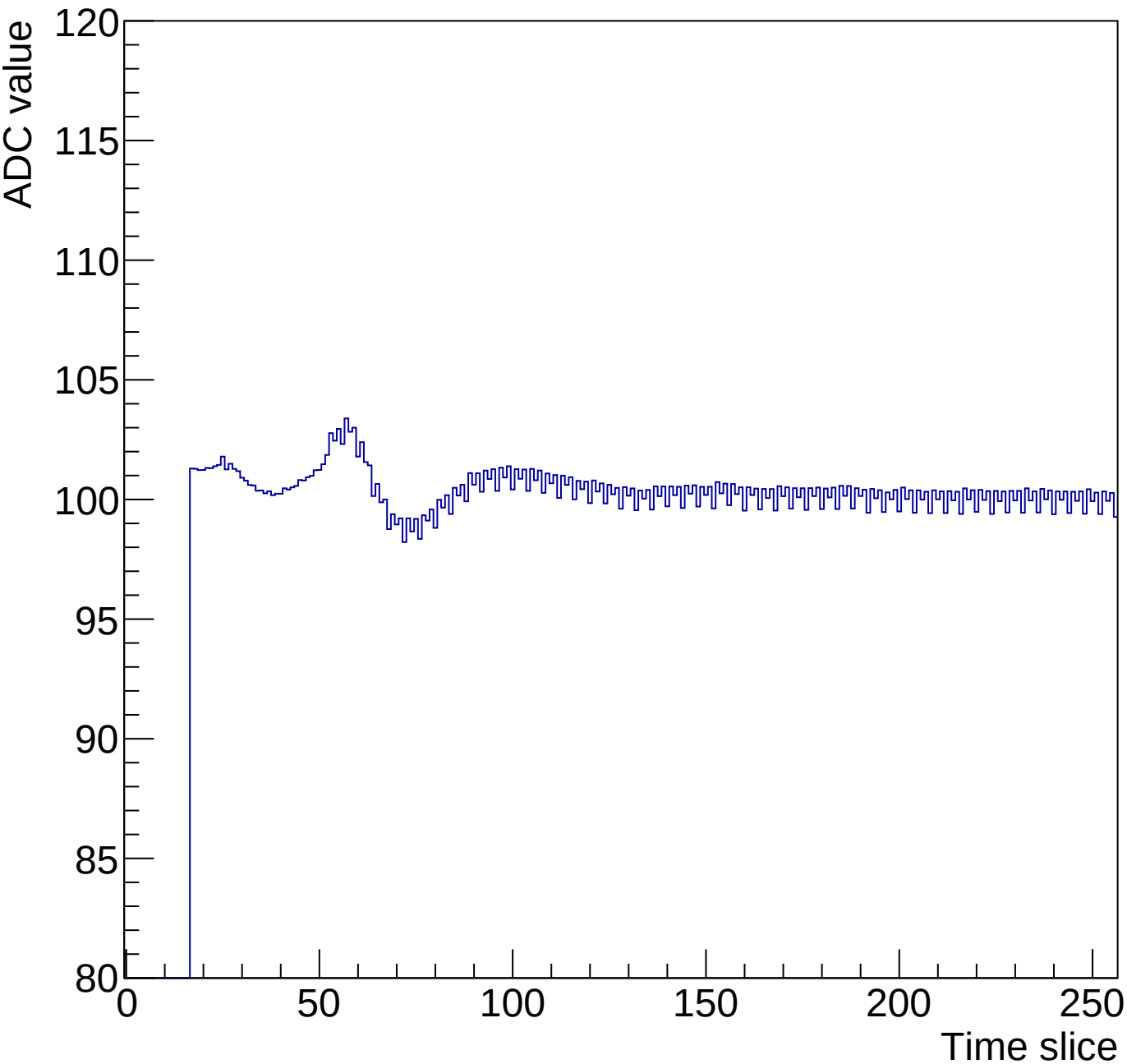
Run 0 Time mcm 0 chip 3 chan 9 256-120ns



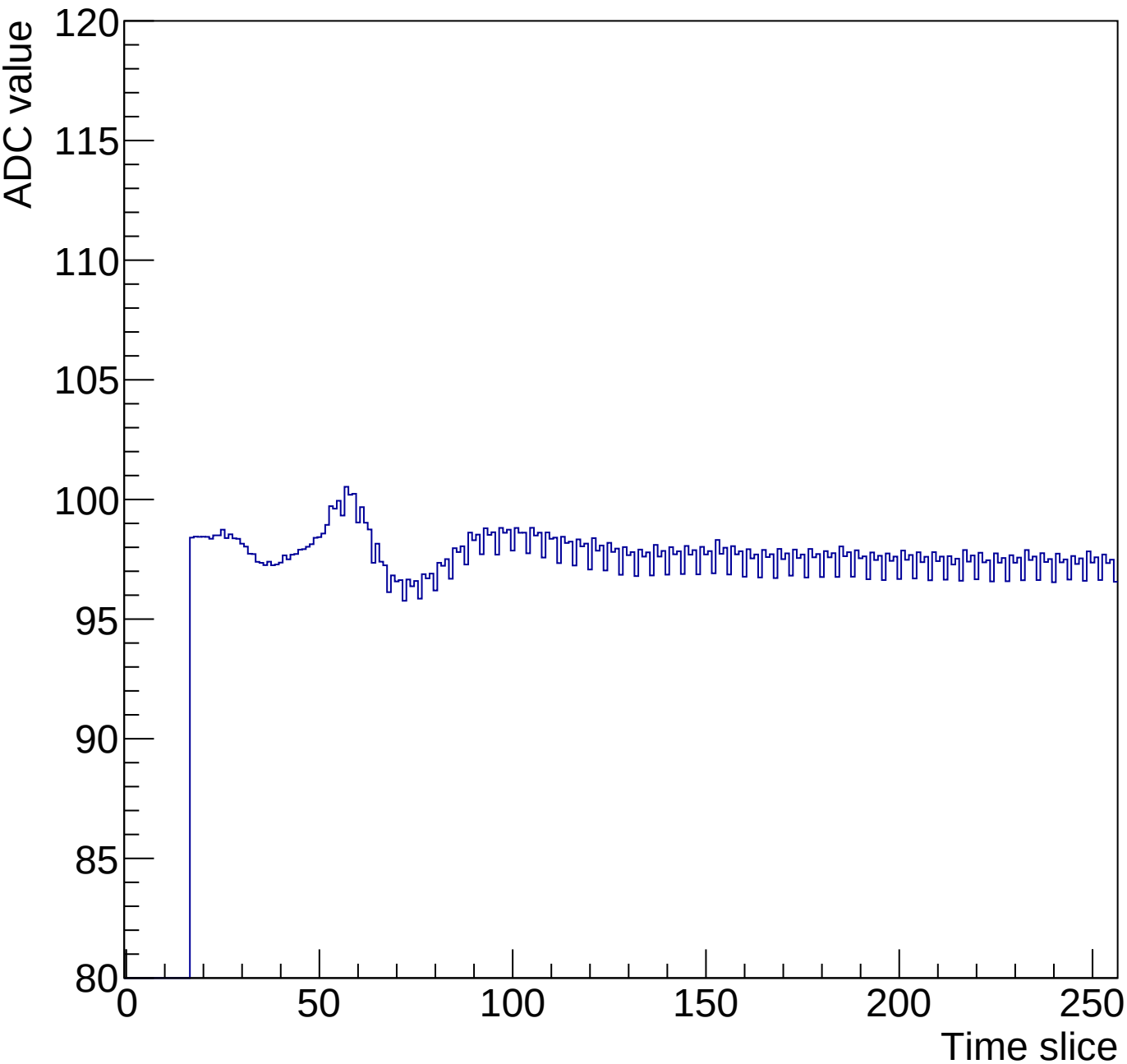
Run 0 Time mcm 0 chip 3 chan 10 256-120ns



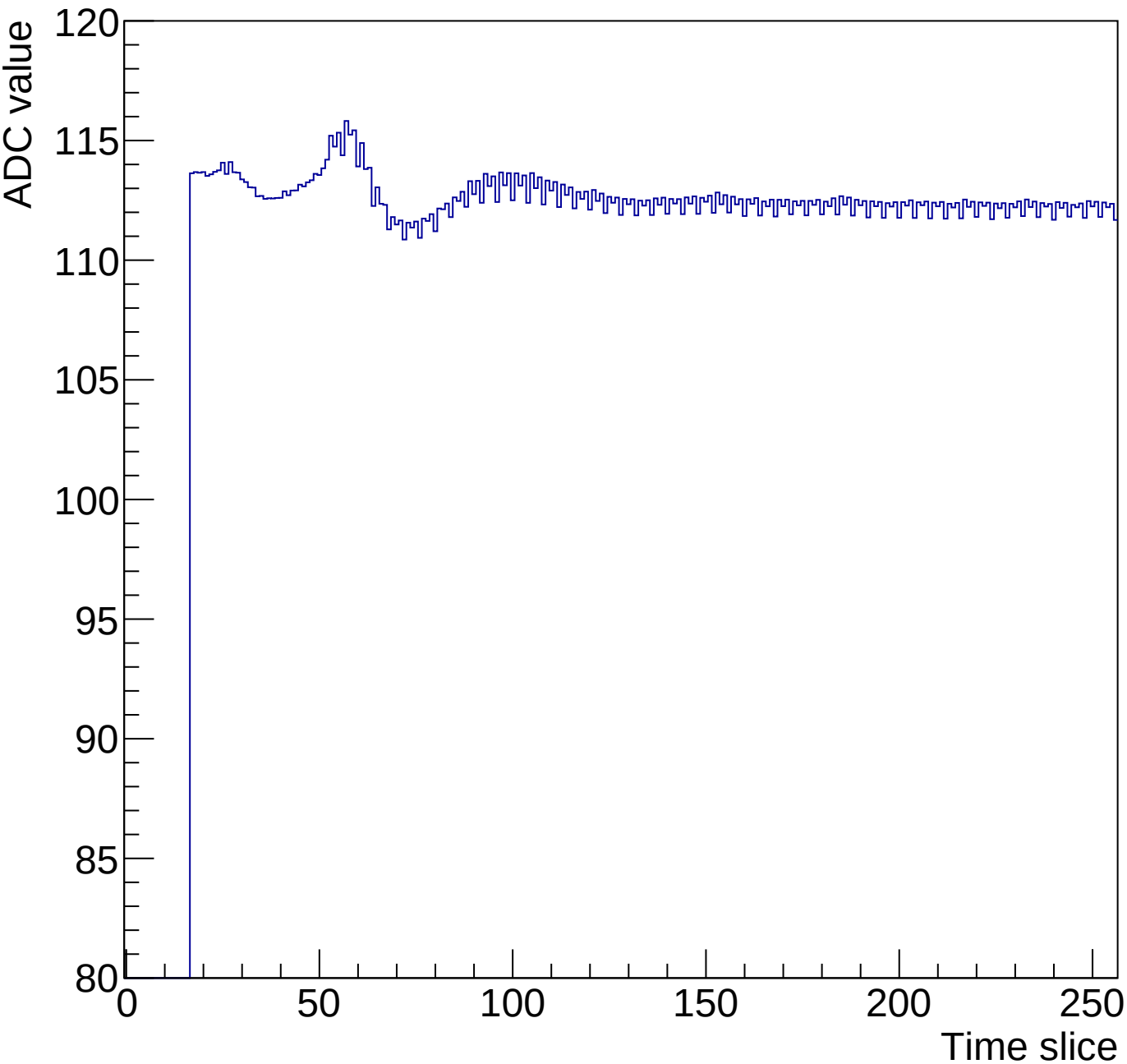
Run 0 Time mcm 0 chip 3 chan 11 256-120ns



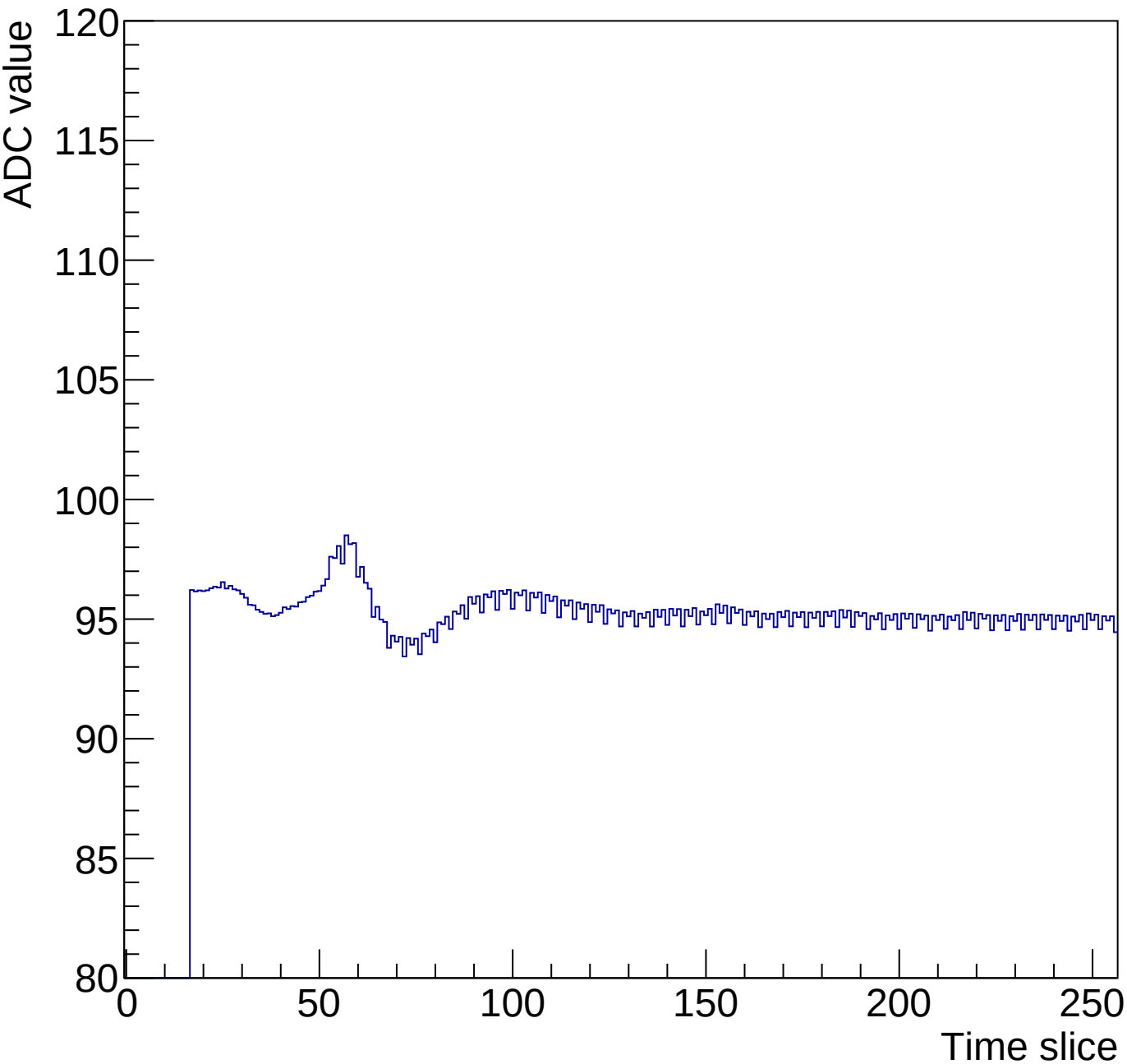
Run 0 Time mcm 0 chip 3 chan 12 256-120ns



Run 0 Time mcm 0 chip 3 chan 13 256-120ns



Run 0 Time mcm 0 chip 3 chan 14 256-120ns



Run 0 Time mcm 0 chip 3 chan 15 256-120ns

