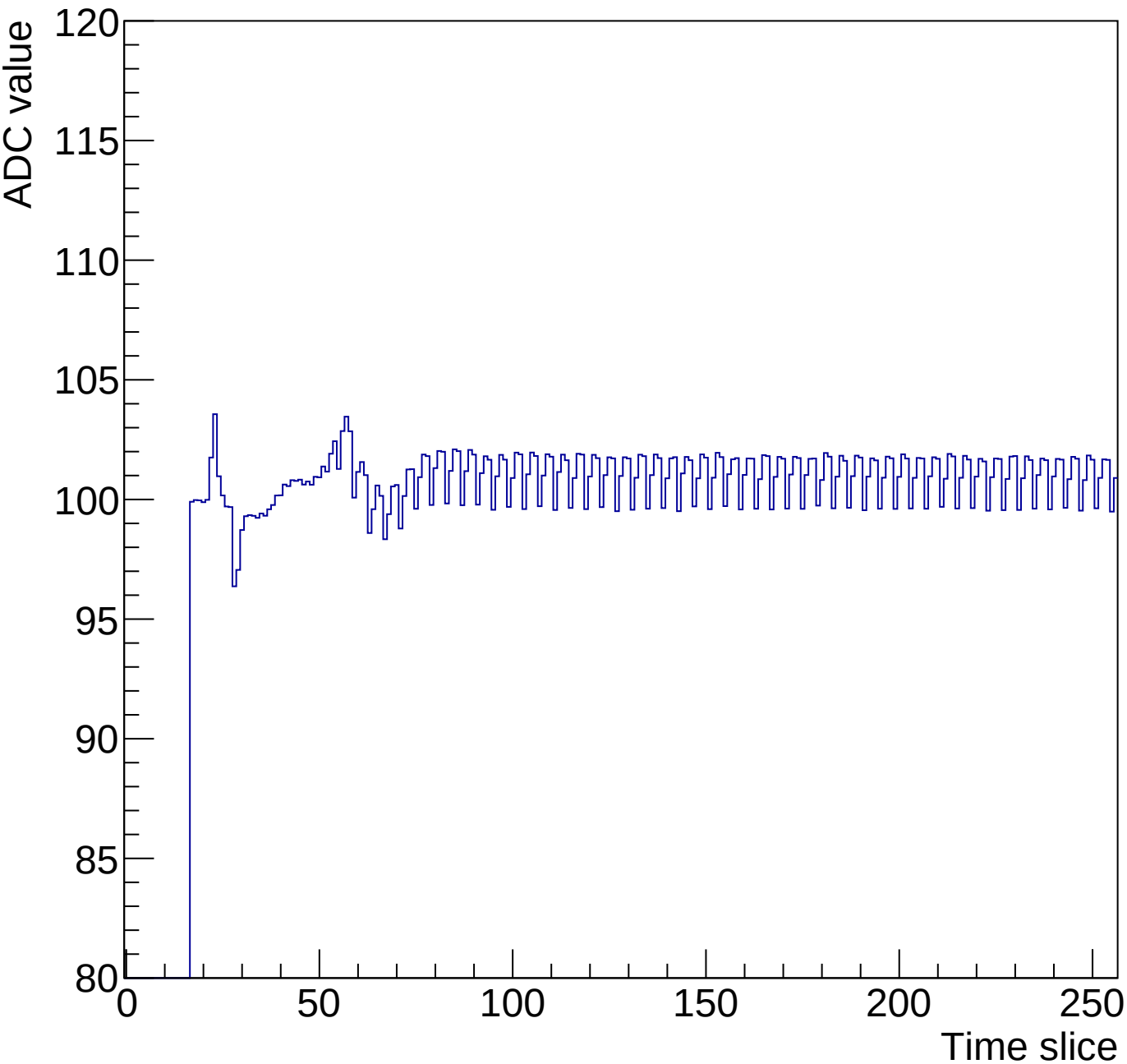
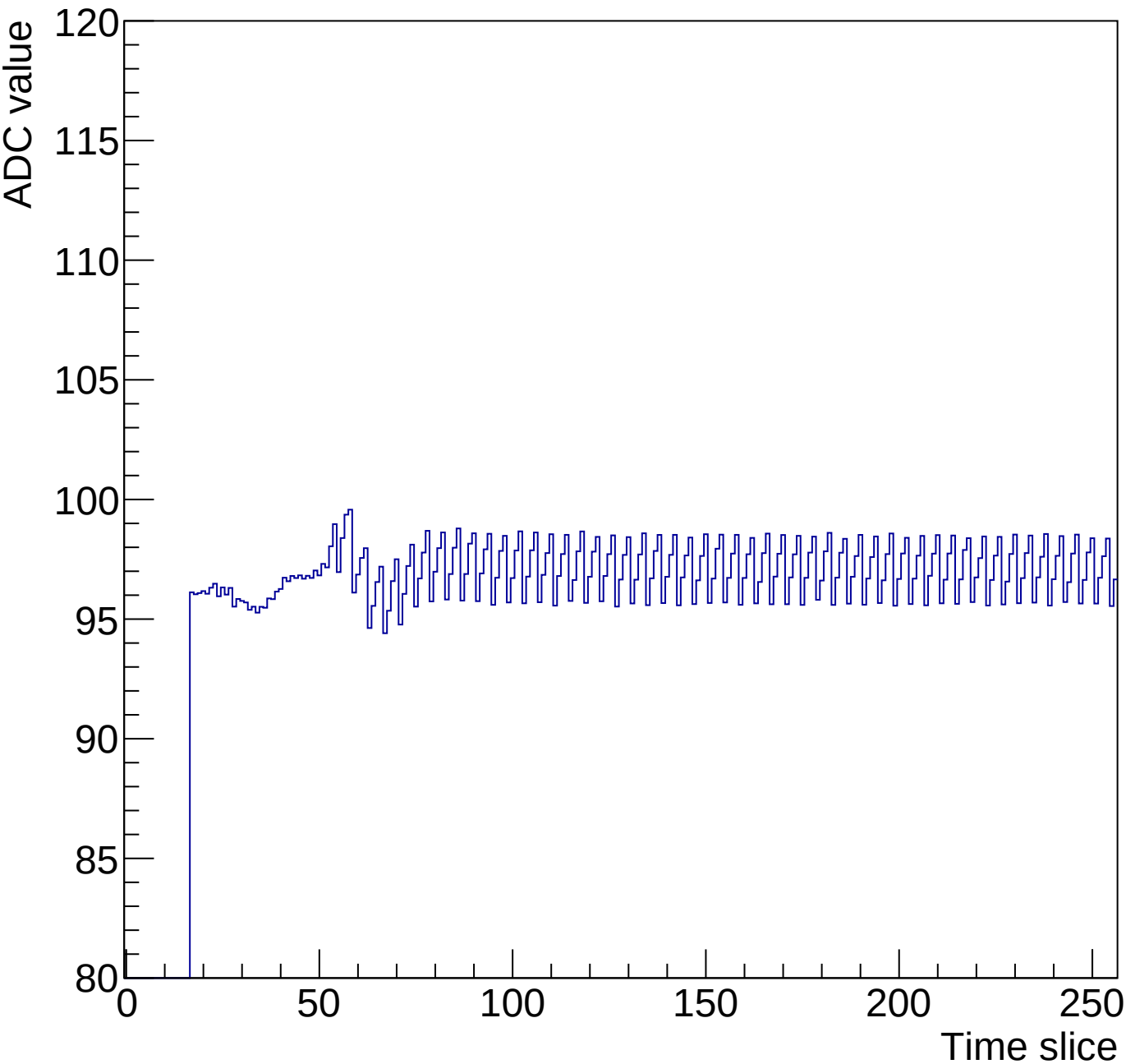


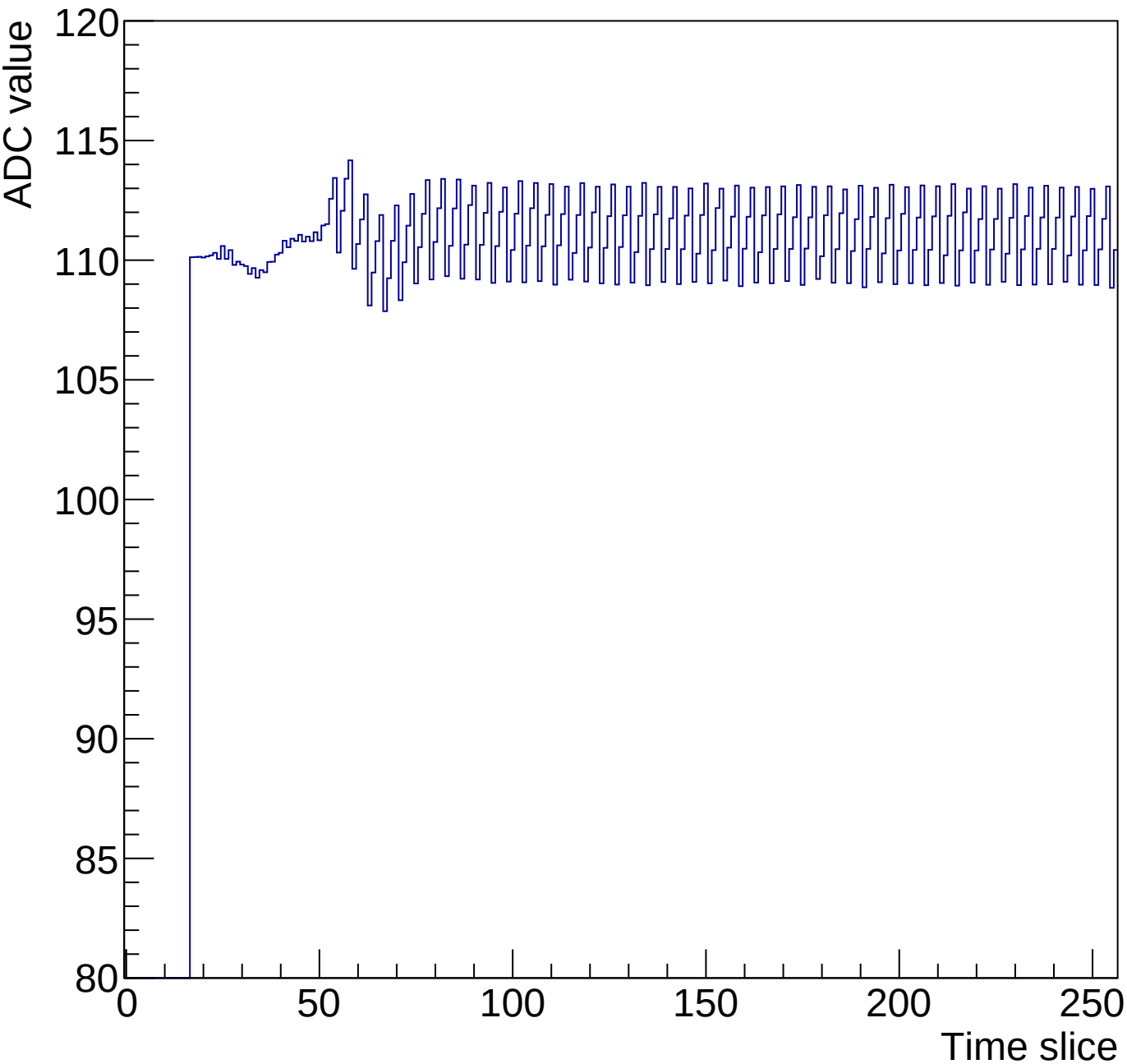
Run 2 Time mcm 0 chip 3 chan 0 256-60ns



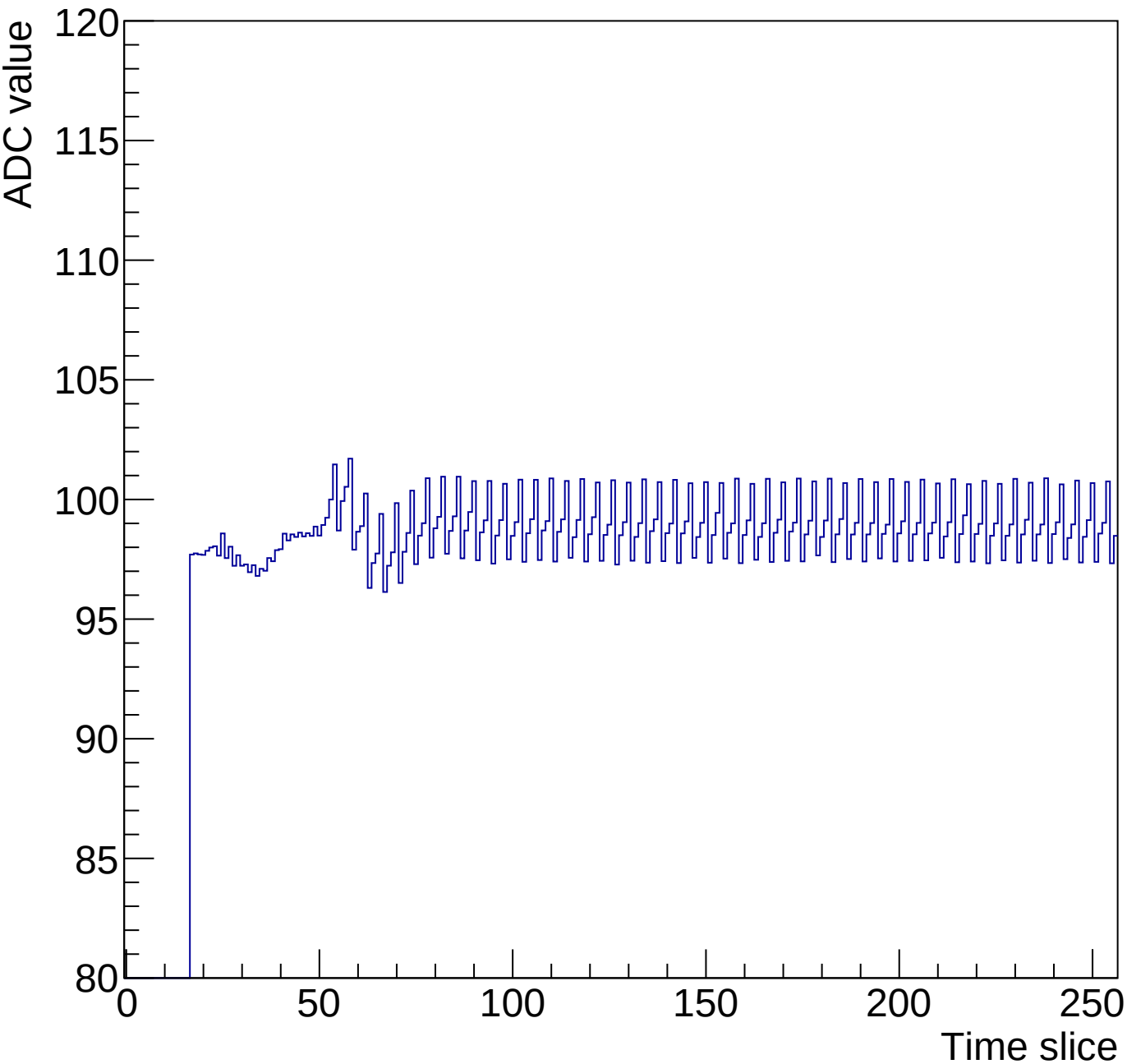
Run 2 Time mcm 0 chip 3 chan 1 256-60ns



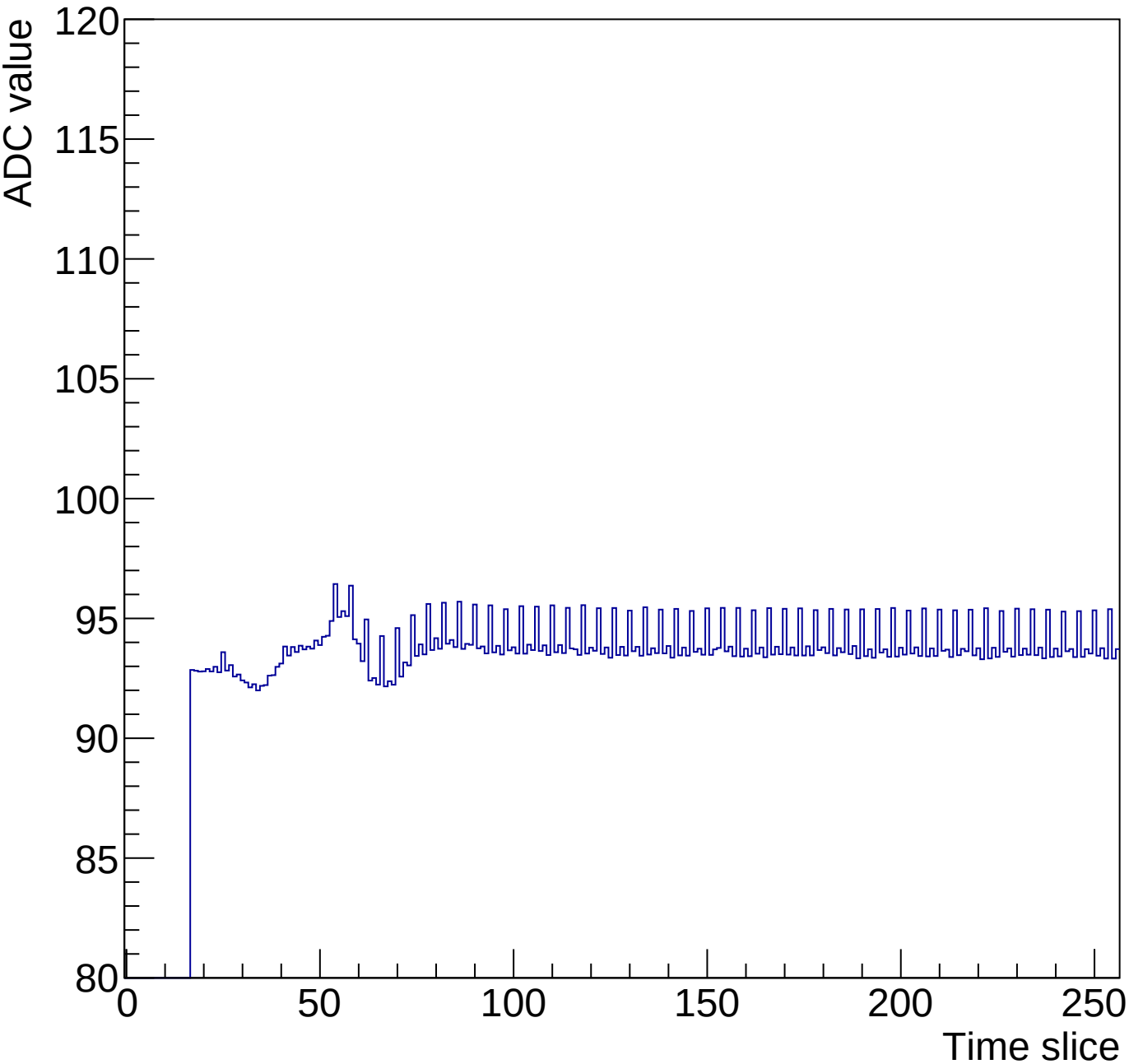
Run 2 Time mcm 0 chip 3 chan 2 256-60ns



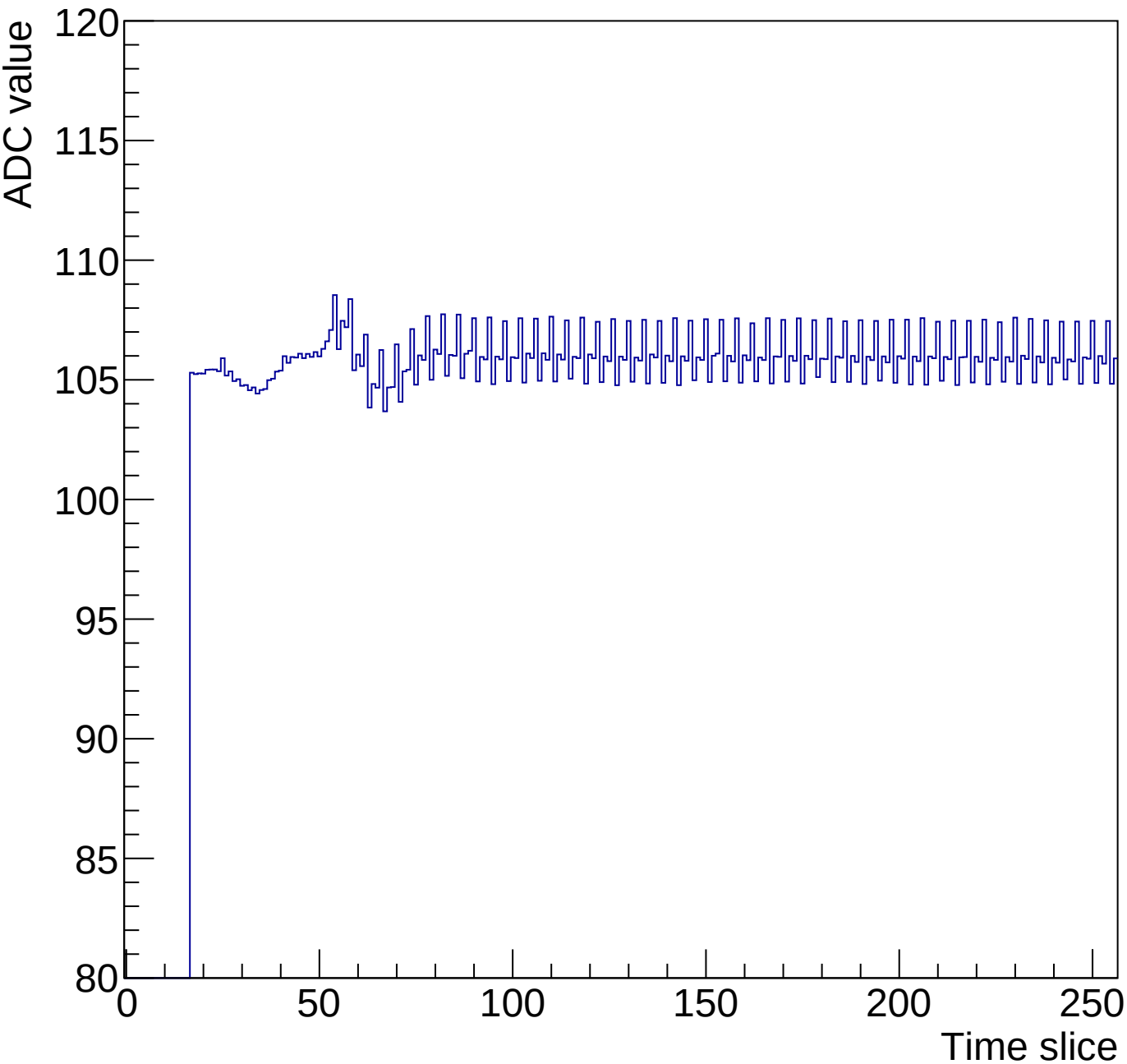
Run 2 Time mcm 0 chip 3 chan 3 256-60ns



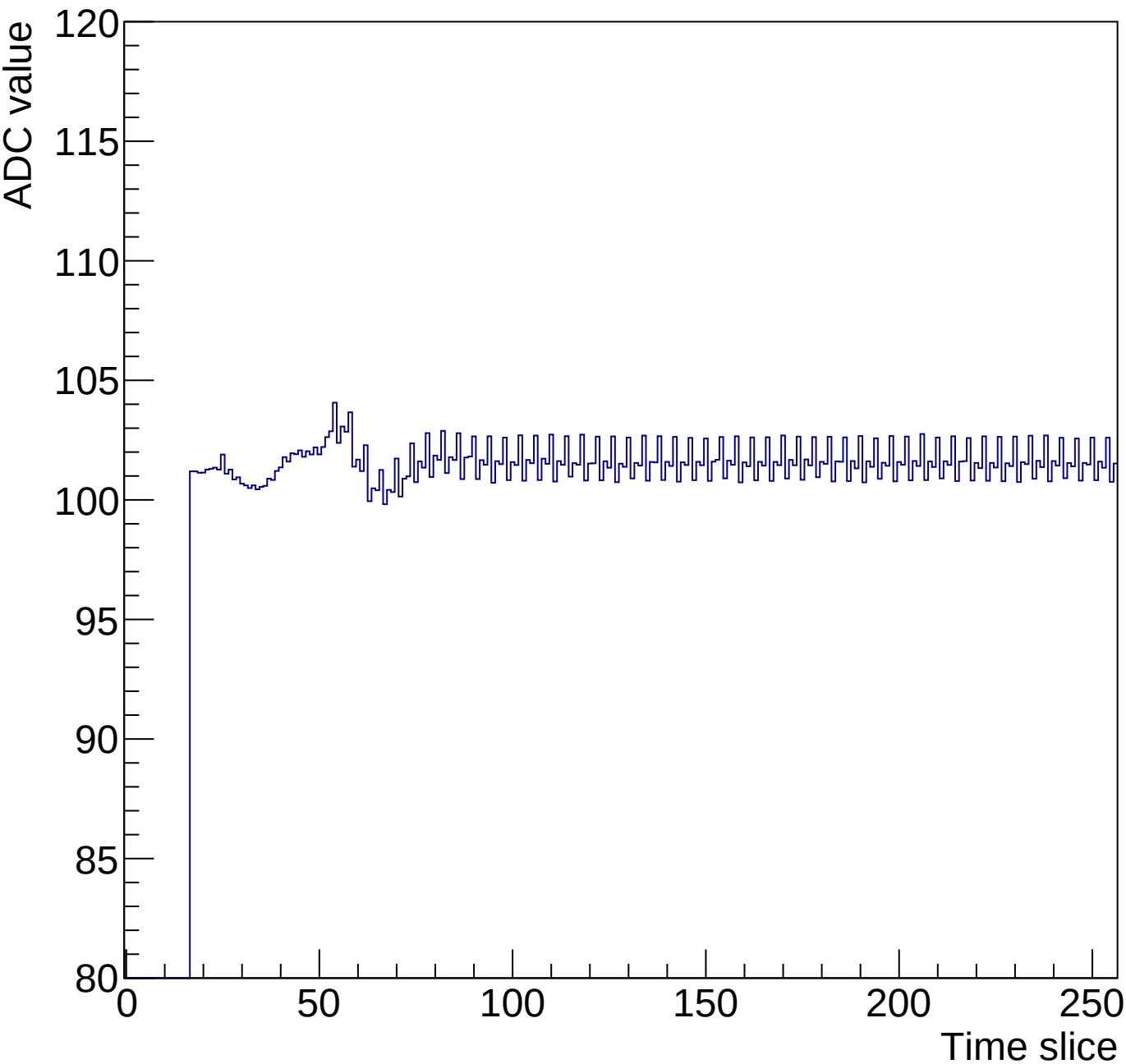
Run 2 Time mcm 0 chip 3 chan 4 256-60ns



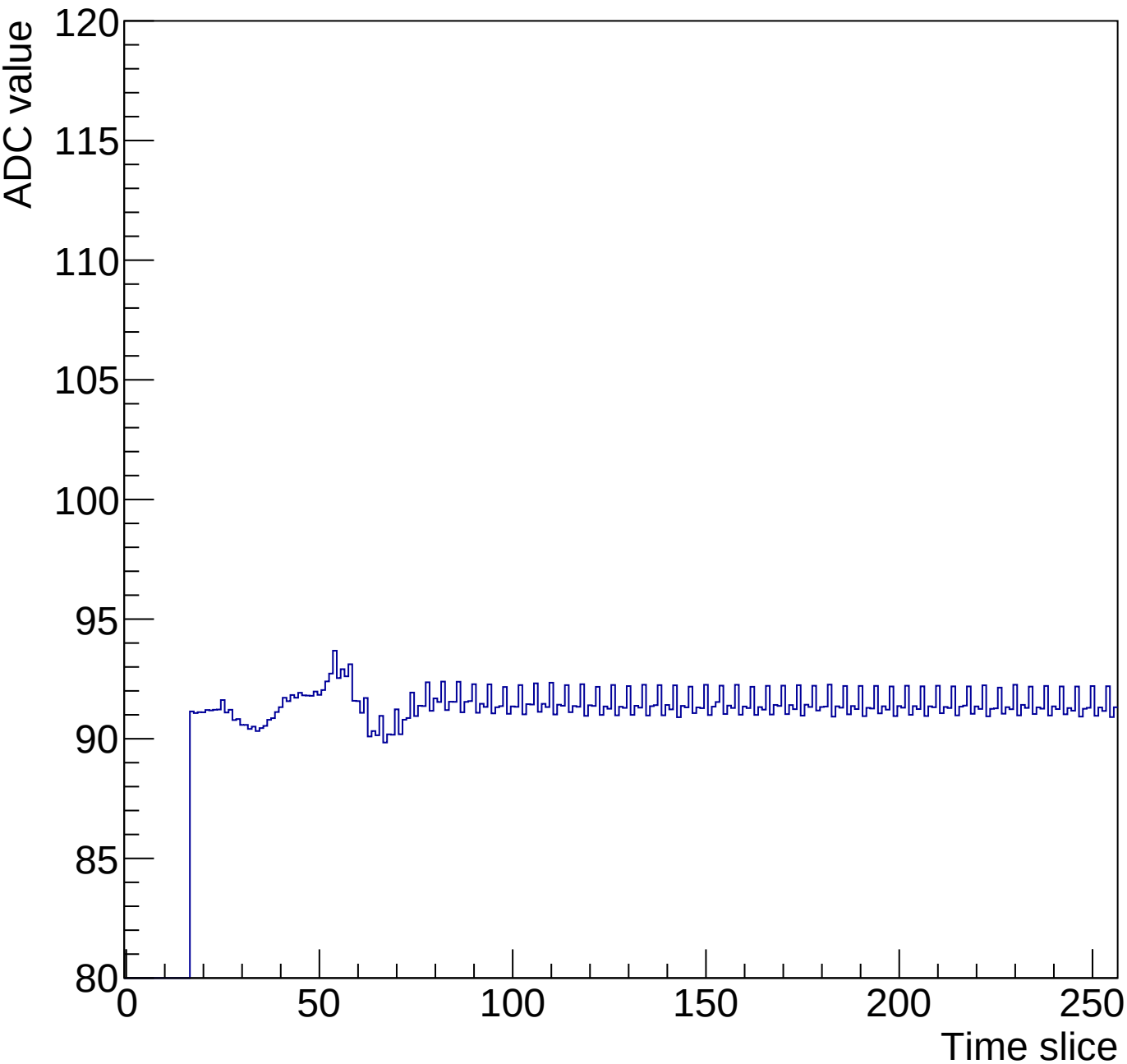
Run 2 Time mcm 0 chip 3 chan 5 256-60ns



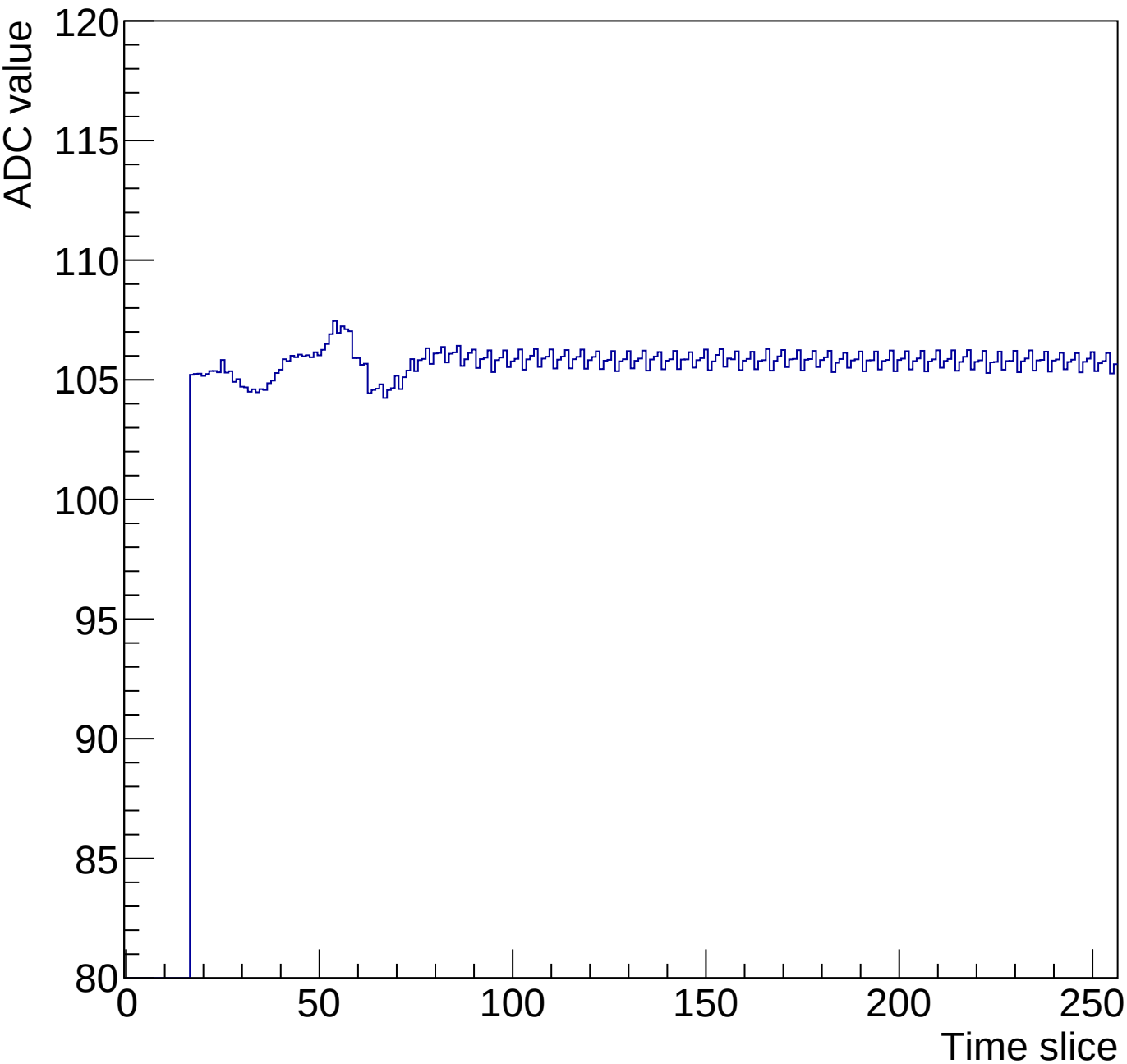
Run 2 Time mcm 0 chip 3 chan 6 256-60ns



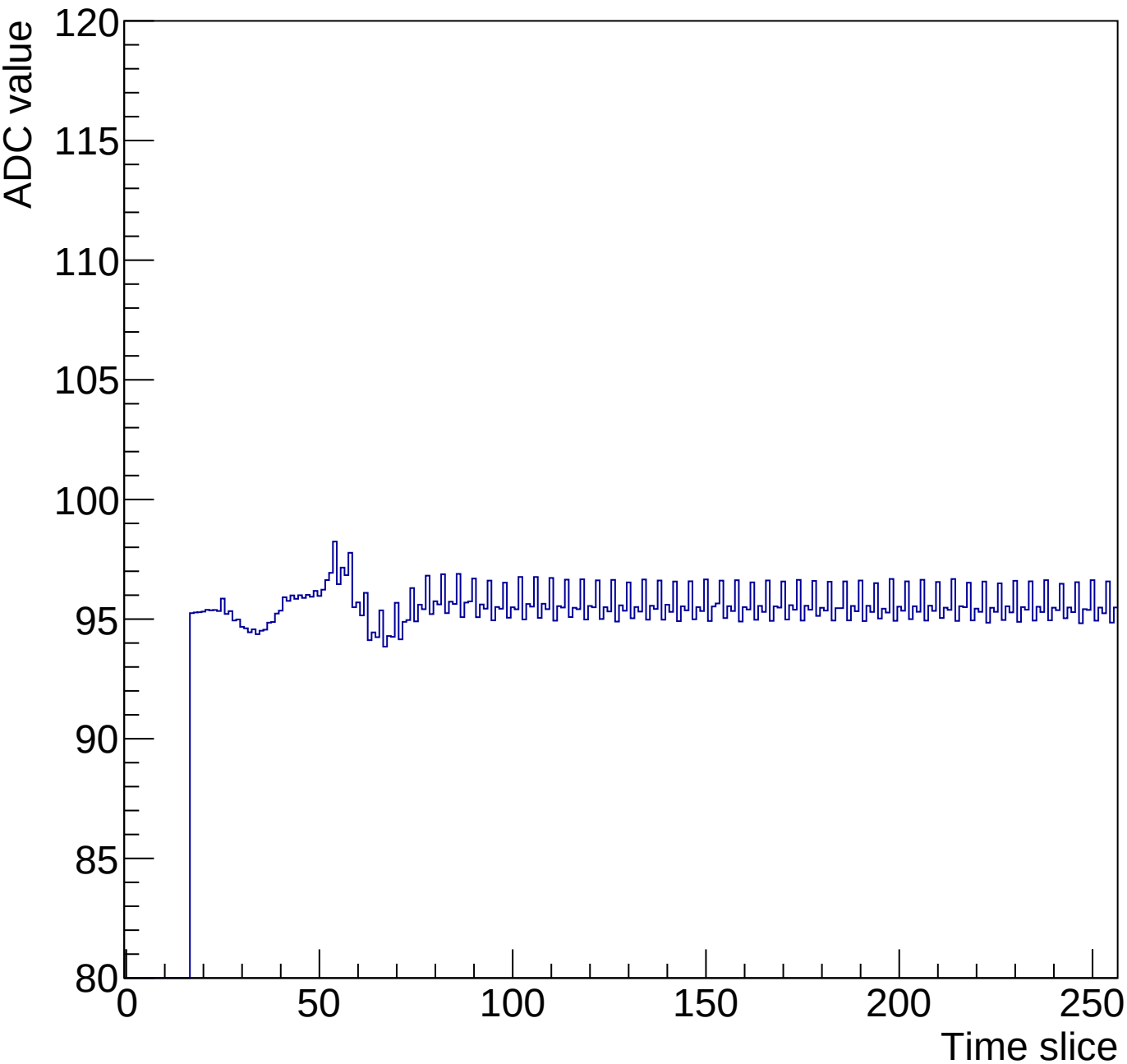
Run 2 Time mcm 0 chip 3 chan 7 256-60ns



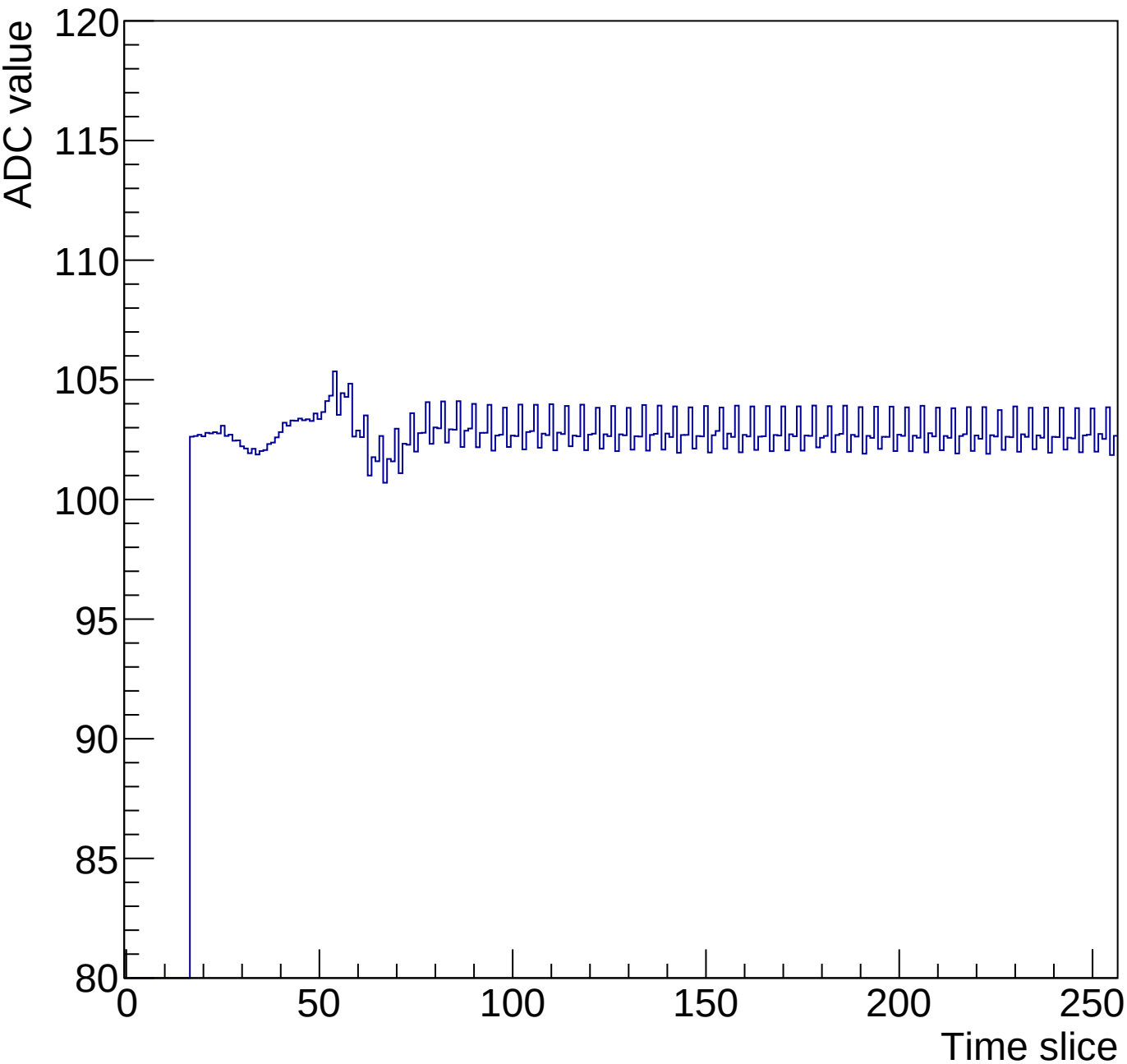
Run 2 Time mcm 0 chip 3 chan 8 256-60ns



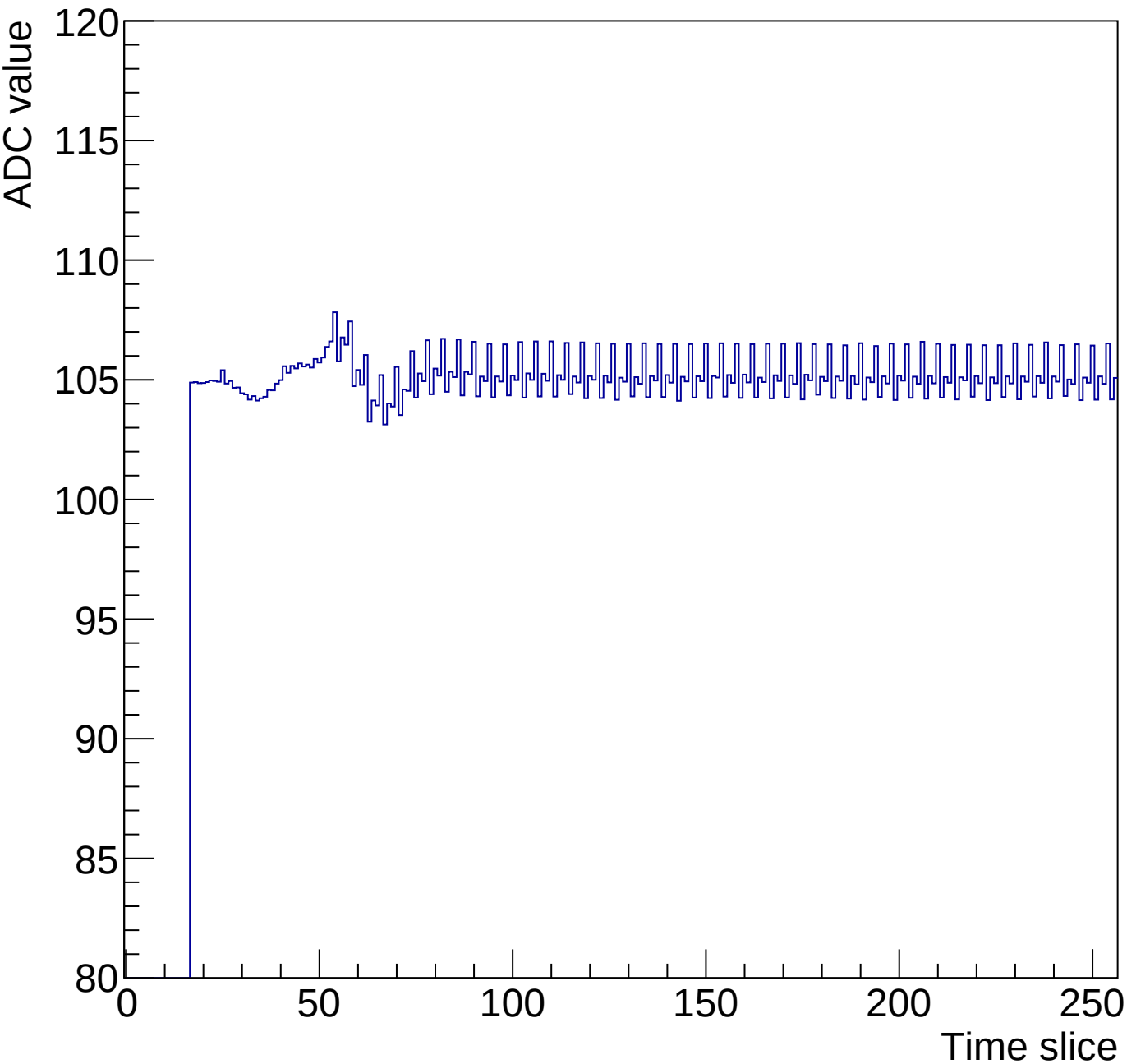
Run 2 Time mcm 0 chip 3 chan 9 256-60ns



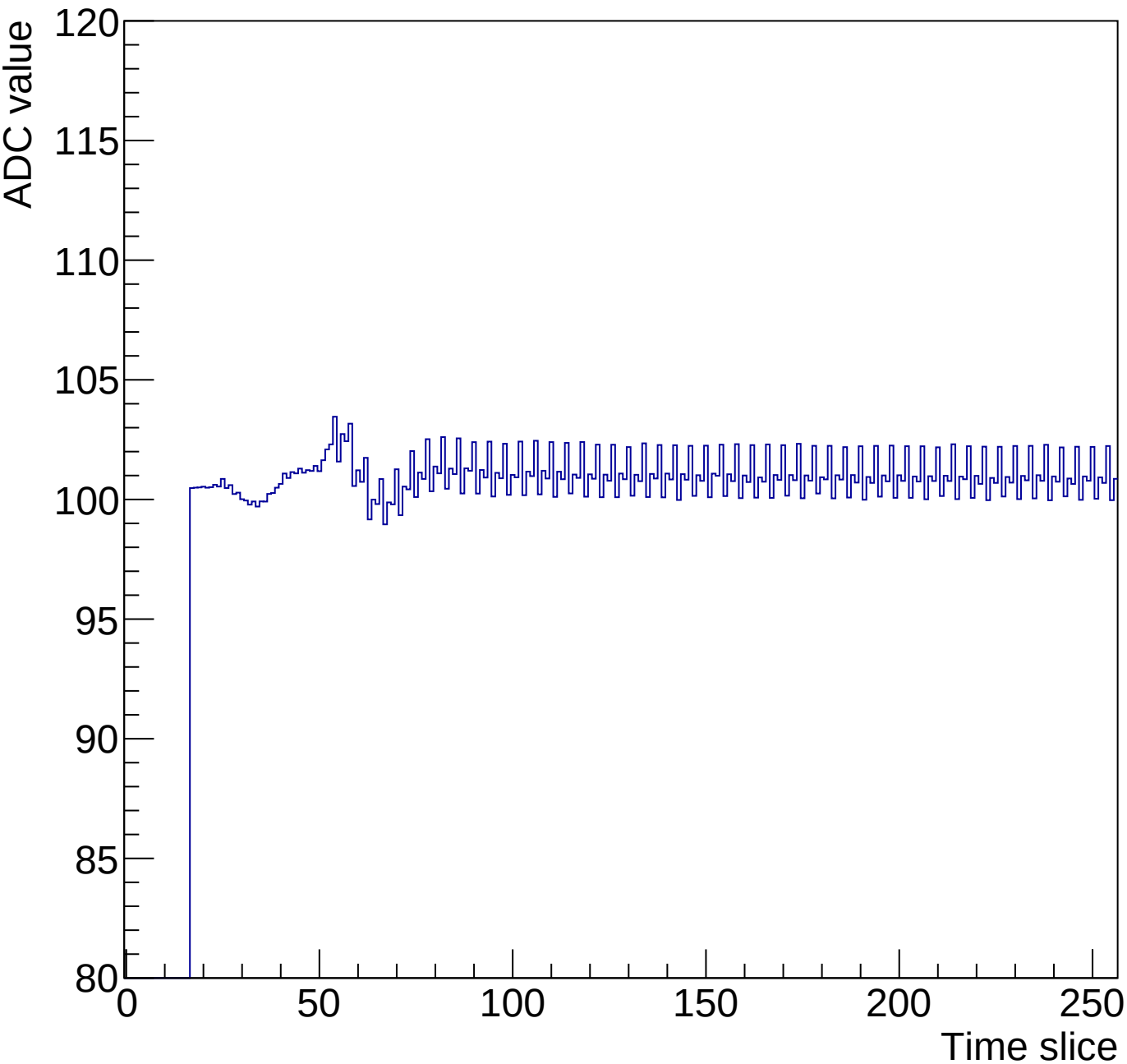
Run 2 Time mcm 0 chip 3 chan 10 256-60ns



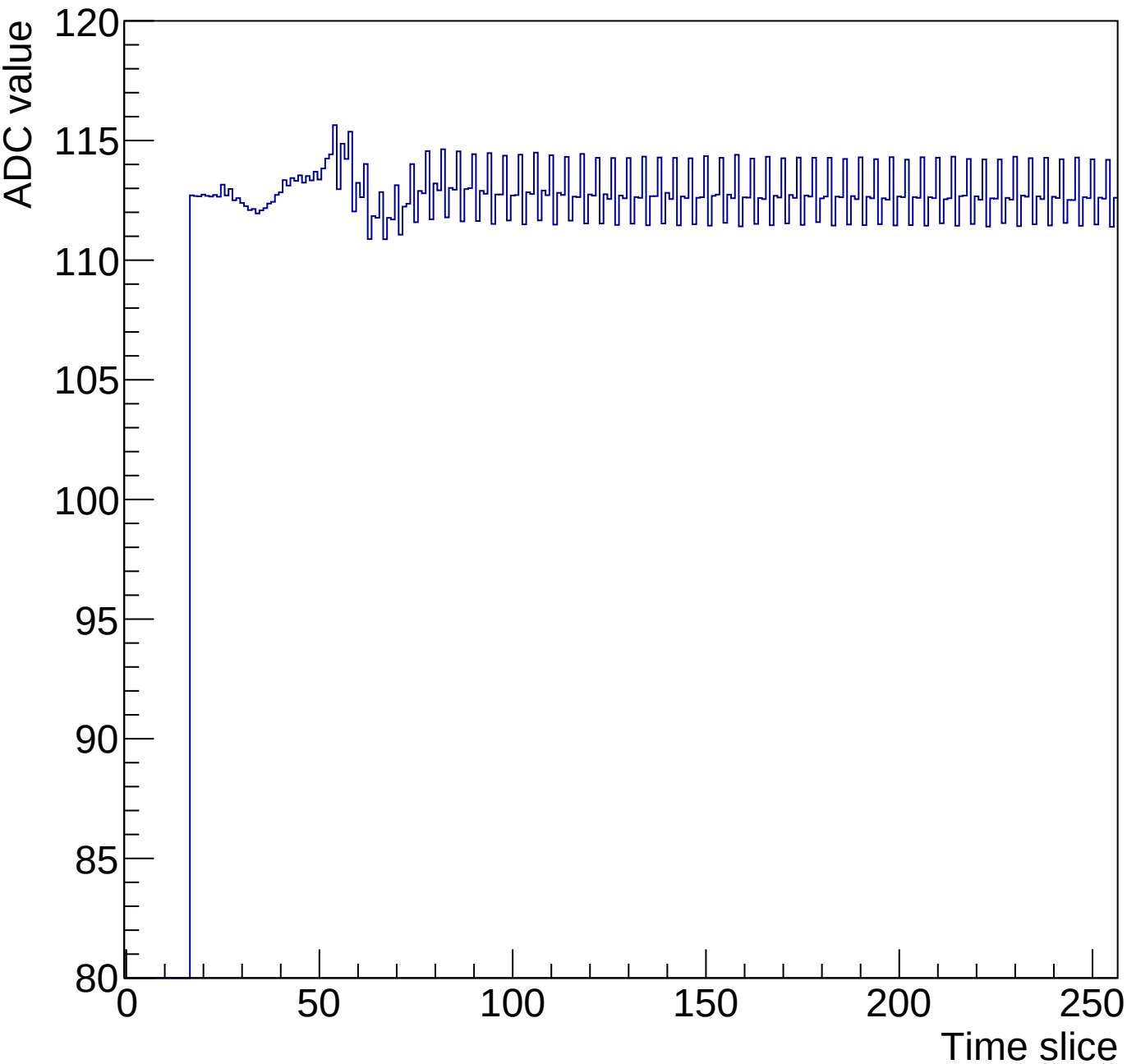
Run 2 Time mcm 0 chip 3 chan 11 256-60ns



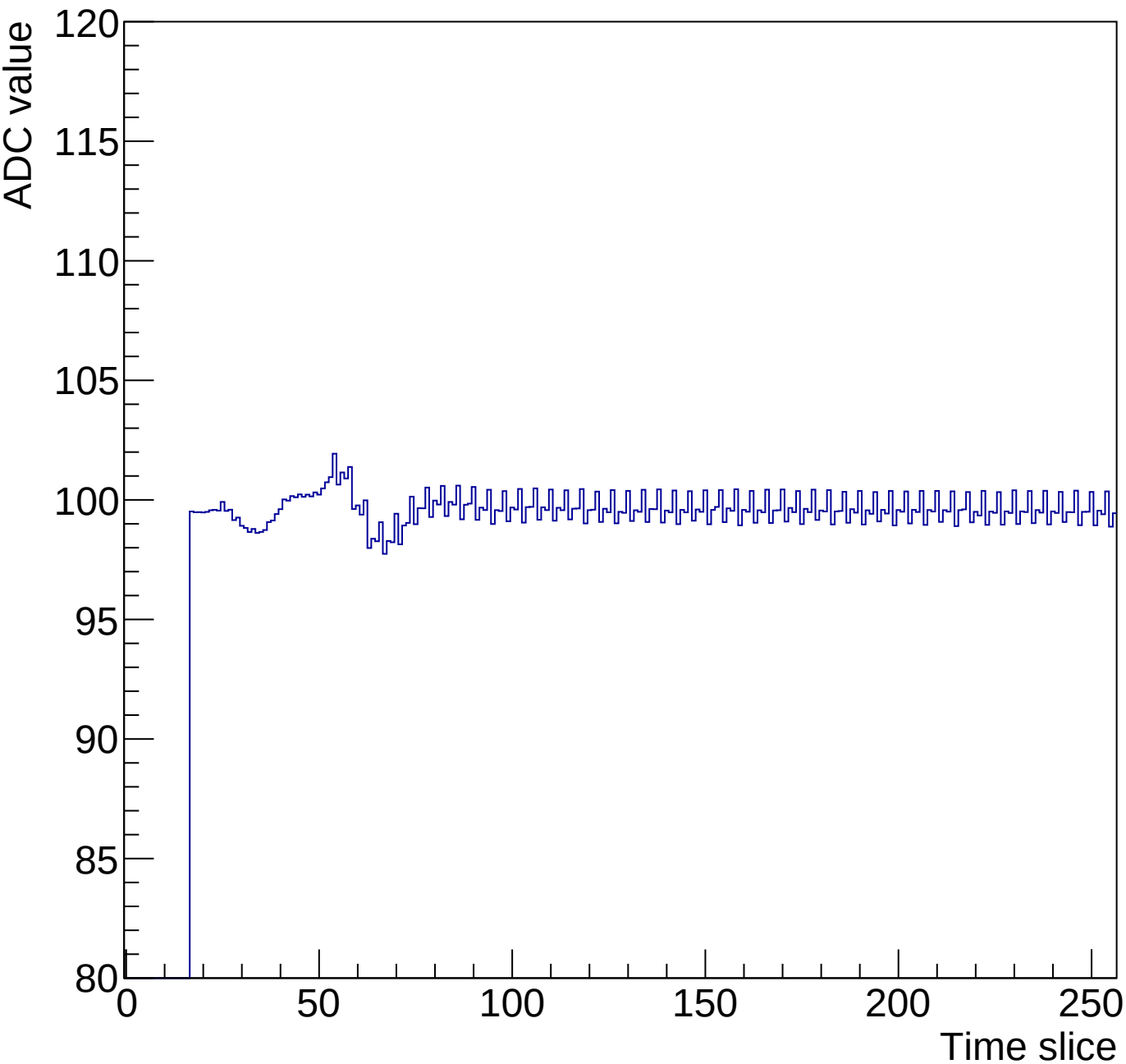
Run 2 Time mcm 0 chip 3 chan 12 256-60ns



Run 2 Time mcm 0 chip 3 chan 13 256-60ns



Run 2 Time mcm 0 chip 3 chan 14 256-60ns



Run 2 Time mcm 0 chip 3 chan 15 256-60ns

