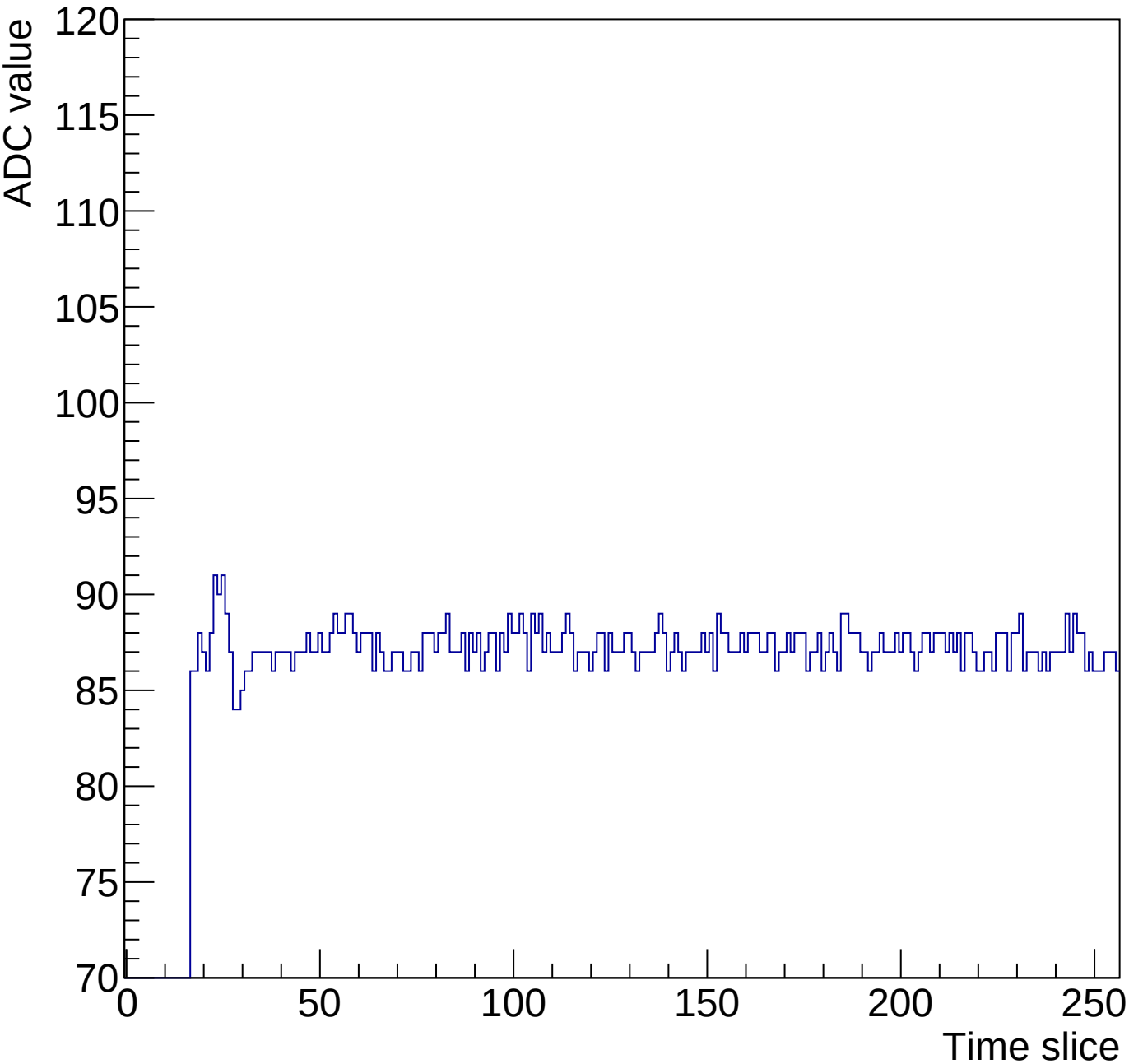
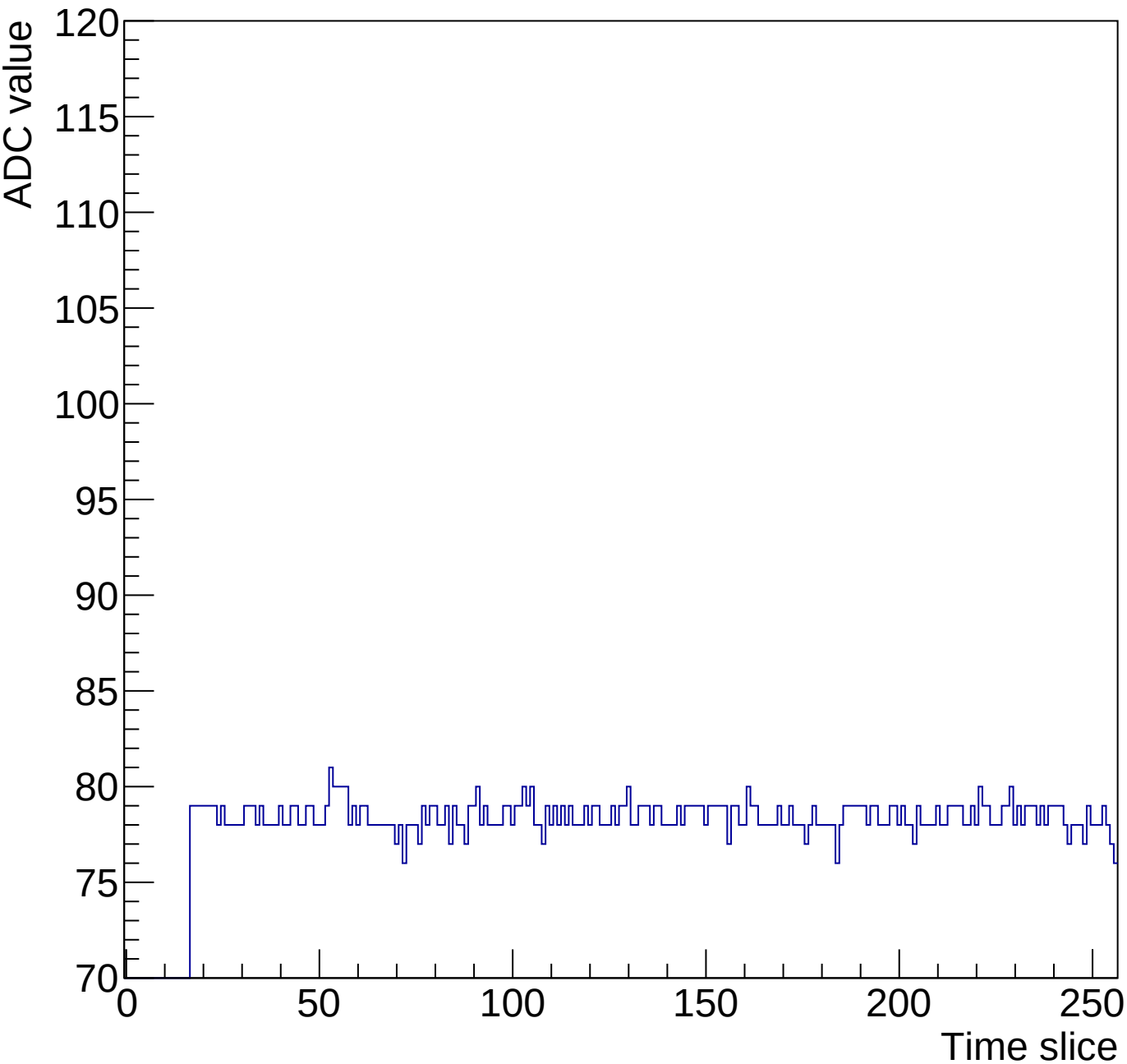


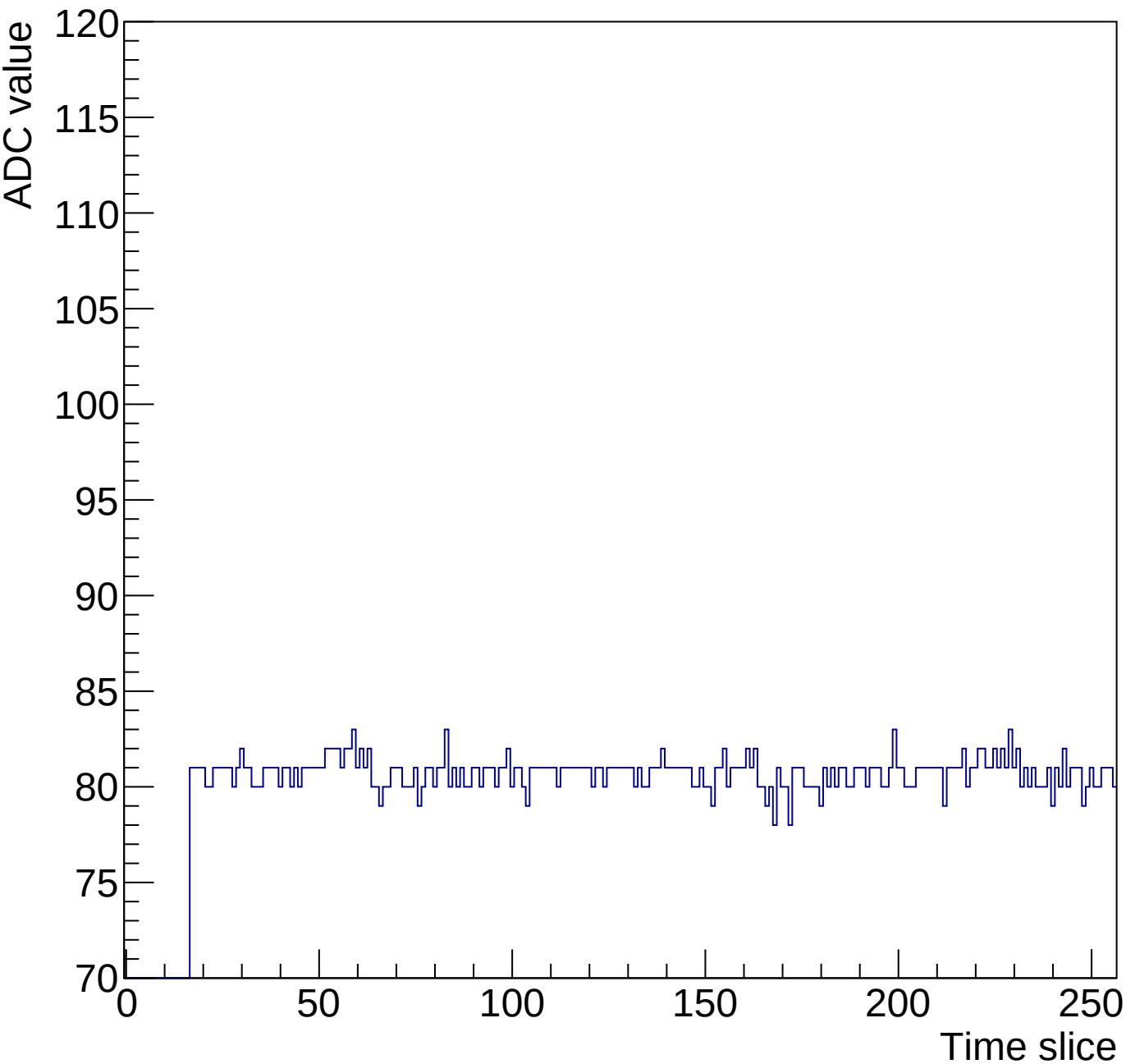
Run 1 event 100 mcm 1 chip 3 channel 0 256-120ns



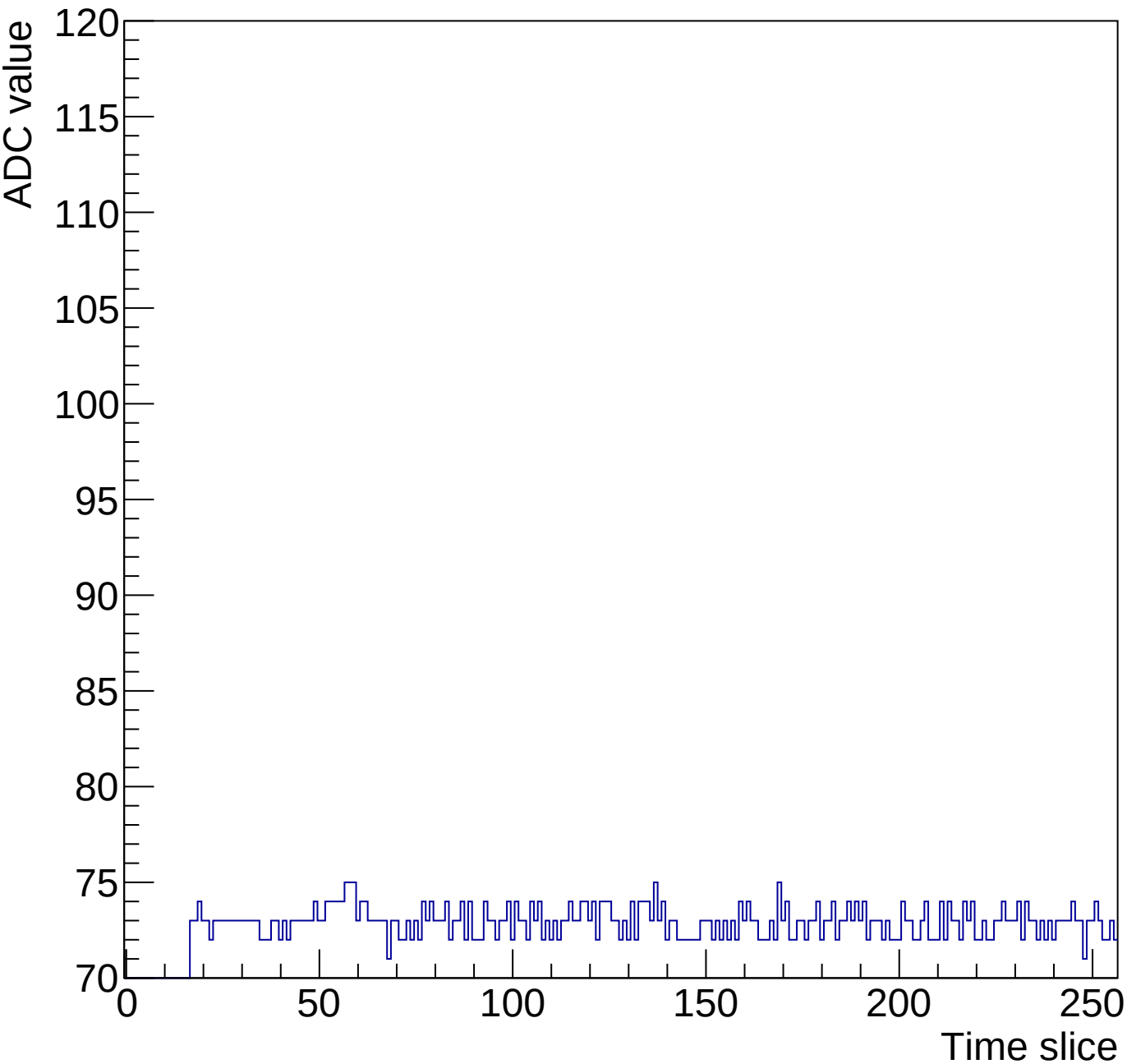
Run 1 event 100 mcm 1 chip 3 channel 1 256-120ns



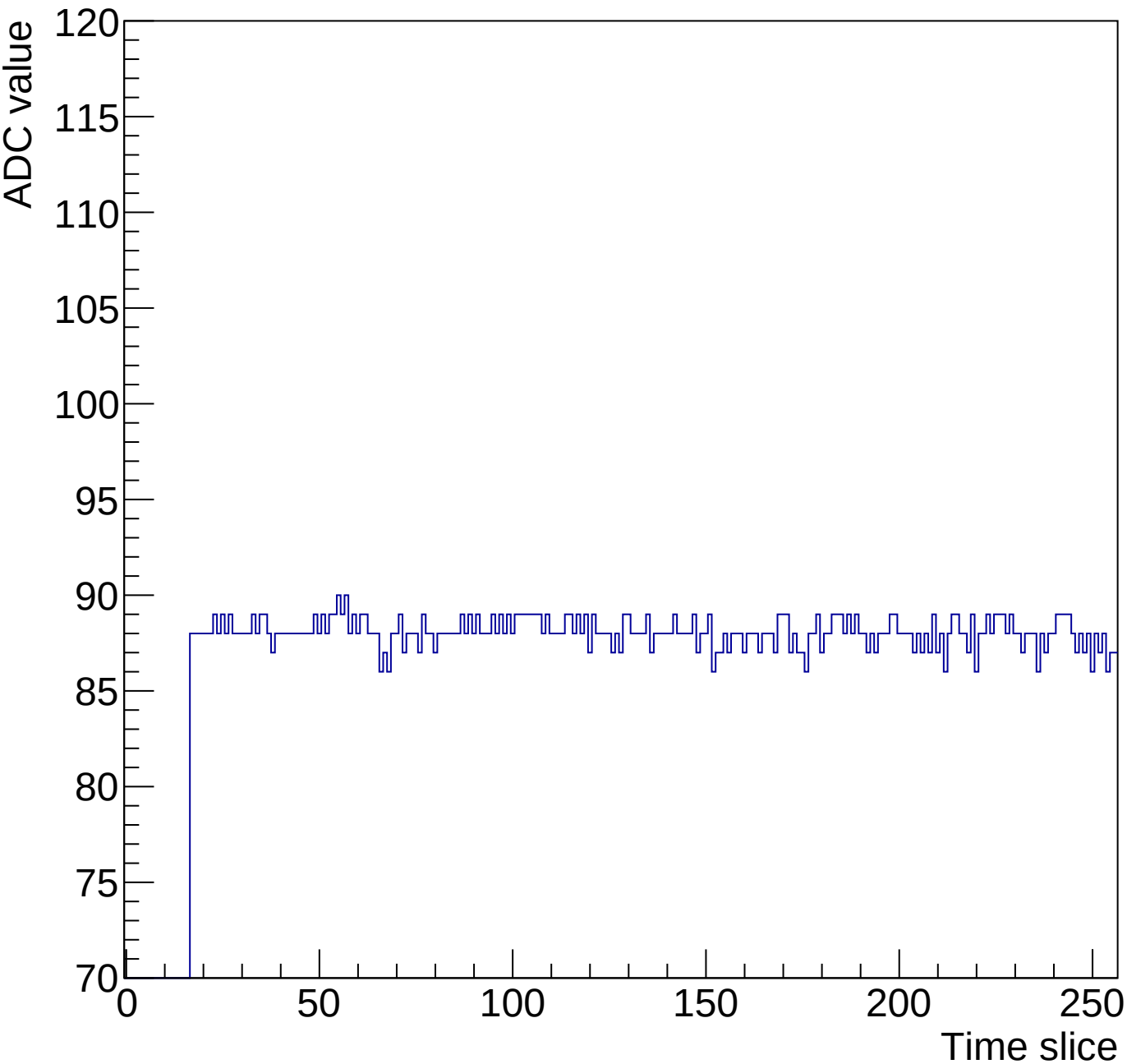
Run 1 event 100 mcm 1 chip 3 channel 2 256-120ns



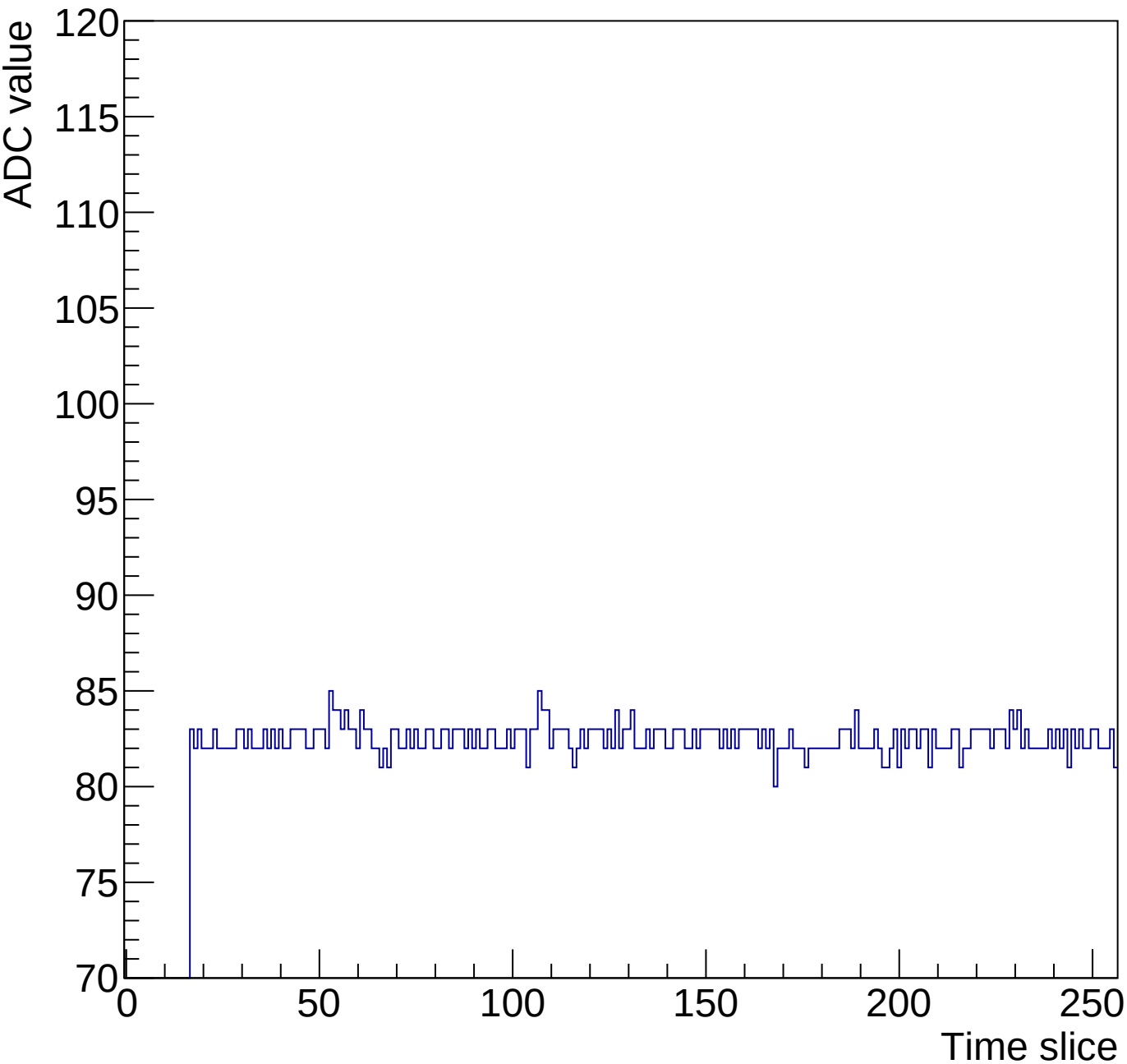
Run 1 event 100 mcm 1 chip 3 channel 3 256-120ns



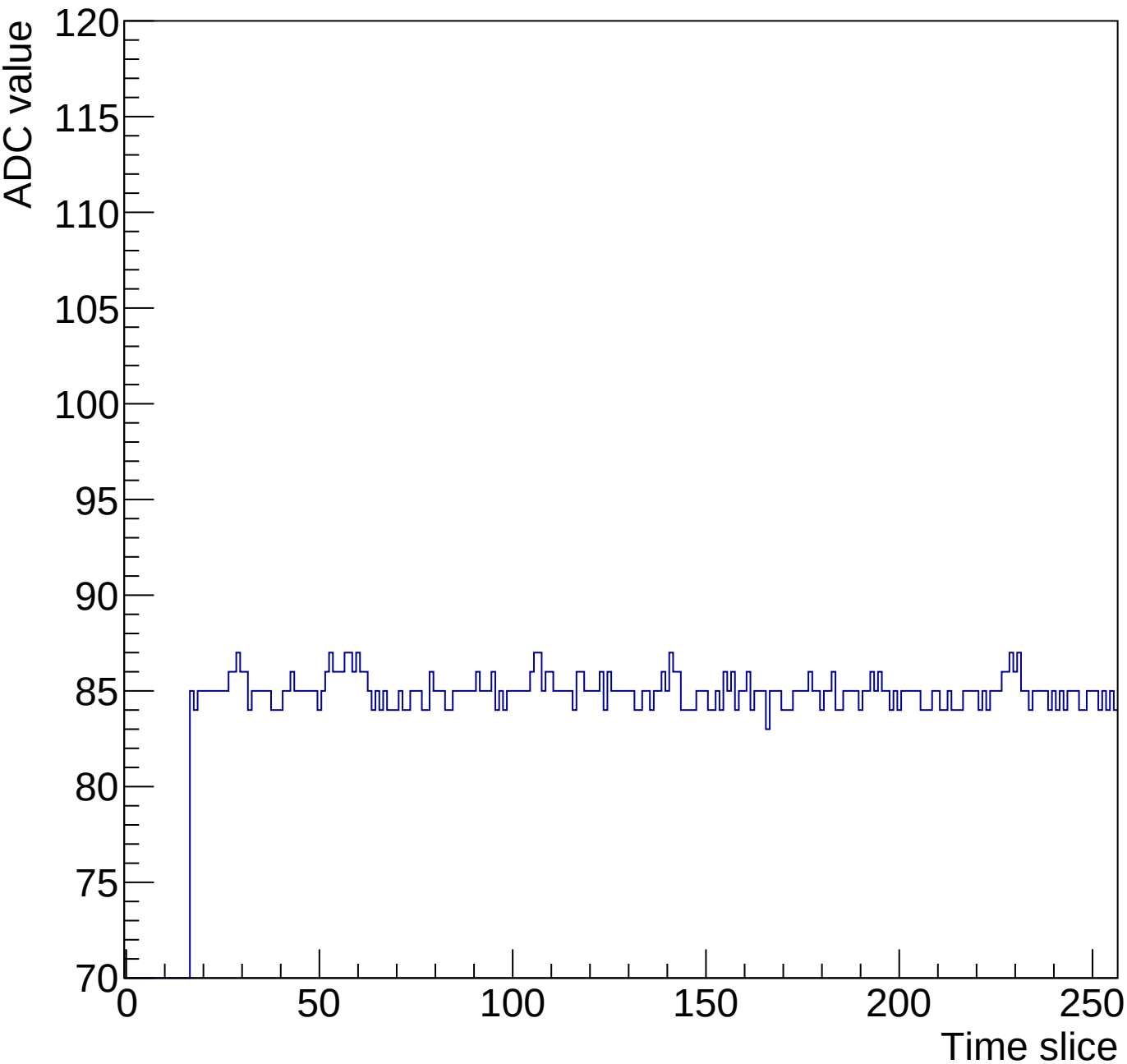
Run 1 event 100 mcm 1 chip 3 channel 4 256-120ns



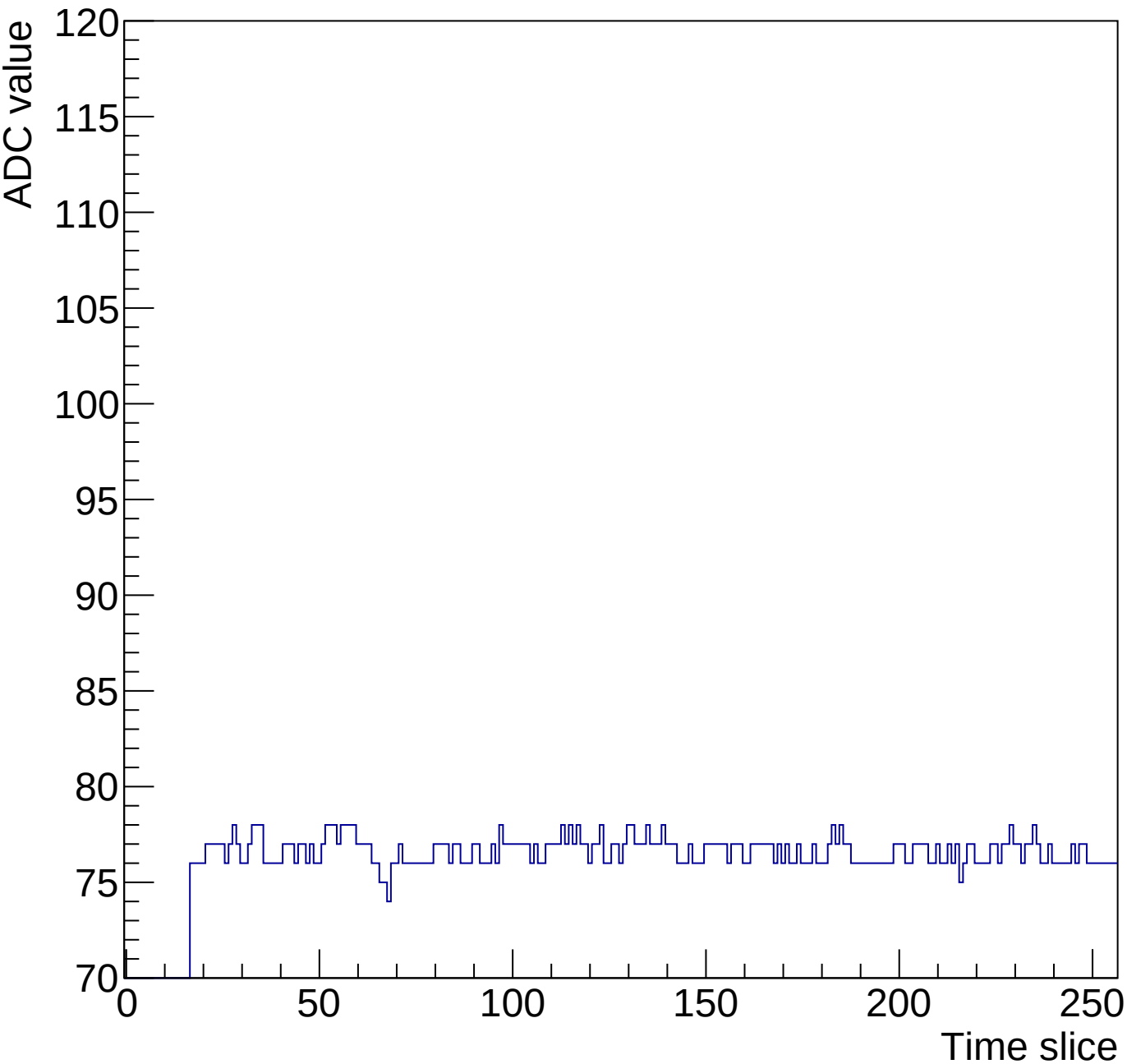
Run 1 event 100 mcm 1 chip 3 channel 5 256-120ns



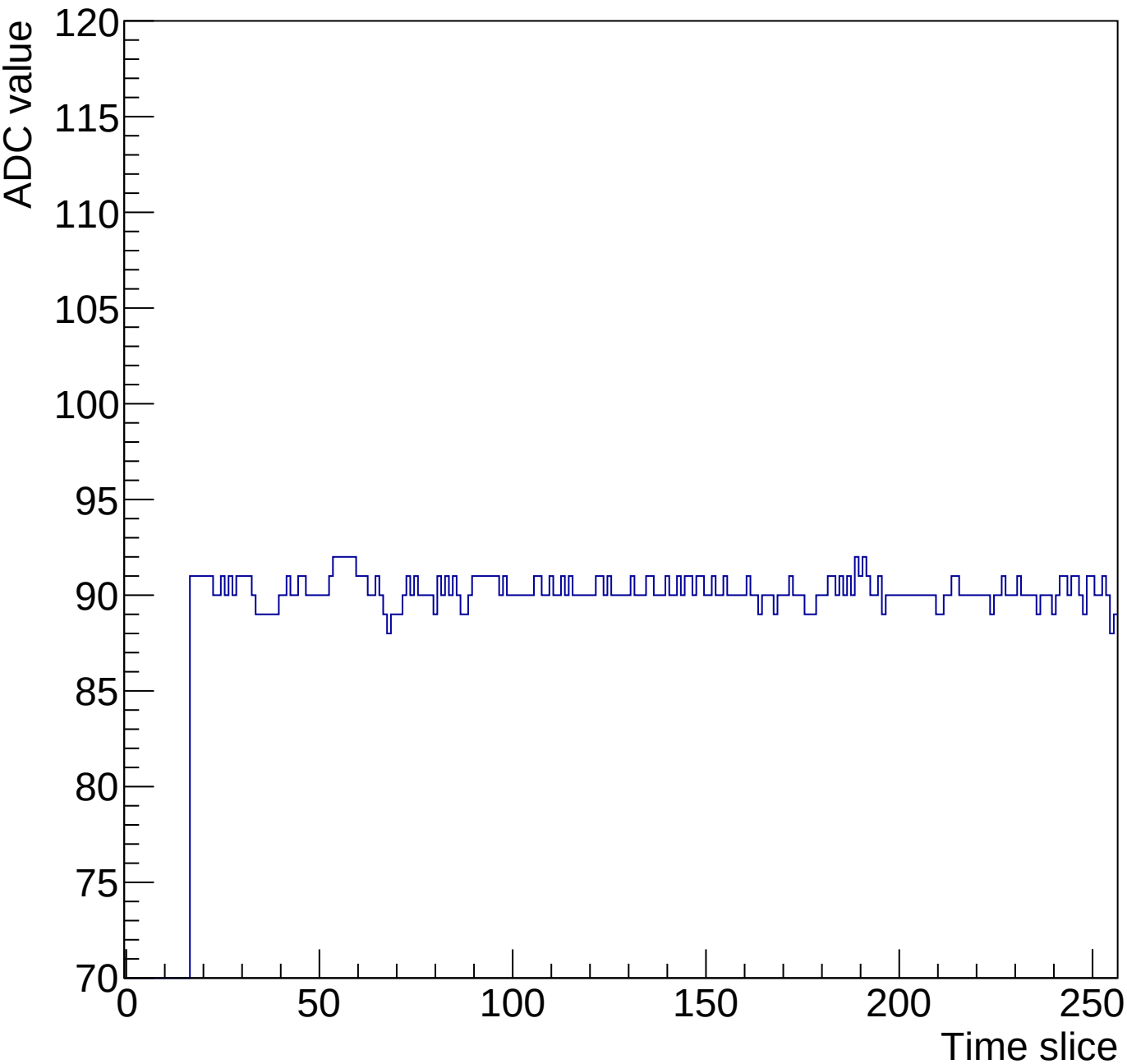
Run 1 event 100 mcm 1 chip 3 channel 6 256-120ns



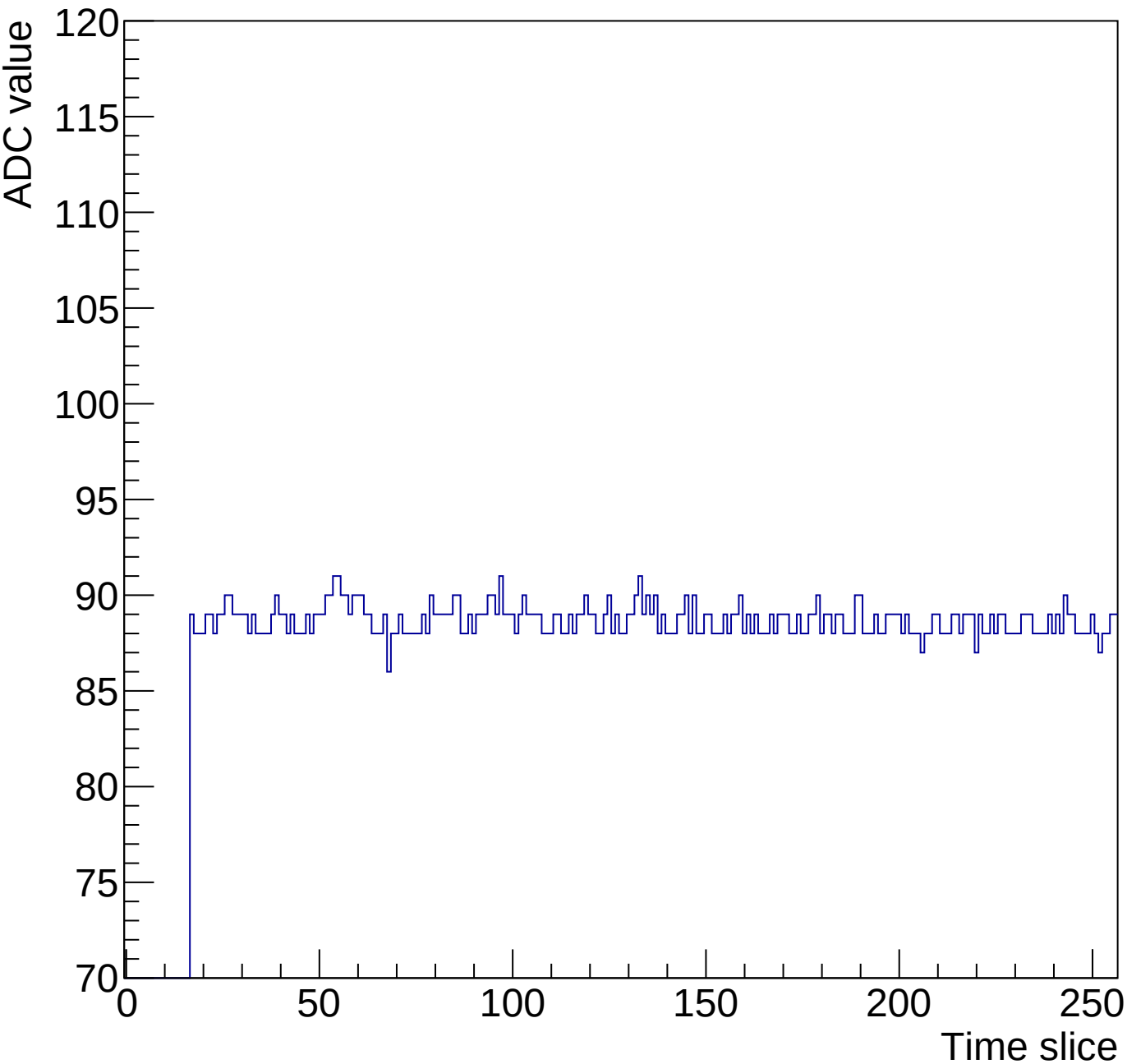
Run 1 event 100 mcm 1 chip 3 channel 7 256-120ns



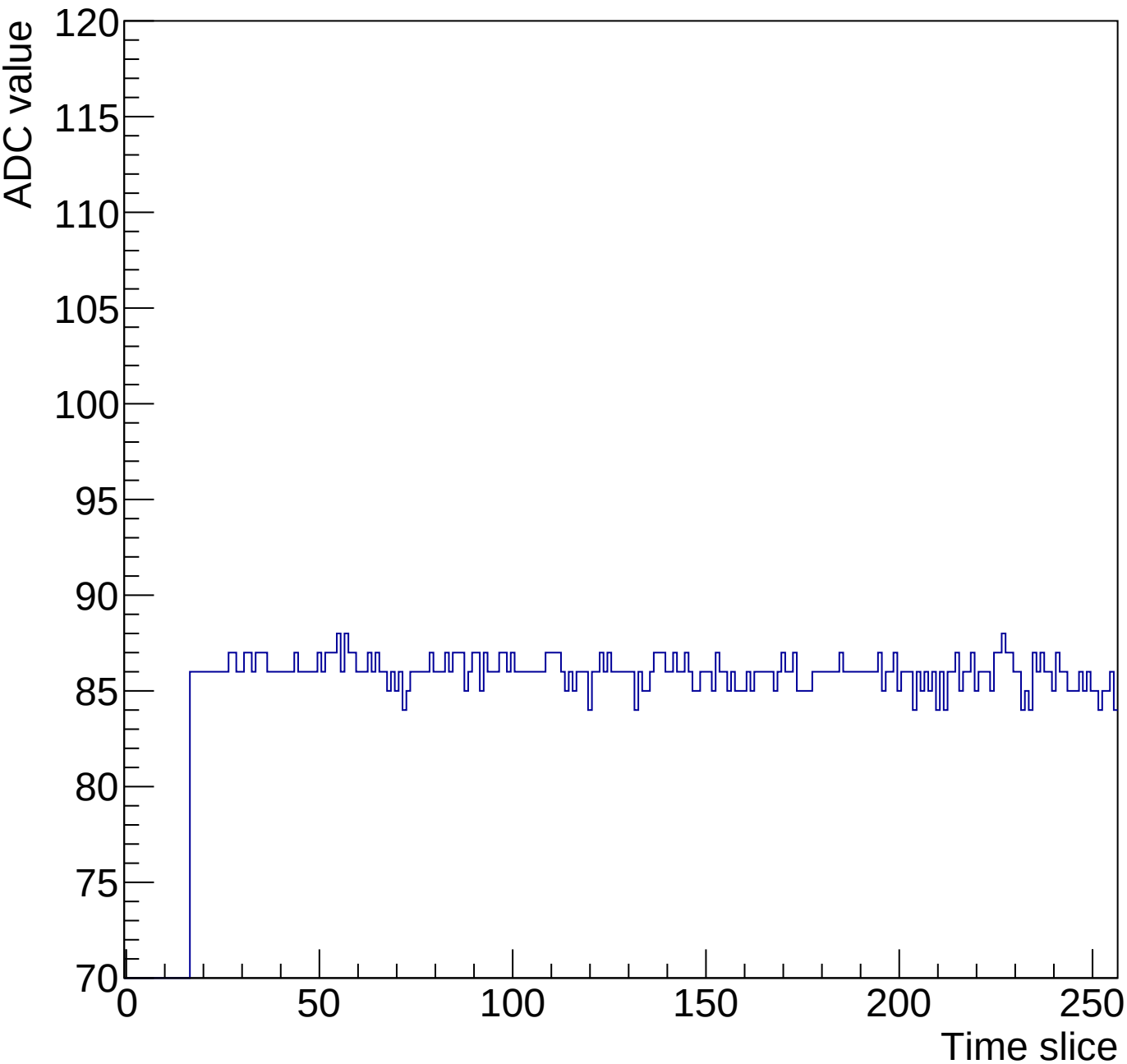
Run 1 event 100 mcm 1 chip 3 channel 8 256-120ns



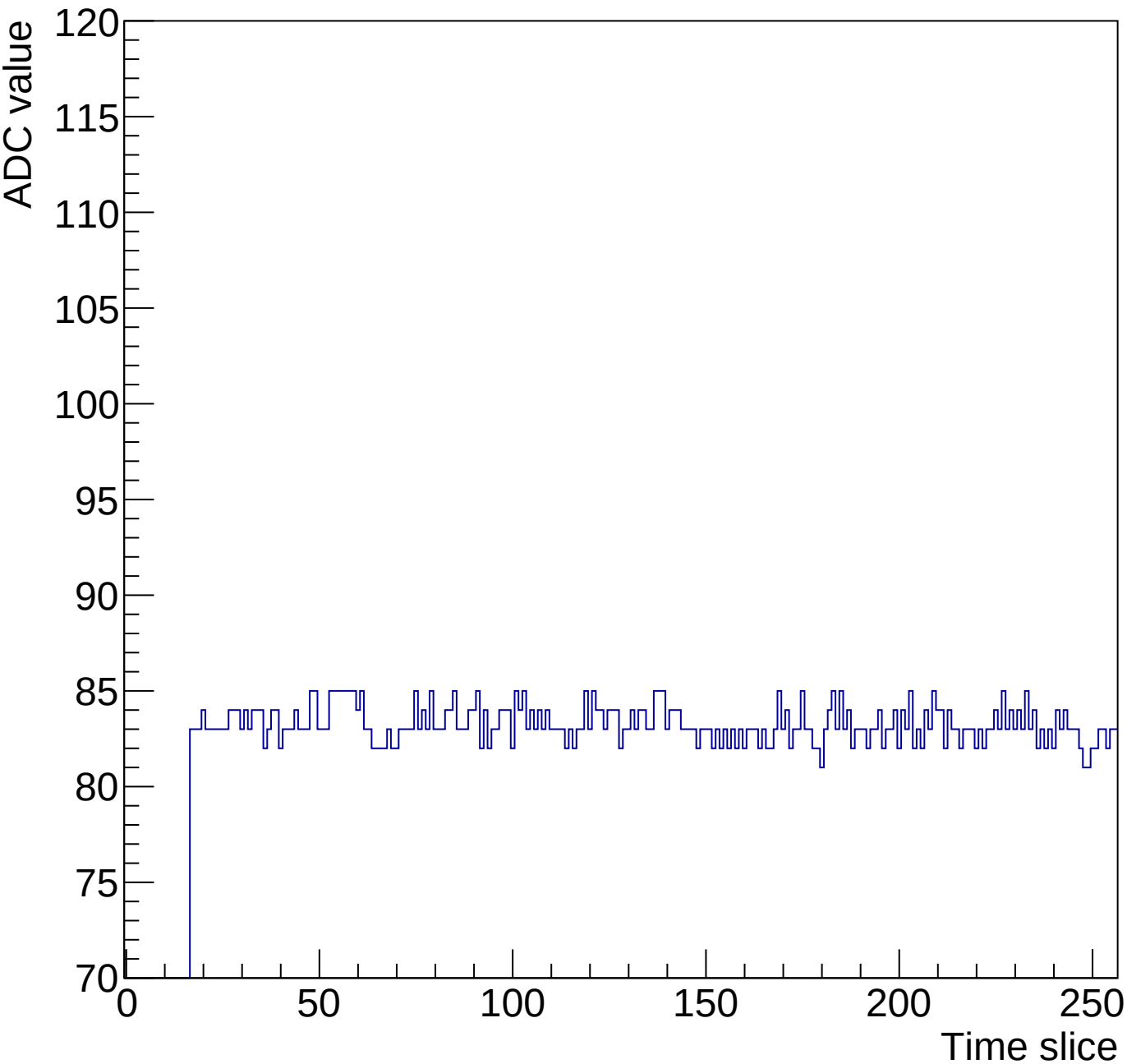
Run 1 event 100 mcm 1 chip 3 channel 9 256-120ns



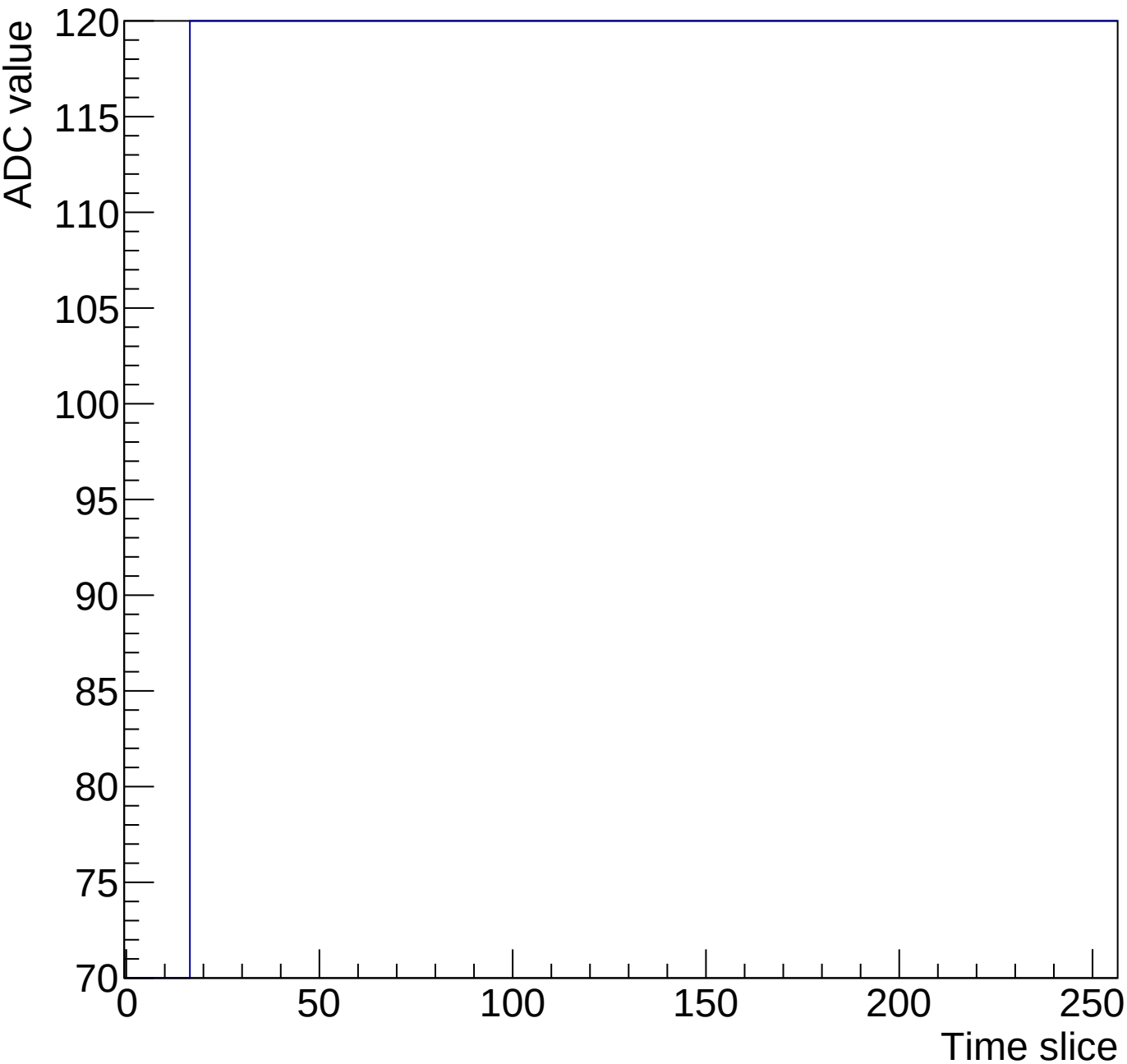
Run 1 event 100 mcm 1 chip 3 channel 10 256-120ns



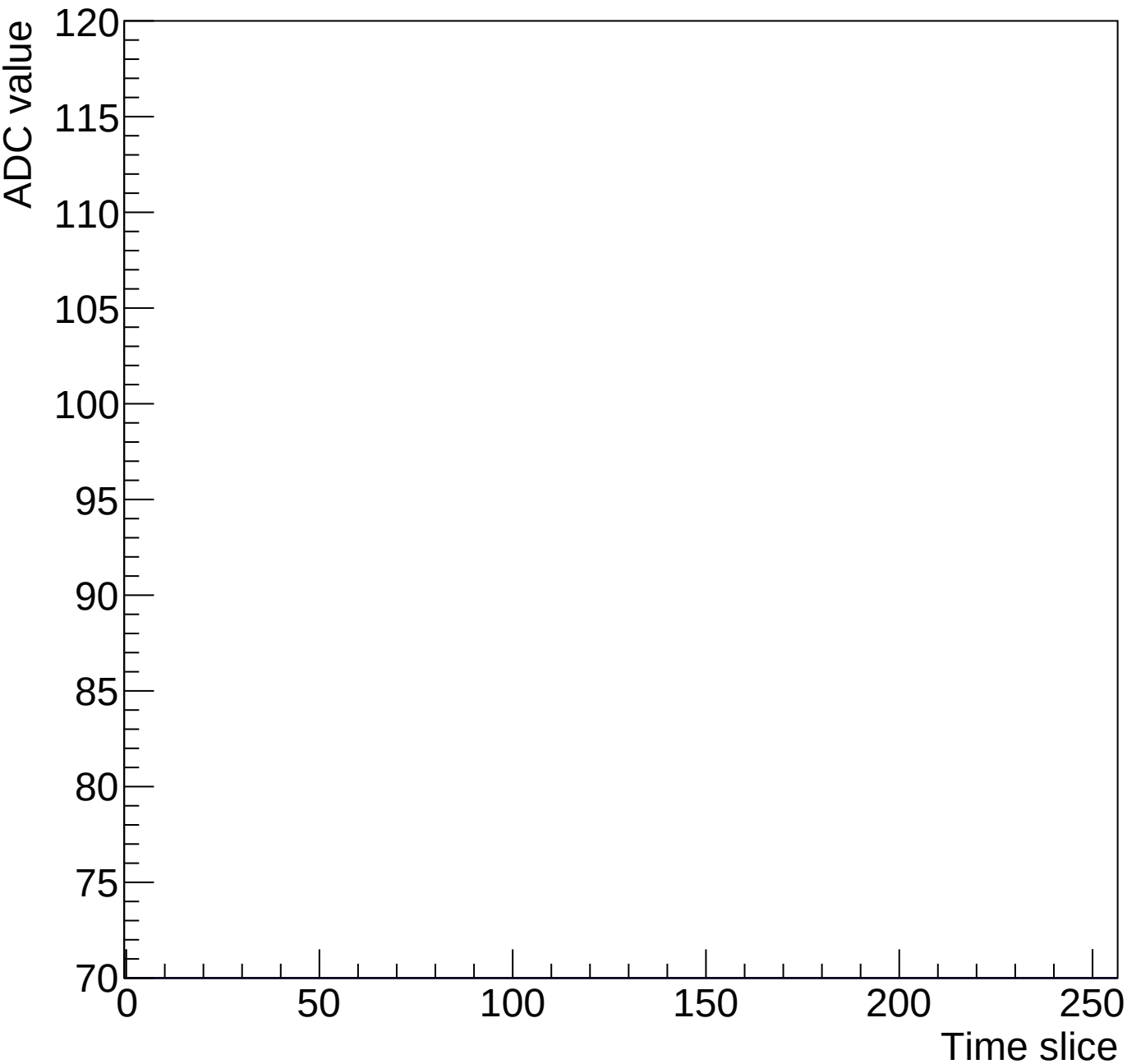
Run 1 event 100 mcm 1 chip 3 channel 11 256-120ns



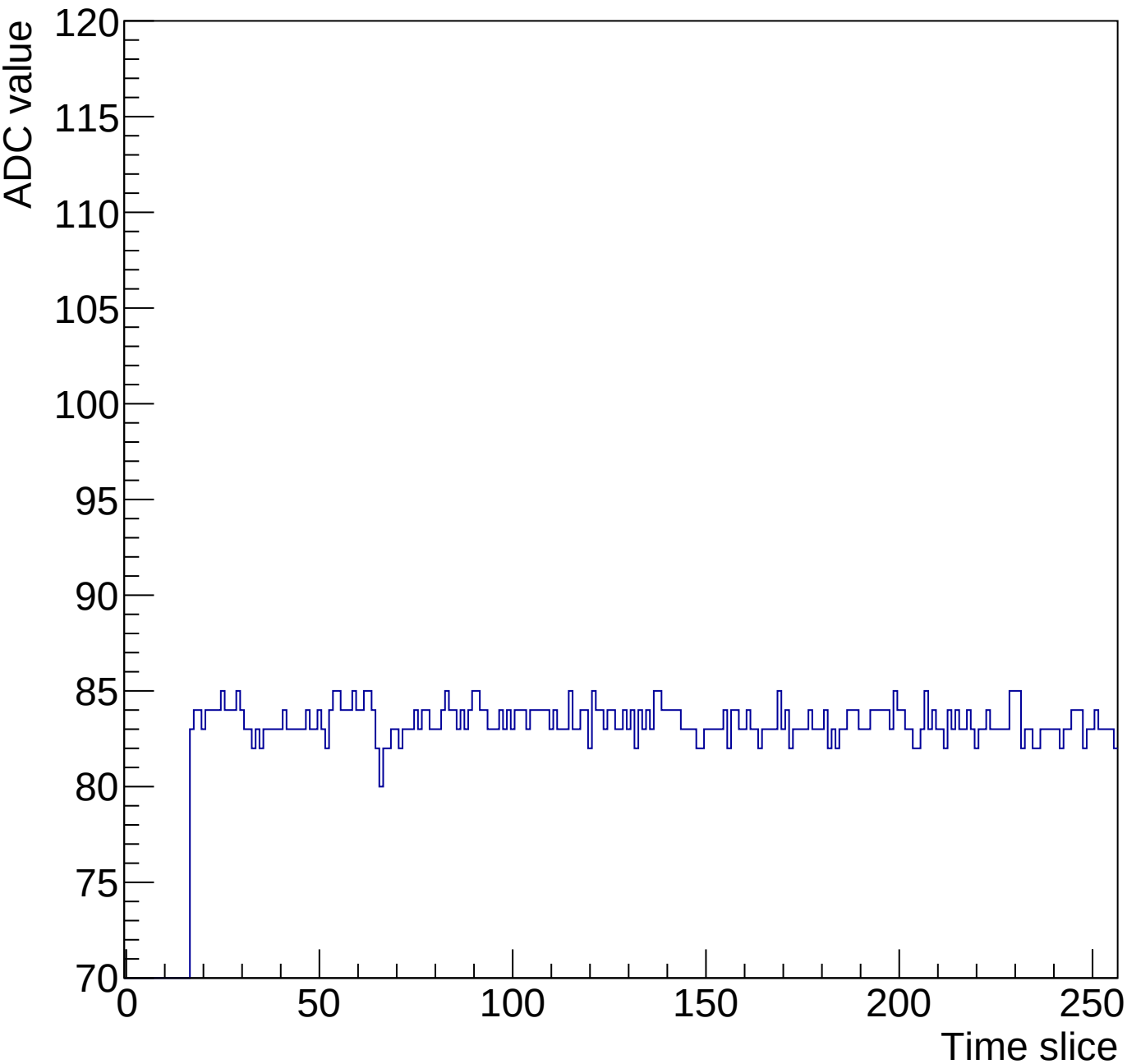
Run 1 event 100 mcm 1 chip 3 channel 12 256-120ns



Run 1 event 100 mcm 1 chip 3 channel 13 256-120ns



Run 1 event 100 mcm 1 chip 3 channel 14 256-120ns



Run 1 event 100 mcm 1 chip 3 channel 15 256-120ns

