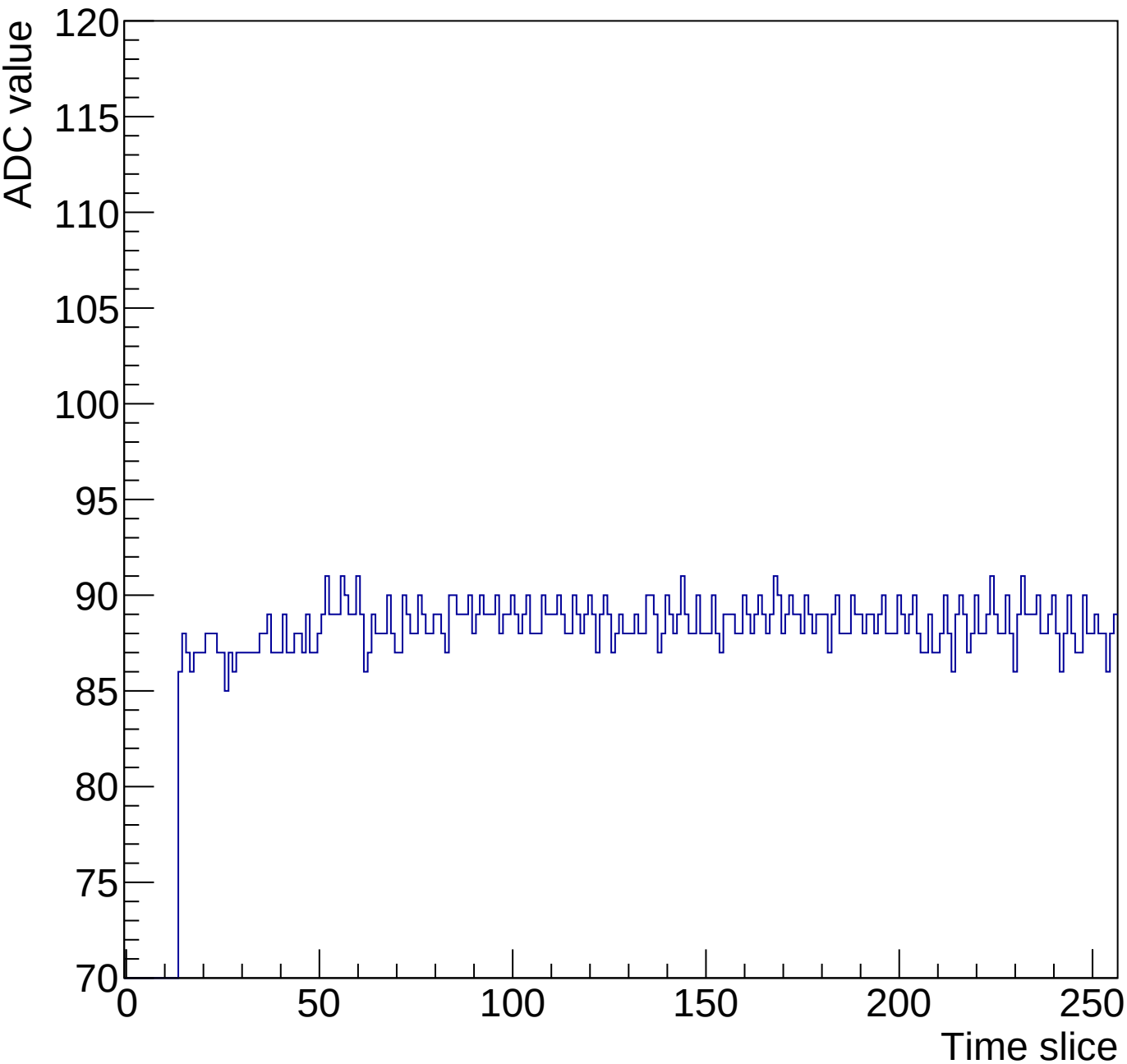
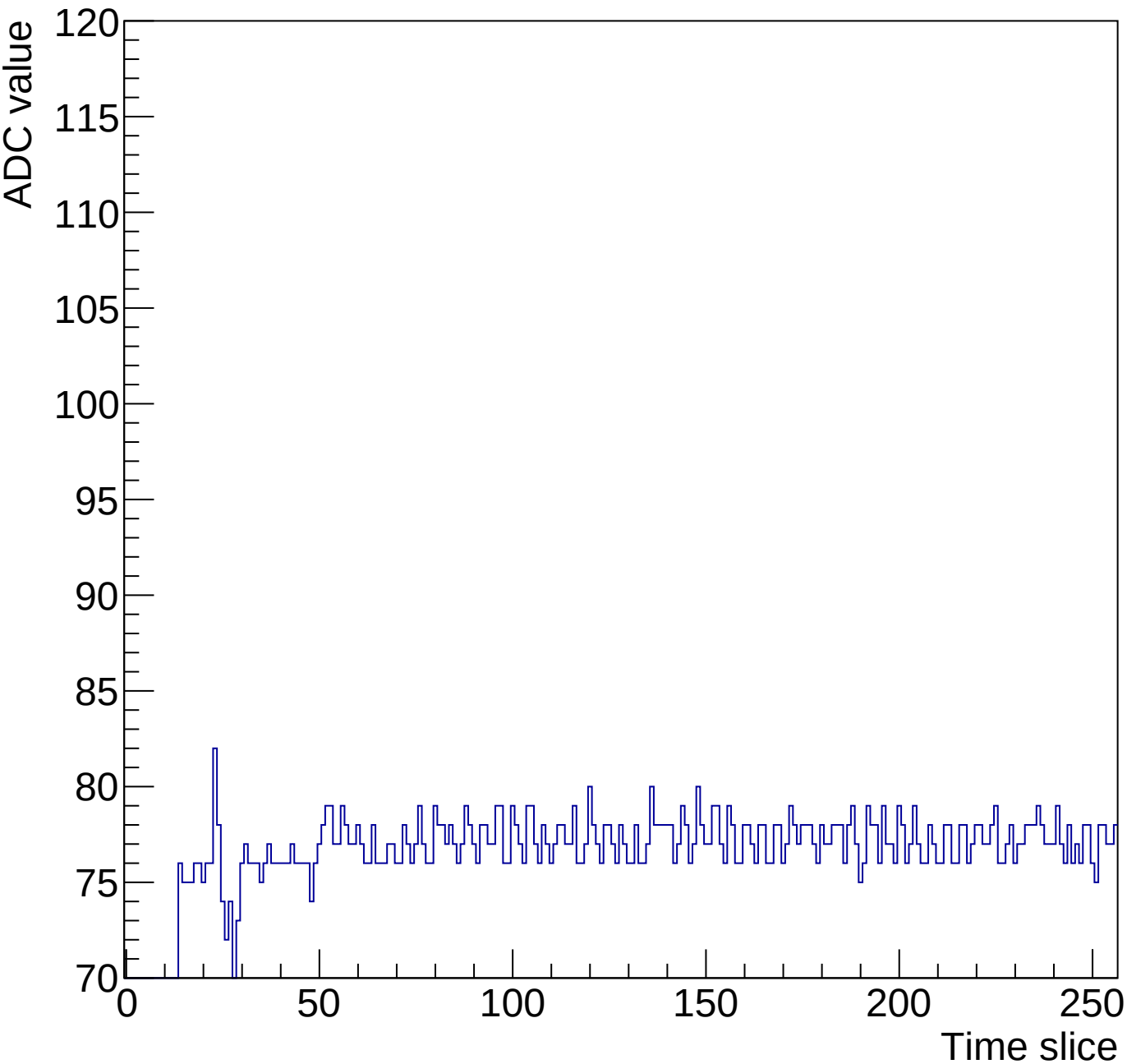


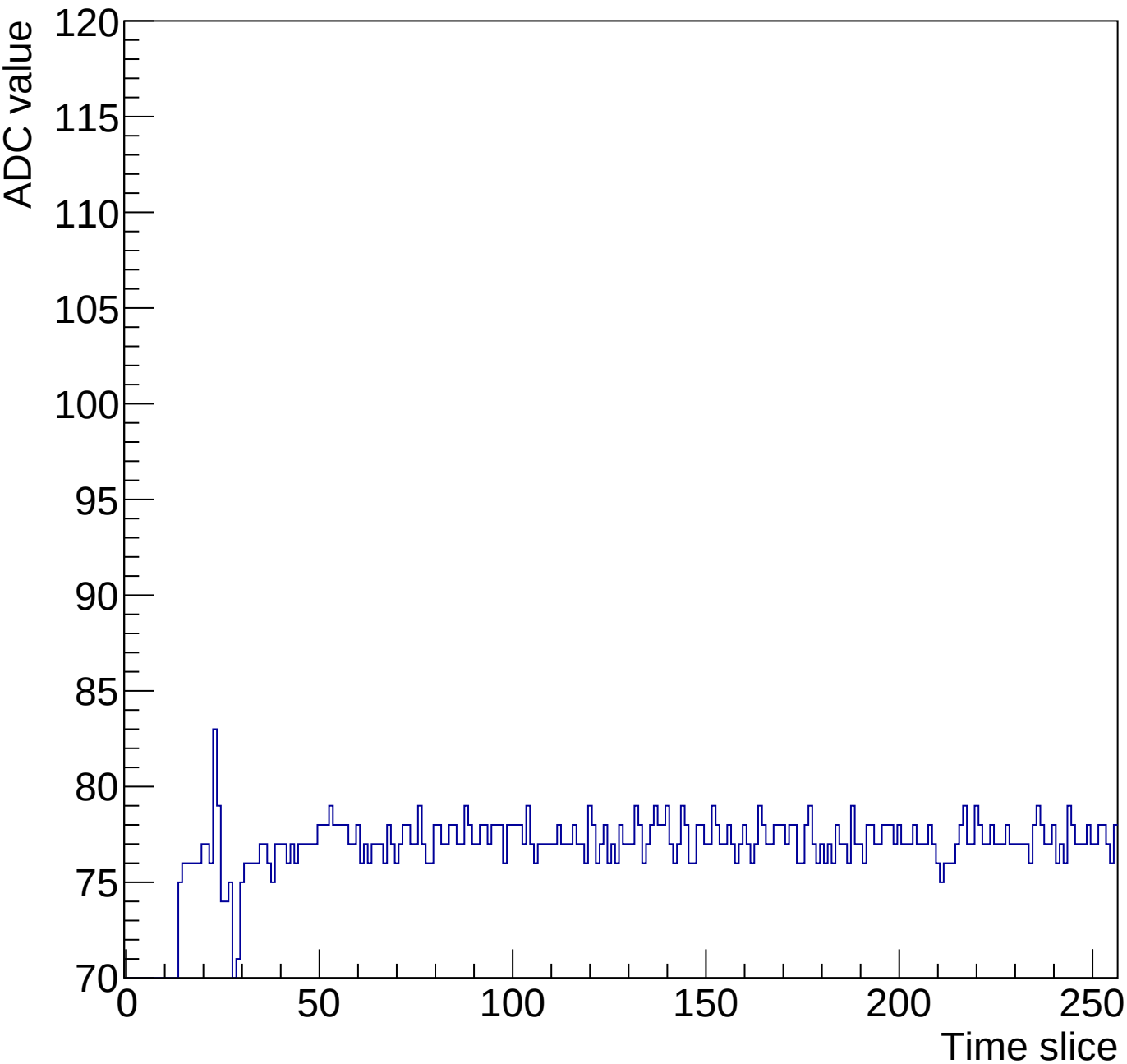
Run 2 event 100 mcm 1 chip 0 channel 0 256-90ns



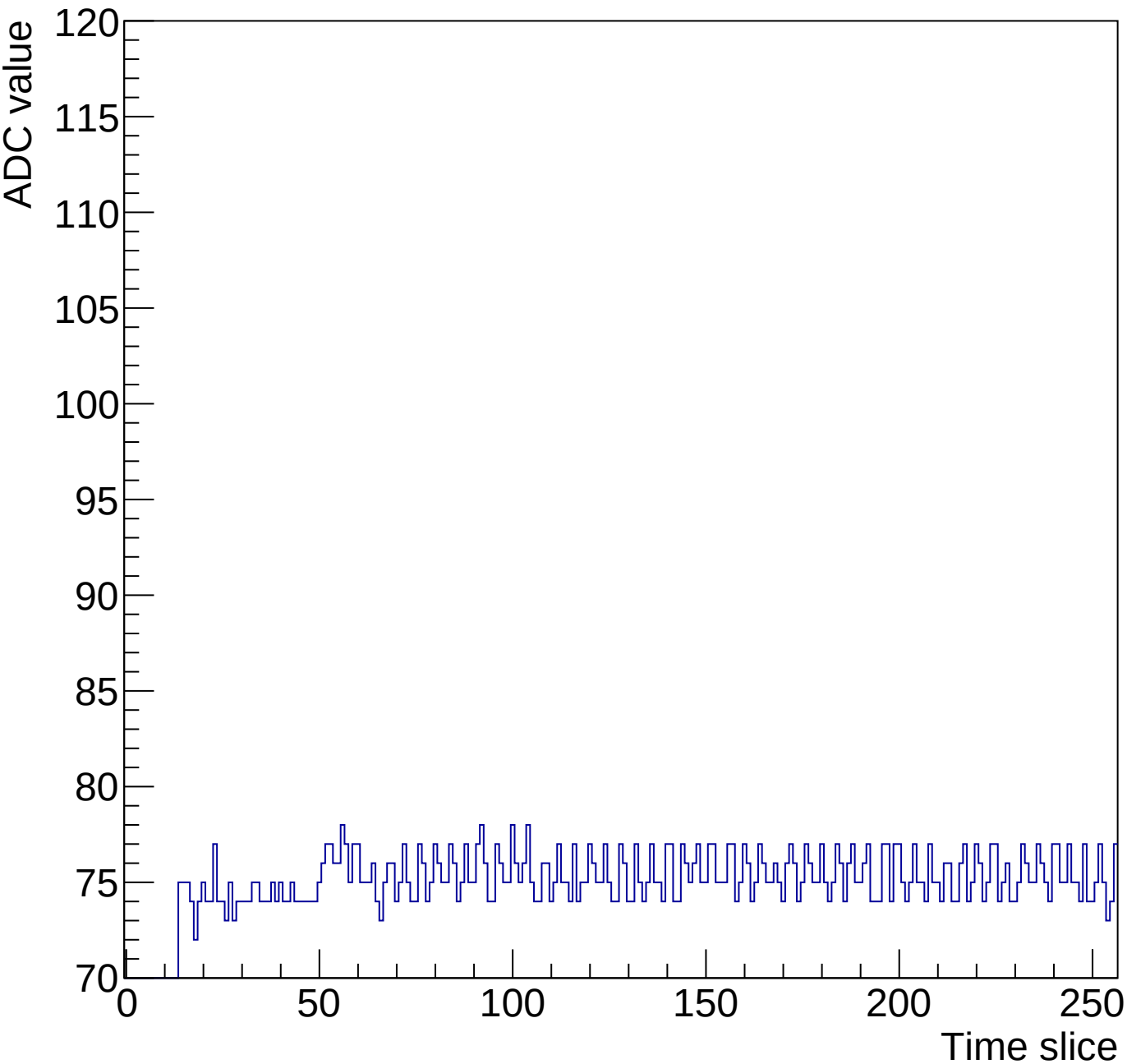
Run 2 event 100 mcm 1 chip 0 channel 1 256-90ns



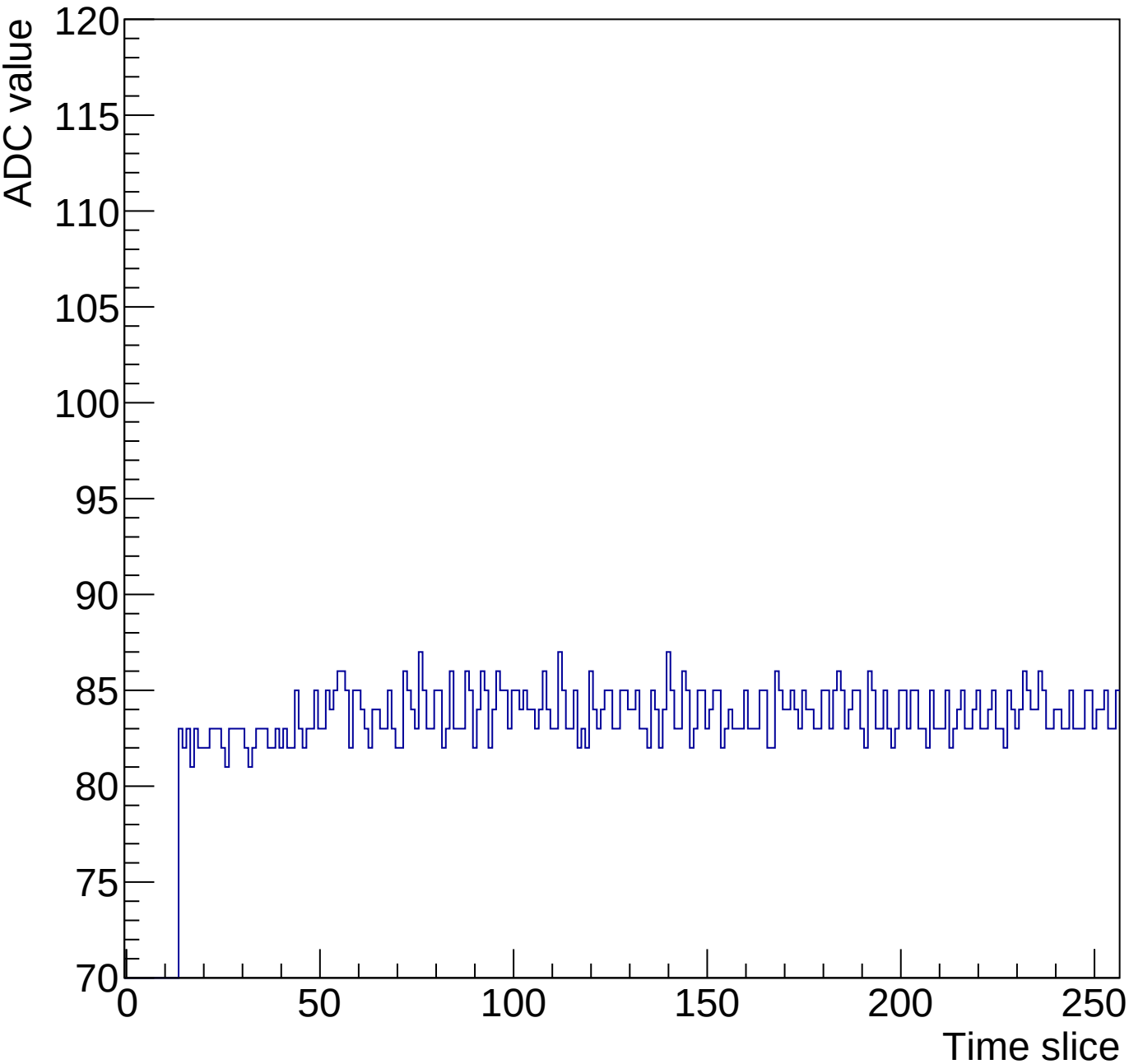
Run 2 event 100 mcm 1 chip 0 channel 2 256-90ns



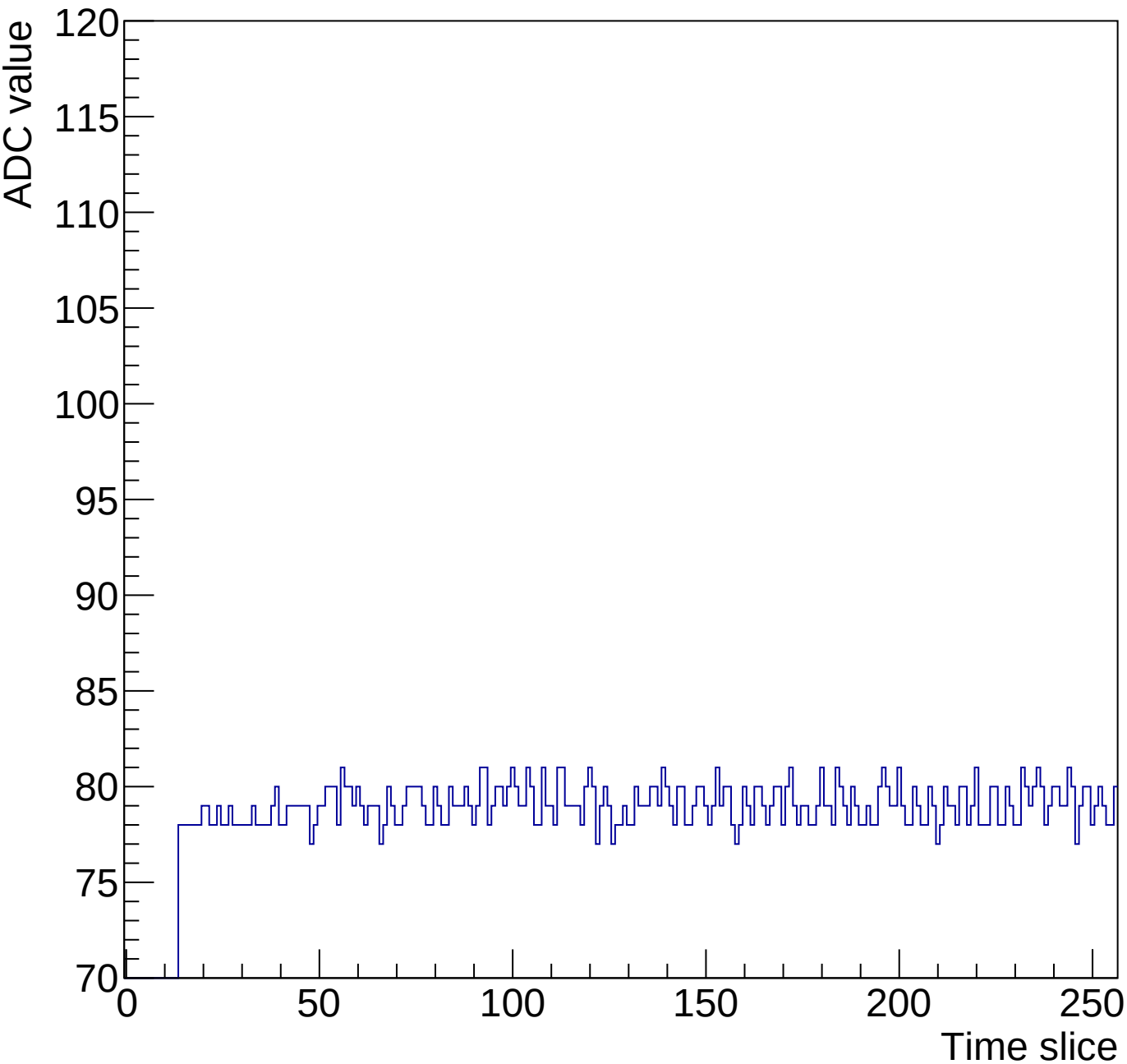
Run 2 event 100 mcm 1 chip 0 channel 3 256-90ns



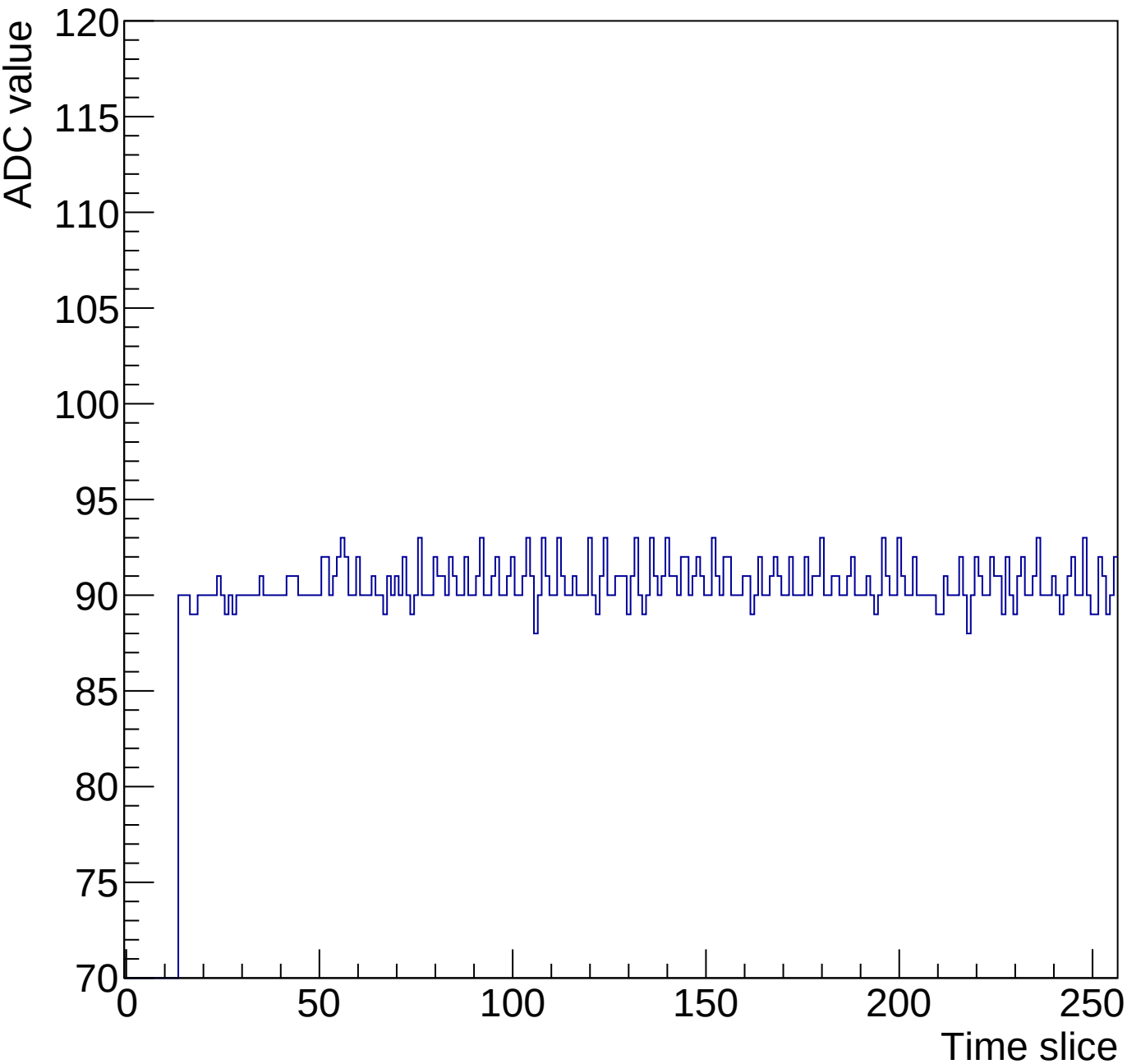
Run 2 event 100 mcm 1 chip 0 channel 4 256-90ns



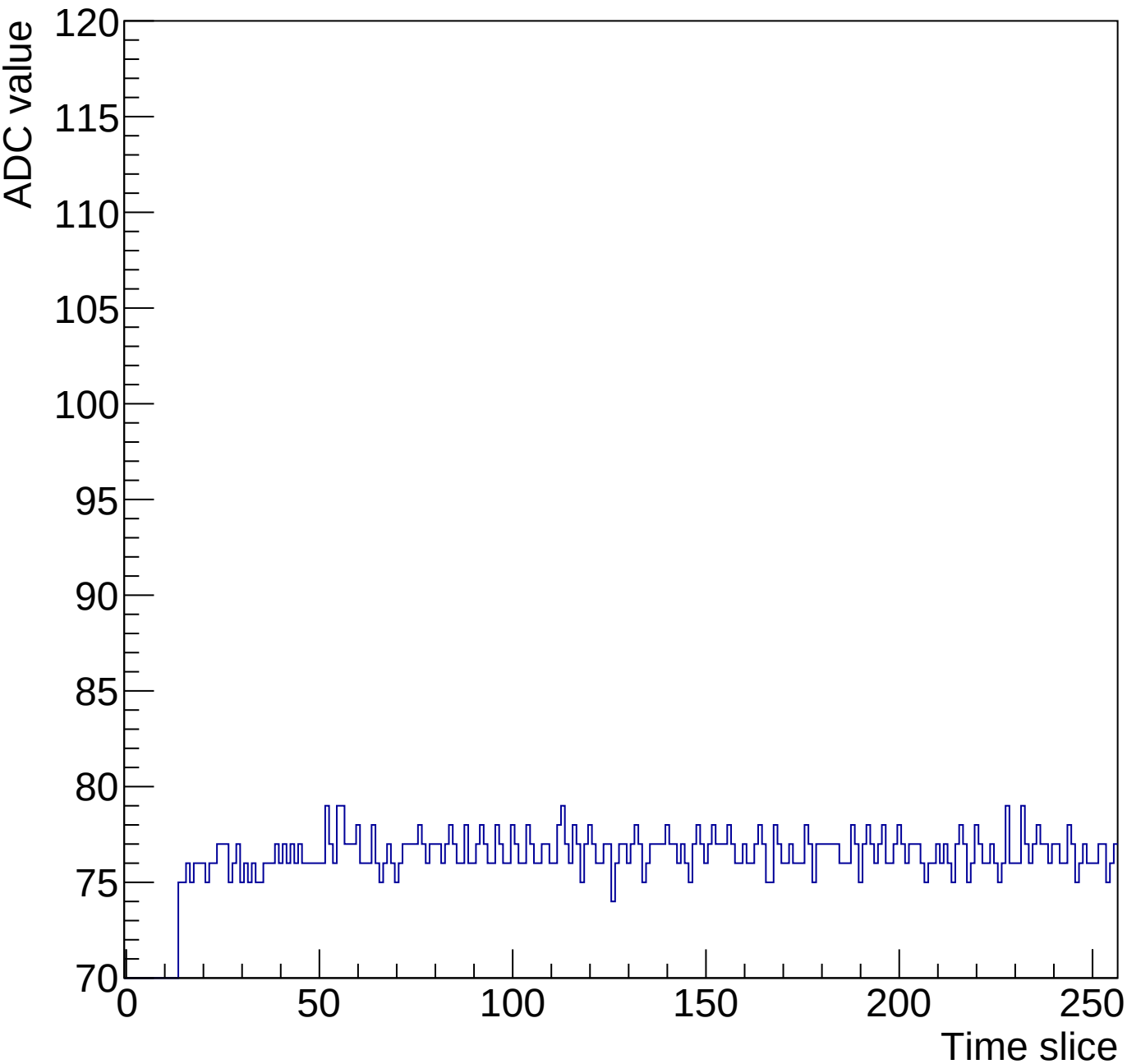
Run 2 event 100 mcm 1 chip 0 channel 5 256-90ns



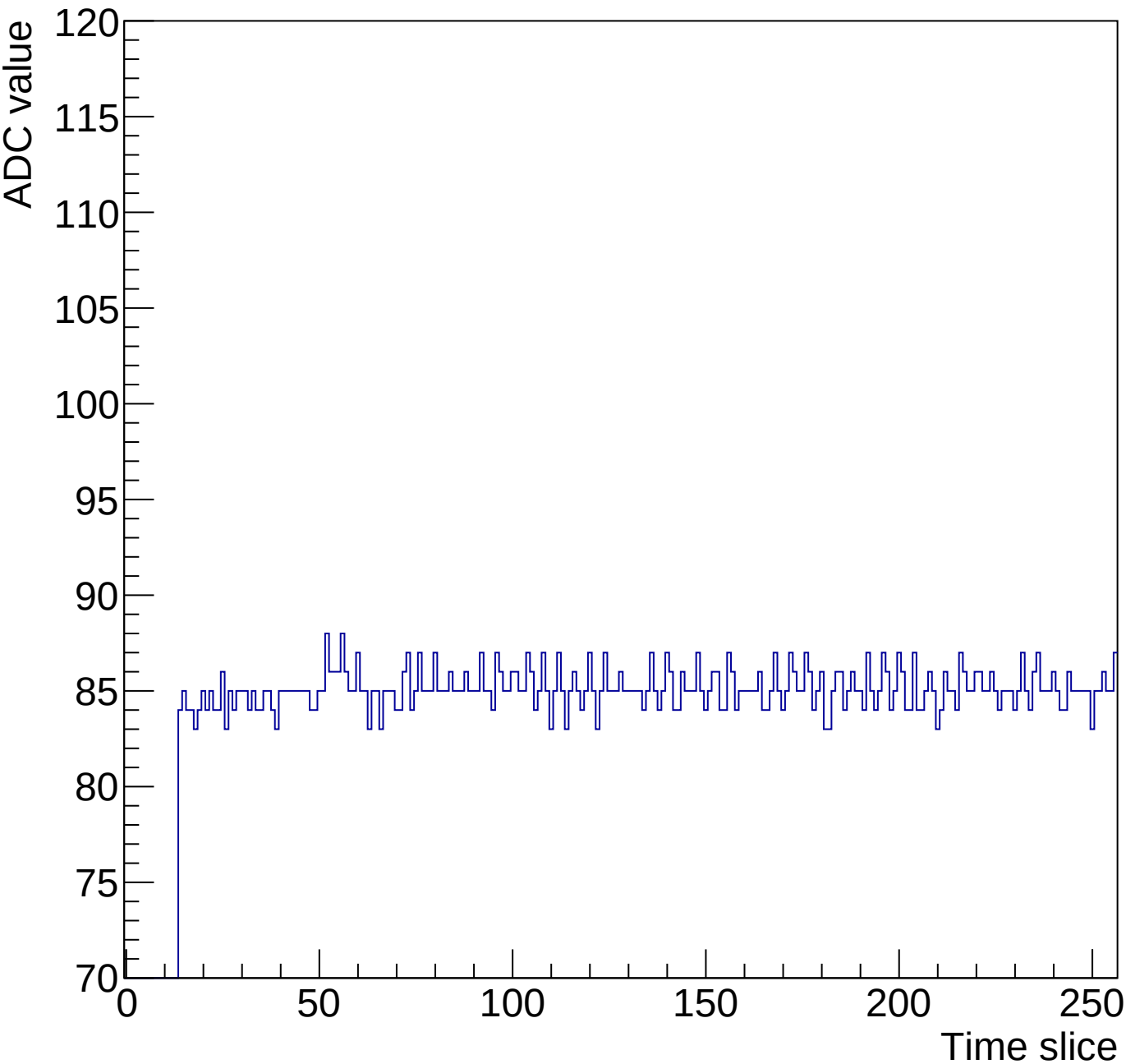
Run 2 event 100 mcm 1 chip 0 channel 6 256-90ns



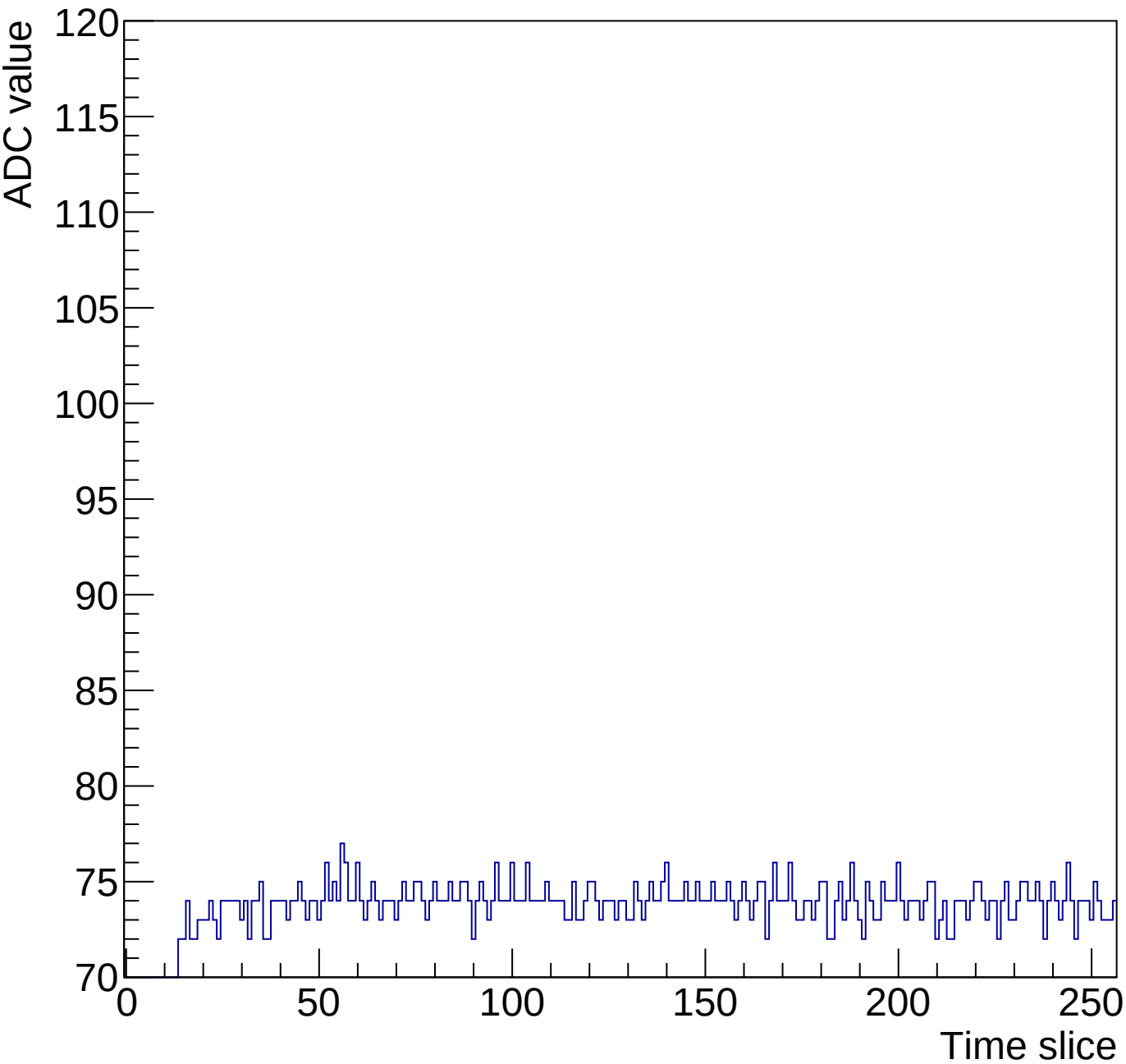
Run 2 event 100 mcm 1 chip 0 channel 7 256-90ns



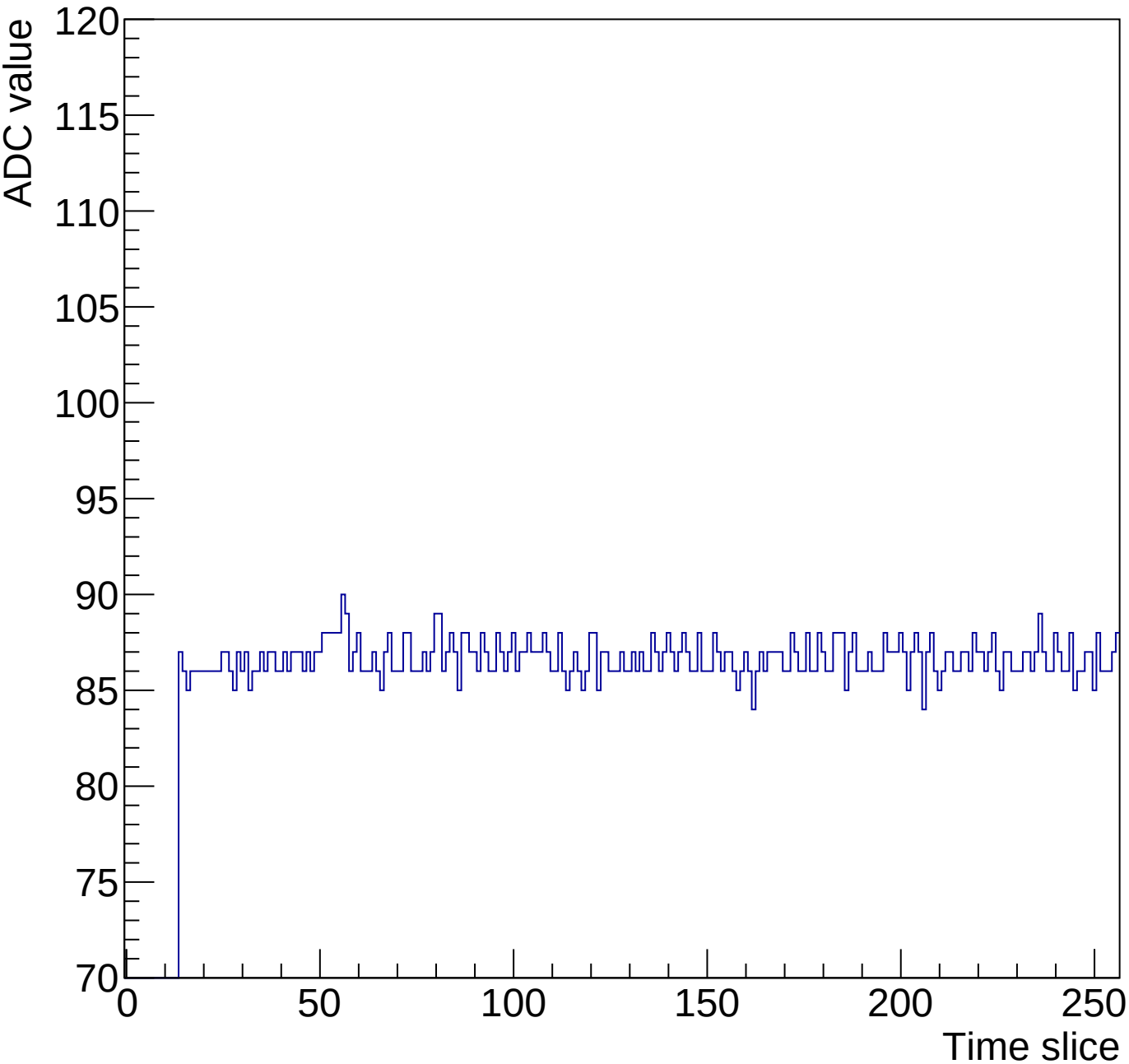
Run 2 event 100 mcm 1 chip 0 channel 8 256-90ns



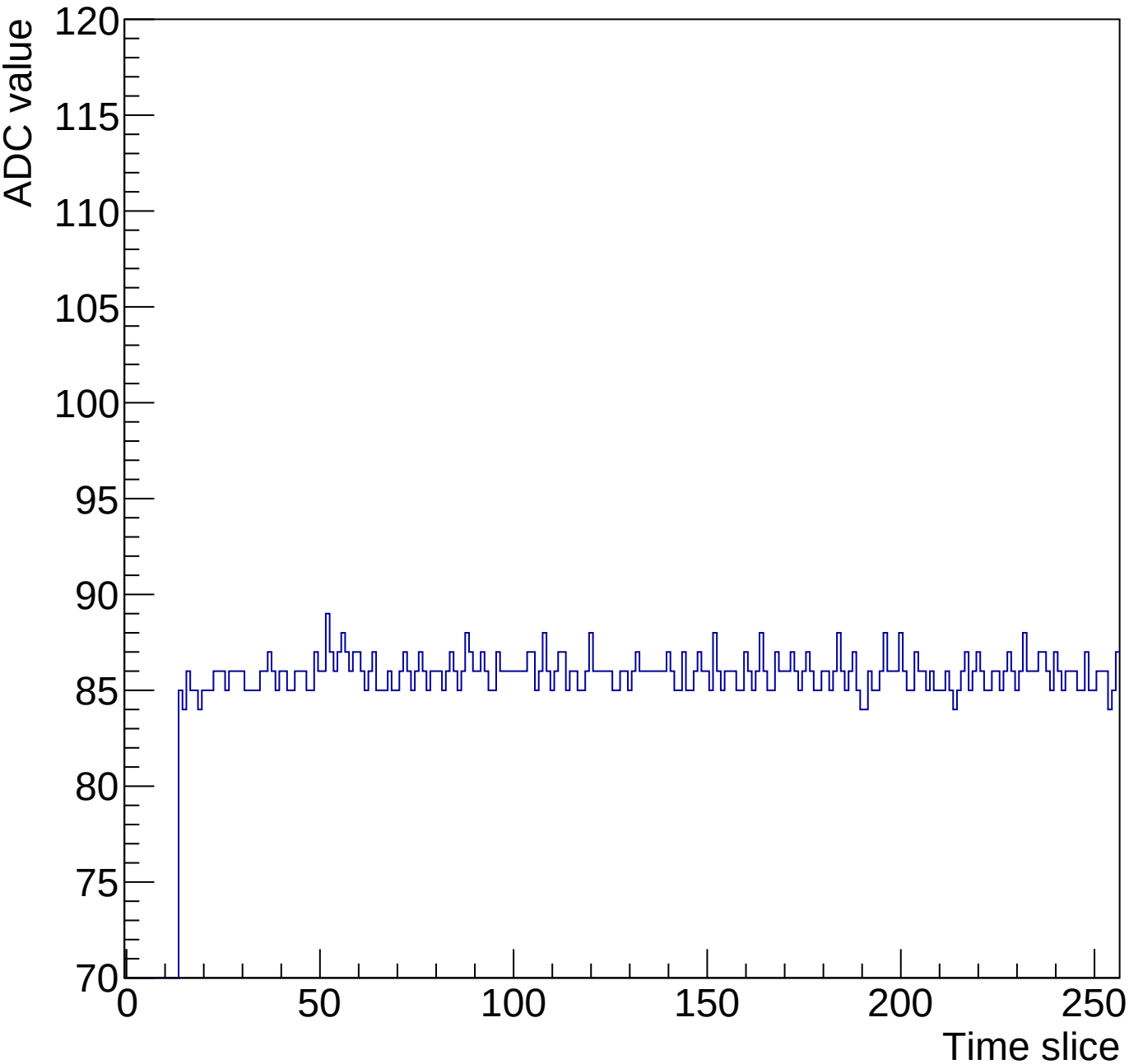
Run 2 event 100 mcm 1 chip 0 channel 9 256-90ns



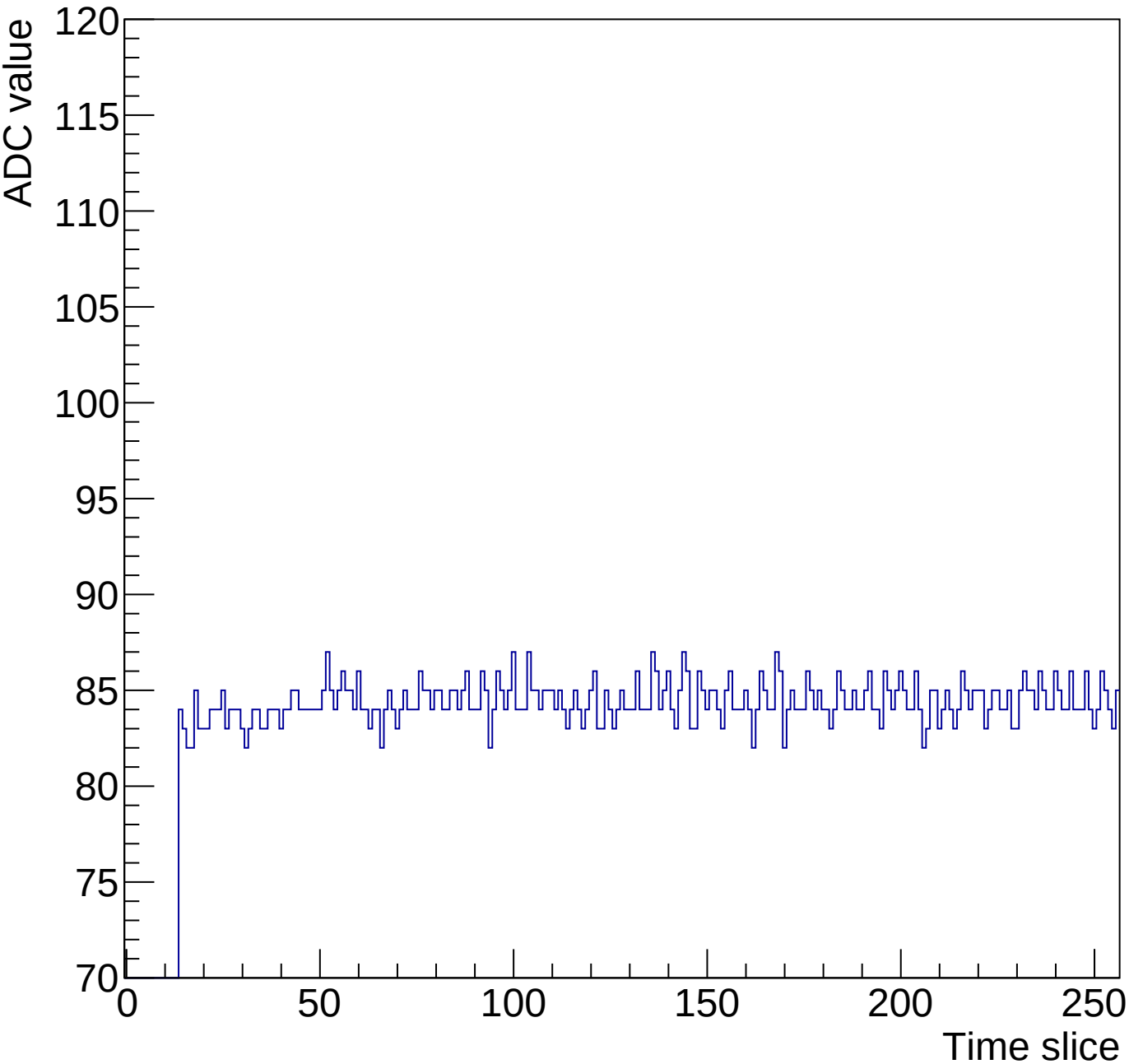
Run 2 event 100 mcm 1 chip 0 channel 10 256-90ns



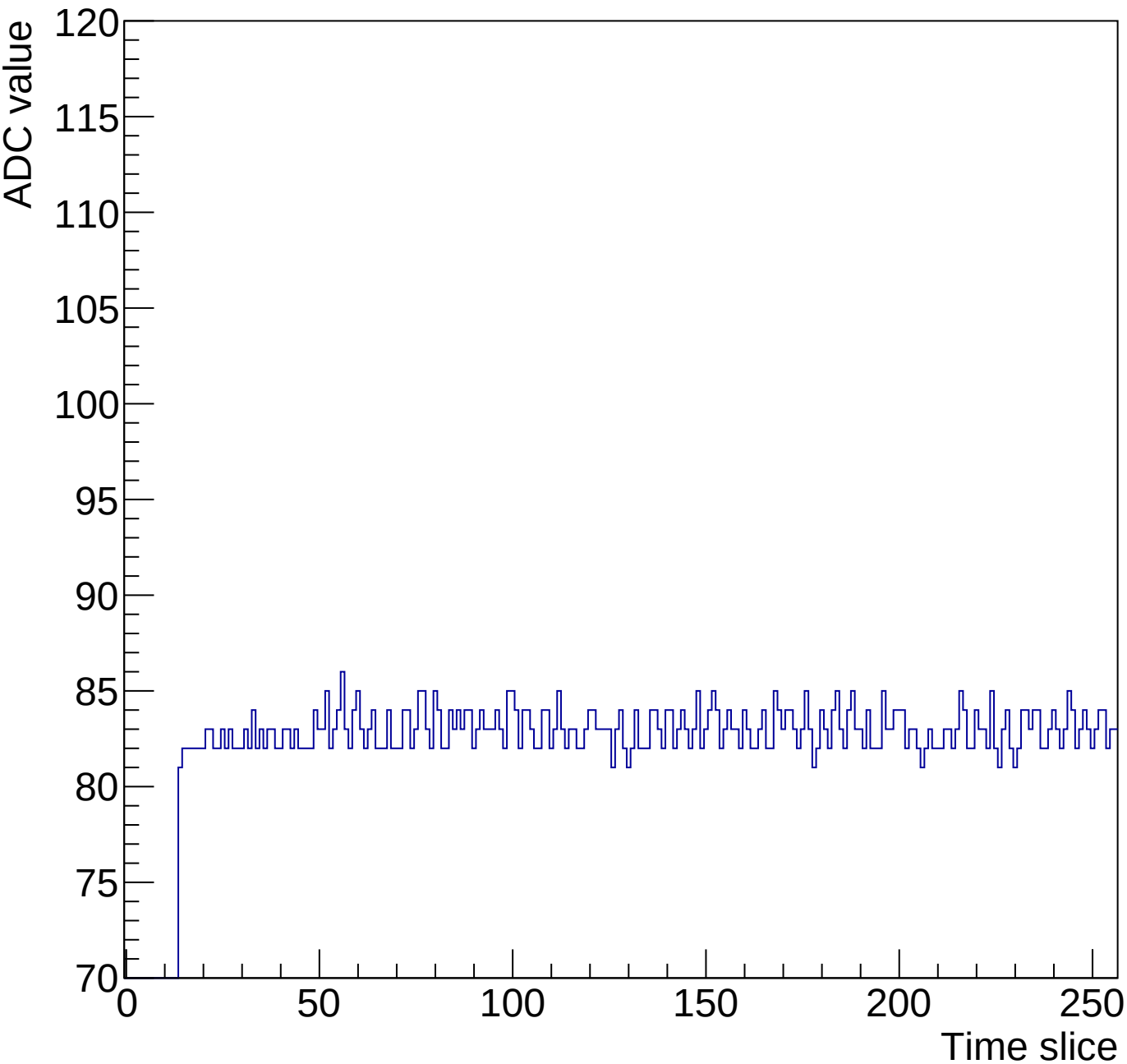
Run 2 event 100 mcm 1 chip 0 channel 11 256-90ns



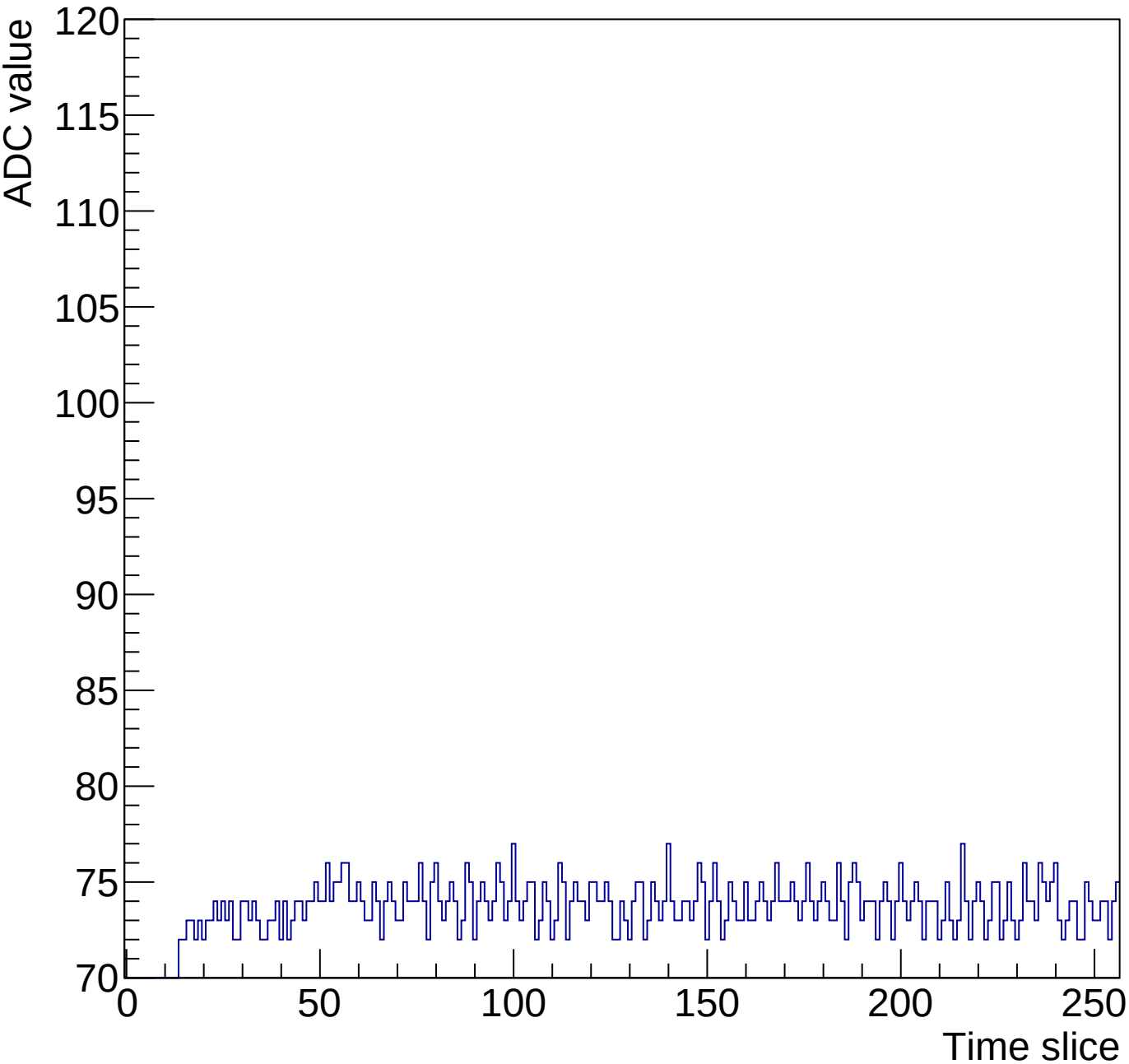
Run 2 event 100 mcm 1 chip 0 channel 12 256-90ns



Run 2 event 100 mcm 1 chip 0 channel 13 256-90ns



Run 2 event 100 mcm 1 chip 0 channel 14 256-90ns



Run 2 event 100 mcm 1 chip 0 channel 15 256-90ns

