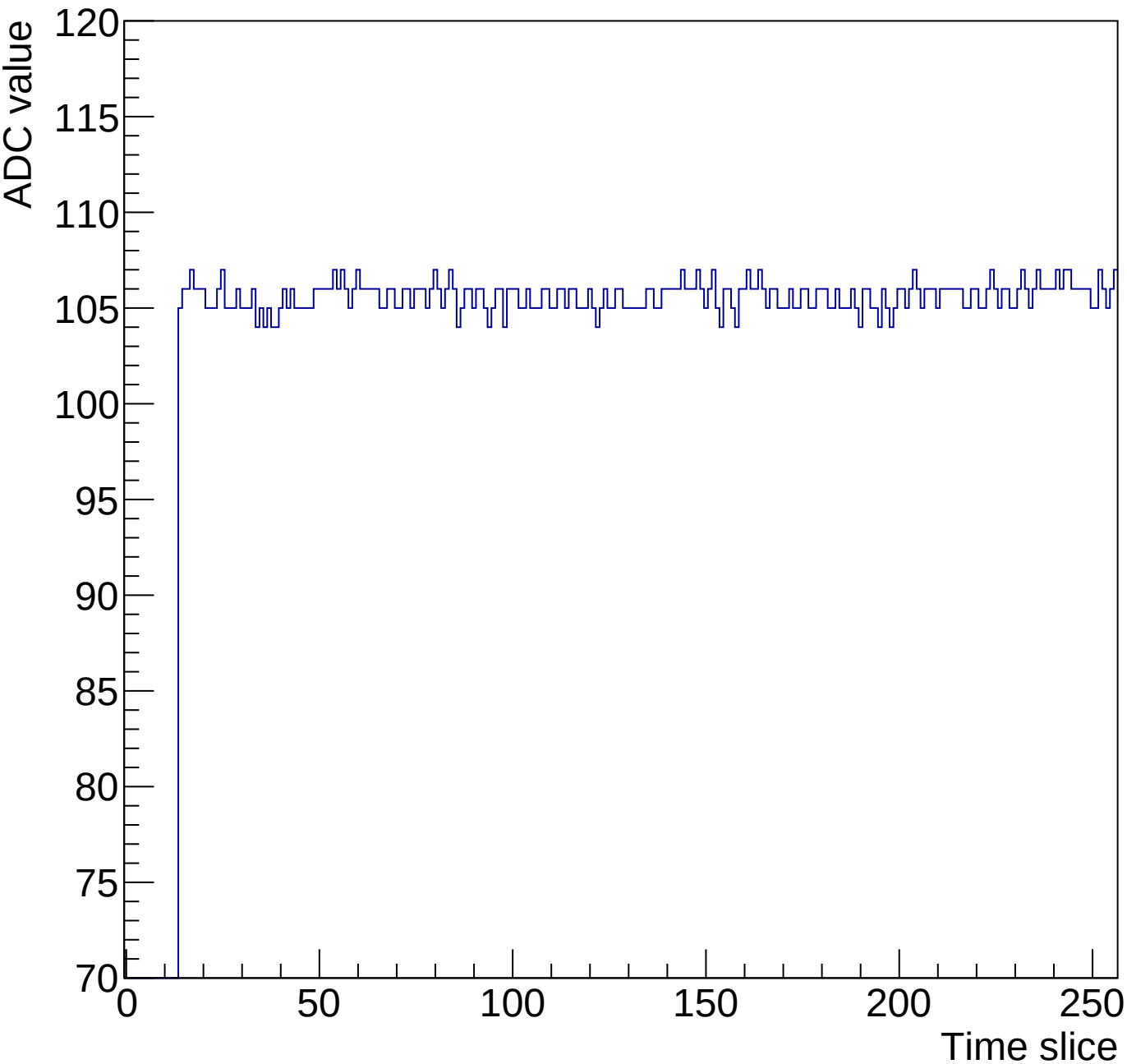
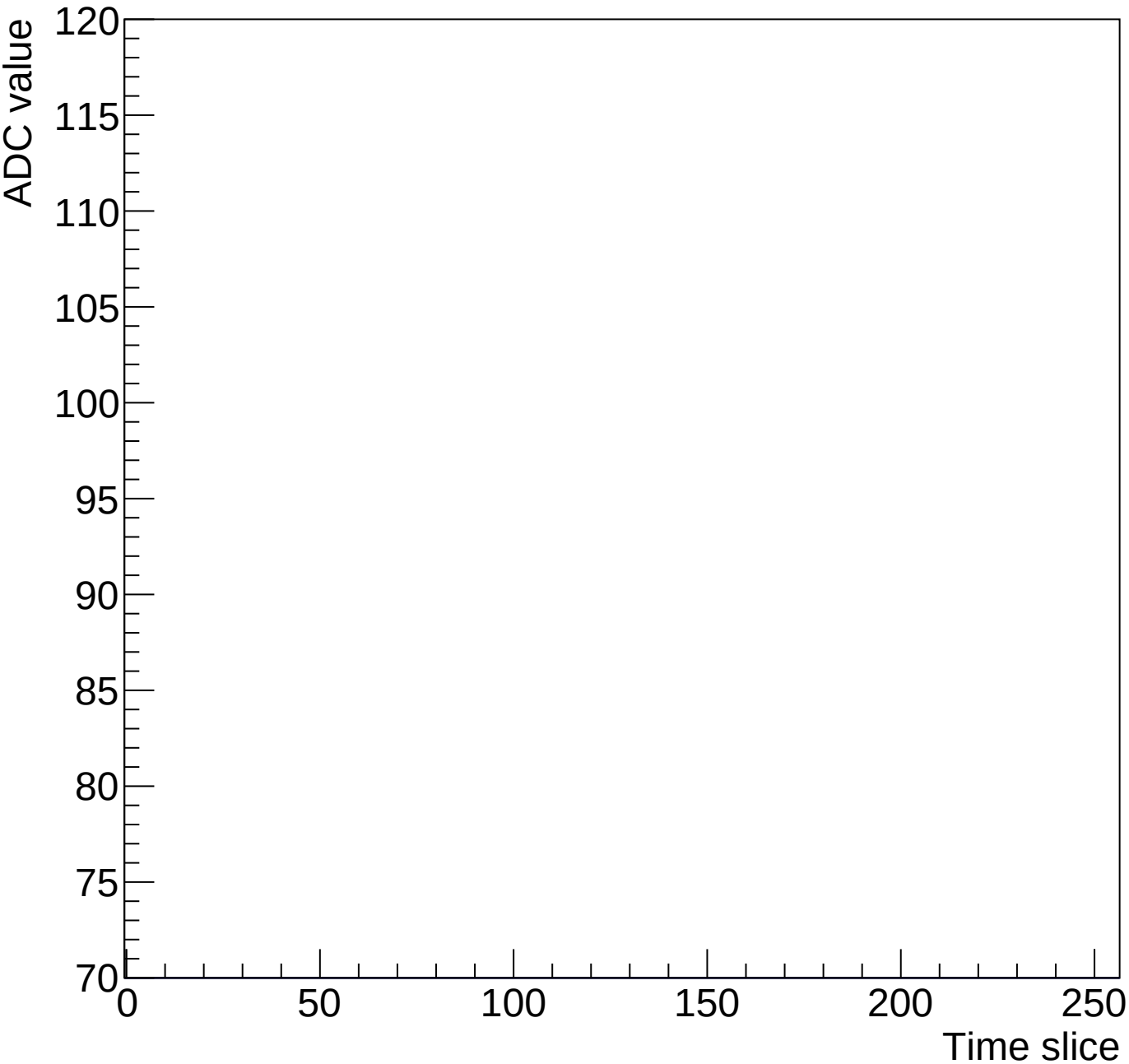


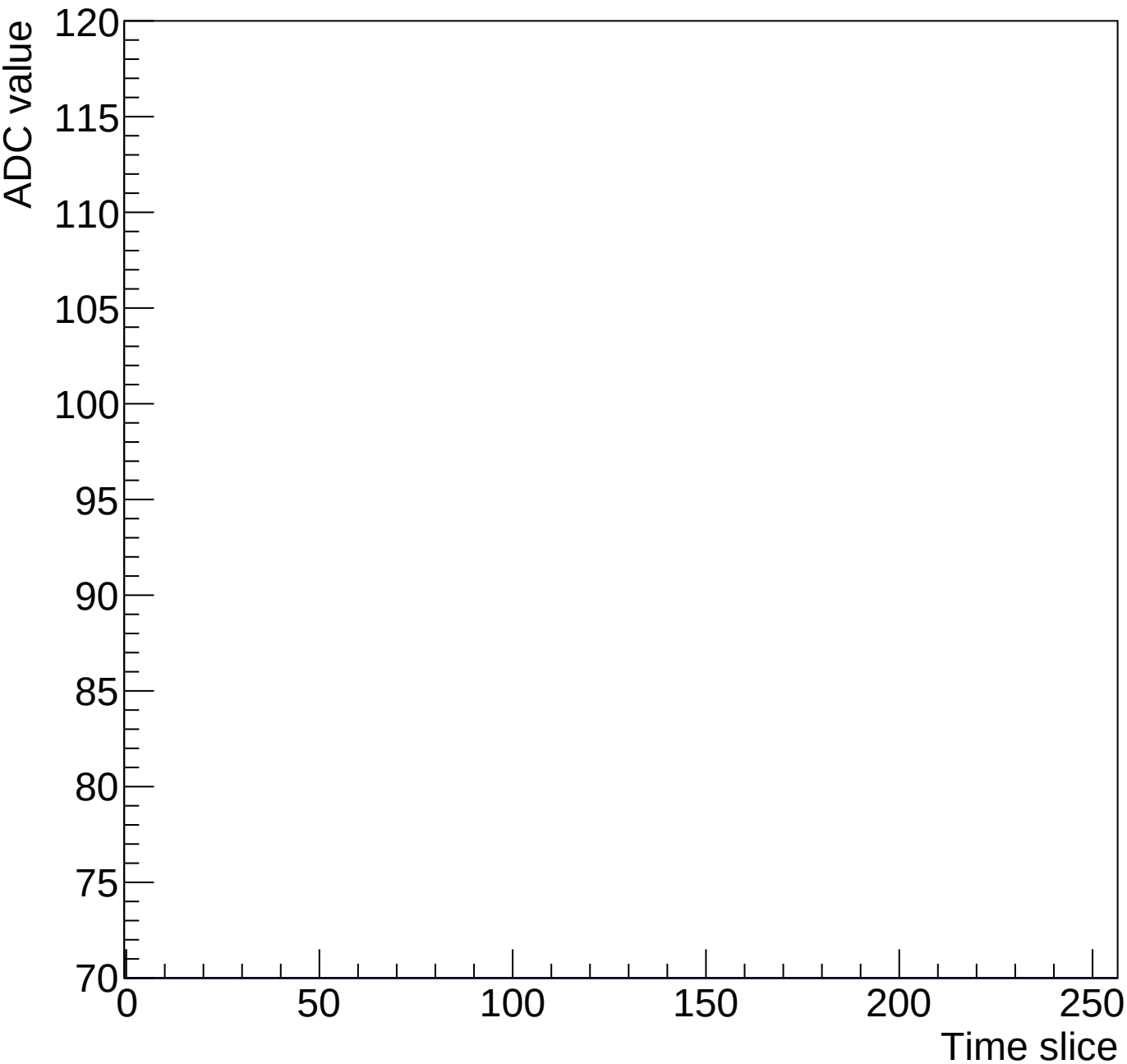
Run 2 event 100 mcm 2 chip 0 channel 0 256-60ns



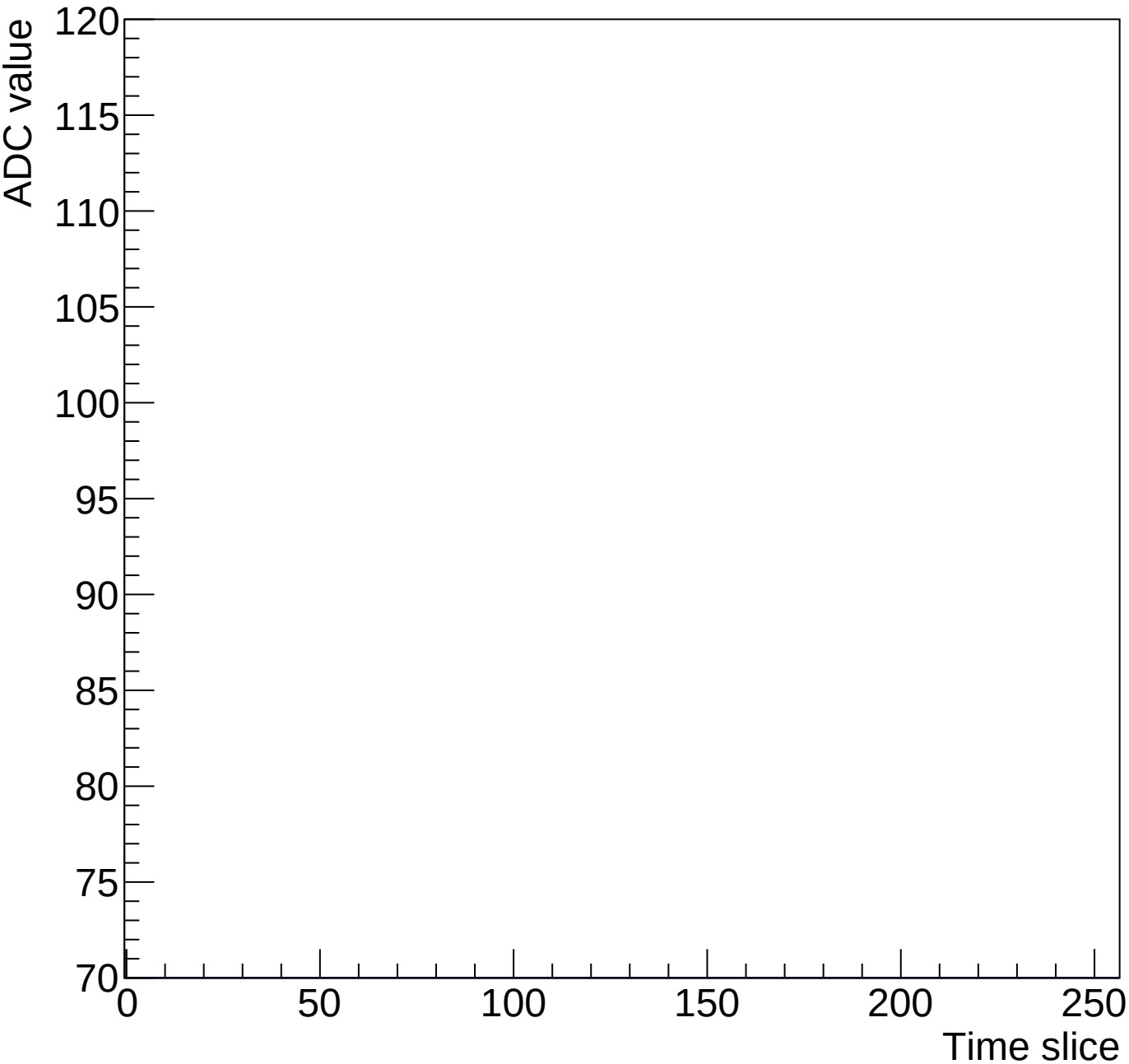
Run 2 event 100 mcm 2 chip 0 channel 1 256-60ns



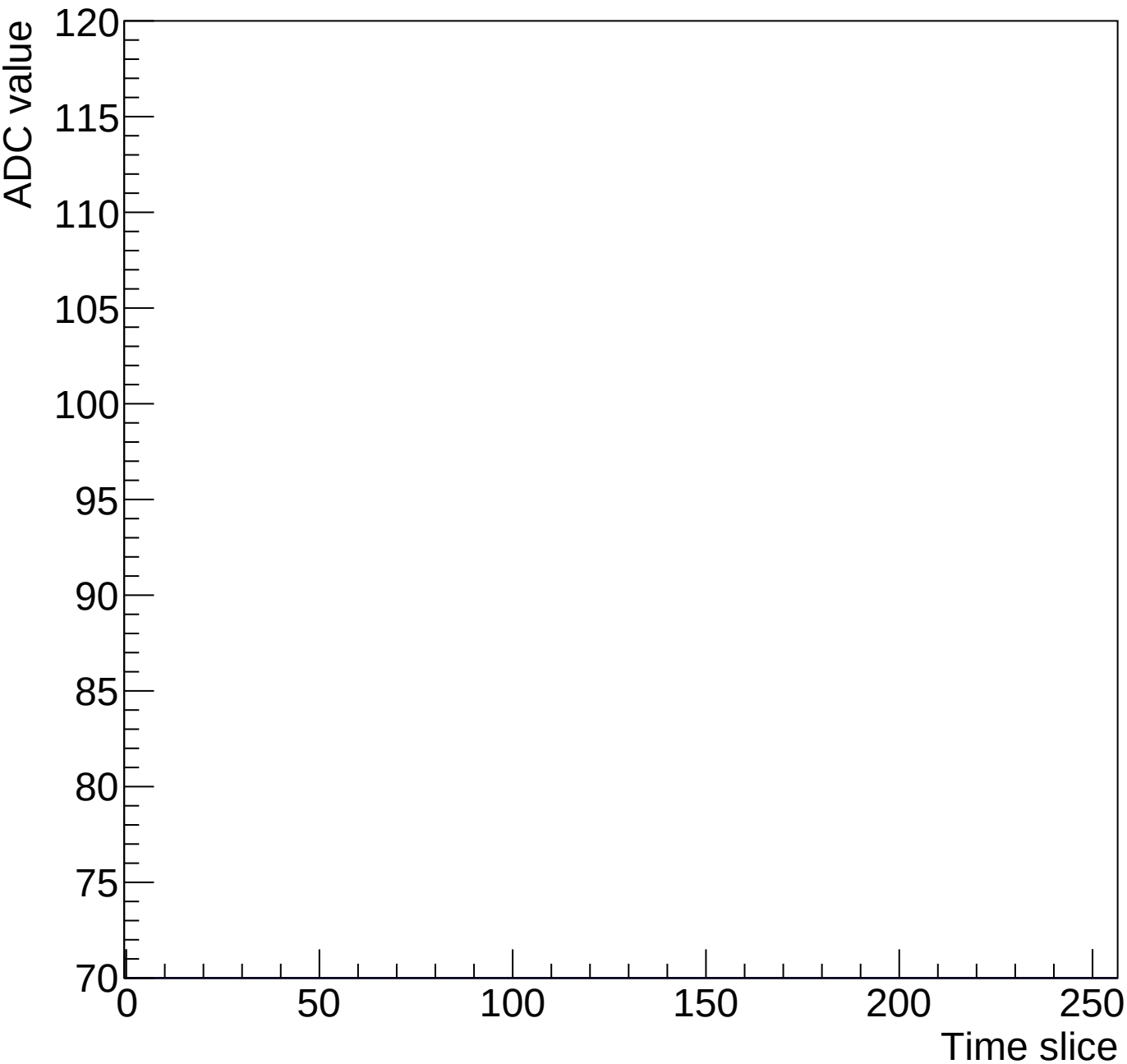
Run 2 event 100 mcm 2 chip 0 channel 2 256-60ns



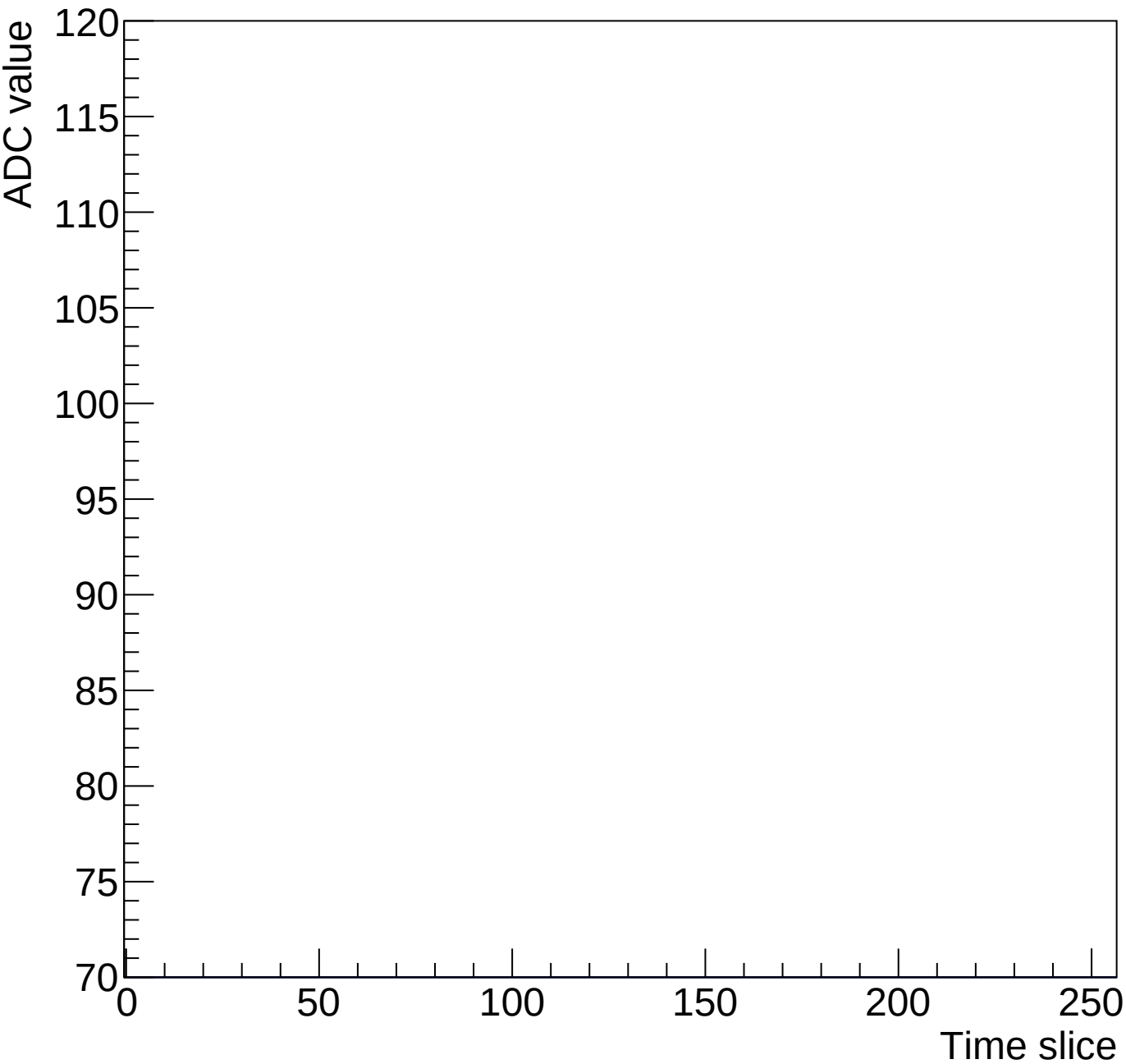
Run 2 event 100 mcm 2 chip 0 channel 3 256-60ns



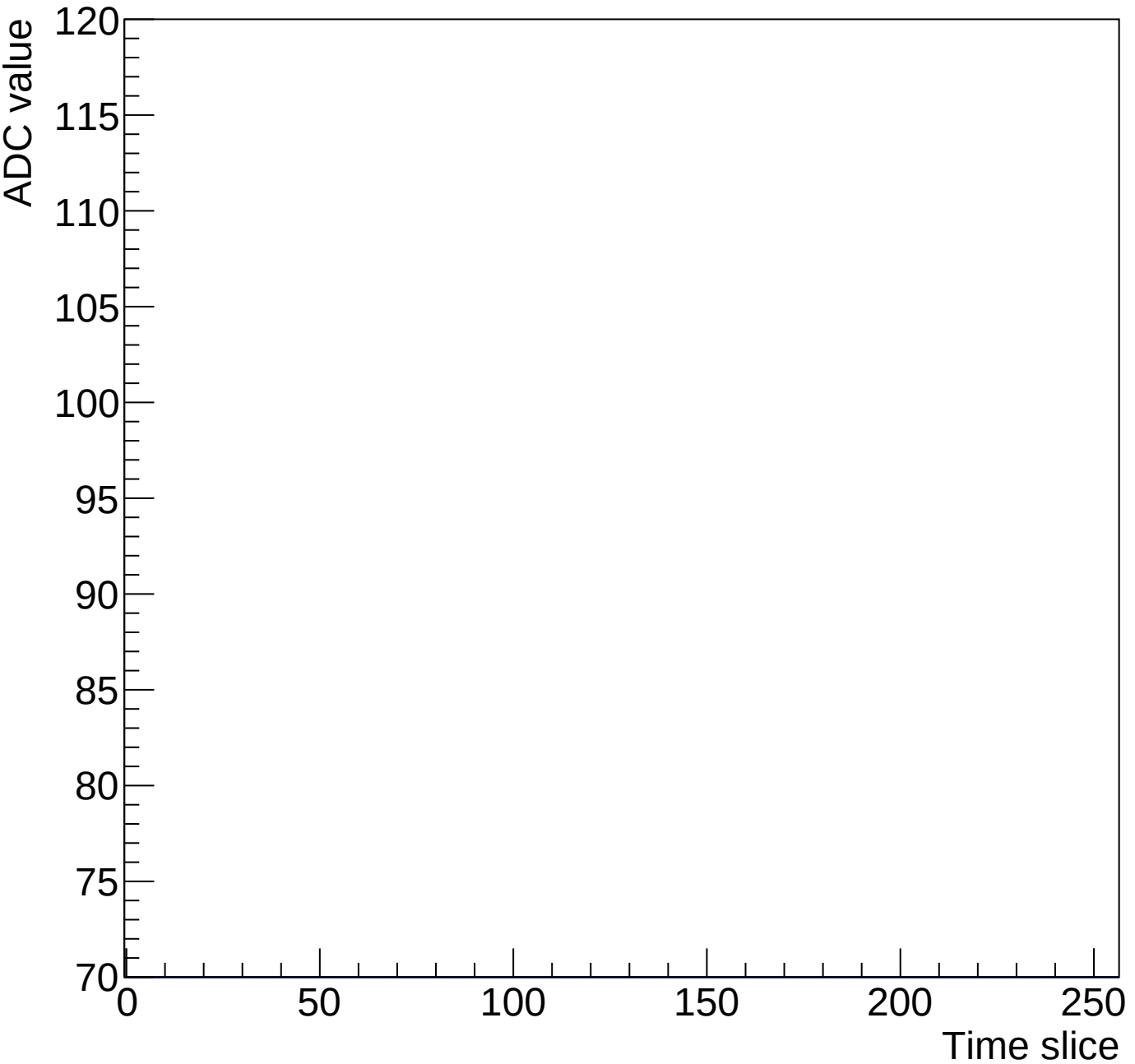
Run 2 event 100 mcm 2 chip 0 channel 4 256-60ns



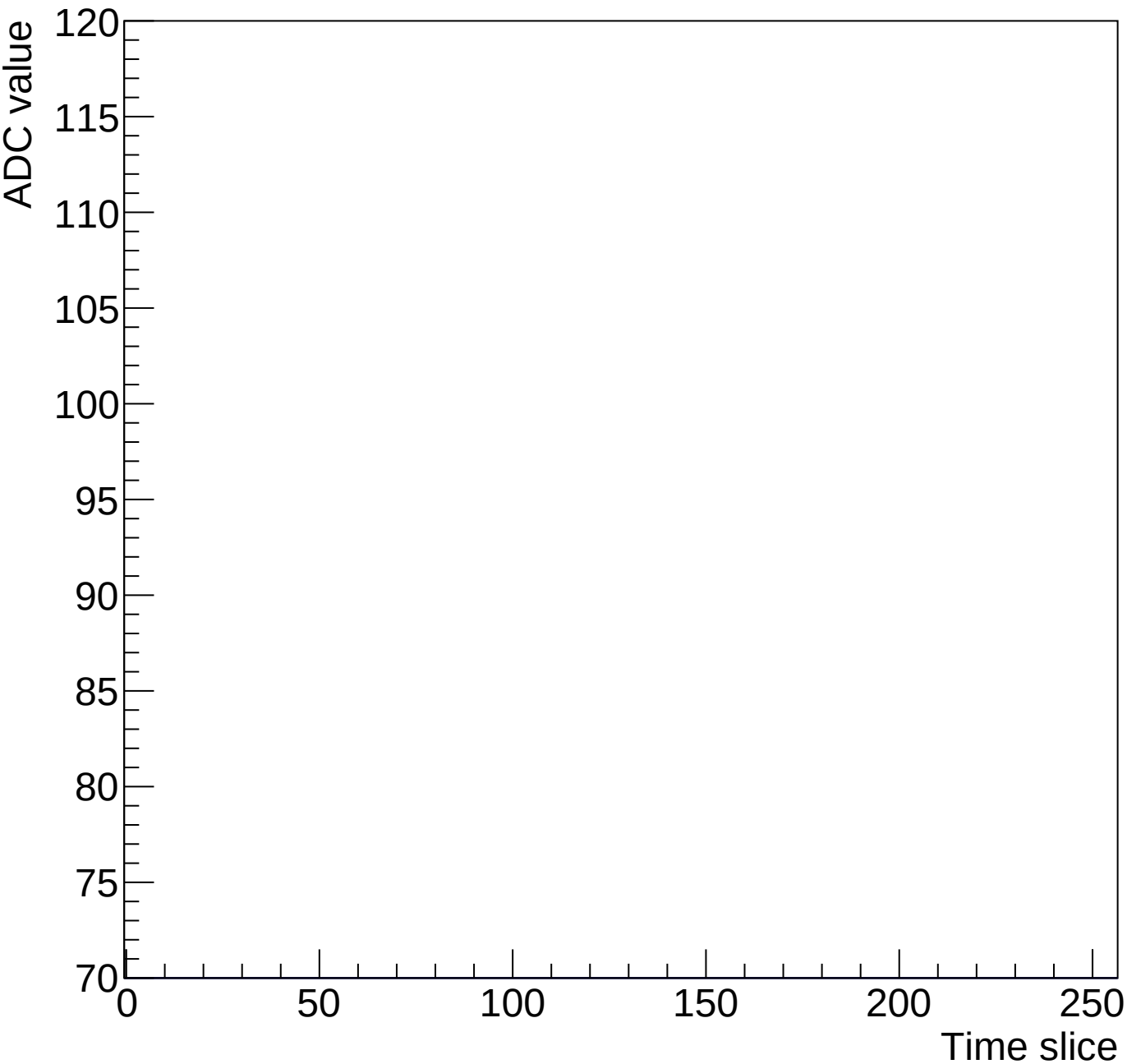
Run 2 event 100 mcm 2 chip 0 channel 5 256-60ns



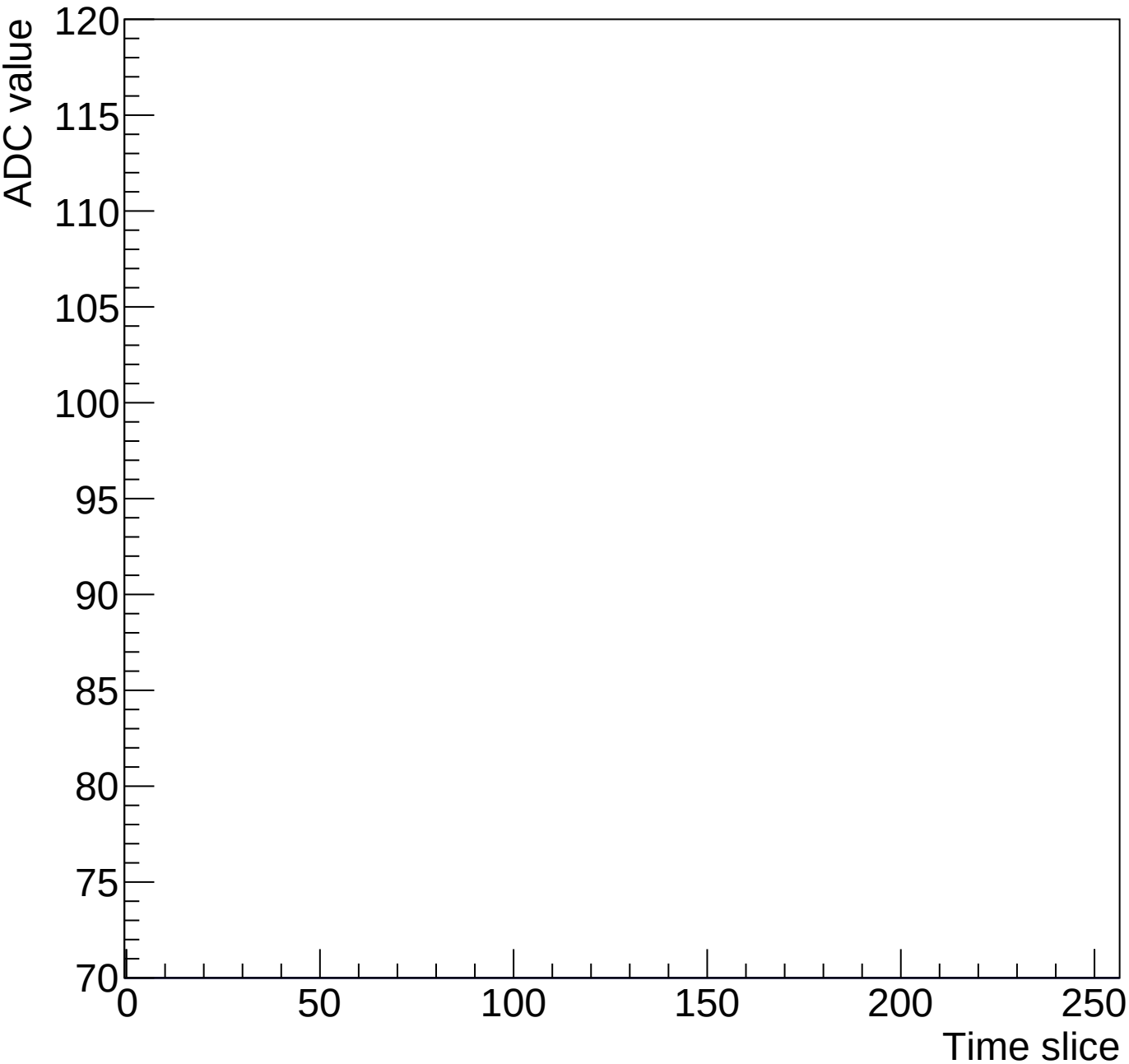
Run 2 event 100 mcm 2 chip 0 channel 6 256-60ns



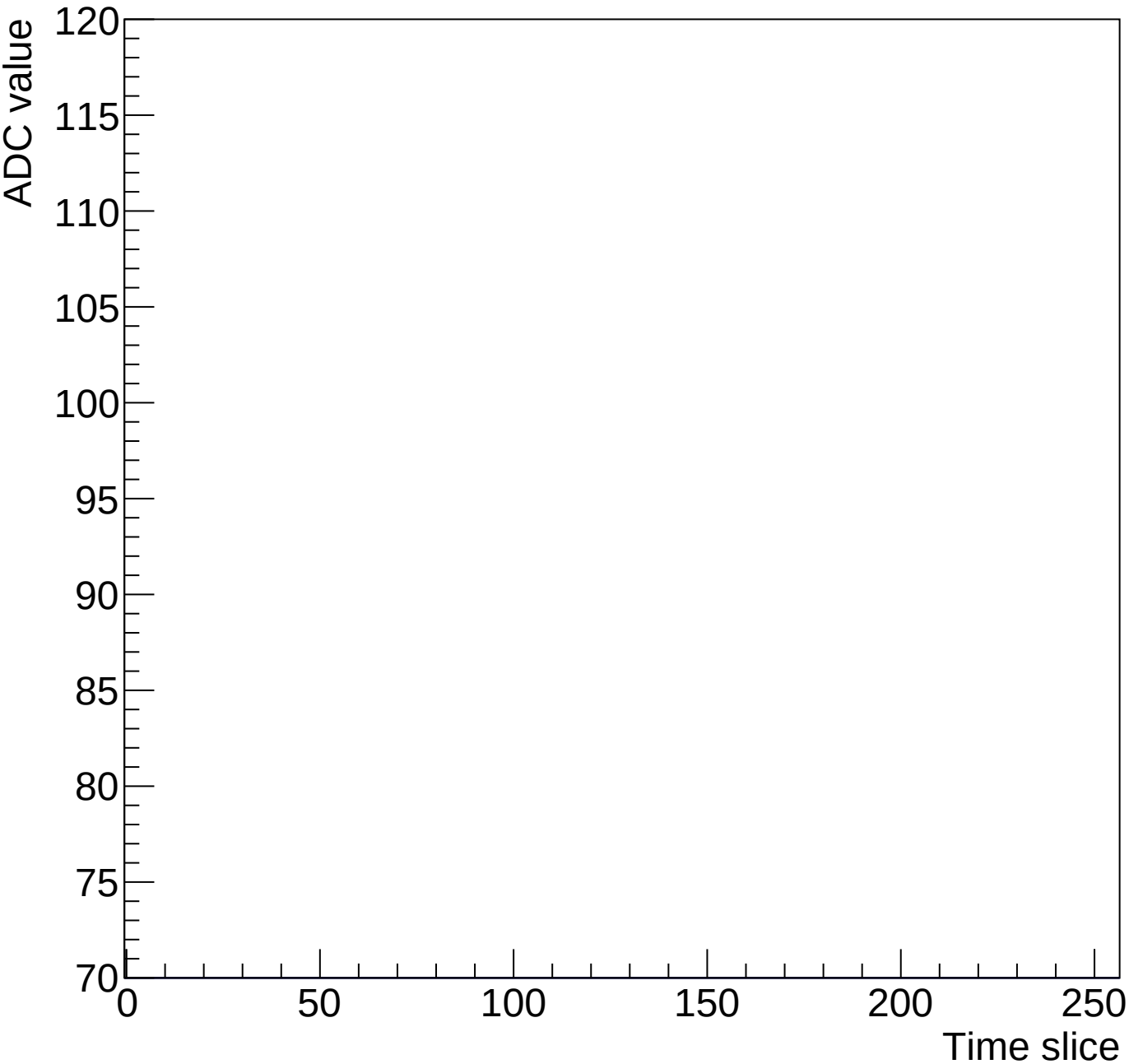
Run 2 event 100 mcm 2 chip 0 channel 7 256-60ns



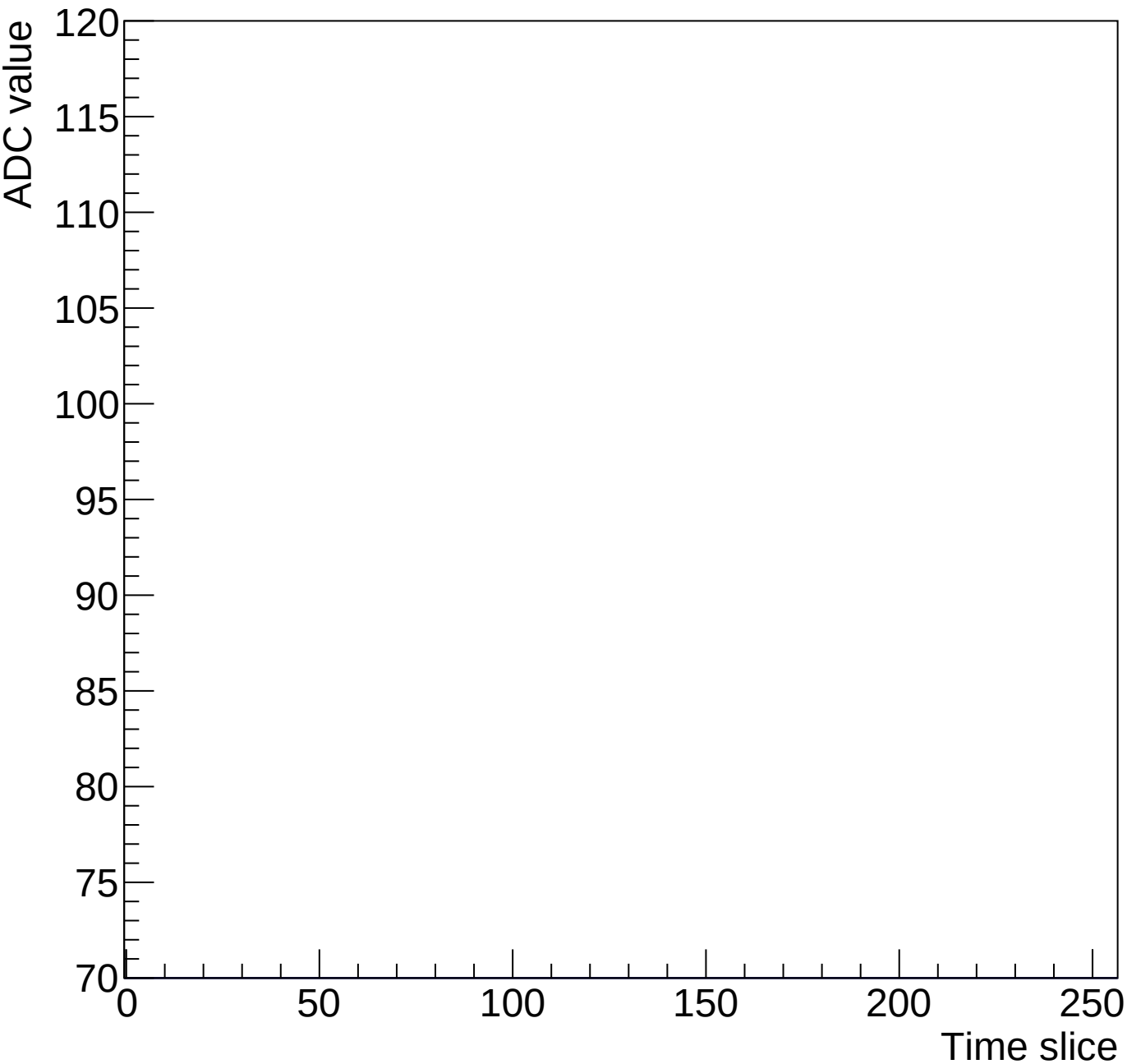
Run 2 event 100 mcm 2 chip 0 channel 8 256-60ns



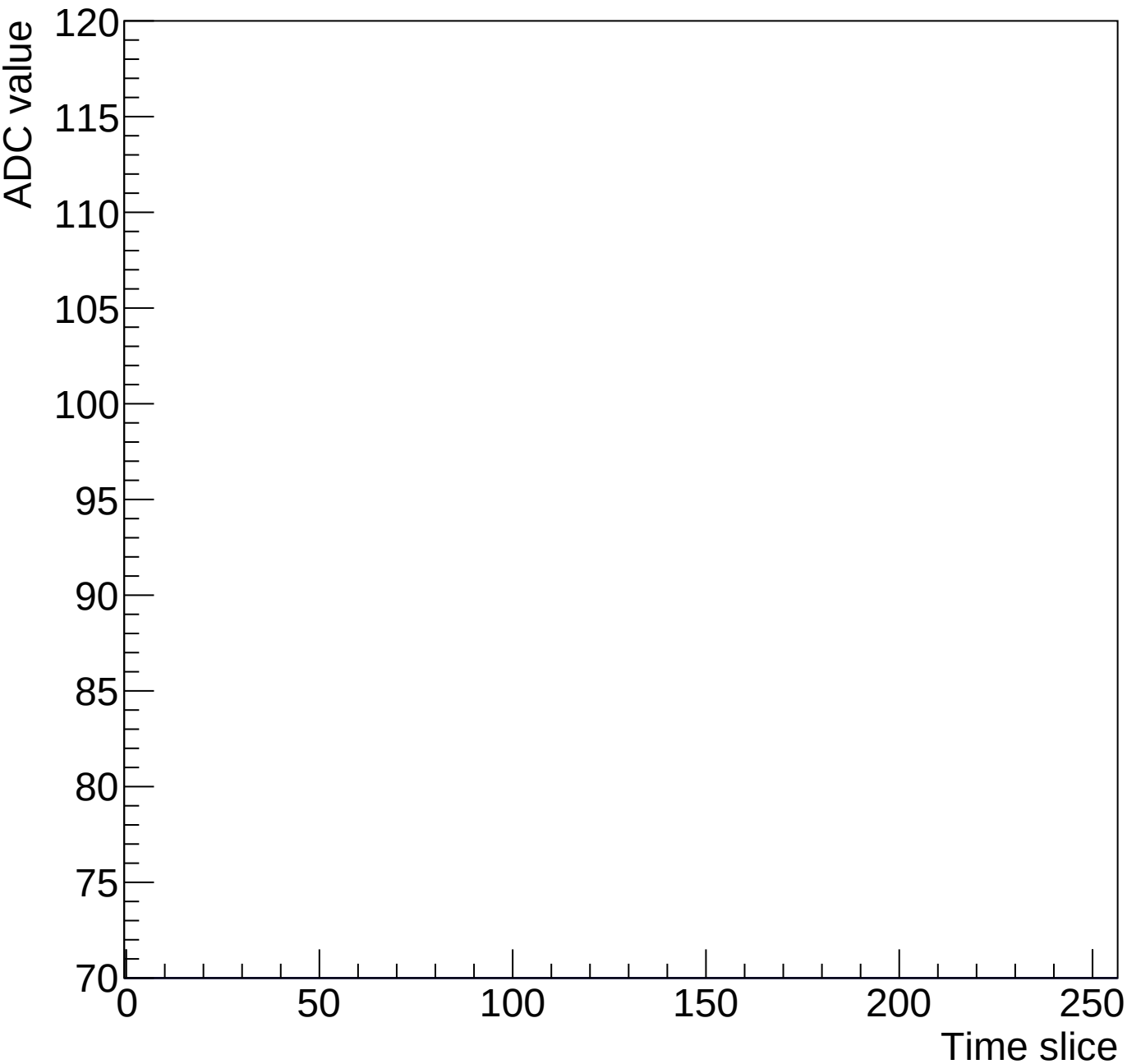
Run 2 event 100 mcm 2 chip 0 channel 9 256-60ns



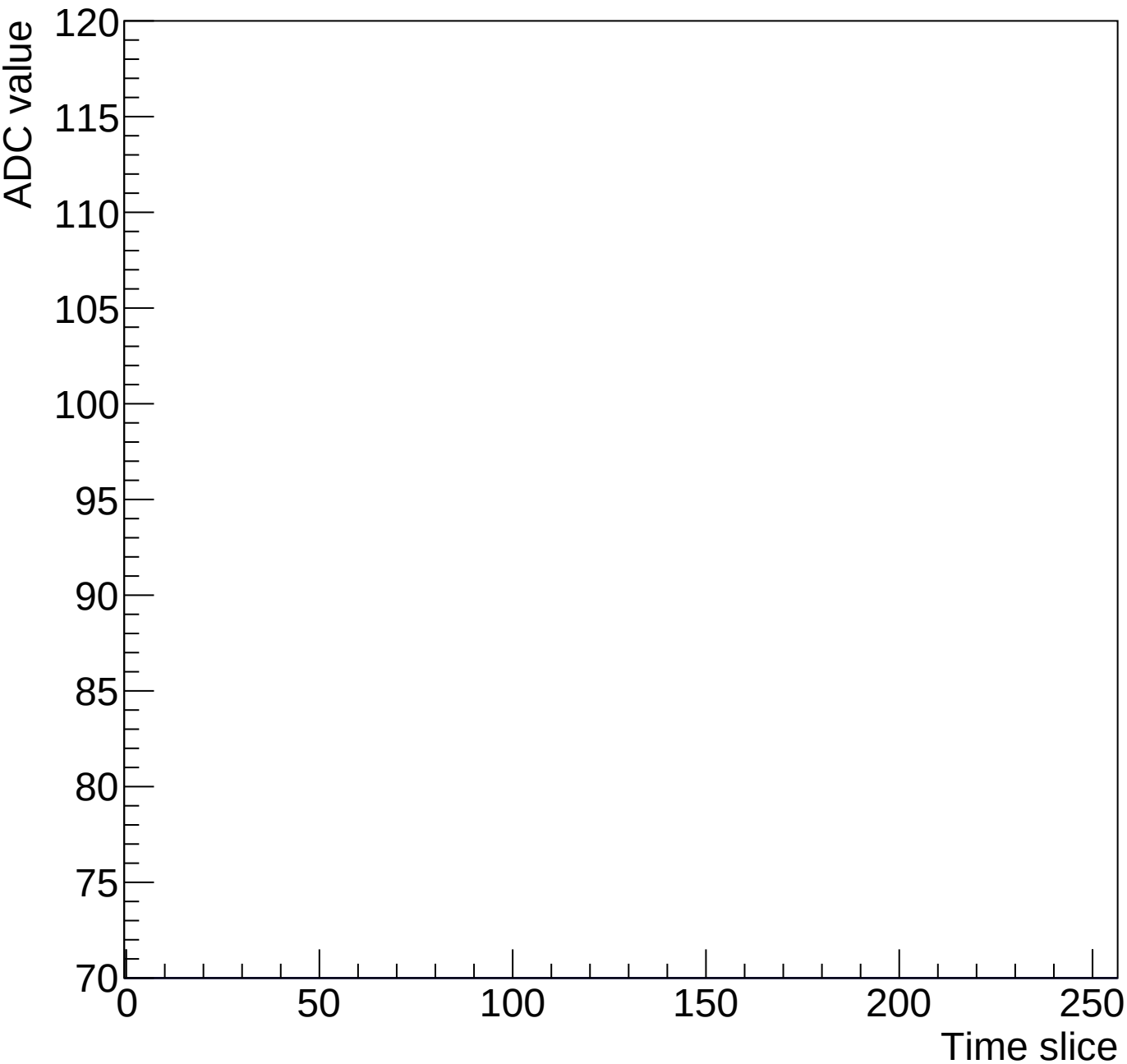
Run 2 event 100 mcm 2 chip 0 channel 10 256-60ns



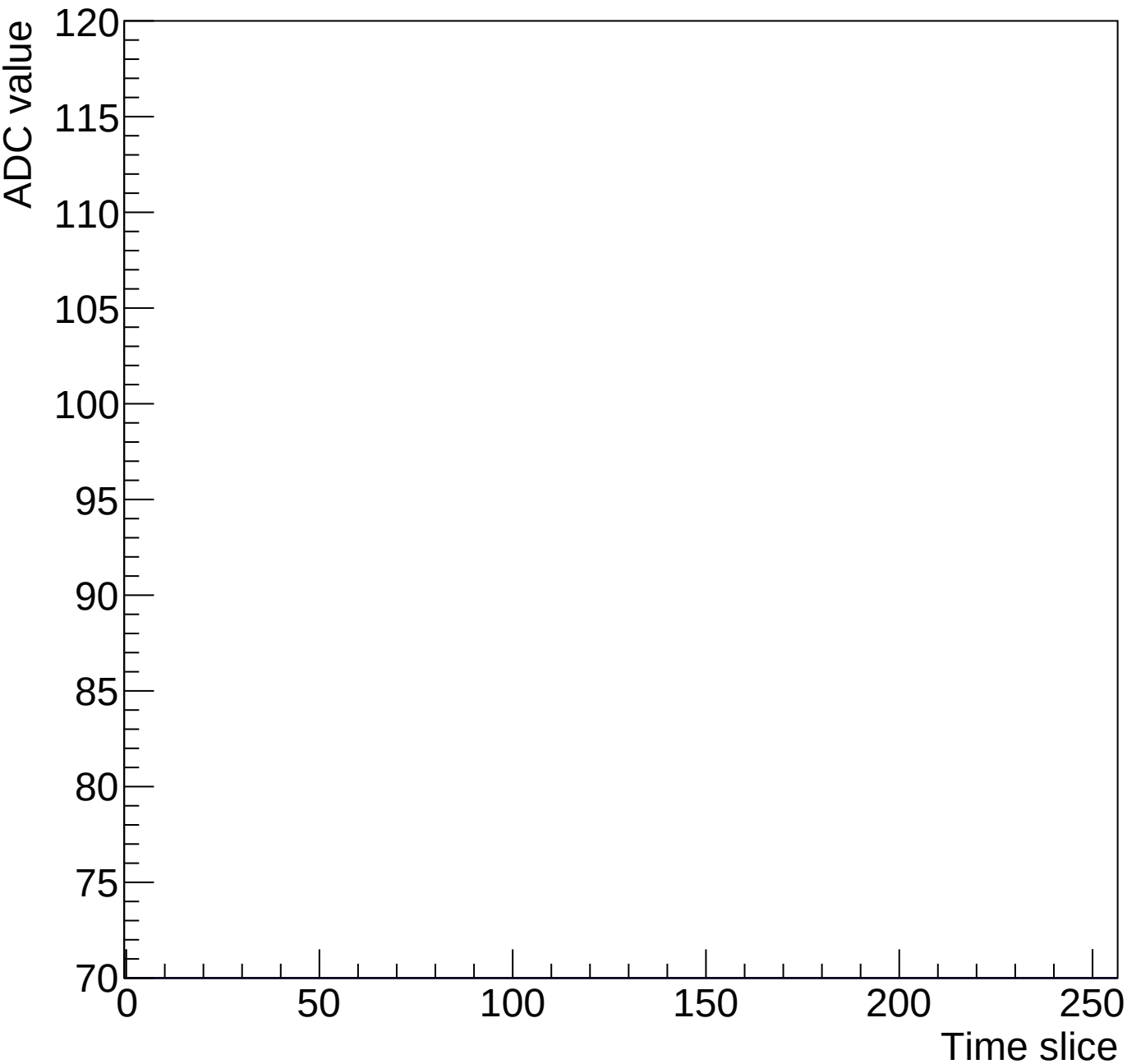
Run 2 event 100 mcm 2 chip 0 channel 11 256-60ns



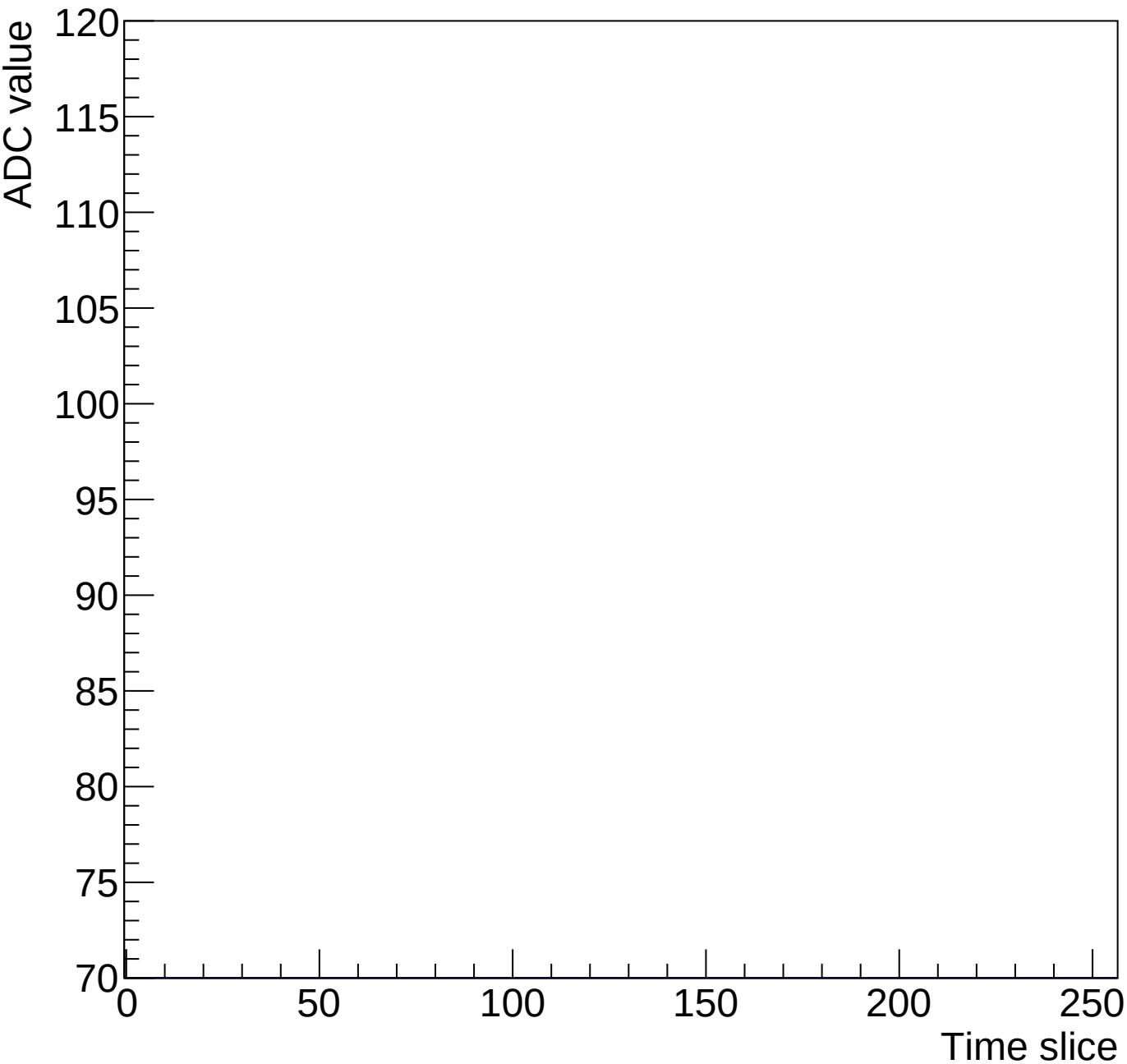
Run 2 event 100 mcm 2 chip 0 channel 12 256-60ns



Run 2 event 100 mcm 2 chip 0 channel 13 256-60ns



Run 2 event 100 mcm 2 chip 0 channel 14 256-60ns



Run 2 event 100 mcm 2 chip 0 channel 15 256-60ns

