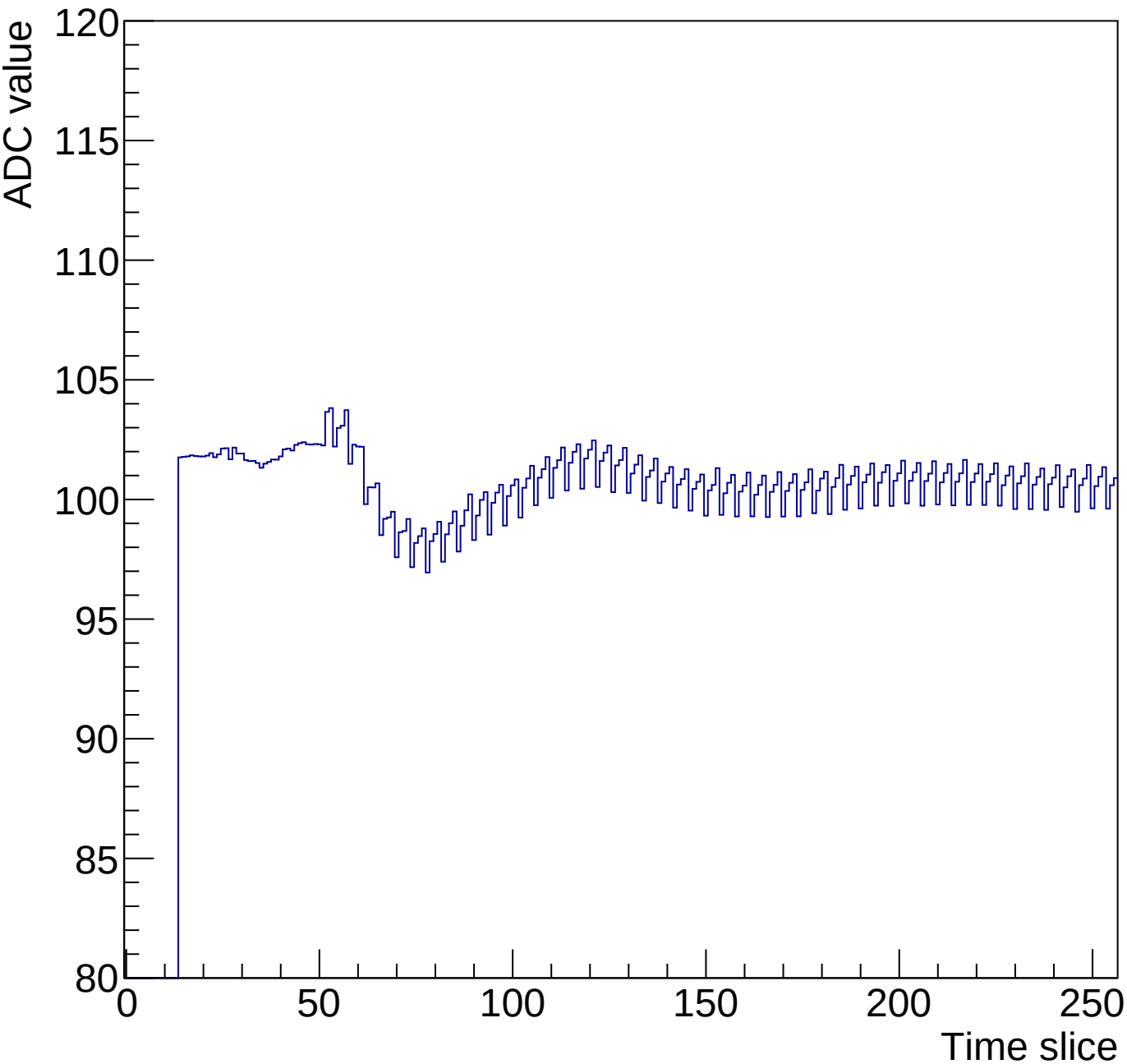
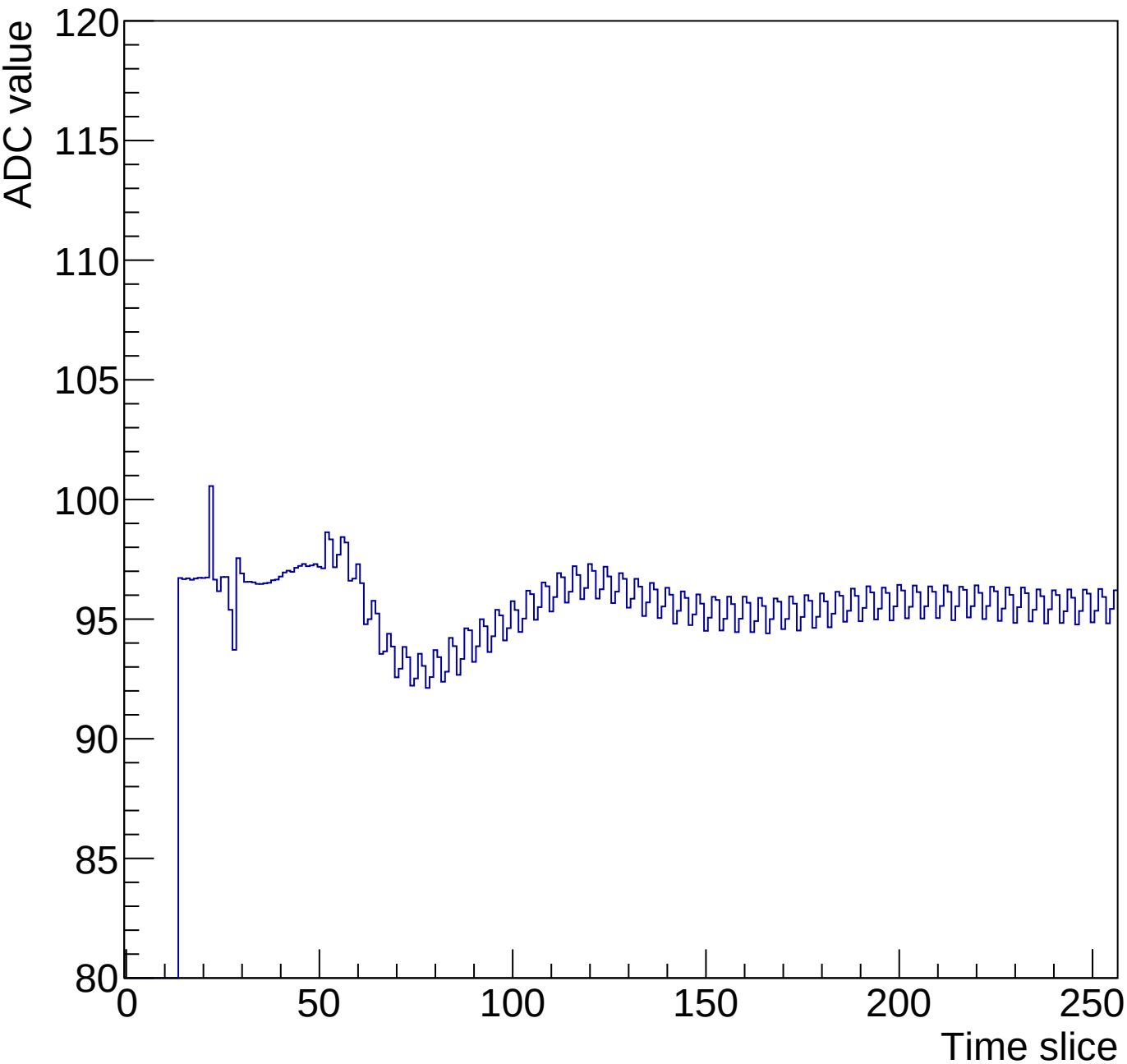


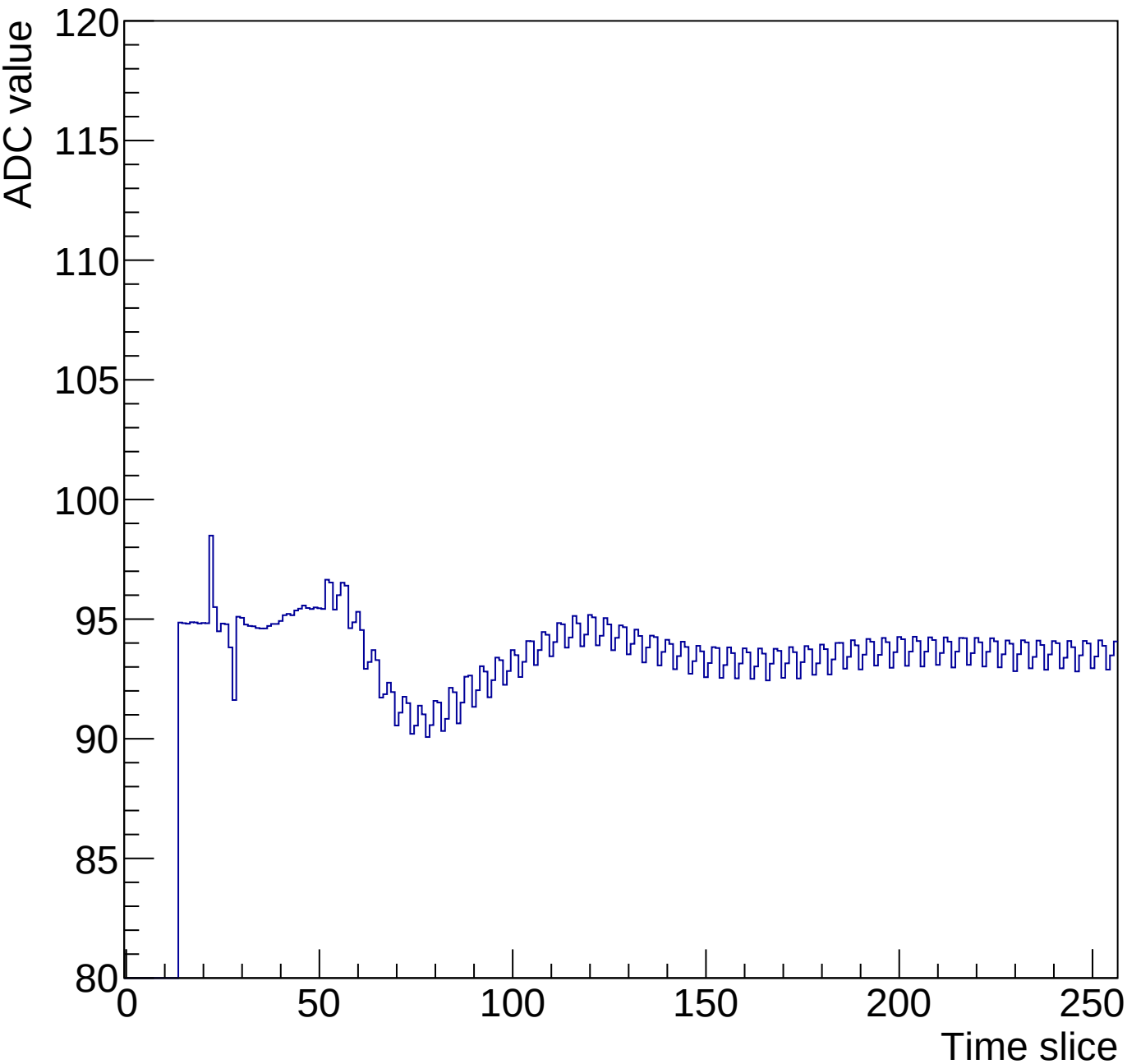
Run 4 Time mcm 2 chip 0 chan 0 256-30ns



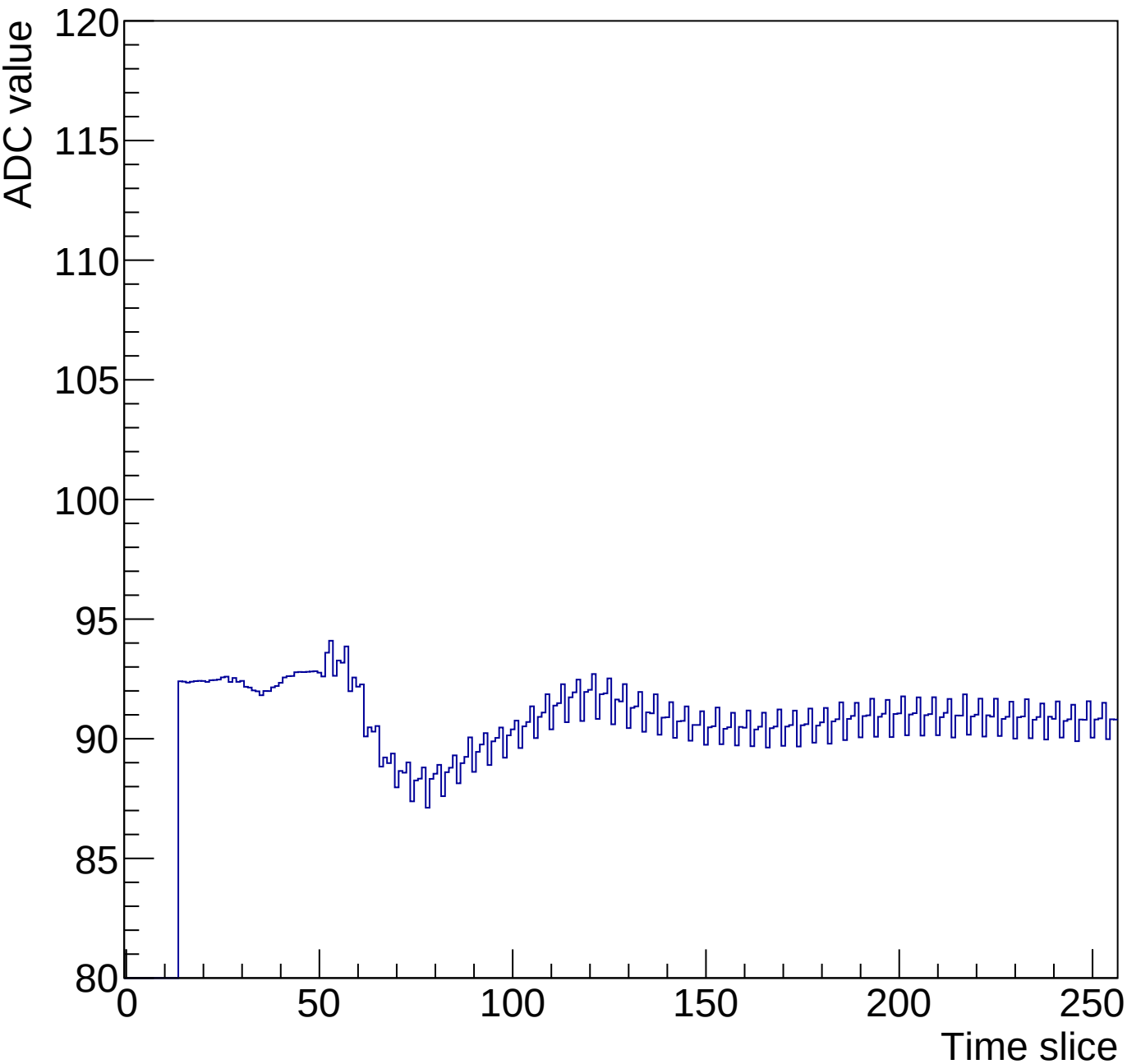
Run 4 Time mcm 2 chip 0 chan 1 256-30ns



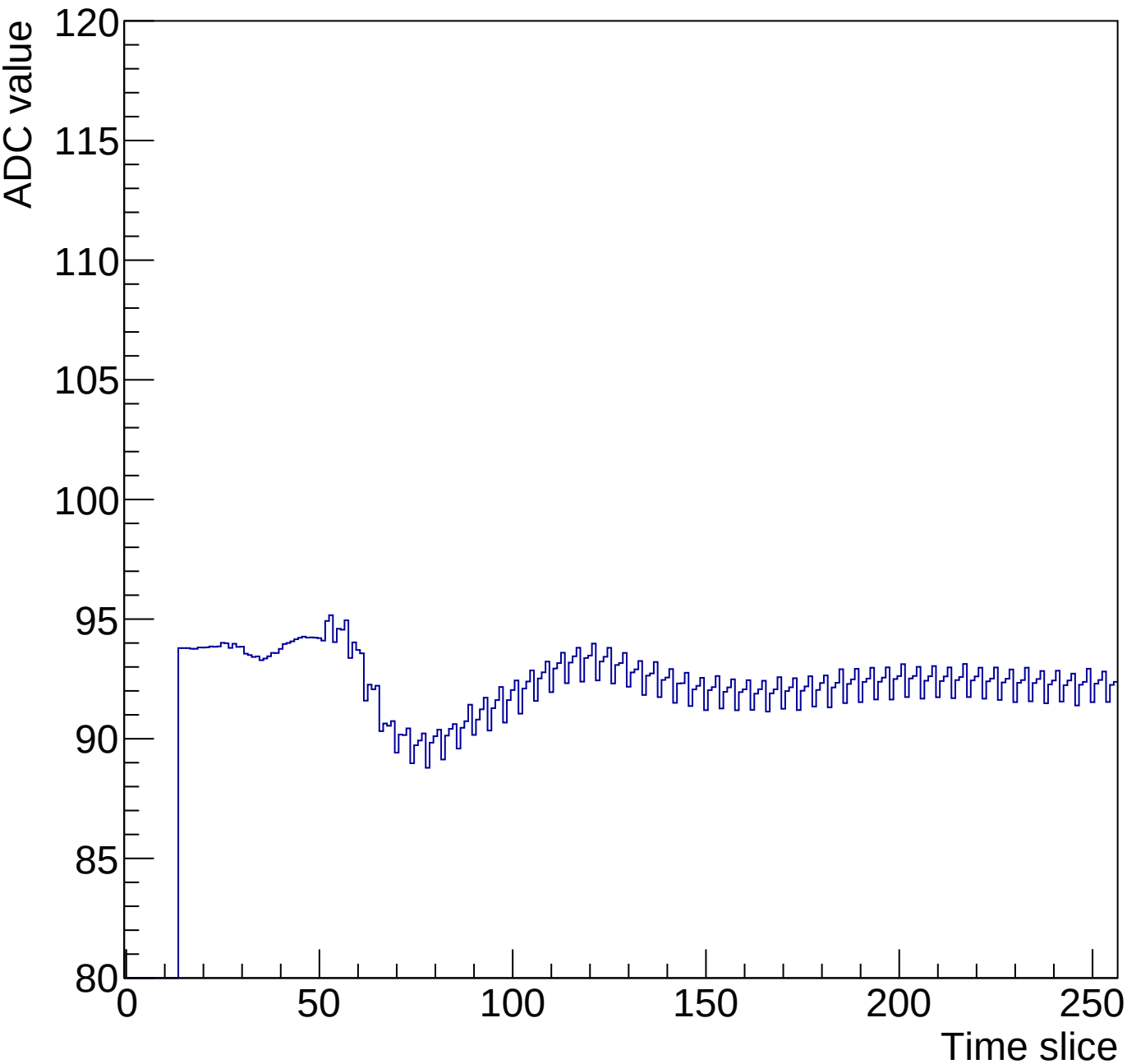
Run 4 Time mcm 2 chip 0 chan 2 256-30ns



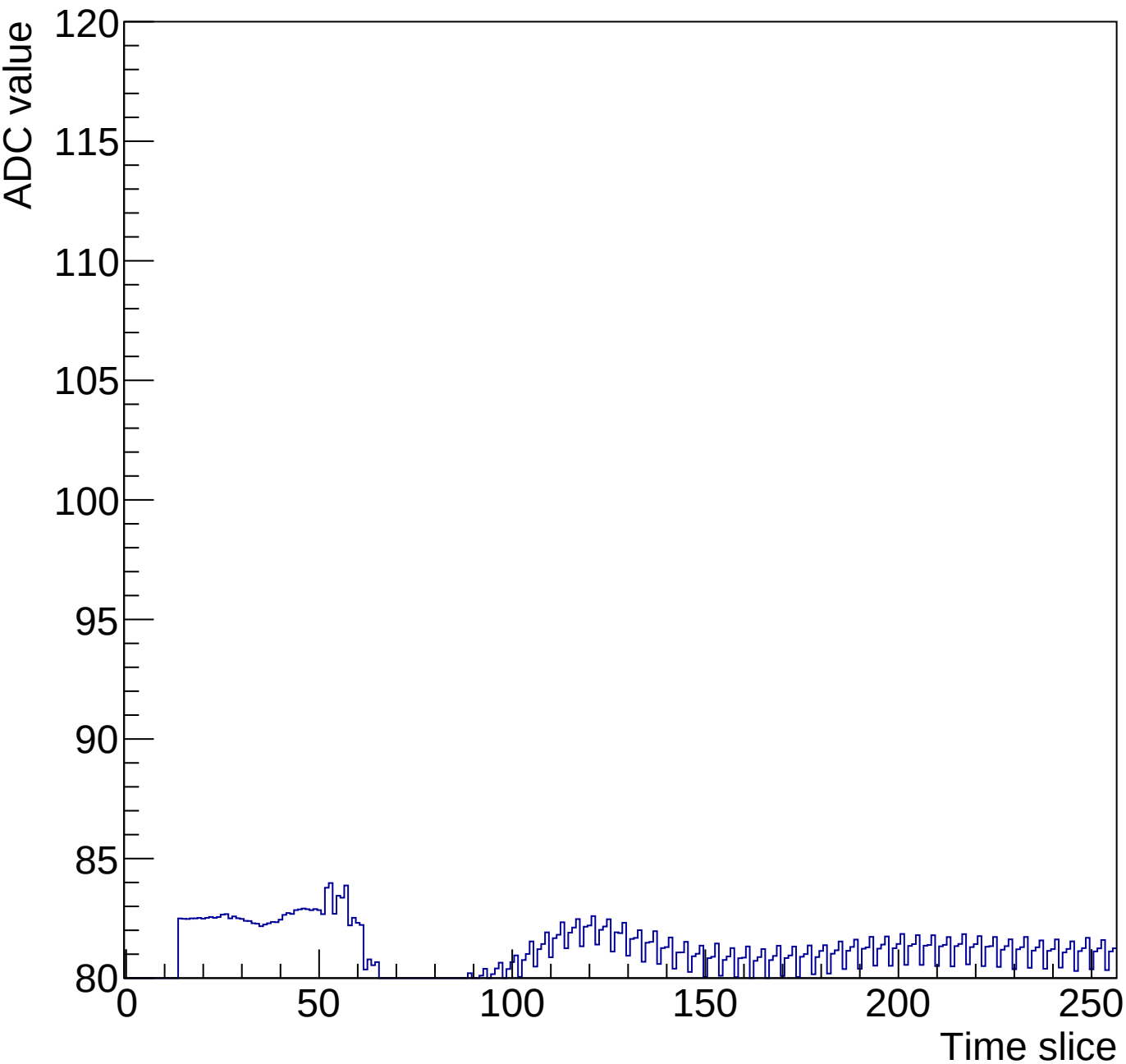
Run 4 Time mcm 2 chip 0 chan 3 256-30ns



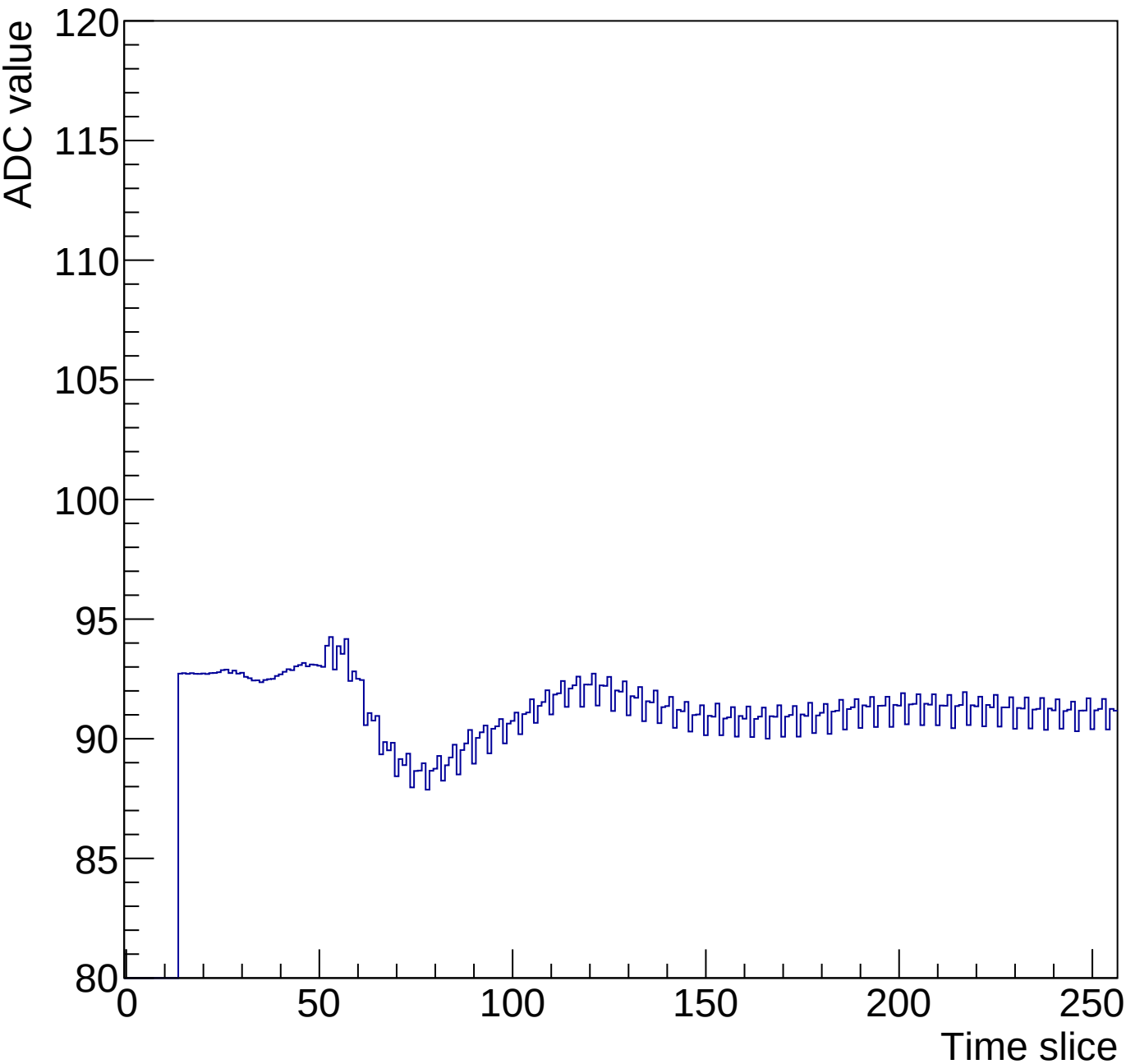
Run 4 Time mcm 2 chip 0 chan 4 256-30ns



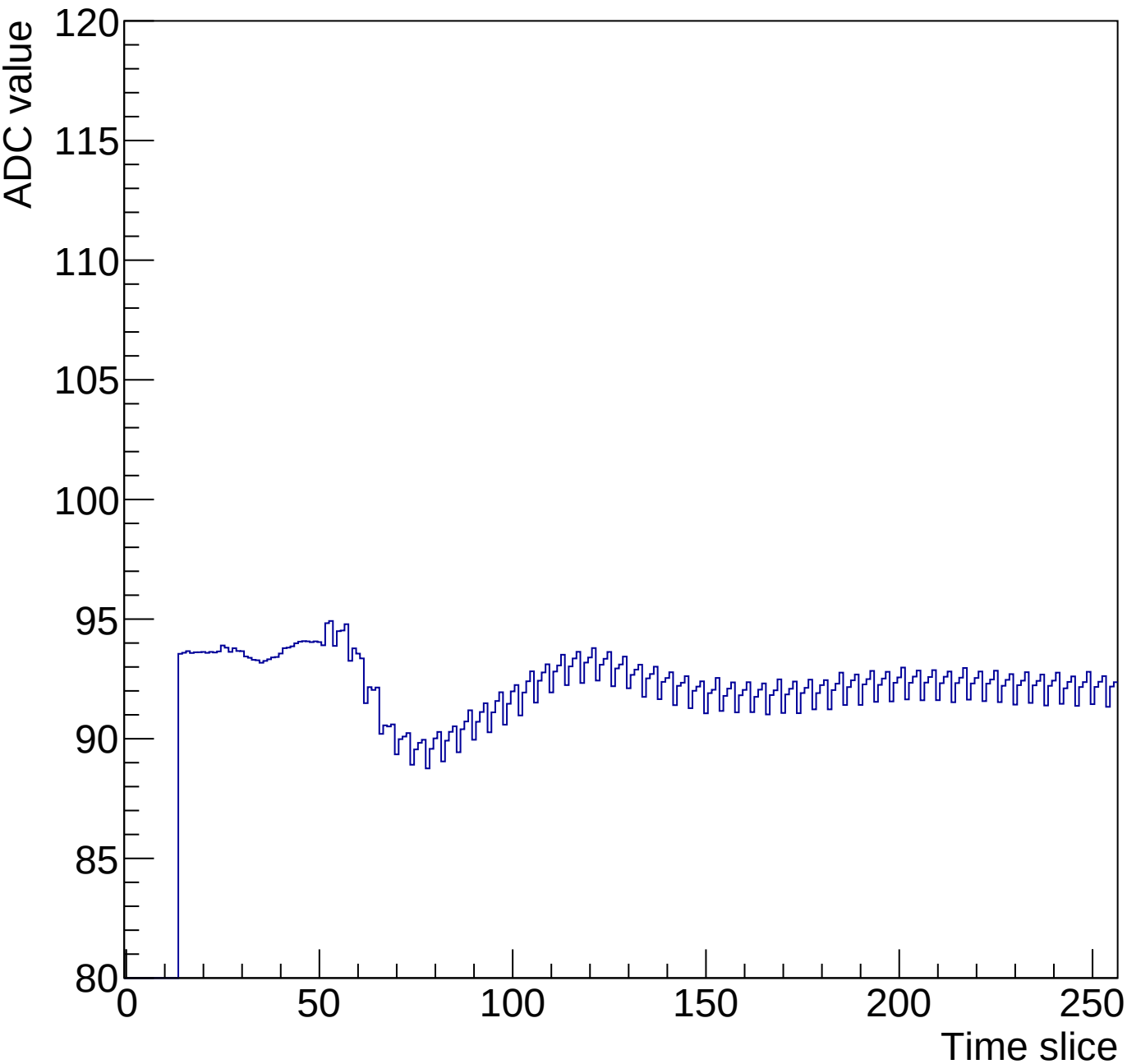
Run 4 Time mcm 2 chip 0 chan 5 256-30ns



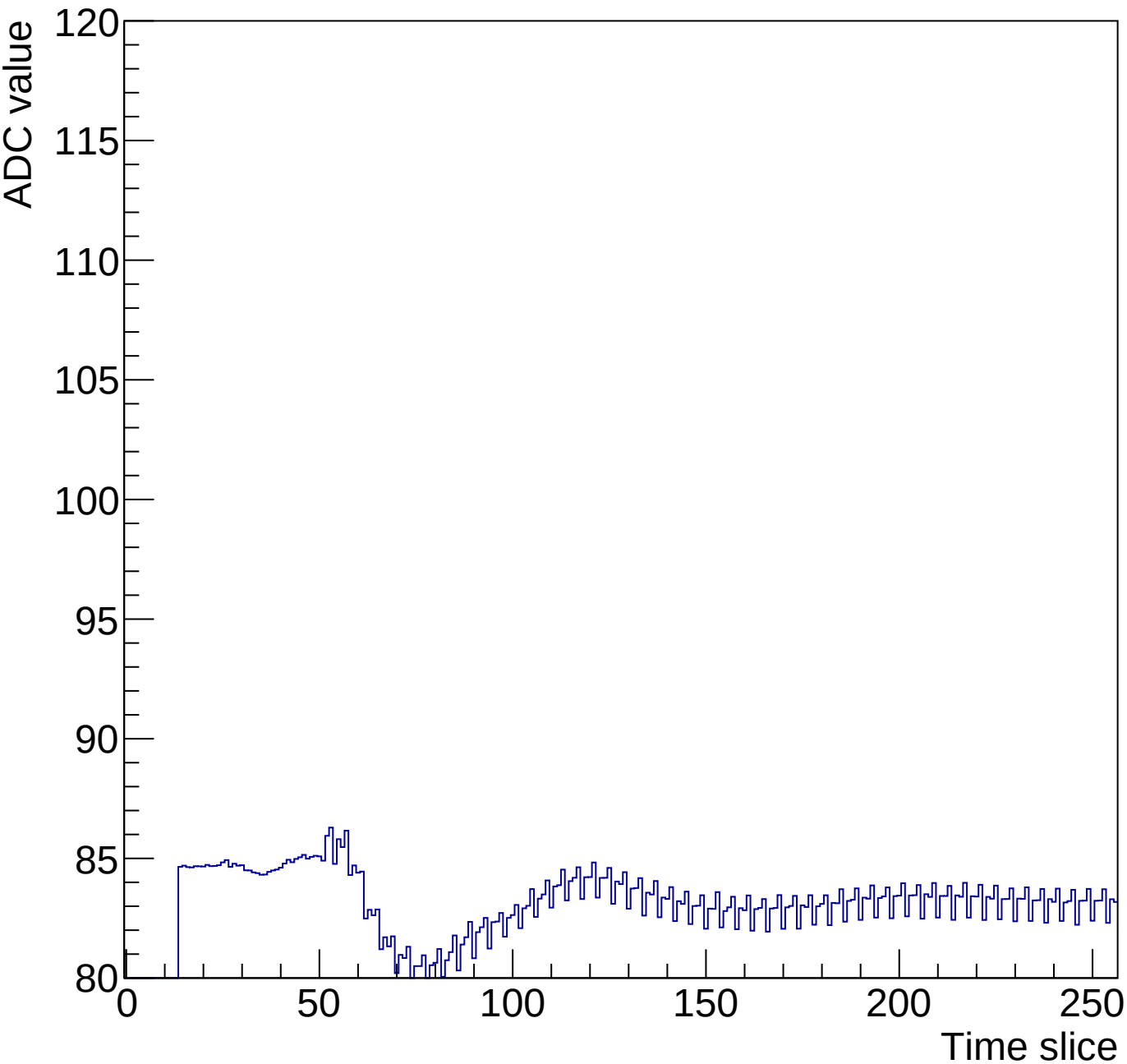
Run 4 Time mcm 2 chip 0 chan 6 256-30ns



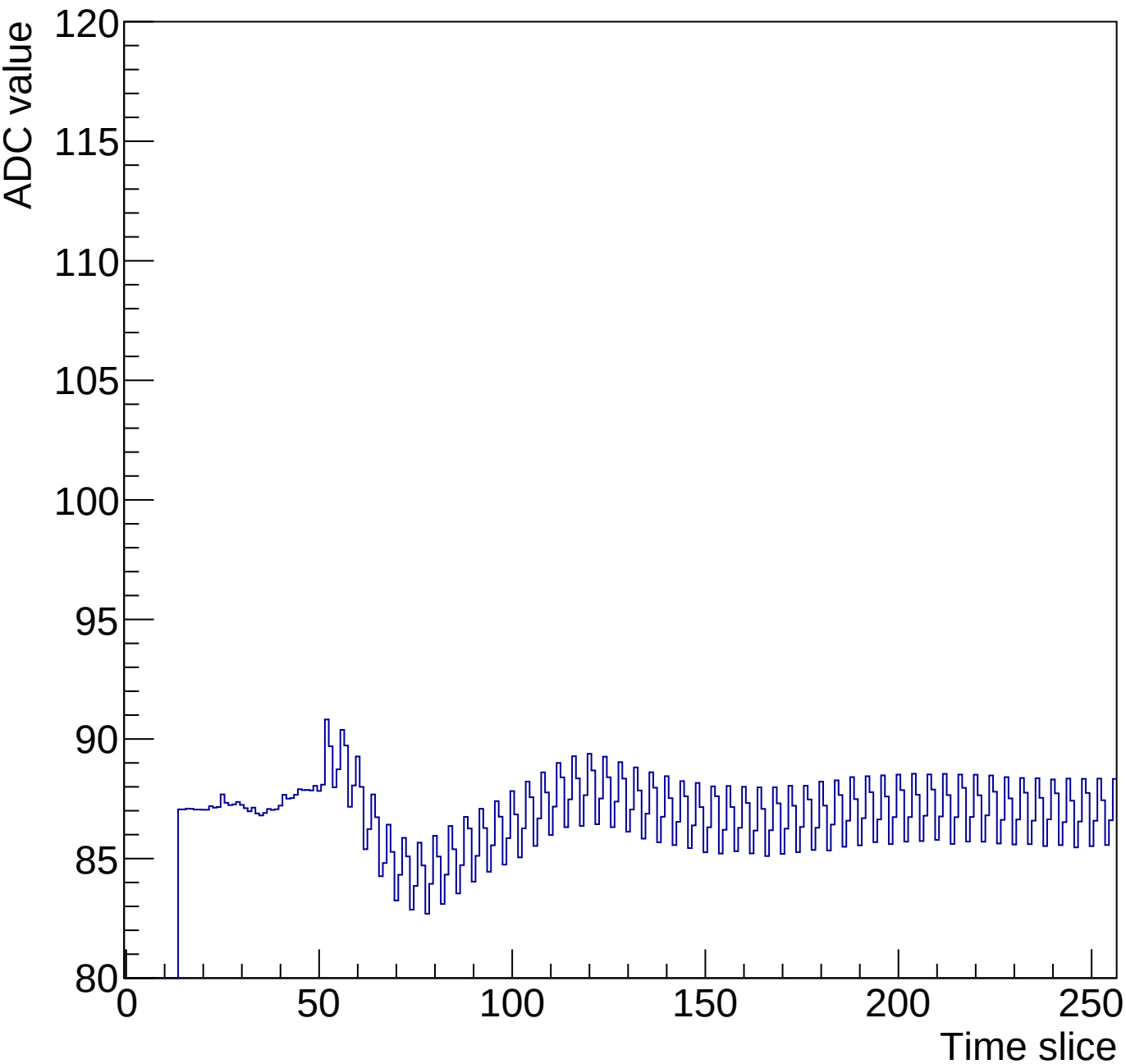
Run 4 Time mcm 2 chip 0 chan 7 256-30ns



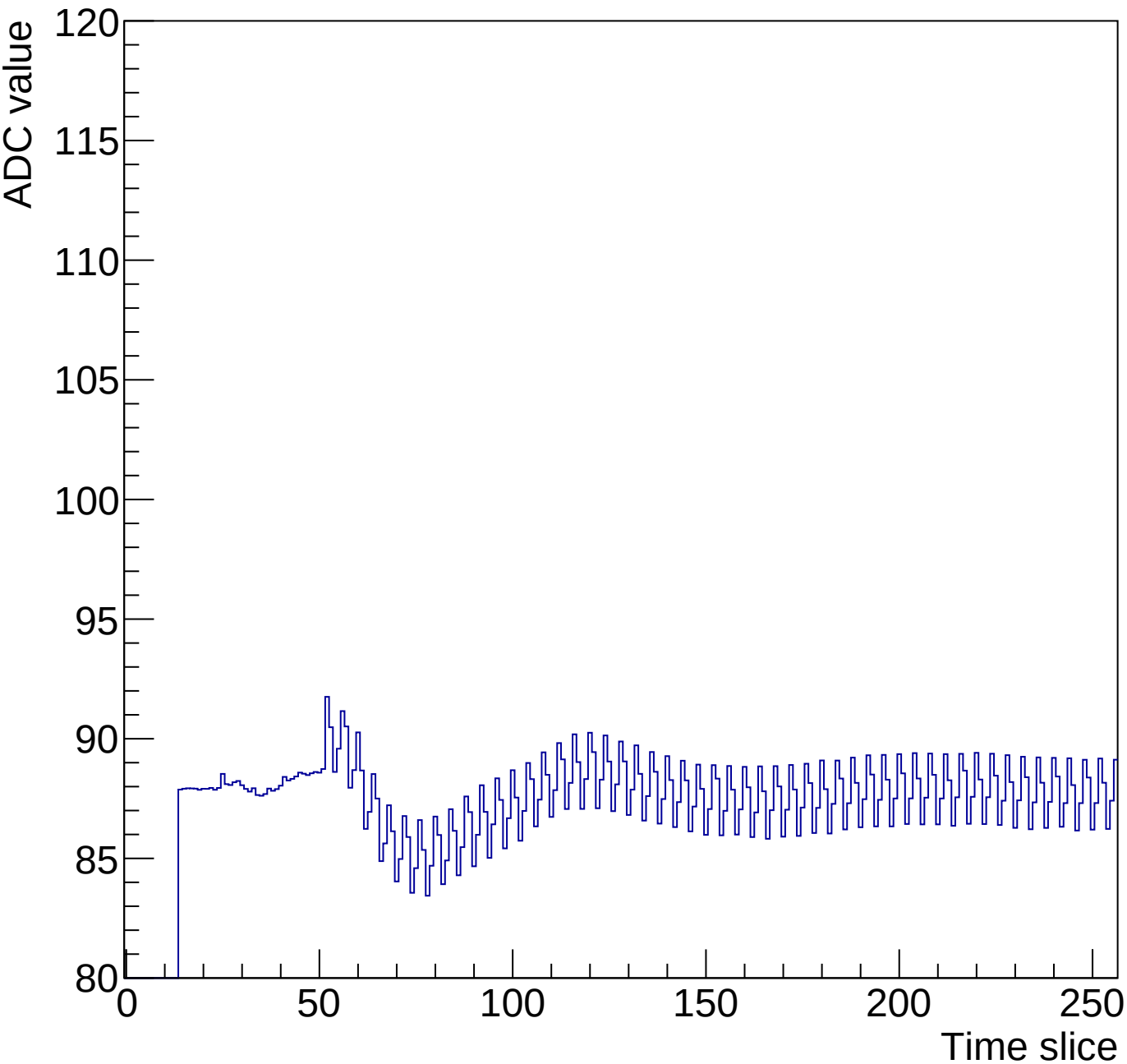
Run 4 Time mcm 2 chip 0 chan 8 256-30ns



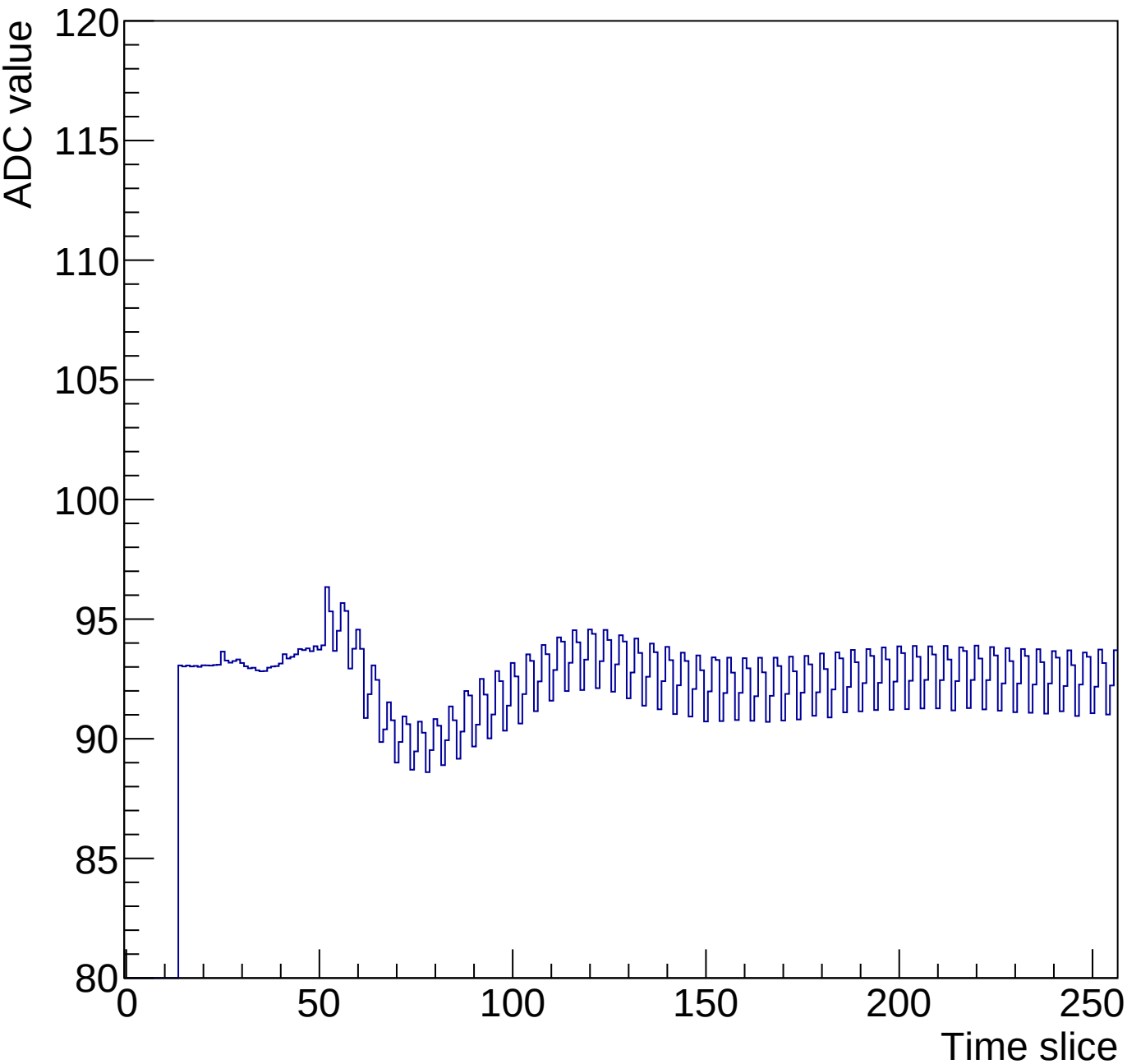
Run 4 Time mcm 2 chip 0 chan 9 256-30ns



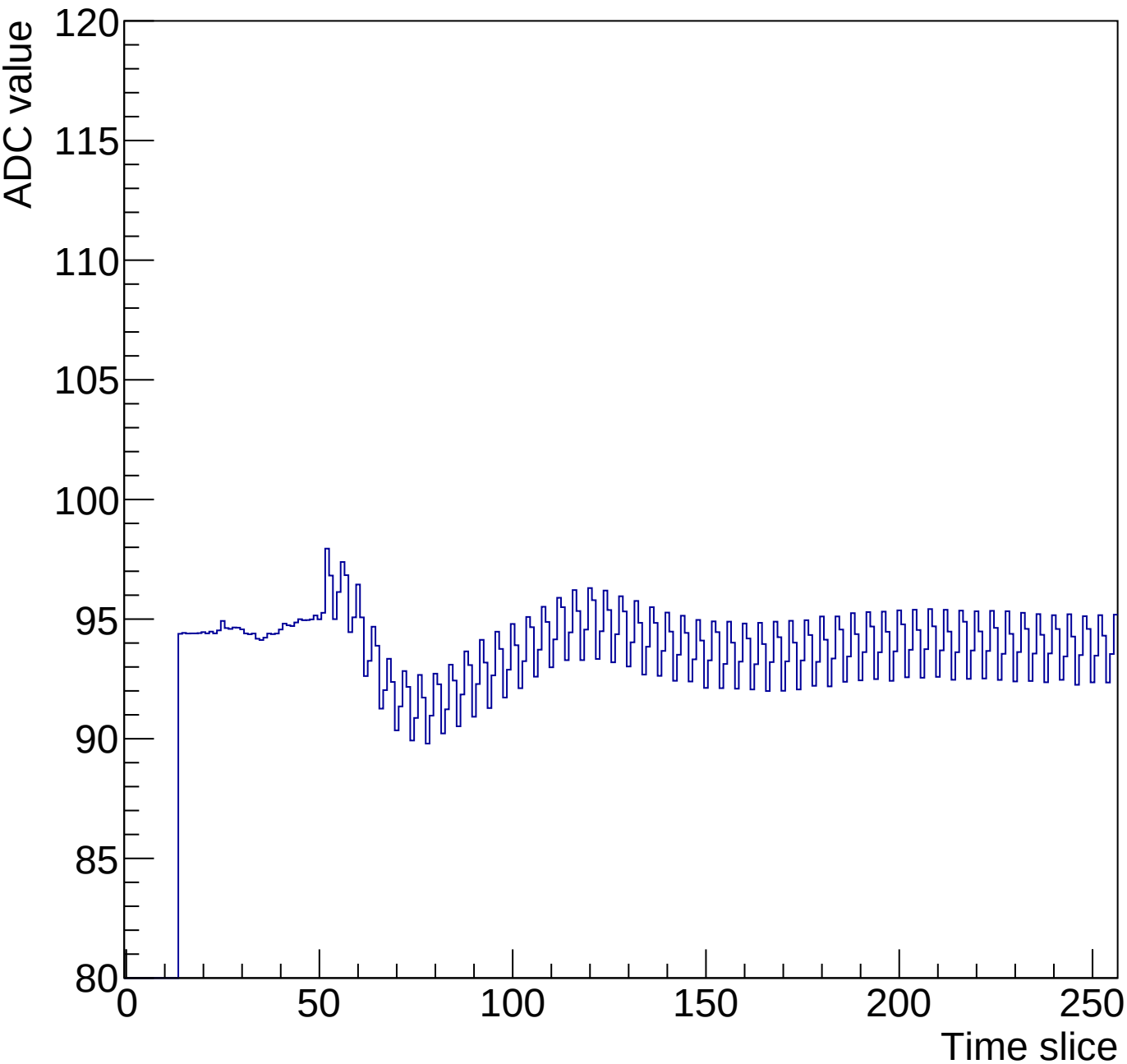
Run 4 Time mcm 2 chip 0 chan 10 256-30ns



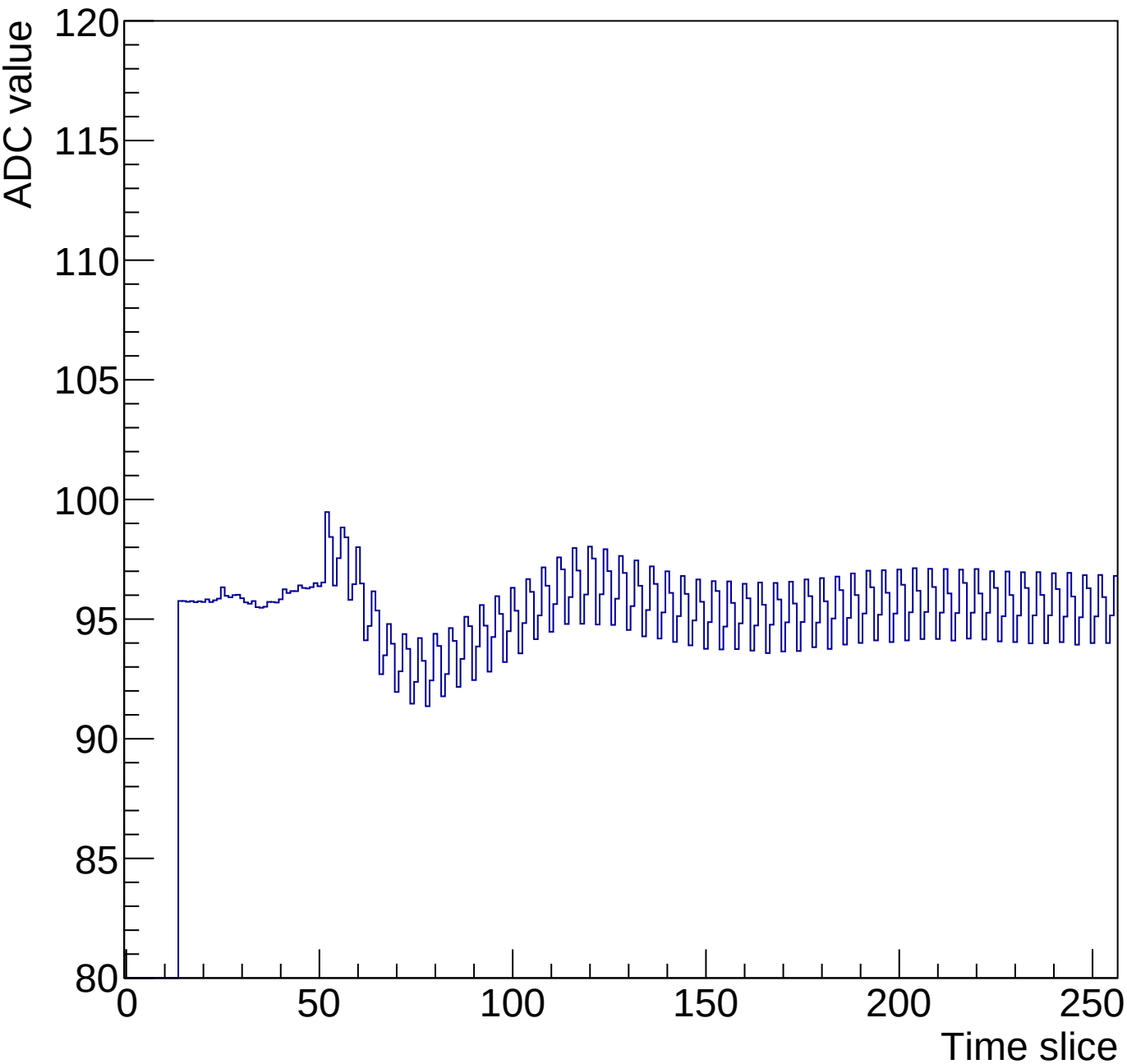
Run 4 Time mcm 2 chip 0 chan 11 256-30ns



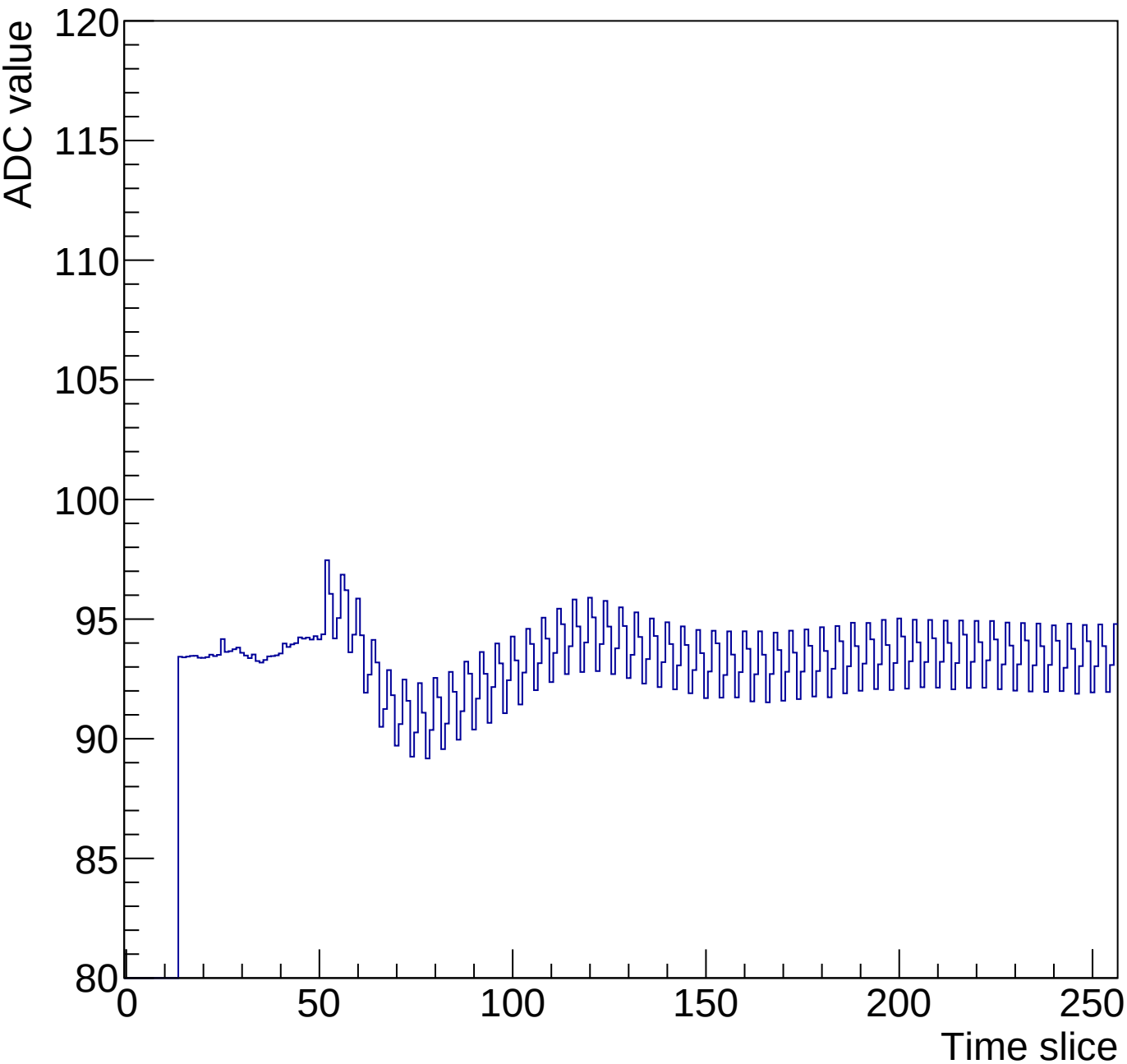
Run 4 Time mcm 2 chip 0 chan 12 256-30ns



Run 4 Time mcm 2 chip 0 chan 13 256-30ns



Run 4 Time mcm 2 chip 0 chan 14 256-30ns



Run 4 Time mcm 2 chip 0 chan 15 256-30ns

