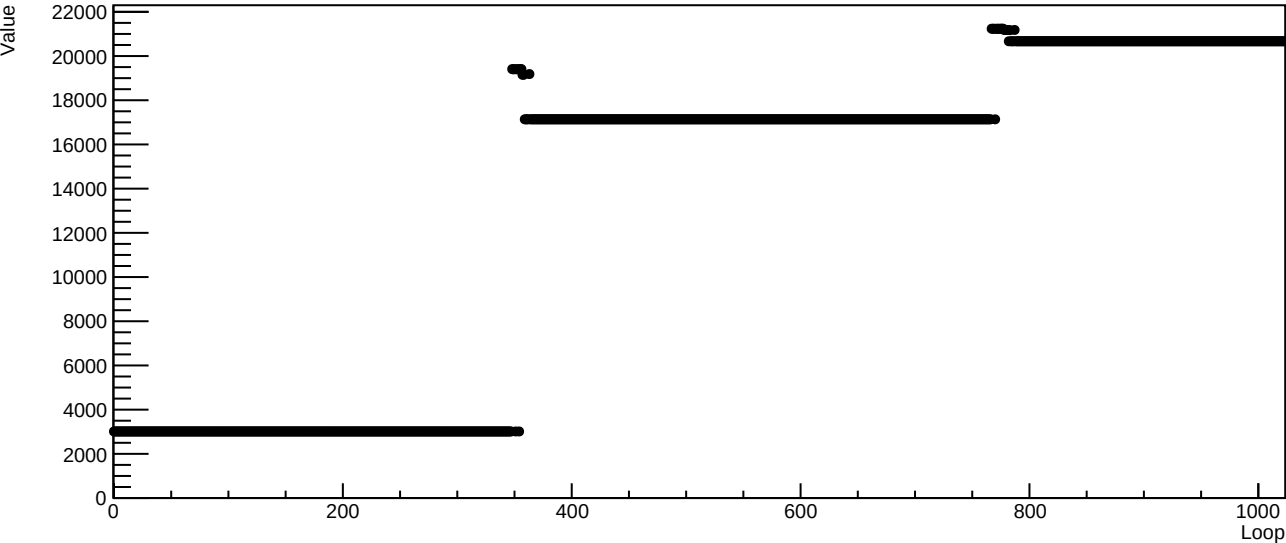
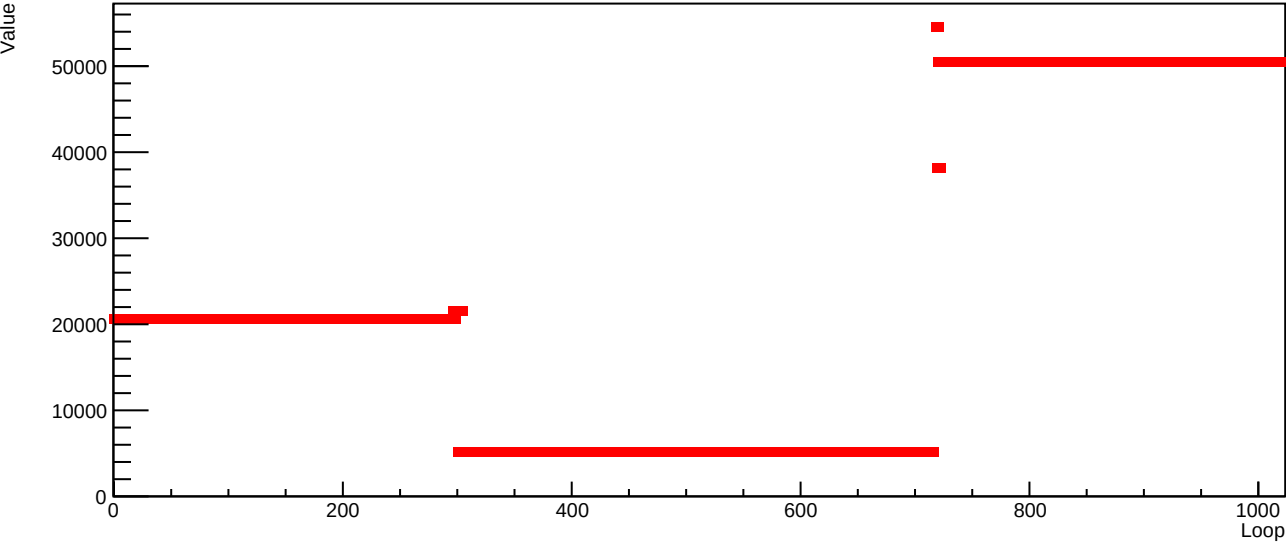


DCL timing1-reset1.out MCM0



DCL timing1-reset1.out MCM1



DCL timing1-reset1.out MCM2

