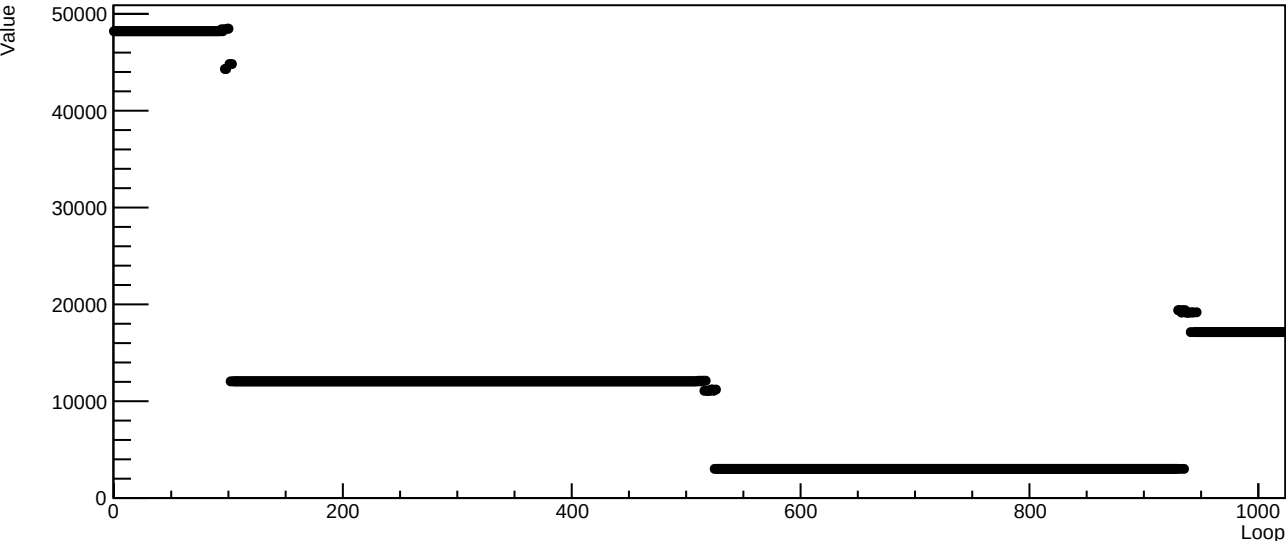
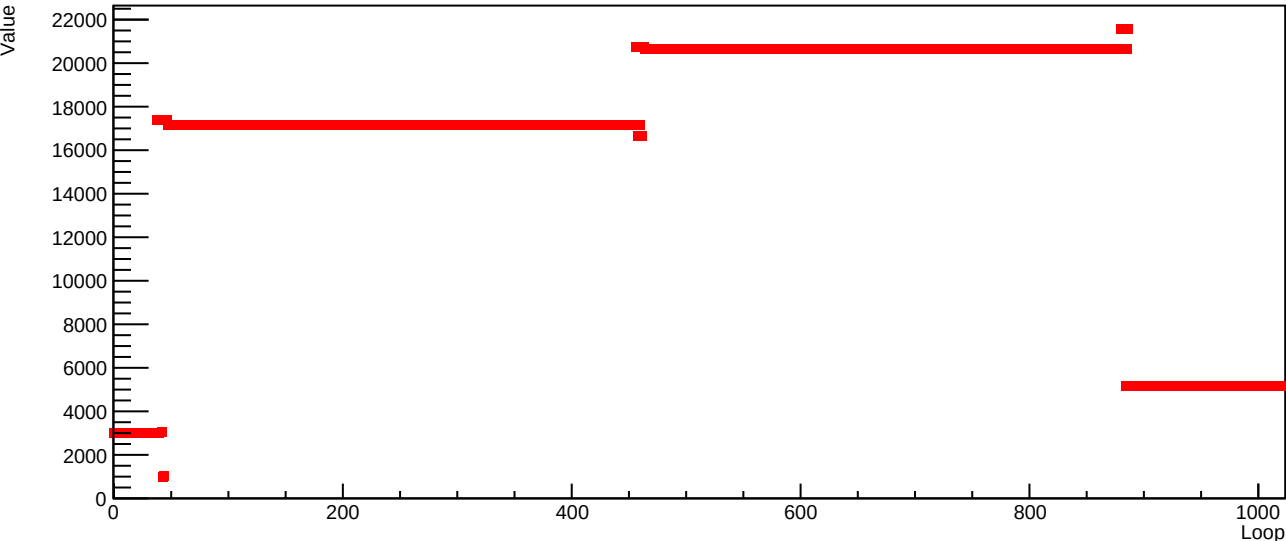


DCL timing1-reset2.out MCM0



DCL timing1-reset2.out MCM1



DCL timing1-reset2.out MCM2

