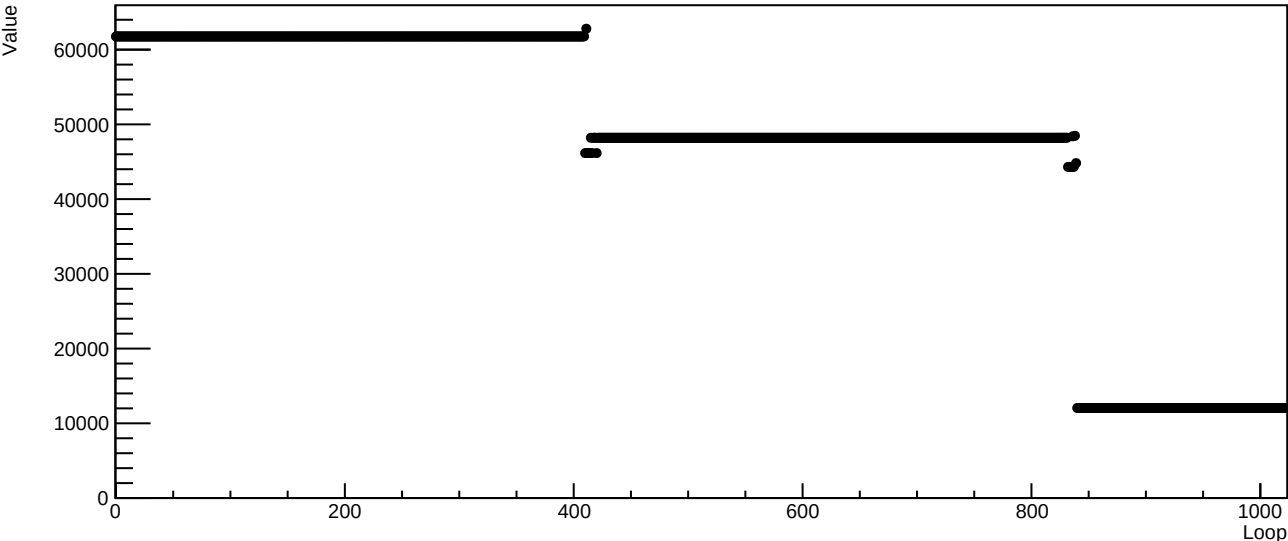
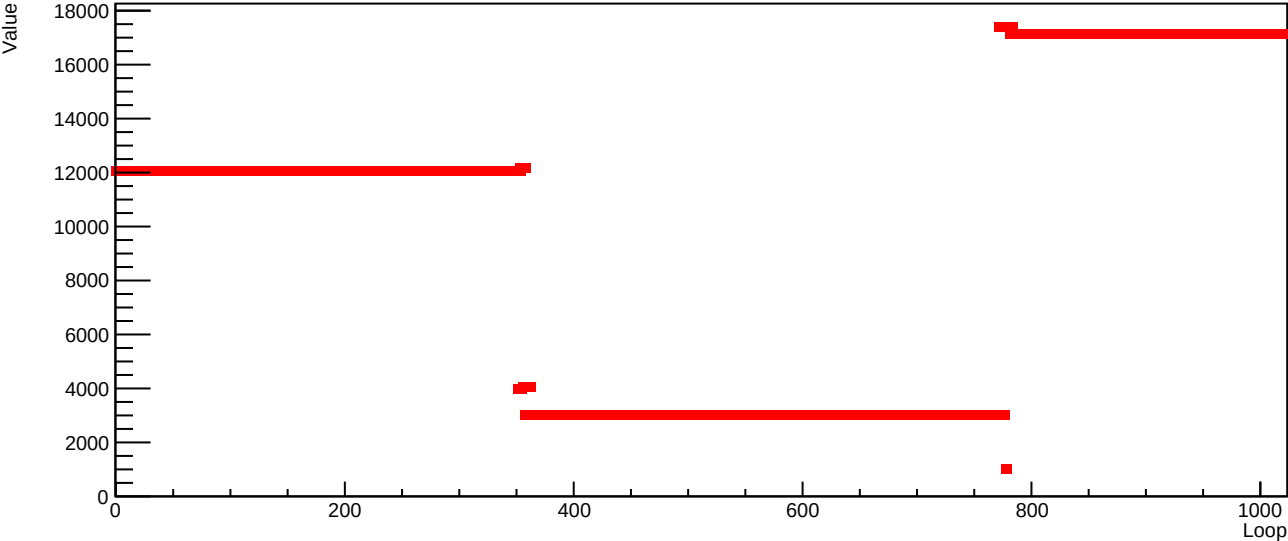


DCL timing1-reset3.out MCM0



DCL timing1-reset3.out MCM1



DCL timing1-reset3.out MCM2

