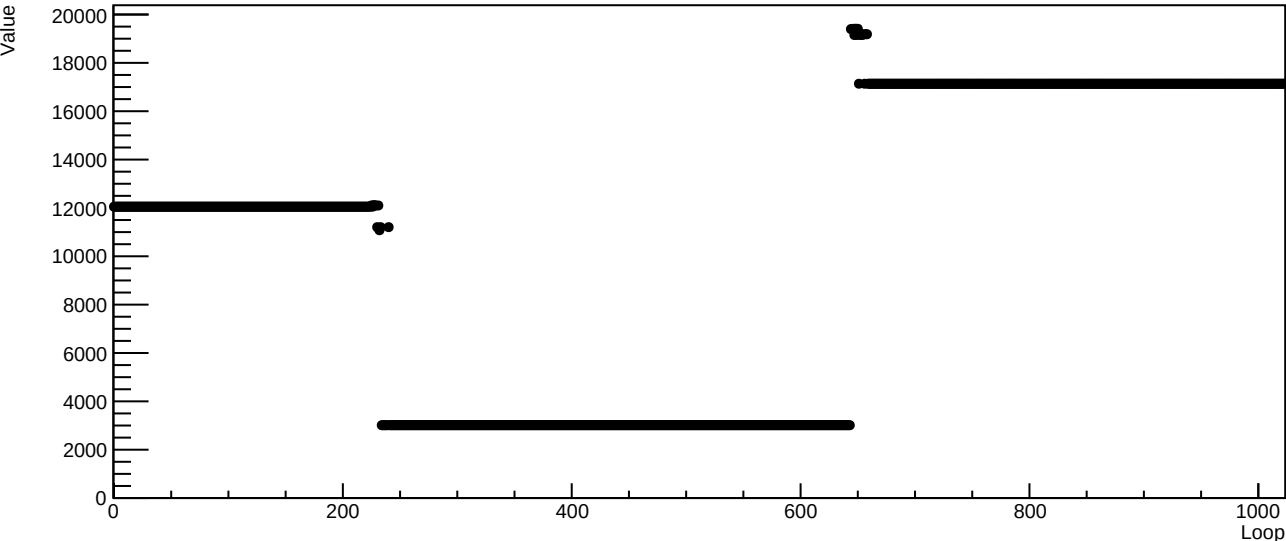
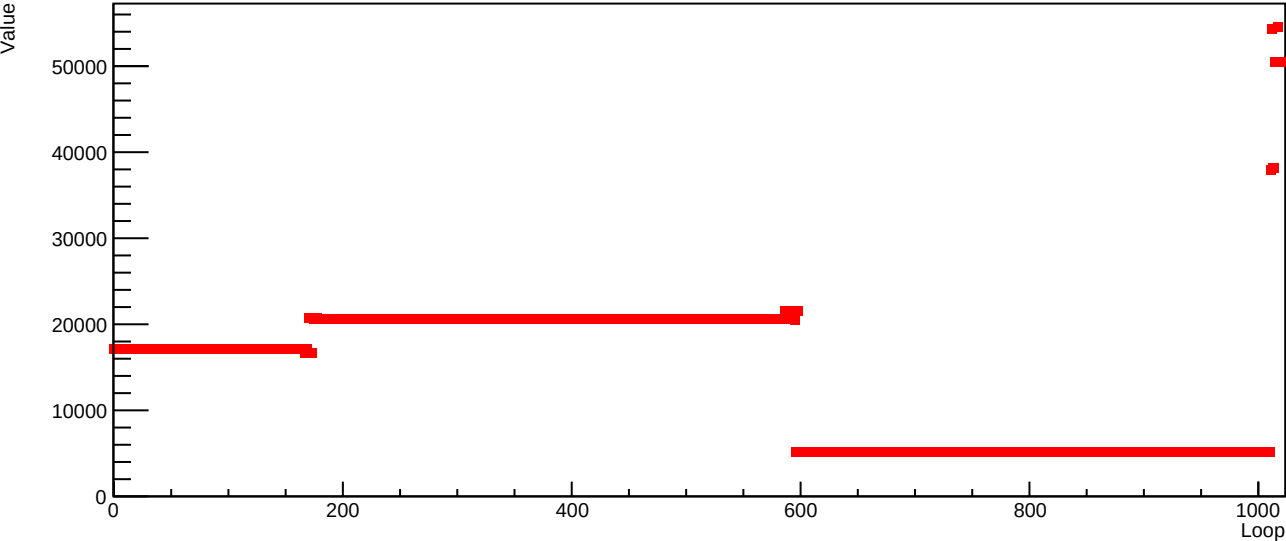


DCL timing1-reset4.out MCM0



DCL timing1-reset4.out MCM1



DCL timing1-reset4.out MCM2

