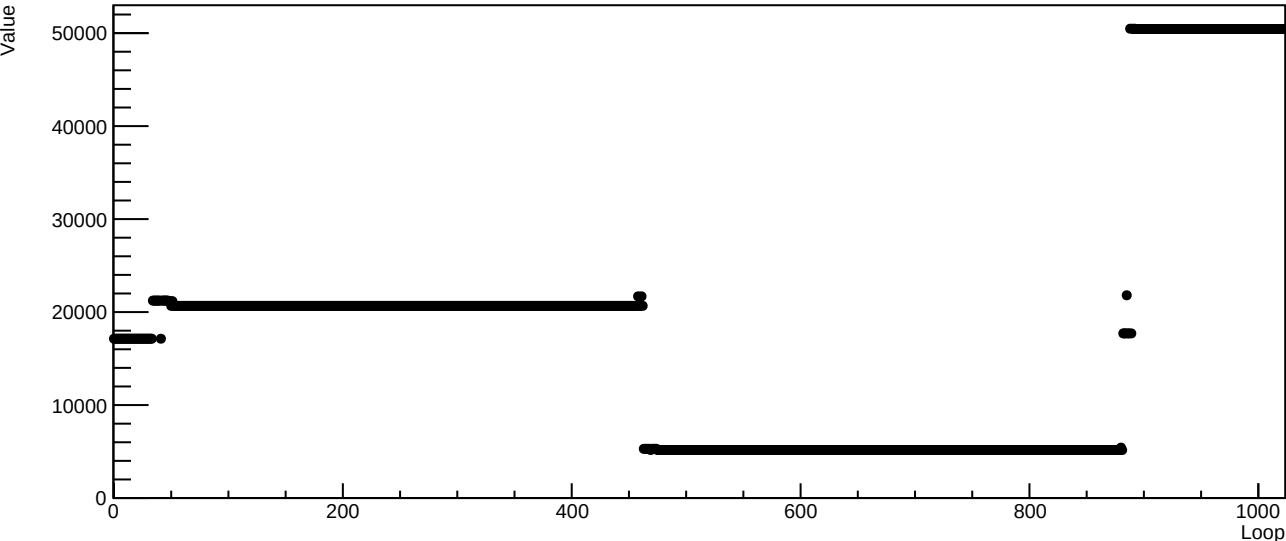
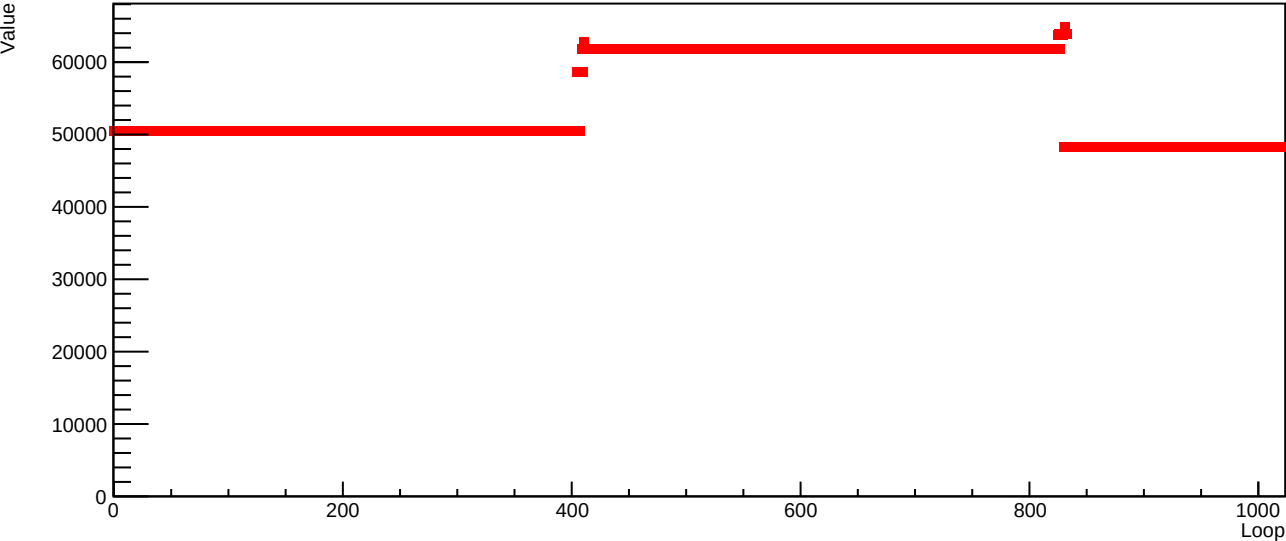


DCL timing1-reset5.out MCM0



DCL timing1-reset5.out MCM1



DCL timing1-reset5.out MCM2

