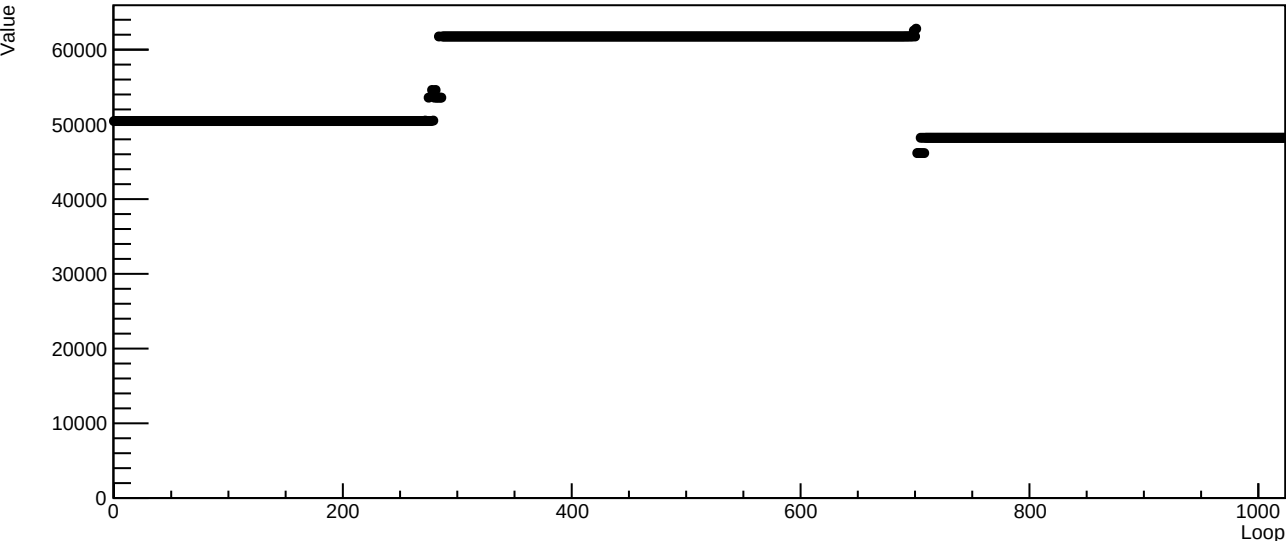
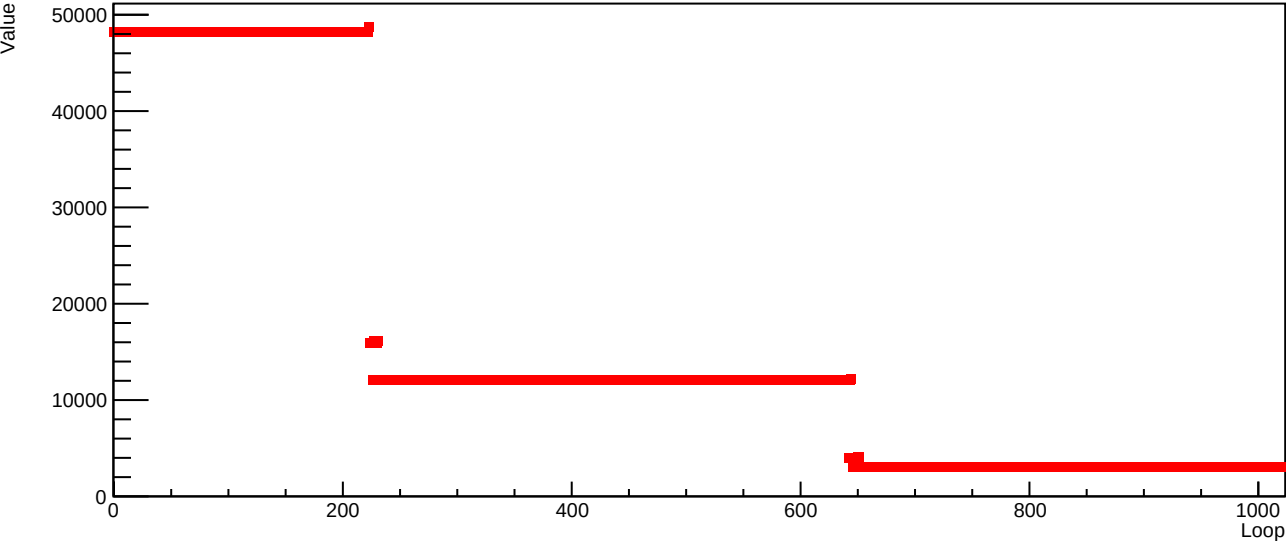


DCL timing1-reset6.out MCM0



DCL timing1-reset6.out MCM1



DCL timing1-reset6.out MCM2

